RENESAS

μ**PD720231A**

ASSP (USB3.0 to SATA3 BRIDGE CONTROLLER)



R19DS0077EJ0100 Rev 1.00 Jul 29, 2013

Data Sheet

1. OVERVIEW

The μ PD720231A is a USB3.0 to SATA3 Bridge LSI which complies with Universal Serial Bus 3.0 (USB3.0) Specification Revision 1.0 and Serial ATA (SATA) Specification Revision 3.0. The LSI is integrated USB3.0 function controller and SATA III host controller with USB3.0 transceiver, USB2.0 transceiver and SATA III transceiver into one chip. The USB3.0 transceiver supports SuperSpeed (SS) 5 Gbps. USB2.0 transceiver supports High-Speed (HS) 480Mbps and Full-Speed (FS) 12 Mbps. And SATA III transceiver supports Gen1 1.5 Gbps / Gen2 3 Gbps / Gen3 6 Gbps.

1.1 Features

- Compliant with Universal Serial Bus 3.0 Specification Revision 1.0
 - Certified by USB Implementers Forum (TID: 340000093)
 - Supports Super/High-/Full-speed
 - > Supports Mass Storage Class UASP (USB Attached SCSI Protocol)
 - > Supports Mass Storage Class BOT (Bulk Only Transport)
 - > Includes SCSI Command hardware accelerator
 - > Supported number of stream is 32 + Task management.
- Compliant with Serial ATA Specification Revision 3.0.
 - Supports Gen1 / Gen2 / Gen3
 - > Supports Host initiated power management
 - Supports multiple LUN
 - > Be capable of providing full ATA-8, 48-Bit LBA support, for drives larger than 2TB.
- Supports power management
 - USB3.0 U1/U2/U3 state
 - USB2.0 Suspend/LPM
- Integrated 32-bit RISC CPU
- 10 configurable GPIOs including
 - > SPI interface for serial flash ROM.
 - Two PWM interface
 - Multi voltage level support
- Clock input: 30 MHz crystal
- On-chip reset circuit to remove external power-on-reset circuit
- Integrated mask firmware into internal mask ROM to eliminate external Flash ROM
- Power supply: 5 V single power supply, using 2 internal regulators
 - > On-chip 1.0 V and 3.3 V regulator
- Package: 48-pin QFN (6 x 6 mm)

1.2 Applications

External USB hard disk/SSD, USB hard disk enclosure, optical drive, etc.

1.3 Ordering Information

Part Number	Package	Remark
μPD720231AK8-612-BAE-A	48-pin QFN (6 x 6)	Lead-free product

1.4 Block Diagram



Figure 1-1. μ PD720231A Block Diagram



CPU	Integrated 32 bit RISC CPU.
CPU Peripherals	Includes bus controller, interrupt controller, timer, GPIO and so on.
Work RAM	Integrated Work RAM for data.
ROM	Integrated Boot ROM.
SATA III Host Controller	The SATA III host supports SATA Gen1 1.5 Gbps, Gen2 3.0 Gbps, and Gen3 6.0 Gbps. Dedicated bus realizes SuperSpeed interface between SATA III host and Direct Command Controller.
SATA LINK	Link layer translates data packets between SATA host and SATA PHY.
SATA Gen3 PHY	Integrated SATAIII Gen1 1.5 Gbps, Gen2 3.0 Gbps, and Gen3 6.0 Gbps compliance transceiver. This is controlled by SATAIII host.
USB Endpoint Controller (EPC)	Transport / Protocol layer. This block supports USB Mass Storage class USB Attached SCSI Protocol and Bulk Only Transport.
USB LINK	Link layer defined in USB specification, which maintains Link connectivity with USB host controller and hub.
USB3.0 PHY	For SuperSpeed Tx/Rx
USB2.0 PHY	For USB High/Full-speed Tx/Rx
CCU	Integrated clock controller to manage system power consumption, and system reset controller.
OSC	Internal oscillator block.
3.3 V to 1.0 V Regulator	Regulator to convert 3.3 V to 1.0 V
5 V to 3.3 V Regulator	Regulator to convert 5 V to 3.3 V



1.5 Pin Configuration

• *µ*PD720231AK8-612-BAE-A, 48-pin QFN (6 x 6)



Figure 1-2. Pin Configuration (Top View)



2. PIN FUNCTION

This section describes each pin functions.

2.1 Power Supply and Regulator and Regulator

Pin Name	Pin No.	Buffer Type	Function
VDD33	25	Power	+3.3 V power supply
VDDGPIO	5, 39	Power	+3.3 V power supply for GPIOs, except for GPIO5/DPC and GPIO6/ACT.
AVDD33	17	Power	+3.3 V power supply for USB analog circuit
VDD10	7, 18, 21, 24, 26, 29, 32, 35, 40	Power	+1.0 V power supply
V50IN	12	Regulator	+5 V input for internal LDO.
VDD33OUT	11	Regulator	+3.3 V output from internal LDO.
AVDD33IN1 Note	45	Regulator	+3.3 V power supply for regulator analog circuit
AVDD33IN2 Note	46	Regulator	+3.3 V power supply for regulator analog circuit
LX1	44	Regulator	1.0 V output from the on-chip regulator
FB	47	Regulator	Feedback for regulator.
GND	Die PAD	-	Connect to ground for digital circuit

Note It is mandatory to put ceramic capacitors (22 μF is recommended) on AVDD25IN1 and AVDD25IN2. Common impedance coupling between AVDD25IN1 and AVDD25IN2 must be avoided.

2.2 Analog Signal

Table 2-2. Analog Signal

Pin Name	Pin No.	Direction	Buffer Type	Active Level	Function
RREF	16	_	USB2	-	This pin must be connected to GND via a 1.6k- ohm resistor with 1% precision.

2.3 VBUS Monitor

Table 2-3.	VBUS and	Regulator
	1 DOO unia	riegulator

Pin Name	Pin No.	Direction	Buffer Type	Active Level	Function
VBUSM	10	I	5V tolerant buffer	High	VBUS detection.



2.4 System Clock and Reset

Pin Name	Pin No.	Direction	Buffer Type	Active Level	Function
XT1	27	I	OSC	_	30 MHz oscillator input. Connect to a 30 MHz crystal.
XT2	28	0	OSC	_	30 MHz oscillator output. Connect to a 30 MHz crystal.
RESETB	38	I	3.3/2.5 V schmitt input with 50 kΩ pull-up resistor	Low	System reset

Table 2-4	System	Clock	and	Reset
	System	Olock	anu	neset

2.5 USB Interface

Table 2-5. USB Interface

Pin Name	Pin No.	Direction	Buffer Type	Active Level	Function
U3RXP	23	I	USB3	-	USB3.0 receive data D+ signal for SuperSpeed
U3RXN	22	I	USB3	-	USB3.0 receive data D- signal for SuperSpeed
U3TXP	20	0	USB3	-	USB3.0 transmit data D+ signal for SuperSpeed
U3TXN	19	0	USB3	-	USB3.0 transmit data D- signal for SuperSpeed
U2DP	15	I/O	USB2	_	USB2.0 D+ signal for High-/Full-speed
U2DM	13	I/O	USB2	_	USB2.0 D- signal for High-/Full-speed

2.6 Serial ATA Interface

Table 2-6. Serial ATA Interface

Pin Name	Pin No.	Direction	Buffer Type	Active Level	Function
SRXP	30	I	SATA III	-	Serial ATA receive data D+ signal
SRXN	31	I	SATA III	-	Serial ATA receive data D- signal
STXP	34	0	SATA III	-	Serial ATA transmit data D+ signal
STXN	33	0	SATA III	-	Serial ATA transmit data D- signal



2.7 General Purpose I/O Interface

Pin Name	Pin No.	Direction	Buffer Type	During reset	After reset	Function												
GPIO0/ SPISO	1			PU	Input	General purpose I/O or SPI read data signal												
GPIO1/ SPISCK	2			PU	Output	General purpose I/O or SPI clock												
GPIO2/ SPISI	3		3.3/2.5 V I/O	PU	Output	General purpose I/O or SPI write data signal												
GPIO3/ SPICSB	4			-		PU	Output	General purpose I/O or SPI chip select for the external serial ROM.										
GPIO4	6	1/0			Output low	Output low or HZ	General purpose I/O Default low drive. ^{№0te4}											
GPIO5/DPC Note1	8	1/0	5 V	Input	Output high or Input ^{Note2}	General purpose I/O or SATA drive power supply control												
GPIO6/ACT Note1	9		buffer	buffer	buffer	buffer	buffer	buffer	buffer	buffer	buffer	buffer	buffer	buffer	buffer	Input	Output low or Input ^{Note3}	General purpose I/O or Disk Activity LED
GPIO7/CLKOUT	41		3.3/2.5 V I/O	HZ	HZ	General purpose I/O or 30 MHz clock output												
GPIO8	37			HZ	HZ	General purpose I/O												
GPIO9/EXTINT	48			HZ	HZ	General purpose I/O or external interrupt such as push button input												

Note 1. Except for GPIO5/DPC and GPIO6, all the other GPIOs are supplied power from VDDGPIO. GPIO5/DPC and GPIO6 are supplied power from internal VDD33 line.

2. In active condition, GPIO5 drives high, otherwise, GPIO5 is input.

3. In active condition, GPIO6 drives low, otherwise, GPIO6 is input.

4. GPIO4 drives low in default. Other GPIO signals are open state in default.

Remark. PU: Internally pulled up, HZ: High impedance

2.8 Renesas Private Signal

Table 2-8.	Renesas	Private	Signal
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Pin Name	Pin No.	Direction	Buffer Type	Active Level	Function
IC	42, 43	I	-	_	Test signal.
					These pins must be connected to GND or left opened.
NC	14, 36	-	-	-	Non connection pin.
					This pin should be opened.



3. ELECTRICAL SPECIFICATIONS

3.1 Buffer List

Buffer type	Pin name
3.3 V input schmitt buffer with 50 k Ω pull-up resistor	RESETB
3.3 V input buffer with 50 k Ω pull-down resistor	IC
3.3 V I _{oL} = 6 mA bi-directional buffer (schmitt input) with 50 k Ω pull-up/down resistor	GPIO0/SPISO, GPIO1/SPISCK, GPIO2/SPISI, GPIO3/SPICSB, GPIO4, GPIO7/CLKOUT, GPIO8, GPIO9/EXTINT
3.3 V input buffer with 5 V tolerant	VBUSM
5 V tolerant 3.3 V I_{OL} = 4mA bi-directional buffer	GPIO5/DPC, GPIO6/ACT
USB3 PHY	U3RXP, U3RXN, U3TXP, U3TXN
USB2 PHY	U2DP, U2DN, RREF
SATA III PHY	SRXP, SRXN, STXP, STXN
3.3 V Oscillator	XT1, XT2
3.3 V to 1.0 V Regulator	LX1, FB
5 V to 3.3 V Regulator	VDD33OUT

Note Uses a 5 V tolerant buffer meeting absolute maximum ratings. Note that the voltage presented at the 5 V tolerant buffer should not be higher than V, at any given time.



3.2 Terminology

Parameter	Symbol	Meaning
Power supply voltage	V50IN, VDD33, AVDD33, AVDD33IN1, AVDD33IN2, VDD10	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to a VDD pin.
Input voltage	V,	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V _o	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I _o	Indicates absolute tolerance values for DC current to prevent damage or reduced reliability when current flows out of or into output pin.
Storage temperature	T _{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current is applied to the device.

Table 3-1. Terms Used in Absolute Maximum Ratings

Table 3-2. Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V50IN, VDD33, AVDD33, AVDD33IN1, AVDD33IN2, VDD10	Indicates the voltage range for normal logic operations occur when GND = 0 V.
High-level input voltage	V _{IH}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the high level states for normal operation of the input buffer.
		* If a voltage that is equal to or greater than the "Min." value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V _{IL}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the low level states for normal operation of the input buffer.
		* If a voltage that is equal to or lesser than the "Max." value is applied, the input voltage is guaranteed as low level voltage.
Hysteresis voltage	V _H	Indicates the differential between the positive trigger voltage and the negative trigger voltage.
Input rise time	T _{ri}	Indicates the limit value for the time period when an input voltage applied to the input pins of the device rises from 10 % to 90 %.
Input fall time	T _{fi}	Indicates the limit value for the time period when an input voltage applied to the input pins of the device falls from 90 % to 10 %.
Operating temperature	T _A	Indicates the ambient temperature range for normal logic operations.



Parameter	Symbol	Meaning
Off-state output leakage current	I _{oz}	Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance.
Input leakage current	I,	Indicates the current that flows when the input voltage is supplied to the input pin.
High-level output voltage	Vol	Indicates the output voltage at low level and when the output pin is open.
Low-level output voltage	Vон	Indicates the output voltage at high level and when the output pin is open.

Table 3-3. Term Used in DC Characteristics



3.3 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Units
Power supply voltage	V50IN		-0.5 to +5.5	V
	VDD33 VDDGPIO AVDD33 AVDD33IN1 AVDD33IN2		-0.5 to +4.6	V
	VDD10		–0.5 to +1.4	V
Input voltage, 3.3 V buffer	V	$V_1 < VDD33/VDDGPIO + 0.5 V$	-0.5 to +4.6	V
Input voltage, 5 V tolerant buffer	V,	V50IN > 4.0 V	-0.5 to +6.0	V
Output voltage, 3.3 V buffer	Vo	V_{o} < VDD33/VDDGPIO + 0.5 V	-0.5 to +4.6	V
Output voltage, 5 V tolerant buffer	V _o	V50IN > 4.0 V	-0.5 to +6.0	V
USB3/SATA differential signals	Vi/Vo	Vi/Vo < VDD10 + 0.5V	-0.5 to +1.4	V
Output current	I _o	4 mA type (5 V tolerant buffer)	10.35	mA
		6 mA type (3.3 V buffer)	16.9	mA
Storage temperature	T _{stg}		-65 to +125	°C

Table 3-4. Absolute Maximum Ratings

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.



3.4 Recommended Operating Ranges

Parameter	Symbol	Condition	Min.	Тур.	Max.	Units
Operating voltage	V50IN		4.0	5.0	5.25	V
	VDD33 ^{Note} AVDD33 ^{Note} AVDD33IN1 ^{Note} AVDD33IN2 ^{Note}		3.0	3.3	3.6	V
	VDDGPIO Note	3.3 V operation	3.0	3.3	3.6	V
		2.5 V operation	2.25	2.5	2.75	V
	VDD10		0.95	1.0	1.05	V
High-level input voltage	V _{IH}	Normal buffer 3.3 V	2		VDD33+0.3	V
		Normal buffer 2.5 V	TBD		TBD	
Low-level input voltage	V _{IL}	Normal buffer 3.3 V	-0.3		0.8	V
		Normal buffer 2.5 V	TBD		TBD	
Positive trigger voltage	V _P	Schmitt buffer 3.3 V	0.9		2.1	V
		Schmitt buffer 2.5 V	TBD		TBD	
Negative trigger voltage	V _N	Schmitt buffer 3.3 V	0.7		1.9	V
		Schmitt buffer 2.5 V	TBD		TBD	
Hysteresis voltage	V _H	Schmitt buffer 3.3 V	0.2		1.4	V
		Schmitt buffer 2.5 V	TBD		TBD	
Input rise time	T _{ri}	Normal buffer	0		200	ns
		Schmitt buffer	0		1	ms
Input fall time	Τ _{fi}	Normal buffer	0		200	ns
		Schmitt buffer	0		1	ms
Operating ambient temperature	T _A		0		+85	°C

Note VDD33, AVDD33, AVDD33IN1, AVDD33IN2 and VDDGPIO must turn on/off at the same time and should be stable within 100 ms from the fastest rising edge of power sources.



3.5 DC Characteristics (VDD33 = $3.3 \text{ V} \pm 10\%$, T_A = 0 to +85 °C)

Parameter	Symbol	Condition		Min.	Max.	Units
Off-state output current	I _{oz}	V ₁ = VDD33/VDDGPIO or GND			±8	μA
Low-level output current	I _{ol}	$V_{oL} = 0.4 V$	6 mA type	6		mA
			4 mA type	4		mA
High-level output current	I _{oh}	V _{OH} = 2.4 V	6 mA type	-6		mA
			4 mA type	-4		mA
Input leakage current	I,	V ₁ = VDD33/VDDGPIO or GND	Normal input		±5	μA
		$V_1 = GND$	With pull-up resistor (50 k Ω)	24	78	μA
		V ₁ = VDD33/VDDGPIO	With pull-down resistor (50 k Ω)	24	78	μA

Table 3-6. DC Characteristics

 $\label{eq:Remark} \textbf{Remark} \quad \mbox{For pins with internal pull-up, the internal pull-up assures that when the pin is open, the pin voltage will be greater than the V_{\tiny H}$ level.

Parameter	Symbol	Conditions	Min.	Max.	Unit
Output pin impedance	ZHSDRV		40.5	49.5	Ω
Termination voltage for upstream facing	VTERM		3.0	3.6	V
port pull-up (RPU)					
Input Levels for Full-speed:		_			_
High-level input voltage (drive)	Vін		2.0		V
High-level input voltage (floating)	VIHZ		2.7	3.6	V
Low-level input voltage	VIL			0.8	V
Differential input sensitivity	VDI	(D+) – (D–)	0.2		V
Differential common mode range	Vсм	Includes VDI range	0.8	2.5	V
Output Levels for Full-speed:					
High-level output voltage	Vон	R∟ of 14.25 kΩ to GND	2.8	3.6	V
Low-level output voltage	Vol	R∟ of 1.425 kΩ to 3.6 V	0.0	0.3	V
SE1	V _{OSE1}		0.8		V
Output signal crossover point voltage	VCRS		1.3	2.0	V
Input Levels for High-speed:					
High-speed squelch detection threshold (differential signal)	VHSSQ		100	150	mV
High-speed data signaling common mode voltage range	VHSCM		-50	+500	mV
High-speed differential input signaling level	See Figure	e 3-2.			

Table 3-7. USB Interface Block

(1/2)



					(2/2
Parameter	Symbol	Conditions	Min.	Max.	Unit
Output Levels for High-speed:	·				
High-speed idle state	VHSOI		-10	+10	mV
High-speed data signaling high	Vнsoн		360	440	mV
High-speed data signaling low	VHSOL		-10	+10	mV
Chirp J level (differential signal)	VCHIRPJ		700	1100	mV
Chirp K level (differential signal)	Vсніврк		-900	-500	mV















3.6 Pin Capacitance

Table 3-8. Pin Capacitance

Parameter	Symbol	Condition	Min.	Max.	Units
GPIO pin capacitance	C _{GPIO}			5	pF



3.7 AC Characteristics (VDD33 = $3.3 \text{ V} \pm 10\%$, T_A = 0 to +85 °C)

3.7.1 System Clock

Parameter	Symbol	Condition	Min.	Тур.	Max.	Units
Clock frequency	F _{CLK}	Crystal	–100 ppm	30	+100 ppm	MHz
Clock duty cycle	T _{duty}		40	50	60	%

Table 3-9. System Clock (XT1/XT2) Ratings

Remark Required accuracy of crystal or oscillator block includes initial frequency accuracy, the spread of Crystal capacitor loading, supply voltage, temperature and aging, etc.

3.7.2 System Reset

Table 3-10	System	Reset	Timinas
	System	neset	rinnigə

Parameter	Symbol	Condition	Min.	Max.	Units
Reset active time	Tresetb		1		μs

Remark RESETB shall be de-asserted after all power sources (excluding VBUS) and the system clock become stable.

3.7.3 GPIO

(1) SPI Type Serial Flash ROM interface

Table 3-11. SPI Type Serial Flash ROM Interface (SPI Mode 0)

Parameter	Symbol	Min.	Тур.	Max.	Units
SPISCK clock frequency	t _{spicyc}	1.5		15	MHz
SPISCK clock duty	t _{spidt}		50		%
SPISO setup time to SPISCK rising edge	t _{sdrsu}	2			ns
SPISO hold time to SPISCK rising edge	t _{sdrh}	3			ns
SPISI validate time from SPISCK falling edge	t _{sdwvalid}			1	ns





Figure 3-4. SPI Type Serial Flash ROM Interface

(2) Pulse Width Modulation (PWM) signal

Table 3-12. PWM Signals

Parameter	Symbol	Min.	Max.	Units
PWM 1/2 cycle time	t _{PWMCYC}	0.067	143,165,576.500	μs
PWM 1/2 high level width	t _{PWMWID}	0.033	143,165,576.467	μs

Note $t_{_{PWMCYC}}$ and $t_{_{PWMWID}}$ are controlled by 33.3 ns step.



Figure 3-5. PWM Signals Waveform



3.7.4 SATA Interface – Differential Transmitter (TX) Specifications

(Refer to Serial ATA Specification Revision 3.0 for more information)

Parameters	Symbol	Limit	S	SATA 3.0 Spec			
			Gen1i	Gen2i	Gen3i		
Sequencing Transient Voltage LL	V _{trans}	Min	—	—	-1.2	V	
		Max	—	—	1.2		
TX Pair Differential Impedance	Z _{diffTX}	Min	86	-	_	Ω	
		Max	115	_	_]	
TX Single-Ended Impedance	Z _{s-eTX}	Min	40		-	Ω	
TX Differential Mode Return Loss (all values Min)	RL _{DD11,TX}	75 MHz- 150 MHz	14	_		dB	
		150 MHz- 300 MHz	8	14	_		
		300 MHz- 600 MHz	6	8	-		
		600 MHz- 1.2 GHz	6	6	_		
		1.2 GHz- 2.4 GHz	3	6	-		
		2.4 GHz- 3.0 GHz	1	3	-		
		3.0 GHz- 5.0 GHz	-	1	_		
TX Differential Mode Return Loss Start for slope	RL _{DD11,TX}	Min at 300 MHz	_	_	14	dB	
Slope of TX Differential Mode Return Loss		Nom	—	—	-13	dB/dec	
TX Differential Mode Return Loss Max Frequency		Max	_	-	3	GHz	
TX Common Mode Return Loss (all values Min)	RL _{CC11,TX}	150 MHz- 300 MHz	-	8	_	dB	
		300 MHz- 600 MHz	-	5	_		
		600 MHz- 1.2 GHz	-	2	-		
		1.2 GHz- 2.4 GHz	_	1	_		
		2.4 GHz- 3.0 GHz	_	1	_		
		3.0 GHz- 5.0 GHz	-	1	_		

Table 3-13.	Differential Transmitter Specification	(1/2)
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Parameters	Symbol	Limit	SATA 3.0 Spec		Units	
			Gen1i	Gen2i	Gen3i	
TX Impedance Balance (all values Min)	RL _{DC11,TX}	150 MHz- 300 MHz	_	30	30	dB
		300 MHz- 600 MHz	_	20	30	
		600 MHz- 1.2 GHz	_	10	20	
		1.2 GHz- 2.4 GHz	_	10	10	
		2.4 GHz- 3.0 GHz	_	4	10	
		3.0 GHz- 5.0 GHz	_	4	4	
		5.0 GHz- 6.5 GHz	-	-	4	

 Table 3-13.
 Differential Transmitter Specification (2/2)

3.7.5 SATA Interface – Differential Receiver (RX) Specifications

(Refer to Serial ATA Specification Revision 3.0 for more information)

Parameters	Symbol	Limit	S	Units		
			Gen1i	Gen2i	Gen3i	
RX Pair Differential Impedance	Z _{diffRX}	Min	85	_	-	Ω
		Мах	115	-	_	
RX Single-Ended Impedance	Z _{s-eRX}	Min	40	-	_	Ω
RX Differential Mode Return Loss (all values Min)	RL _{DD11,RX}	75 MHz- 150 MHz	18	_	-	dB
		150 MHz- 300 MHz	14	18	_	
		300 MHz- 600 MHz	10	14	_	
		600 MHz- 1.2 GHz	8	10	_	
		1.2 GHz- 2.4 GHz	3	8	-	
		2.4 GHz- 3.0 GHz	1	3	_	
		3.0 GHz- 5.0 GHz	_	1	-	

 Table 3-14.
 Differential Receiver Specification (1/2)



Parameters	Symbol	Limit	SATA 3.0 Spec			Units
			Gen1i	Gen2i	Gen3i	
RX Differential Mode Return Loss	RL _{dd11,RX}	Min at 300 MHz	_	_	18	dB
Slope of RX Differential Mode Return Loss		Nom	_	_	-13	dB/dec
RX Differential Mode Return Loss Max Frequency		Max	-	_	6	GHz
RX Common Mode Return Loss (all values Min)	RL _{CC11,RX}	150 MHz- 300 MHz	_	5	-	dB
		300 MHz- 600 MHz	_	5	_	
		600 MHz- 1.2 GHz	_	2	_	
		1.2 GHz- 2.4 GHz	_	1	-	
		2.4 GHz- 3.0 GHz	_	1	_	
		3.0 GHz- 5.0 GHz	_	1	-	
RX Impedance Balance (all values Min)	RL _{DC11,RX}	150 MHz- 300 MHz	_	30	30	dB
		300 MHz- 600 MHz	_	30	30	
		600 MHz- 1.2 GHz	_	20	20	
		1.2 GHz- 2.4 GHz	_	10	10	
		2.4 GHz- 3.0 GHz	-	4	4	
		3.0 GHz- 5.0 GHz	_	4	4	
		5.0 GHz- 6.5 GHz	_	4	4	

Table3-14.	Differential	Receiver	Specification	(2/2)
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3.7.6 USB3.0 SuperSpeed Interface – Differential Transmitter (TX) Specifications

(Refer to Universal Serial Bus 3.0 Specification Revision 1.0 for more information)

Parameter	Symbol	Min	Max	Units
Unit Interval	UI	199.94	200.06	ps
Differential p-p Tx voltage swing	V _{TX-DIFF-PP}	0.8	1.2	V
Tx de-emphasis	V _{TX-DE-RATIO}	3.0	4.0	dB
DC differential impedance	R _{TX-DIFF-DC}	72	120	Ω
The amount of voltage change allowed during Receiver Detection	V _{TX-RCV-DETECT}		0.6	V
AC Coupling Capacitor	C _{AC-COUPLING}	75	200	nF
Maximum slew rate	t _{CDR-SLEW-MAX}		10	ms/s

Table 3-15. T	ransmitter N	lormative	Electrical	Parameters
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Parameter	Symbol	Min	Max	Units
Deterministic min pulse	t _{min-Pulse-Dj}	0.96		UI
Tx min pulse	t _{min-pulse-tj}	0.90		UI
Transmitter Eye	t _{TX-EYE}	0.625		UI
Tx deterministic jitter	t _{TX-DJ-DD}		0.205	UI
Tx input capacitance for return loss	C _{TX-PARASITIC}		1.25	pf
Transmitter DC common mode impedance	R _{TX-DC}	18	30	Ω
Transmitter short-circuit current limit	I _{TX-SHORT}		60	mA
Transmitter DC common-mode voltage	V _{TX-DC-CM}	0	2.2	V
Tx AC common mode voltage	V _{TX-CM-AC-PP-ACTIVE}		100	mVp-p
Absolute DC Common Mode Voltage between U1 and U0	V _{TX-CM-DC-ACTIVE-IDLE-DELTA}		200	mV
Electrical Idle Differential Peak- Peak Output voltage	V _{TX-IDLE-DIFF-AC-pp}	0	10	mV
DC Electrical Idle Differential Output Voltage	V _{TX-IDLE-DIFF-DC}	0	10	mV

Table 3-16.	Transmitter Informative Electrical Parameters

3.7.7 USB3.0 SuperSpeed Interface – Differential Receiver (RX) Specifications

(Refer to Universal Serial Bus 3.0 Specification Revision 1.0 for more information)

Parameter	Symbol	Min	Max	Units
Unit Interval	UI	199.94	200.06	ps
Receiver DC common mode impedance	R _{RX-DC}	18	30	Ω
DC differential impedance	R _{RX-DIFF-DC}	72	120	Ω
DC Input CM Input Impedance for V>0 during Reset of Power down	Z _{RX-HIGH-IMP-DC-POS}	25k		Ω
LFPS Detect Threshold	V _{RX-LFPS-DET-DIFF-p-p}	100	300	mV

Table 3-17. Receiver Normative Electrical Parameters

 Table 3-18.
 Receiver Informative Electrical Parameters

Parameter	Symbol	Min	Max	Units
Differential Rx peak-to-peak voltage	V _{RX-DIFF-PP-POST-EQ}	30		mV
Max Rx inherent timing error	T _{RX-Tj}		0.45	UI
Max Rx inherent deterministic timing error	T _{RX-DJ-DD}		0.285	UI
Rx input capacitance for return loss	C _{RX-PARASITIC}		1.1	pF
Rx AC common mode voltage	V _{RX-CM-AC-P}		150	mVPeak
Rx AC common mode voltage during the U1 to U0 transition	V _{RX-CM-DC-ACTIVE-IDLE-DELTA-P}		200	mVPeak



3.7.8 USB2.0 Interface

(Refer to Universal Serial Bus Specification Revision 2.0 for more information)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Rise time (10 to 90%)	tfr	C∟ = 50 pF	4	20	ns
Fall time (90 to 10%)	tff	C∟ = 50 pF	4	20	ns
Differential rise and fall time matching	t FRFM	(tfr/tff)	90	111.11	%
Full-speed data rate	t FDRATHS	Average bit rate	11.9940	12.0060	Mbps
Frame interval	t FRAME		0.9995	1.0005	ms
Consecutive frame interval jitter	t RFI	No clock adjustment		42	ns
Source jitter total (including frequency tolerance): To next transition	t _{DJ1}		-3.5	+3.5	ns
For paired transitions	t _{DJ2}		-4.0	+4.0	ns
Source jitter for differential transition to SE0 transition	t fdeop		-2	+5	ns
Receiver jitter: To next transition For paired transitions	tjri tjr2		-18.5 -9	+18.5 +9	ns ns
Source SE0 interval of EOP	t feopt		160	175	ns
Receiver SE0 interval of EOP	t FEOPR		82		ns
Width of SE0 interval during differential transition	tfst			14	ns

Table 3-19. Full-speed Source Electrical Characteristics

Table 3-20. High-speed Source Electrical Characteristics

Parameter	Symbol	Conditions	Min.	Max.	Unit
Rise time (10 to 90%)	t HSR		500		ps
Fall time (90 to 10%)	thsf		500		ps
Driver waveform	See Figure	3-6.			
High-speed data rate	t hsdrat		479.760	480.240	Mbps
Microframe interval	t HSFRAM		124.9375	125.0625	μs
Consecutive microframe interval difference	thsrfi			4 high- speed	Bit times
Data source jitter	See Figure	3-6.			
Receiver jitter tolerance	See Figure	3-2.			



Parameter	Symbol	Conditions	Min.	Max.	Unit
Time from internal power good to device	t sigatt			100	ms
pulling D+ beyond V _{IHZ} (min.) (signaling					
attached)					
Debounce interval provided by USB	t attdb			100	ms
system software after attach					
Inter-packet delay for full-speed	tipd		2		Bit times
Inter-packet delay for device response	t RSPIPD1			6.5	Bit times
w/detachable cable for full-speed					
Time for which a suspended high-speed	t FILTSE0		2.5		μs
capable device must see a continuous					
SE0 before beginning the high-speed					
detection handshake					
Time a high-speed capable device	t WTRSTFS		2.5	3000	μs
operating in non-suspended full-speed					
must wait after start of SE0 before					
beginning the high-speed detection					
handshake					
Time a high-speed capable device	t wtrev		3.0	3.125	ms
operating in high-speed must wait after					
start of SE0 before reverting to full-speed					
Time a device must wait after reverting to	twrrsths		100	875	μs
full-speed before sampling the bus state					
for SE0 and beginning the high-speed					
detection handshake					
Minimum duration of a Chirp K from a	tucн		1.0		ms
high-speed capable device within the					
reset protocol					
Time after start of SE0 by which a high-	t UCHEND			7.0	ms
speed capable device is required to have					
completed its Chirp K within the reset					
protocol					
Time between detection of downstream	twтнs			500	μs
chirp and entering high-speed state					
Time after end of upstream chirp at which	twrfs		1.0	2.5	ms
device reverts to fullspeed default state if					
no downstream chirp is detected					

Table 3-21.	Device	Event	Timings
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Figure 3-6. Transmit Waveform for Transceiver at U2DP/U2DM













Figure 3-9. USB Differential-to-EOP Transition Skew and EOP Width for Full-speed







3.8 Power Consumption

3.8.1 Power consumption with on-chip switching regulator

Cumbol	Condition	V50IN	V50IN	Linita
Symbol	Condition	(Bus-power setting)	(Self-power setting)	Units
${\sf P}_{{\rm SS_U0Uncnf}}$	USB Unconfigured state			
	with SATA Slumber	63	63	mA
P_{SS_UODT}	Data transfer at SuperSpeed			
	with SATA Gen3	126	126	mA
	with SATA Gen2	116	116	mA
	with SATA Gen1	108	108	mA
P _{ss_u3}	USB3.0 U3 state	2.0	5.6	mA

Table 3-22.	Power Consumption in	SuperSpeed	Operation Mode

Typical condition: $T_A = 25 \text{ °C}$, V50IN = 5.0 V

Note 1. On-chip switching regulator is cascaded to on-chip LDO.

Table 3-23.	Power Consum	ption in High-s	peed Operation Mode

Symbol	Condition	V50IN	V50IN	Unite	
Symbol	Condition	(Bus-power setting)	(Self-power setting)	Units	
Р	USB Unconfigured state				
P _{HS_L0Uncnf}	with SATA Slumber	66	66	mA	
P_{HS_LODT}	Data transfer at High-Speed				
	with SATA Gen1	122	122	mA	
$P_{_{HS_U3}}$	USB2.0 L2	2.2	5.8	mA	

Typical condition: $T_A = 25 \text{ °C}$, V50IN = 5.0 V

Note 1. On-chip switching regulator is cascaded to on-chip LDO.



3.8.2 Power consumption without on-chip switching regulator

Symbol	Condition	Bus-power setting		Self-power setting		Units
Cymbol	Contaition	VDD10	V50IN	VDD10	V50IN	Onno
P _{SS_U0Uncnf}	USB Unconfigured state					
	with SATA Slumber	140	14	140	14	mA
P _{SS_UODT}	Data transfer at SuperSpeed					
	with SATA Gen3	270	24	270	24	mA
	with SATA Gen2	245	24	245	24	mA
	with SATA Gen1	228	24	228	24	mA
P_{SS_U3}	USB3.0 U3 state	1.2	0.9	1.7	2.5	mA

 Table 3-24.
 Power Consumption in SuperSpeed Operation Mode

Typical condition: $T_A = 25 \text{ °C}$, VDD10=1.0 V, V50IN = 5.0 V

Note 1. Power consumption of 3.3 V(VDD33, AVDD33, AVDD33IN1, AVDD33IN2) is included in V50IN.

Table 3-25. Power Consumption in Fight-speed Operation mode						
Symbol	Condition Bus-power setting Self-power setting		er setting	Linite		
		VDD10	V50IN	VDD10	V50IN	Onito
D	USB Unconfigured state					
HS_L0Uncnf	with SATA Slumber	62	42	62	42	mA
$P_{\text{HS}_\text{LODT}}$	Data transfer at High-Speed					
	with SATA Gen1	150	68	150	68	mA
P_{HS_L2}	USB2.0 L2 (Suspend) state	1.2	1.1	1.7	2.6	mA

 Table 3-25.
 Power Consumption in High-speed Operation Mode

Typical condition: $T_A = 25 \ ^{\circ}C$, VDD10 = 1.0 V, V50IN = 5.0 V

Note 1. Power consumption of 3.3 V(VDD33, AVDD33, AVDD33IN1, AVDD33IN2) is included in V50IN.



4. PACKAGE DRAWINGS

• *µ*PD720231AK8-612-BAE-A





5. RECOMMENDED SOLDERING CONDITIONS

The μ PD720231A should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact a Renesas Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.renesas.com/prod/package/manual/)

• μPD720231AK8-612-BAE-A : 48-pin QFN (6x6)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Peak package's surface temperature: 260 °C, Reflow time: 60 seconds or less	
	(220 °C or higher), Maximum allowable number of reflow processes: 3,	
	Exposure limit ^{Note} : 7 days (10 to 72 hours pre-backing is required at 125C° afterwards),	
	Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended.	
	<caution></caution>	
	Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	

Note The Maximum number of days during which the product can be stored at a temperature of 25 °C and a relative humidity of 65 % or less after dry-pack package is opened.



REVISION HISTORY	μ PD720231A Data Sheet
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Rev.	Date	Description		
		Page	Summary	
0.01	Mar 15, 2013	-	First Edition issued	
0.02	Apr 10, 2013	P7	P7 Added GPIO signal state during reset and after reset.	
		P8	Corrected buffer type of GPIO pins.	
1.00	Jul 29, 2013	_	Document promoted from Preliminary Data to full Data.	

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