User's Manual

μPD720231

User's Manual: Hardware

USB3.0 to SATA3 BRIDGE CONTROLLER

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NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

PREFACE

Readers

This manual is intended for engineers who need to be familiar with the capability of the μPD720231 in order to develop application systems based on it.

Purpose

The purpose of this manual is to help users understand the hardware capabilities (listed below) of the μPD720231.

Configuration

This manual consists of the following chapters:

- Overview
- Pin functions
- Endpoint configuration
- USB descriptor information
- External Serial ROM information
- General Purpose I/O
- Security features
- How to Connect to External Elements

Guidance

Readers of this manual should already have a general knowledge of electronics, logic circuits, and microcomputers.

Notation

This manual uses the following conventions:

Data bit significance:	High-order bits on the left side; Low-order bits on the right side
Active low:	XXXXB (Pin and signal names are suffixed with B.)
Note:	Explanation of an indicated part of text
Caution:	Information requiring the user's special attention
Remark:	Supplementary information
Numerical value:	Binary ... xxxx or xxxxb Decimal ... xxxx Hexadecimal ... xxxxh

Related Document

Use this manual in combination with the following document.
The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- μPD720231 Data Sheet: R19DS0073E

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1. Overview

The μPD720231 is a USB3.0 to SATA3 Bridge LSI which complies with Universal Serial Bus 3.0 (USB3.0) Specification Revision 1.0 and Serial ATA (SATA) Specification Revision 3.0. The LSI is integrated USB3.0 function controller and SATA III host controller with USB3.0 transceiver, USB2.0 transceiver and SATA III transceiver into one chip. The USB3.0 transceiver supports SuperSpeed (SS) 5 Gbps. USB2.0 transceiver supports High-Speed (HS) 480 Mbps and Full-Speed (FS) 12 Mbps. And SATA III transceiver supports Gen1 1.5 Gbps / Gen2 3 Gbps / Gen3 6 Gbps.

1.1 Features

- Compliant with Universal Serial Bus 3.0 Specification Revision 1.0
  - Certified by USB Implementers Forum (TID: 340840002)
  - Supports Super/High-/Full-speed
  - Supports Mass Storage Class UASP (USB Attached SCSI Protocol)
  - Supports Mass Storage Class BOT (Bulk Only Transport)
  - Includes SCSI Command hardware accelerator
  - Supported number of stream is 32 + Task management.
- Compliant with Serial ATA Specification Revision 3.0.
  - Supports Gen1 / Gen2 / Gen3
  - Supports Host initiated power management
  - Supports multiple LUN
  - Be capable of providing full ATA-8, 48-Bit LBA support, for drives larger than 2TB.
- Supports power management
  - USB3.0 U1/U2/U3 state
  - USB2.0 Suspend/LPM
- Integrated 32-bit RISC CPU
- 10 configurable GPIOs including
  - SPI interface for serial flash ROM.
  - Two PWM interface
  - Multi voltage level support
- Clock input: 30 MHz crystal
- On-chip reset circuit to remove external power-on-reset circuit
- Power supply: 5 V single power supply, using 2 internal regulators
  - On-chip 1.0 V and 3.3 V regulator
- Package: 48-pin QFN (6 x 6 mm)

1.2 Applications

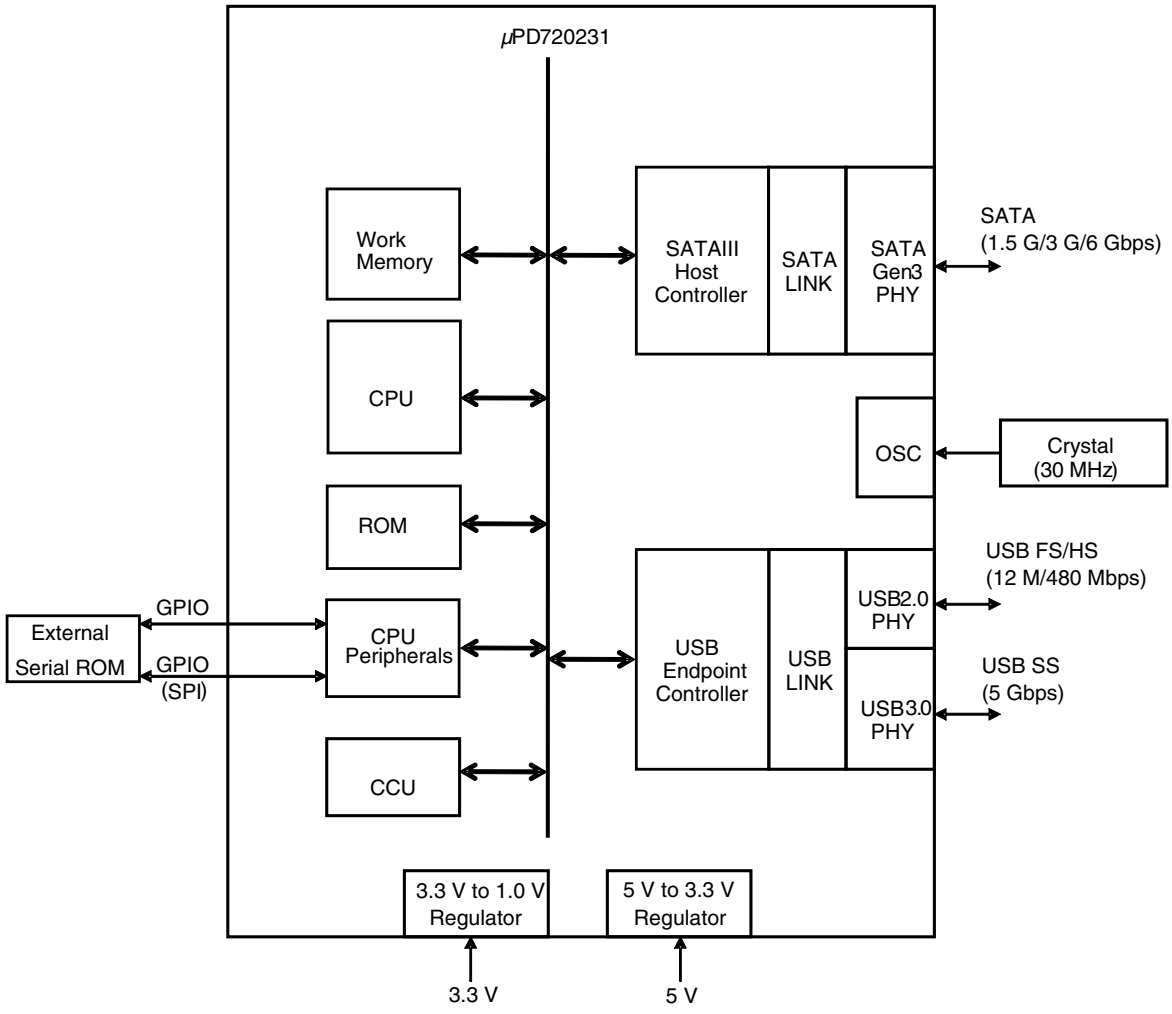
External USB hard disk and USB hard disk enclosure,optical drive, etc.

1.3 Ordering Information

Part Number	Package	Remark
μPD720231K8-611-BAE-A	48-pin QFN (6 x 6)	Lead-free product

1.4 Block Diagram

Figure 1-1. μPD720231 Block Diagram

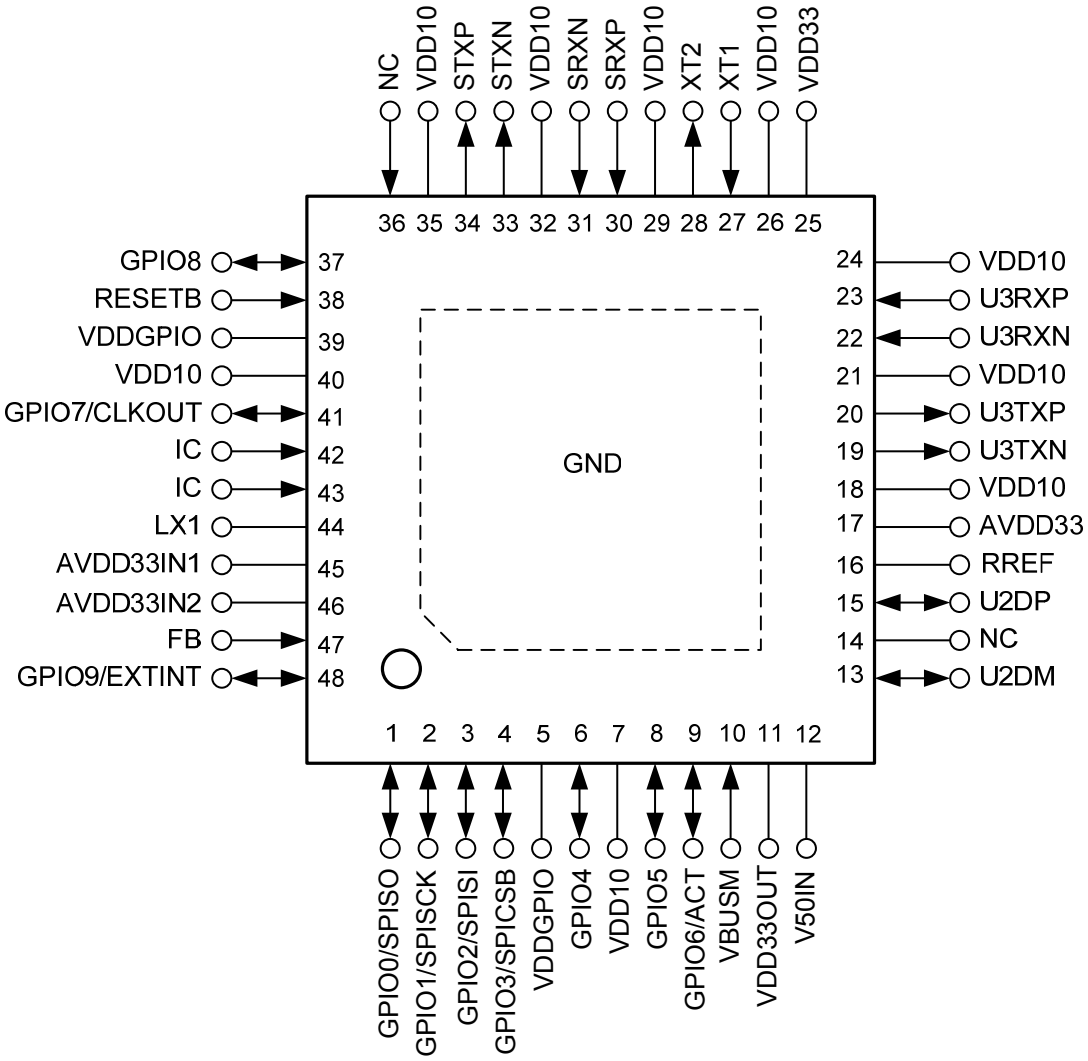


CPU	Integrated 32bit RISC CPU.
CPU Peripherals	Includes bus controller, interrupt controller, timer, GPIO and so on.
Work RAM	Integrated Work RAM for data.
ROM	Integrated Boot ROM.
SATA III Host Controller	The SATA III host supports SATA Gen1 1.5 Gbps, Gen2 3.0 Gbps, and Gen3 6.0 Gbps. Dedicated bus realizes SuperSpeed interface between SATA III host and Direct Command Controller.
SATA LINK	Link layer translates data packets between SATA host and SATA PHY.
SATA Gen3 PHY	Integrated SATAIII Gen1 1.5Gbps, Gen2 3.0Gbps, and Gen3 6.0 Gbps compliance transceiver. This is controlled by SATAIII host.
USB Endpoint Controller (EPC)	Transport / Protocol layer. This block supports USB Mass Storage class USB Attached SCSI Protocol and Bulk Only Transport.
USB LINK	Link layer defined in USB specification, which maintains Link connectivity with USB host controller and hub.
USB3.0 PHY	For SuperSpeed Tx/Rx
USB2.0 PHY	For USB High/Full-speed Tx/Rx
CCU	Integrated clock controller to manage system power consumption, and system reset controller.
OSC	Internal oscillator block.
3.3 V to 1.0 V Regulator	Regulator to convert 3.3 V to 1.0 V
5 V to 3.3 V Regulator	Regulator to convert 5 V to 3.3 V

1.5 Pin Configuration

- **48-pin QFN (6 x 6)**
  μPD720231K8-611-BAE-A

Figure 1-2. Pin Configuration (Top View)



2. Pin Function

This section describes each pin's function.

2.1 Power supply and regulator

Table 2-1. Power Supply

Pin Name	Pin No.	Buffer Type	Function
VDD33	25	Power	+3.3 V power supply
VDDGPIO	5, 39	Power	+3.3 V power supply for GPIOs, except for GPIO5 and GPIO6/ACT.
AVDD33	17	Power	+3.3 V power supply for USB analog circuit
VDD10	7, 18, 21, 24, 26, 29, 32, 35, 40	Power	+1.0 V power supply
V50IN	12	Regulator	+5 V input for internal LDO.
VDD33OUT	11	Regulator	+3.3 V output from internal LDO.
AVDD33IN1 Note	45	Regulator	+3.3 V power supply for regulator analog circuit
AVDD33IN2 Note	46	Regulator	+3.3 V power supply for regulator analog circuit
LX1	44	Regulator	1.0 V output from the on-chip regulator
FB	47	Regulator	Feedback for regulator.
GND	Die PAD	–	Connect to ground for digital circuit

Note It is mandatory to put ceramic capacitors (22 μF is recommended) on AVDD25IN1 and AVDD25IN2. Common impedance coupling between AVDD25IN1 and AVDD25IN2 must be avoided.

2.2 Analog Signal

Table 2-2. Analog Signal

Pin Name	Pin No.	Direction	Buffer Type	Active Level	Function
RREF	16	–	USB2	–	This pin must be connected to GND via a 1.6k-ohm resistor with 1 % precision.

2.3 VBUS

Table 2-3. VBUS and Regulator

Pin Name	Pin No.	Direction	Buffer Type	Active Level	Function
VBUSM	10	I	5 V tolerant buffer	High	VBUS detection.

2.4 System Clock and Reset

Table 2-4. System Clock and Reset

Pin Name	Pin No.	Direction	Buffer Type	Active Level	Function
XT1	27	I	OSC	–	30 MHz oscillator input. Connect to a 30 MHz crystal.
XT2	28	O	OSC	–	30 MHz oscillator output. Connect to a 30 MHz crystal.
RESETB	38	I	3.3/2.5 V schmitt input with 50 kΩ pull-up resistor	Low	System reset

2.5 USB Interface

Table 2-5. USB Interface

Pin Name	Pin No.	Direction	Buffer Type	Active Level	Function
U3RXP	23	I	USB3	–	USB3.0 receive data D+ signal for SuperSpeed
U3RXN	22	I	USB3	–	USB3.0 receive data D– signal for SuperSpeed
U3TXP	20	O	USB3	–	USB3.0 transmit data D+ signal for SuperSpeed
U3TXN	19	O	USB3	–	USB3.0 transmit data D– signal for SuperSpeed
U2DP	15	I/O	USB2	–	USB2.0 D+ signal for High-/Full-speed
U2DM	13	I/O	USB2	–	USB2.0 D– signal for High-/Full-speed

2.6 Serial ATA Interface

Table 2-6. Serial ATA Interface

Pin Name	Pin No.	Direction	Buffer Type	Active Level	Function
SRXP	30	I	SATA III	–	Serial ATA receive data D+ signal
SRXN	31	I	SATA III	–	Serial ATA receive data D– signal
STXP	34	O	SATA III	–	Serial ATA transmit data D+ signal
STXN	33	O	SATA III	–	Serial ATA transmit data D– signal

2.7 General Purpose I/O Interface

Table 2-7. General Purpose I/O Interface

Pin Name	Pin No.	Direction	Buffer Type	Active Level	Function
GPIO0/ SPISO	1	I/O	3.3/2.5 V I/O	–	General purpose I/O or SPI read data signal
GPIO1/ SPISCK	2				General purpose I/O or SPI clock
GPIO2/ SPISI	3				General purpose I/O or SPI write data signal
GPIO3/ SPICSB	4				General purpose I/O or SPI chip select for the external serial ROM.
GPIO4	6				General purpose I/O Default low drive. Note2
GPIO5 Note1	8		5 V tolerant buffer		General purpose I/O
GPIO6/ACT Note1	9				General purpose I/O or Disk Activity LED
GPIO7/CLKOUT	41		3.3/2.5 V I/O		General purpose I/O or 30 MHz clock output
GPIO8	37				General purpose I/O
GPIO9/EXTINT	48				General purpose I/O or external interrupt such as push button input

Note 1. Except for GPIO5 and GPIO6, all the other GPIOs are supplied power from VDDGPIO. GPIO5 and GPIO6 are supplied power from internal VDD33 line.

2. GPIO4 drives low in default. Other GPIO signals are open state in default.

2.8 Renesas private signal

Table 2-8. Test signal

Pin Name	Pin No.	Direction	Buffer Type	Active Level	Function
IC	42, 43	I	–	–	Test signal. These pins must be connected to GND or left opened.
NC	14, 36	–	–	–	Non connection pin. This pin should be opened.

3. Endpoint Configuration

The μPD720231 is capable of working in either USB Mass Storage Class Bulk Only Transport protocol (BOT) or UAS protocol (UASP) both in SS/HS mode. Configuration Interface, Alternate Setting for each speed mode is shown in table below.

If UASP driver is not supported in the system, μPD720231 works as BOT device.

Table 3-1. Configuration Interface, Alternate Setting for each speed mode

Speed mode	Configuration	Interface	Alternate Setting	Endpoint	Protocol
Super-speed	1	0	0	1: Bulk-OUT 2: Bulk-IN	BOT
			1	1: Bulk-OUT (Stream) 2: Bulk-IN (Stream) 3: Bulk-OUT 4: Bulk-IN (Stream)	UASP
High-speed	1	0	0	1: Bulk-OUT 2: Bulk-IN	BOT
			1	1: Bulk-OUT (Stream) 2: Bulk-IN (Stream) 3: Bulk-OUT 4: Bulk-IN (Stream)	UASP
Full-speed	1	0	0	1: Bulk-OUT 2: Bulk-IN	BOT

3.1 Super-speed UASP Mode

Configuration for Super-speed UASP mode is show in Table 3-2.

Table 3-2. Configuration for Super-speed UASP mode

EP No.	Direction	Transfer type	Max Packet Size	Max Burst Size	Stream
0	IN/OUT	Control	512 bytes	1	–
1	OUT	Bulk	1024 bytes	16	Available
2	IN	Bulk	1024 bytes	16	Available
3	OUT	Bulk	1024 bytes	1	Not available
4	IN	Bulk	1024 bytes	1	Available

3.2 Super-speed BOT Mode

Configuration for Super-speed BOT mode is show in Table 3-3.

Table 3-3. Configuration for Super-speed BOT mode

EP No.	Direction	Transfer type	Max Packet Size	Max Burst Size	Stream
0	IN/OUT	Control	512 bytes	1	–
1	OUT	Bulk	1024 bytes	16	Not available
2	IN	Bulk	1024 bytes	16	Not available

3.3 High-speed UASP Mode

Configuration for Super-speed UASP mode is show in Table 3-4.

Table 3-4. Configuration for Super-speed UASP mode

EP No.	Direction	Transfer type	Max Packet Size	Max Burst Size	Stream
0	IN/OUT	Control	64 bytes	1	–
1	OUT	Bulk	512 bytes	1	Not available
2	IN	Bulk	512 bytes	1	Not available
3	OUT	Bulk	512 bytes	1	Not available
4	IN	Bulk	512 bytes	1	Not available

3.4 High-speed BOT Mode

Configuration for High-speed BOT mode is show in Table 3-5.

Table 3-5. Configuration for High-speed BOT mode

EP No.	Direction	Transfer type	Max Packet Size	Max Burst Size	Stream
0	IN/OUT	Control	64 bytes	1	–
1	OUT	Bulk	512 bytes	1	Not available
2	IN	Bulk	512 bytes	1	Not available

3.5 Full-speed BOT mode

Configuration for Full-speed BOT mode is show in Table 3-6.

Table 3-6. Configuration for Full-speed BOT mode

EP No.	Direction	Transfer type	Max Packet Size	Max Burst Size	Stream
0	IN/OUT	Control	64 bytes	1	–
1	OUT	Bulk	64 bytes	1	Not available
2	IN	Bulk	64 bytes	1	Not available

4. USB Descriptor Information

This chapter describes the USB descriptors used in this device.

4.1 Device Descriptor (All speeds)

A device descriptor describes general information about a USB device. It includes information that applies globally to the device and the device's configuration.

Offset	Field	Size	Value	Description
0	bLength	1	12h	Size of descriptor
1	bDescriptorType	1	01h	Device descriptor type
2	bcdUSB	2	0300h or 0210h	USB specification version number (BCD) 0300h: Super-speed 0210h: High-/Full-speed
4	bDeviceClass	1	00h	Class Code
5	bDeviceSubClass	1	00h	SubClass Code
6	bDeviceProtocol	1	00h	Protocol Code
7	bMaxPacketSize0	1	09h or 40h	Maximum packet size for this speed. 09h: 512 bytes for Super-speed. 40h: 64 bytes for High/Full-speed
8	idVender	2	045Bh	Vender ID of Renesas Electronics
10	idProduct	2	021Fh/ 0220h	μPD720231's product ID 021Fh: UASP support 0220h: Bulk Only support
12	bcdDevice	2	0100h	Device release number (BCD)
14	iManufacturer	1	01h	Index of string descriptor describing manufacturer
15	iProduct	1	02h	Index of string descriptor describing product
16	iSerialNumber	1	03h	Index of string descriptor describing device's serial number.
17	bNumConfigurations	1	01h	Number of possible configuration

Remarks 1. The value of idVender, idProduct, and bcdDevice are loaded from the serial ROM or SATA device.

2. The value of iManufacturer, iProduct, and iSerialNumber are defined by data in the serial ROM or SATA device.

4.2 BOS (Binary device Object Store) Descriptor

The BOS descriptor defines a root descriptor that is similar to the configuration descriptor, and is the base descriptor for accessing a family of related descriptors.

Offset	Field	Size	Value	Description
0	bLength	1	05h	Size of descriptor
1	bDescriptorType	1	0Fh	BOS descriptor type
2	wTotalLength	2	0016h	Length of this descriptor and all of its sub descriptors
4	bNumDeviceCaps	1	02h	The number of separate device capability descriptors in the BOS.

4.2.1 USB2.0 Extension Descriptor (High-/Full-speed only)

A Super-speed device shall include the USB2.0 Extension descriptor and shall support LPM when operating in USB2.0 High-speed mode.

Offset	Field	Size	Value	Description
0	bLength	1	07h	Size of descriptor
1	bDescriptorType	1	10h	Device capability descriptor type
2	bDevCapabilityType	1	02h	Capability type: USB2.0 Extension
3	bmAttributes	4	00000002h	Link Power Management protocol supported

4.2.2 Super Speed USB Device Capability Descriptor (High-/Full-speed only)

Device Capability descriptors describe individual technology-specific or generic device-level capability.

Offset	Field	Size	Value	Description
0	bLength	1	0Ah	Size of descriptor
1	bDescriptorType	1	10h	Device capability descriptor type
2	bDevCapabilityType	1	03h	Capability type: Super Speed USB Device Capability
3	bmAttributes	1	00h	Latency Tolerance Messages not supported
4	wSpeedsSupported	2	000Eh	Super/High/Full-speed supported
6	bFuntionalitySupport	1	03h	Full functionality
7	bU1DevExitLat	1	0Ah	U1 Device Exit Latency
8	bU2DevExitLat	2	03E8h	U2 Device Exit Latency

4.3 Configuration Descriptor (All speeds)

A configuration descriptor describes information about a specific device configuration. When the host requests the configuration descriptor, all related interface and endpoint descriptors are returned.

Offset	Field	Size	Value	Description
0	bLength	1	09h	Size of descriptor
1	bDescriptorType	1	02h	Configuration descriptor type
2	wTotalLength	2	0079h	Total length
4	bNumInterfaces	1	01h	Number of interfaces supported by this configuration
5	bConfigurationValue	1	01h	Number of this configuration
6	iConfiguration	1	00h	Index of string descriptor describing configuration.
7	bmAttributes	1	C0h	Configuration characteristics. C0h: Self-powered
8	bMaxPower	1	12h (in Super-speed) 32h (in High-/Full-speed)	Maximum power consumption of the USB device from the bus in this configuration when the device is fully operational. Expressed in 2-mA units when the device is operating in High/Full-speed mode and in 8-mA units when operating in Super-speed mode.

4.4 Interface Descriptor

An interface descriptor describes a specific interface within a configuration. An interface descriptor is returned as part of the configuration information returned by a GET_DESCRIPTOR Configuration request.

4.4.1 Interface descriptor for BOT mode (All speeds)

Offset	Field	Size	Value	Description
0	bLength	1	09h	Size of descriptor
1	bDescriptorType	1	04h	Interface descriptor type
2	bInterfaceNumber	1	00h	Number of interface
3	bAlternateSetting	1	00h	Value used to select alternate setting for the interface identified in the prior field
4	bNumEndpoints	1	02h	Number of endpoints used by this interface
5	bInterfaceClass	1	08h	Class code: Mass Storage Class.
6	bInterfaceSubClass	1	06h or 02h	SubClass Code: SCSI Transport or ATAPI
7	bInterfaceProtocol	1	50h	Protocol Code: Bulk-Only Protocol
8	iInterface	1	00h	Index of string descriptor describing interface

4.4.2 Interface descriptor for UASP mode (Super-/High-speed only)

Offset	Field	Size	Value	Description
0	bLength	1	09h	Size of descriptor
1	bDescriptorType	1	04h	Interface descriptor type
2	bInterfaceNumber	1	00h	Number of supported interface
3	bAlternateSetting	1	01h	Value used to select alternate setting for the interface identified in the prior field
4	bNumEndpoints	1	04h	Number of endpoints used by this interface
5	bInterfaceClass	1	08h	Class code: Mass Storage Class.
6	bInterfaceSubClass	1	06h	SubClass Code: SCSI Transport
7	bInterfaceProtocol	1	62h	Protocol Code: USB Attached SCSI Protocol
8	iInterface	1	00h	Index of string descriptor describing interface

4.5 Endpoint Descriptor

Each endpoint used for an interface has its own descriptor. This descriptor contains the information required by the host to determine the bandwidth requirements of each endpoint. An endpoint descriptor is always returned as part of the configuration information returned by a GET_DESCRIPTOR Configuration request.

Each Super-speed endpoint described in an interface is followed by a SuperSpeed Endpoint Companion descriptor. This descriptor contains additional endpoint characteristics that are only defined for Super-speed endpoints.

4.5.1 BOT mode

4.5.1.1 Data-OUT

(1) Endpoint Descriptor (All speeds)

Offset	Field	Size	Value	Description
0	bLength	1	07h	Size of descriptor
1	bDescriptorType	1	05h	Endpoint descriptor type
2	bEndpointAddress	1	01h	Address: 1, Direction: OUT
3	bmAttributes	1	02h	Endpoint's attributes (Bulk)
4	wMaxPacketSize	2	0400h or 0200h or 0040h	Maximum packet size 0400h: 1024 bytes in Super-speed mode. 0200h: 512 bytes in High-speed mode. 0040h: 64 bytes in Full-speed mode.
6	bInterval	1	00h	Interval for polling endpoint for data transfers.

(2) SuperSpeed Endpoint Companion Descriptor (Super-speed only)

Offset	Field	Size	Value	Description
0	bLength	1	06h	Size of descriptor
1	bDescriptorType	1	30h	SUPERSPEED_USB_ENDPOINT_COMPANION descriptor type.
2	bMaxBurst	1	0Fh	Max. burst = 16
3	bmAttributes	1	00h	Stream not supported
4	wBytesPerInterval	2	0000h	–

4.5.1.2 Data-IN

(1) Endpoint Descriptor (All speeds)

Offset	Field	Size	Value	Description
0	bLength	1	07h	Size of descriptor
1	bDescriptorType	1	05h	Endpoint descriptor type
2	bEndpointAddress	1	82h	Address: 2, Direction: IN
3	bmAttributes	1	02h	Endpoint's attributes (Bulk)
4	wMaxPacketSize	2	0400h or 0200h or 0040h	Maximum packet size 0400h: 1024 bytes in Super-speed mode. 0200h: 512 bytes in High-speed mode. 0040h: 64 bytes in Full-speed mode.
6	bInterval	1	00h	Interval for polling endpoint for data transfers.

(2) SuperSpeed Endpoint Companion Descriptor (Super-speed only)

Offset	Field	Size	Value	Description
0	bLength	1	06h	Size of descriptor
1	bDescriptorType	1	30h	SUPERSPEED_USB_ENDPOINT_COMPANION descriptor type.
2	bMaxBurst	1	0Fh	Max. burst=16
3	bmAttributes	1	00h	Stream not supported
4	wBytesPerInterval	2	0000h	–

4.5.2 UASP mode (Super-/High-speed only)

4.5.2.1 Data-OUT

(1) Endpoint Descriptor

Offset	Field	Size	Value	Description
0	bLength	1	07h	Size of descriptor
1	bDescriptorType	1	05h	Endpoint descriptor type
2	bEndpointAddress	1	01h	Address: 1, Direction: OUT
3	bmAttributes	1	02h	Endpoint's attributes (Bulk)
4	wMaxPacketSize	2	0400h or 0200h	Maximum packet size 0400h: 1024 bytes in Super-speed mode. 0200h: 512 bytes in High-speed mode.
6	bInterval	1	00h	Interval for polling endpoint for data transfers.

(2) SuperSpeed Endpoint Companion Descriptor (Super-speed only)

Offset	Field	Size	Value	Description
0	bLength	1	06h	Size of descriptor
1	bDescriptorType	1	30h	SUPERSPEED_USB_ENDPOINT_COMPANION descriptor type.
2	bMaxBurst	1	0Fh	Max. burst = 16
3	bmAttributes	1	05h	Max. stream = 32.
4	wBytesPerInterval	2	0000h	–

(3) Pipe Usage Descriptor

Offset	Field	Size	Value	Description
0	bLength	1	04h	Size of descriptor
1	bDescriptorType	1	24h	Pipe Usage descriptor type.
2	bPipeID	1	04h	Data-OUT pipe
3	Reserved	1	00h	–

4.5.2.2 Data-IN

(1) Endpoint Descriptor

Offset	Field	Size	Value	Description
0	bLength	1	07h	Size of descriptor
1	bDescriptorType	1	05h	Endpoint descriptor type
2	bEndpointAddress	1	82h	Address: 2, Direction: IN
3	bmAttributes	1	02h	Endpoint's attributes (Bulk)
4	wMaxPacketSize	2	0400h or 0200h	Maximum packet size 0400h: 1024 bytes in Super-speed mode. 0200h: 512 bytes in High-speed mode.
6	bInterval	1	00h	Interval for polling endpoint for data transfers.

(2) SuperSpeed Endpoint Companion Descriptor (Super-speed only)

Offset	Field	Size	Value	Description
0	bLength	1	06h	Size of descriptor
1	bDescriptorType	1	30h	SUPERSPEED_USB_ENDPOINT_COMPANION descriptor type.
2	bMaxBurst	1	0Fh	Max. burst = 16
3	bmAttributes	1	05h	Max. stream = 32.
4	wBytesPerInterval	2	0000h	–

(3) Pipe Usage Descriptor

Offset	Field	Size	Value	Description
0	bLength	1	04h	Size of descriptor
1	bDescriptorType	1	24h	Pipe Usage descriptor type.
2	bPipeID	1	03h	Data-IN pipe
3	Reserved	1	00h	–

4.5.2.3 UASP Command

(1) Endpoint Descriptor

Offset	Field	Size	Value	Description
0	bLength	1	07h	Size of descriptor
1	bDescriptorType	1	05h	Endpoint descriptor type
2	bEndpointAddress	1	03h	Address: 3, Direction: OUT
3	bmAttributes	1	02h	Endpoint's attributes (Bulk)
4	wMaxPacketSize	2	0400h or 0200h	Maximum packet size 0400h: 1024 bytes in Super-speed mode. 0200h: 512 bytes in High-speed mode.
6	bInterval	1	00h	Interval for polling endpoint for data transfers.

(2) SuperSpeed Endpoint Companion Descriptor

Offset	Field	Size	Value	Description
0	bLength	1	06h	Size of descriptor
1	bDescriptorType	1	30h	SUPERSPEED_USB_ENDPOINT_COMPANION descriptor type.
2	bMaxBurst	1	00h	Max. burst = 1
3	bmAttributes	1	00h	Stream not supported
4	wBytesPerInterval	2	0000h	–

(3) Pipe Usage Descriptor

Offset	Field	Size	Value	Description
0	bLength	1	04h	Size of descriptor
1	bDescriptorType	1	24h	Pipe Usage descriptor type.
2	bPipeID	1	01h	Command pipe
3	Reserved	1	00h	–

4.5.2.4 UASP Status

(1) Endpoint Descriptor

Offset	Field	Size	Value	Description
0	bLength	1	07h	Size of descriptor
1	bDescriptorType	1	05h	Endpoint descriptor type
2	bEndpointAddress	1	84h	Address 4, Direction: IN
3	bmAttributes	1	02h	Endpoint's attributes (Bulk)
4	wMaxPacketSize	2	0400h or 0200h	Maximum packet size 0400h: 1024 bytes in Super-speed mode. 0200h: 512 bytes in High-speed mode.
6	bInterval	1	00h	Interval for polling endpoint for data transfers.

(2) SuperSpeed Endpoint Companion Descriptor

Offset	Field	Size	Value	Description
0	bLength	1	06h	Size of descriptor
1	bDescriptorType	1	30h	SUPERSPEED_USB_ENDPOINT_COMPANION descriptor type.
2	bMaxBurst	1	00h	Max. burst = 1
3	bmAttributes	1	05h	Max. stream = 32.
4	wBytesPerInterval	2	0000h	–

(3) Pipe Usage Descriptor

Offset	Field	Size	Value	Description
0	bLength	1	04h	Size of descriptor
1	bDescriptorType	1	24h	Pipe Usage descriptor type.
2	bPipeID	1	02h	Status pipe
3	Reserved	1	00h	–

4.6 String Descriptor

String descriptors describe Language ID, Manufacturer, Product and/or Serial Number. This string information is defined with the serial ROM utility.

Language ID (string descriptor index 0)

Offset	Field	Size	Value	Description
0	bLength	1	4h	Size of descriptor
1	bDescriptorType	1	03h	String descriptor Type
2	WLANGID[0]	2	0409h	General (U.S English)

Standard string descriptor format for index 1-3

Offset	Field	Size	Value	Description
0	bLength	1	Xh	Size of descriptor
1	bDescriptorType	1	03h	String descriptor Type
2	bString	N	XXXXh	UNICODE encoded string

4.7 Device Qualifier Descriptor (High-/Full-speed only)

A device qualifier descriptor describes general information about a high-speed capable device that would change if the device were operating at the other speed. For example, if the device is currently operating at full-speed, the device qualifier returns information about how it would operate at high-speed and vice-versa.

Offset	Field	Size	Value	Description
0	bLength	1	0Ah	Size of descriptor
1	bDescriptorType	1	06h	Device qualifier descriptor type
2	bcdUSB	2	0210h	USB specification version number (BCD)
4	bDeviceClass	1	00h	Class Code
5	bDeviceSubClass	1	00h	SubClass Code
6	bDeviceProtocol	1	00h	Protocol Code
7	bMaxPacketSize0	1	40h	Maximum packet size for this speed (64 bytes)
8	bNumConfigurations	1	01h	Number of this speed configuration
9	Reserved	1	00h	Reserved for future use.

4.8 Other_Speed_Configuration Descriptor (High-/Full-speed only)

An other_speed_configuration descriptor describes a configuration of a high-speed capable device if it were operating at its other possible speed. The structure of the other_speed_configuration is identical to a configuration descriptor. When the host requests the other_speed_configuration descriptor, all related interface and endpoint descriptors are returned.

Offset	Field	Size	Value	Description
0	bLength	1	09h	Size of descriptor
1	bDescriptorType	1	07h	Other_speed_configuration descriptor type
2	wTotalLength	2	0020h	Total length of data returned for this configuration.
4	bNumInterfaces	1	01h	Number of interfaces supported by this speed configuration
5	bConfigurationValue	1	01h	Value to use to select configuration
6	iConfiguration	1	00h	Index of string descriptor describing configuration.
7	bmAttributes	1	C0h	Configuration characteristics
8	bMaxPower	1	32h	Maximum power consumption of the USB device from the bus in this configuration when the device is fully operational.

5. Boot Mode

There are 2 boot modes in the μPD720231, SROM boot mode and HDD/SSD boot mode. HDD/SDD boot mode has Quick/Slow enumeration option. These are selected from GPIO setting during initialization.

Table 5-1. Boot Mode selection

GPIO0	GPIO1	GPIO2	GPIO3	Mode	Option
x	x	x	1	SROM boot	–
1	0	0	0	HDD/SSD boot	Slow enumeration
1	0	1	0		Quick enumeration

5.1 SROM boot mode

μPD720231 boots up with internal firmware, and uses parameters and firmware patches from external SROM (SPI Flash). Utility tool is used to set these parameters and firmware patches into external SROM. Please refer to the application note of utility tool in more detail.

5.2 HDD/SSD boot mode

μPD720231 boots up with internal firmware, and uses parameters and firmware patches from HDD/SSD devices. Utility tool is used to set these parameters and patches into HDD/SSD. Please refer to the application note of utility tool in more detail.

Quick/Slow enumeration are selected with pin strapping option, as in Table 5-2.

Table 5-2. Quick and Slow enumeration setting

Setting	Behavior
Quick enumeration	Some HDD drives take time for spin up, and if PC may not wait this period, μPD720231 may not be enumerated properly. To prevent this case, μPD720231 responds default information of internal mask FW to host system. After getting information of SATA device, it disconnects, connects again, and responds the latest information of SATA device to host system.
Slow enumeration	μPD720231 starts the connection to host system, afer Initialization of SATA device completes. In this mode, μPD720231 keeps its connection to host until it actually plug out. This mode is recommended, in submitting to USB compliance test.

6. General Purpose I/O

6.1 Features

The μPD720231 supports 10 configurable GPIO pins with the following features. Each function is configured as shown in Table 6-1.

- SPI interface for external serial flash ROM.
- Disk Activity LED
- Reset/Clock output for external device
- External trigger input

Table 6-1 Function configuration

Pin Name	Function
GPIO0/SPISO	General purpose I/O or SPI master input / slave output
GPIO1/SPISCK	General purpose I/O or SPI clock
GPIO2/SPISI	General purpose I/O or SPI master output / slave input
GPIO3/SPICSB	General purpose I/O or SPI chip select for the external serial flash ROM.
GPIO4	General purpose I/O
GPIO5	General purpose I/O
GPIO6/ACT	General purpose I/O or Disk Activity LED
GPIO7/CLKOUT	General purpose I/O or 30MHz clock output
GPIO8	General purpose I/O
GPIO9/EXTINT	General purpose I/O or external interrupt such as push button input

6.2 SPI interface

The μPD720231 supports SPI interface and it is required to connect to the external serial Flash ROM to store parameter or firmware patch.

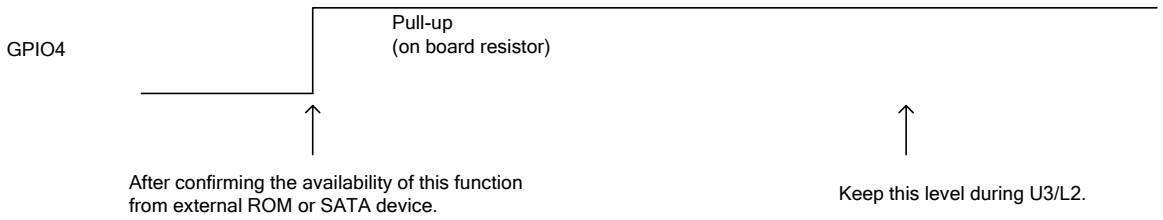
6.3 Disk Activity LED

The μPD720231 provides LED support to indicate the access to SATA device. GPIO6 is used for this function. In ATAPI device attached to μPD720231, this function is not available.

6.4 Reset signal for external device

The μPD720231 provides reset signal for external device from GPIO4. GPIO4 drives low in default and it changes to Hi-Z after μPD720231 read parameter from external SROM or SATA devices and confirms that this function is supported. If this is not supported, GPIO4 remains low drive. This function is enabled from utility tool.

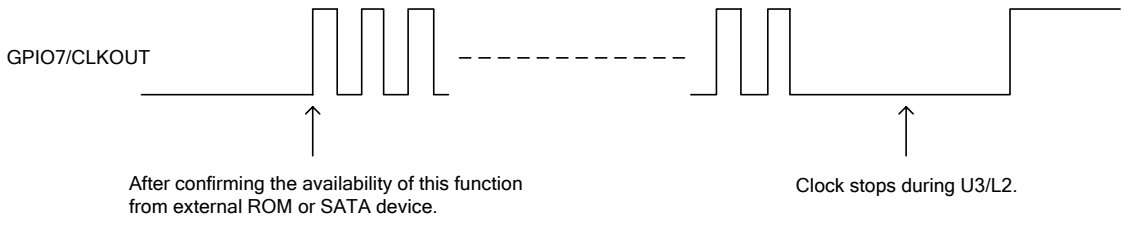
Figure 6-1 GPIO4 signal timing chart



6.5 Clockout function

The μPD720231 provides clock signal for external device from GPIO7/CLKOUT. GPIO7CLKOUT starts clock output after μPD720231 read parameter from external SROM or SATA devices and confirms that this function is supported. If this is not supported, GPIO4 remains low drive. This function is enabled from utility tool.

Figure 6-2 GPIO7/CLKOUT signal timing chart



6.6 External trigger in

The μPD720231 provides external interrupt solution using GPIO9/EXTINT. This is used for button solution. This function is enabled from utility tool and active level is also set from same tool. Host system can check the status of GPIO9/EXTINT, using vendor command.

7. How to Connect to External Elements

7.1 Handling Unused Pins

Unused pins shall be connected as shown below.

Table 7-1. Unused Pin Connection

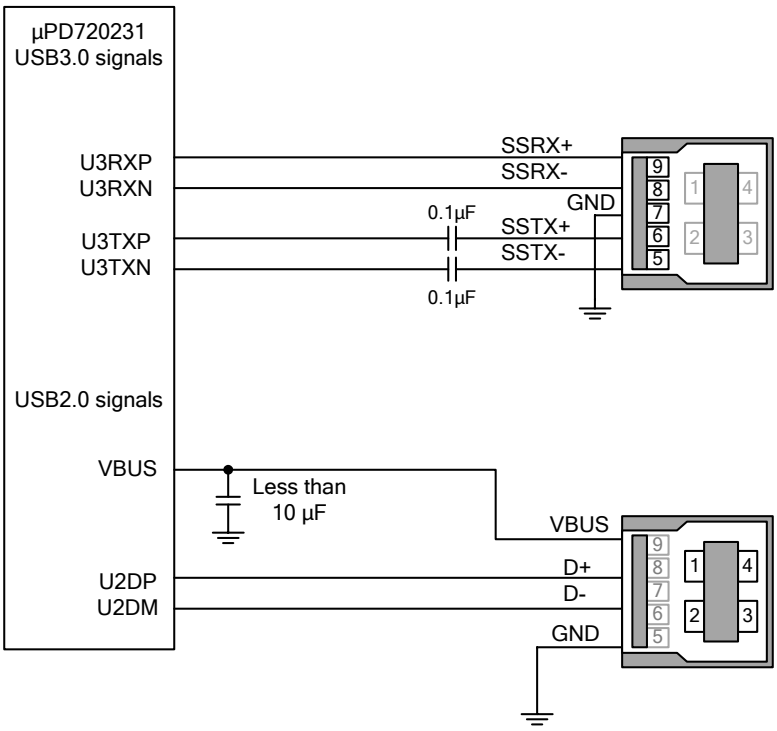
Pin	Direction	Connection Method
GPIO0/SPISO, GPIO1/SPISCK, GPIO2/SPISI, GPIO3/SPICSB	I/O	Please refer to Table 5-1
GPIO4, GPIO7/CLKOUT, GPIO8, GPIO9/EXTINT	I/O	Open
GPIO5, GPIO6/ACT	I/O	Pull-up or down on board.

If the USB to SATA bridge system needs only USB2.0 (High/Full-speed), but not USB3.0 (SuperSpeed), unused pins related to SuperSpeed shall be handled as shown below.

Pin	Direction	Connection Method
U3RXP	I	Open
U3RXN	I	Open
U3TXP	O	Open
U3TXN	O	Open

7.2 Upstream Port Connection

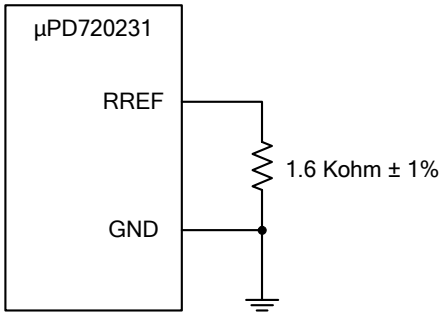
Figure 7-1. USB Upstream Port Connection



Remark The maximum capacitance that can be placed on VBUS line should be less than 10 μF for the inrush current limiting requirement specified by USB3.0 specification. Please see section 11.4.4.1 in USB3.0 specification for details.

7.3 RREF Connection

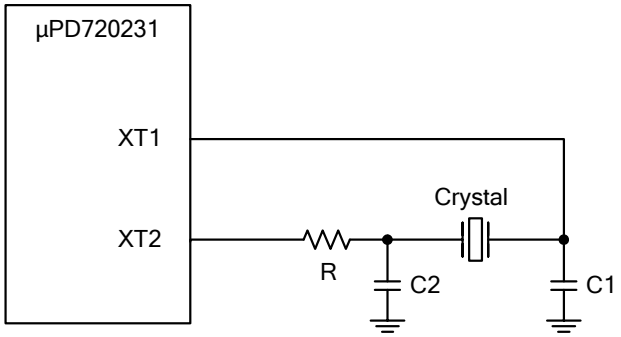
Figure 7-2. RREF Connection



Remark The board layout should minimize the total path length from RREF through the resistor to GND and path length to GND. GND must be stable.
Due to analog sensitivity, 1.60 K within ±1% must be used, and two or more resistors in series or parallel should not be used in place of a single 1.60 K resistor.

7.4 Crystal Connection

Figure 7-3. Crystal Connection



The following crystal is evaluated on our reference design board. Table 7-2 shows the external parameters.

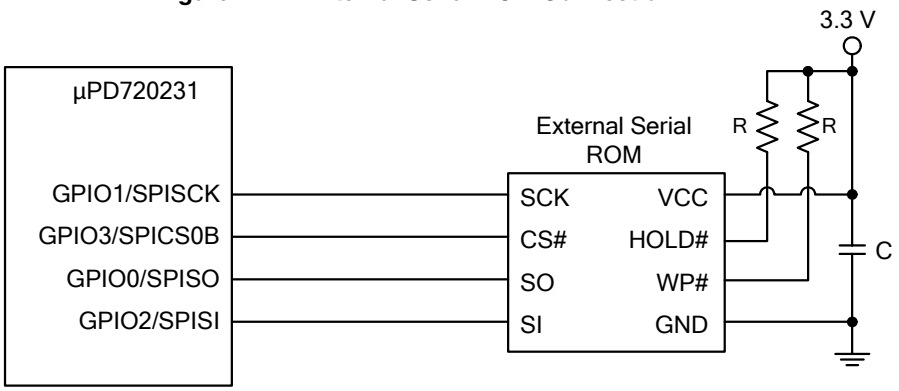
Table 7-2. External Parameters

Vendor	Crystal	R	C1	C2
NDK	NX2520SA, 30MHz	100 Ω	12 pF	12 pF

Remark Clock shall be 30 MHz within 100ppm. Moreover optimal crystal parameters and RC component values may be affected by the PCB layout.

7.5 External Serial ROM Connection

Figure 7-4. External Serial ROM Connection



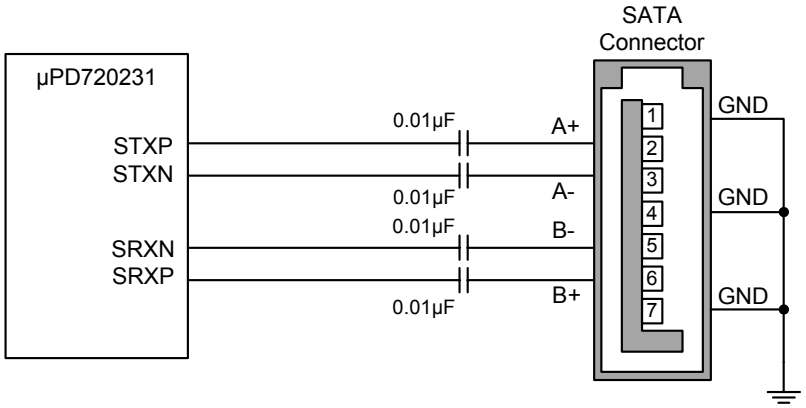
The supported serial ROMs are listed in Table 7-5.

Table 7-5. Supported External Serial ROM (3.3V) list

Manufacturer	Product Name
Atmel	AT25F512B/AT25DF021/AT25DF041A
AMIC	A25L010/A25L020/A25L512
Eon Silicon Solution	EN25F05/EN25F10/EN25F20/ EN25LF10/EN25LF20/EN25LF40
Macronix International	MX25V512E/MX25V1006E/MX25V2006E/MX25V4005C/MX25V4006E/ MX25L512E/MX25L1006E//MX25L2006E/MX25L4006E/ MX25L5121E/MX25L1021E/MX25L1026E/MX25L2026E
Micron Technology (Numonyx)	M25P20
Microchip (SST)	SST25VF512/SST25VF512A/SST25VF010A/SST25VF020B/SST25VF080B SST25LF020A
Sanyo Semiconductor	LE25FU106B/LE25FU206/LE25FU406B
Winbond Electronics	W25Q40BL/W25Q80BL W25X05CL/W25X10CL /W25X20CL/W25X40CL

7.6 Serial ATA Interface Connection

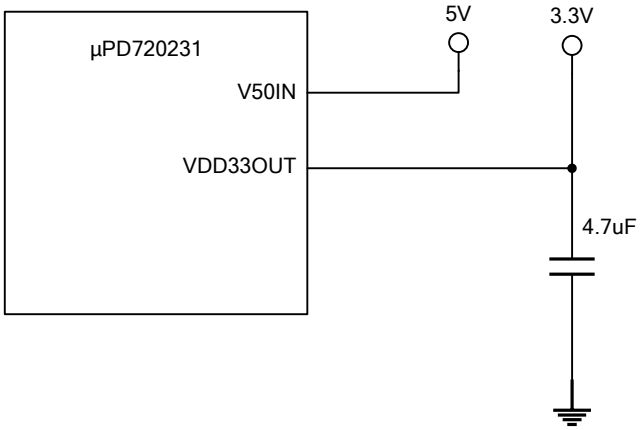
Figure 7-6. Serial ATA Interface Connection



7.7 On-Chip LDO (5 V to 3.3 V) Connection

It is prohibited not to use internal LDO and V50IN must be always supplied.

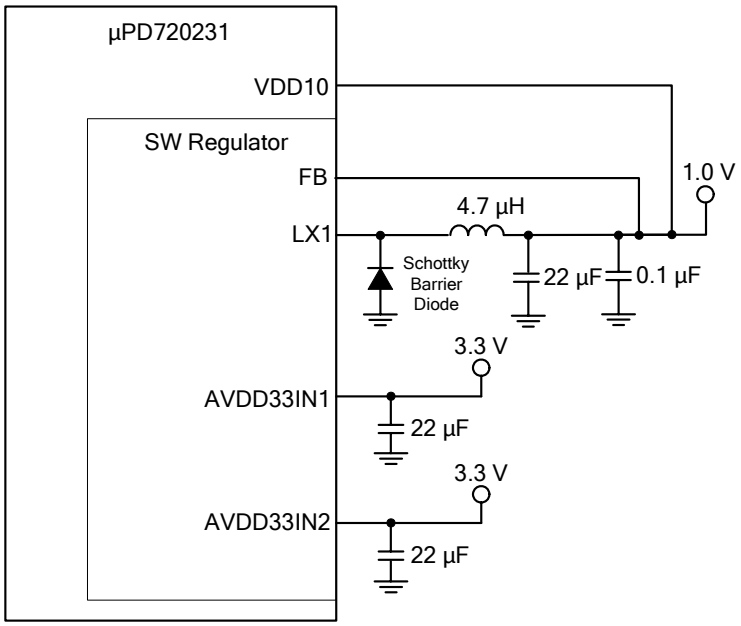
Figure 7-7. On-Chip LDO Pin Connection



Remark 4.7 μF capacitor is required, and the capacitor should be placed closed to VDD33OUT.

7.8 On-Chip Switching Regulator (3.3 V to 1.0 V) Connection

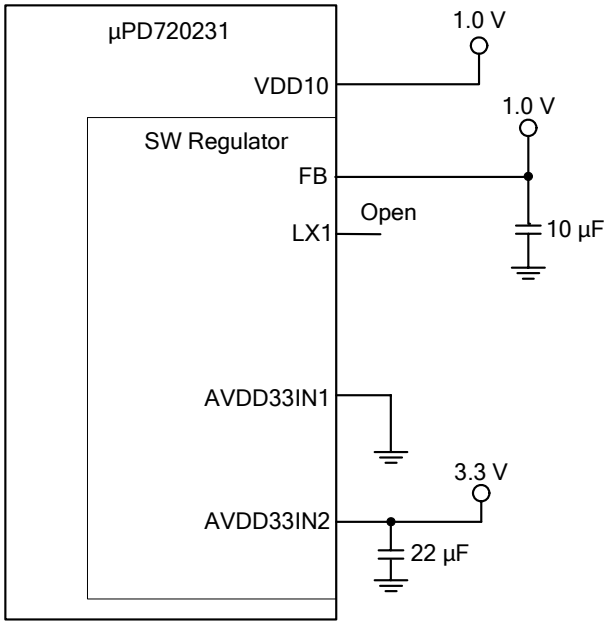
Figure 7-8. On-Chip Switching Regulator Pin Connection



Remark It is mandatory to put ceramic capacitors (22 μF is recommended) on AVDD33IN1 and AVDD33IN2. Common impedance coupling between AVDD33IN1 and AVDD33IN2 must be avoided.

In case of not using internal switching regulators, please handle each pins as in Figure 7-9.

Figure 7-9. On-Chip Switching Regulator Pin Connection (out of use)



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