RENESAS

# MOS INTEGRATED CIRCUIT

# μPD16781

## 480 OUTPUT TFT-LCD SOURCE DRIVER

### DESCRIPTION

The μPD16781 is a source driver for 480-output TFT-LCDs, providing support for only striped pixel array LCD.

The driver consists of a shift register for generating the sampling timing and sample & hold circuits for sampling the analog voltage. The high picture quality obtained by the alternate sample & hold execution of the two types of on-chip sample & hold circuits enables employment in applications such as car navigation panels.

### FEATURES

- 5.0 V Drive (Dynamic range 4.6 $V_{P-P}$, $V_{DD2}$ = 5.0 V)
- 480 Output channel
- $f_{CLK}$ = 20 MHz MAX. ($V_{DD1}$ = 3.0 V)
- 1-phase/3-phase sampling clocks supported
- Corresponds only to LCD of Stripe array color filter
- Two on-chip sample-and-hold circuits
- Small output deviation between pins (deviation between chip pins: ±20 mV MAX.)
- Switch between right and left shift using the R,/L pin
- Logic power supply voltage ($V_{DD1}$): 3.0 to 5.5 V
- Driver power supply voltage($V_{DD2}$): 5.0 ± 0.5 V

**Remark** /xxx indicates active low signal.

### ORDERING INFORMATION

| Part Number | Package |
|---|---|
| μPD16781N-xxx | TCP (TAB package) |

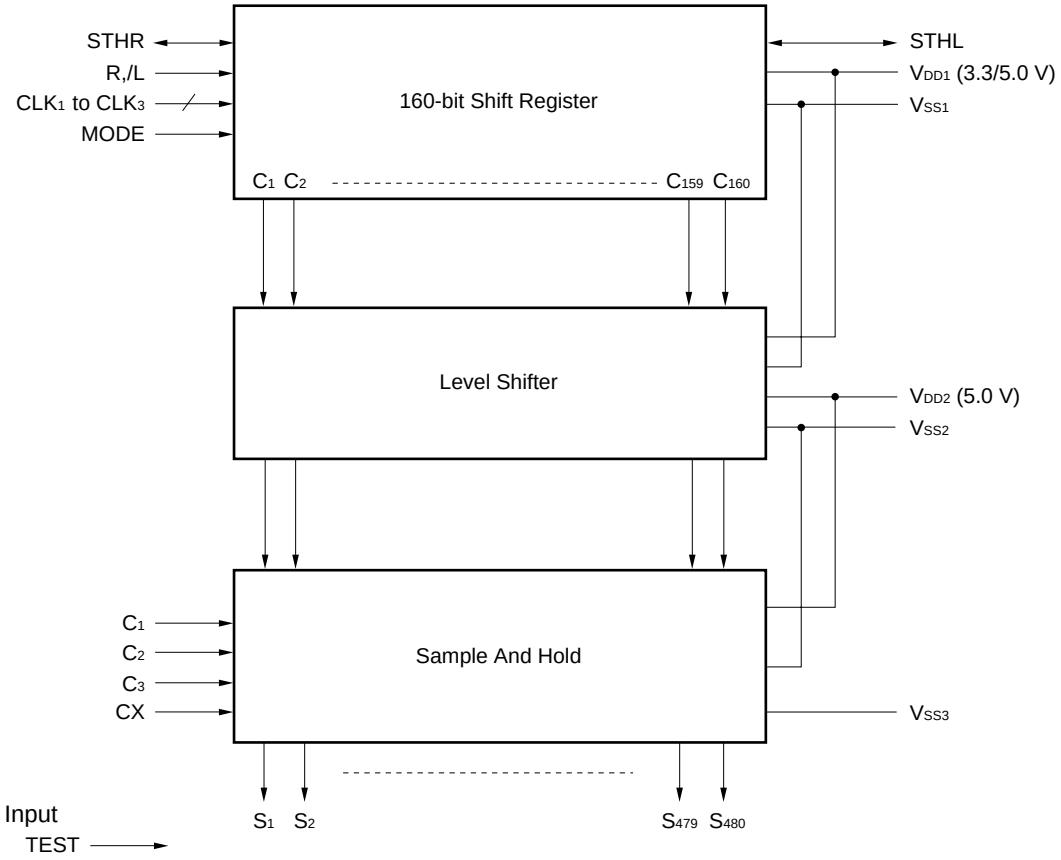
**Remark** The TCP's external shape is customized. To order the required shape, so please contact one of our sales representatives.



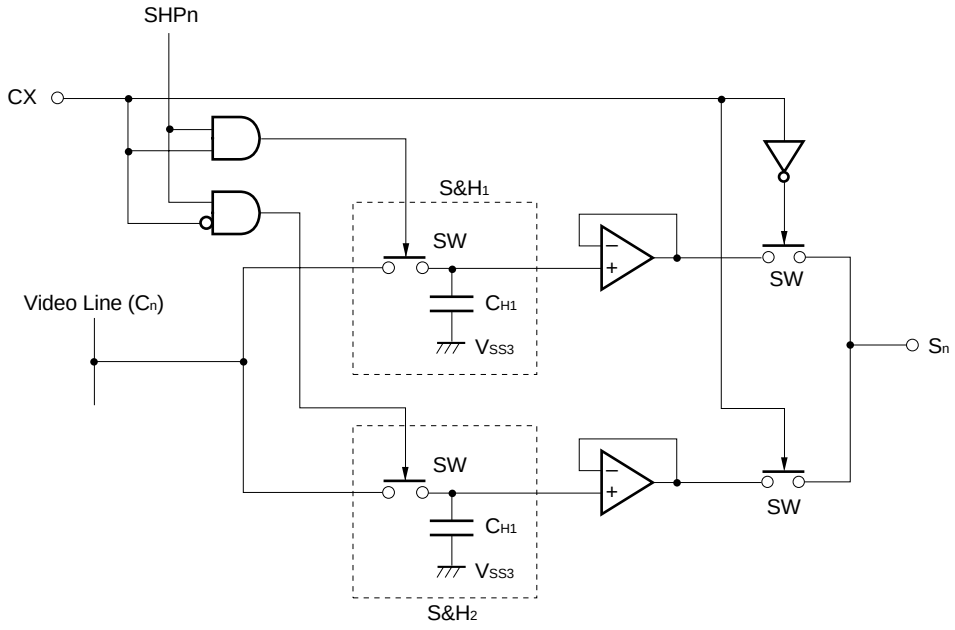
Document No. S14634EJ1V0DS00 (1st edition)
Date Published February 2002 NS CP(K)
Printed in Japan

**The mark ★ shows major revised points.**

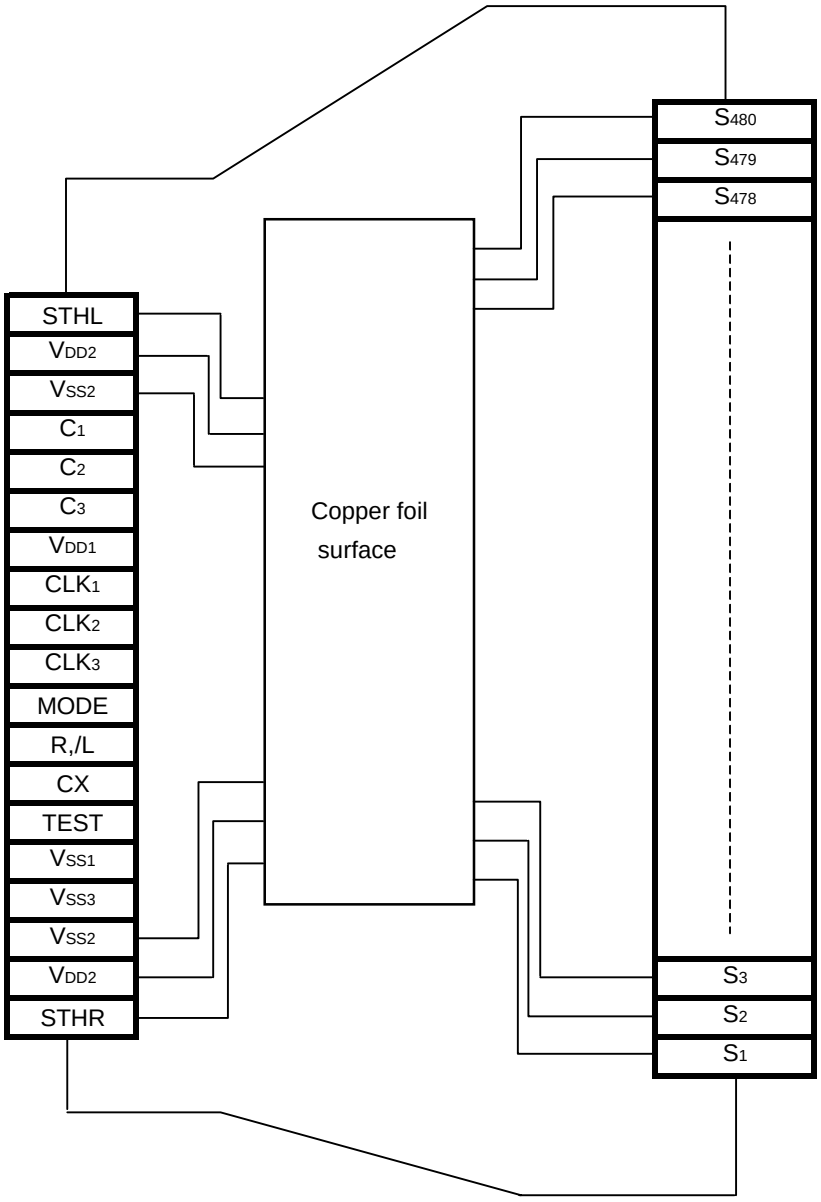
## ★ 1. BLOCK DIAGRAM




## 2. SAMPLE-AND HOLD CIRCUIT AND OUTPUT CIRCUIT



### 3. PIN CONFIGURATION (μPD16781N-xxx) (Copper Foil Surface, Face-up)




**Remark** This figure does not specify the TCP package.

## 4. PIN FUNCTIONS

| Pin Symbol | Pin Name | I/O | Description |
|---|---|---|---|
| $C_1$ to $C_3$ | Video signal input | I | These pins are input video signals R, G, and B. |
| $S_1$ to $S_{480}$ | Video signal output | O | These pins are output video signals, which have been sampled and hold.<br>The relationship between the video signal input ($C_1$ to $C_3$) and video signal output is shown below.<br>$C_1$: $S_{3n-2}$ (n = 1, 2, ·····160)<br>$C_2$: $S_{3n-1}$<br>$C_3$: $S_{3n}$ |
| STHR,<br>STHL | Cascade I/O | I/O | These pins are inputs/outputs for the start pulse for sample and hold timing.<br>High level of STHR/STHL is read at rising edge of CLK and start sampling video signal. STHR serves as the input pin and STHL serves as output pin for the right shift. For left shift, STHL serves as the input pins and STHR serves as the output pin. |
| R,/L | Shift direction control | I | The shift direction control pin of shift register. The shift directions of the shift registers are as follows.<br>R,/L = H (right shift): STHR input, $S_1 \rightarrow S_{480}$, STHL output.<br>R,/L = L (left shift): STHL input, $S_{480} \rightarrow S_1$, STHR output. |
| $CLK_1$ to $CLK_3$ | Shift clock input | I | The start pulse is read at rising edge of CLK. The sampling pulse SHPn is generated at rising edge of CLK. For details, refer to **6. TIMING CHART**.<br>The relationship between the clocks and the output pins is shown below.<br>(1) When MODE = L or open (sequential sampling)<br>$CLK_1$ R,/L = H: $S_{3n-2}$<br>R,/L = L: $S_{3n}$<br>$CLK_2$: $S_{3n-1}$<br>$CLK_3$ R,/L = H: $S_{3n}$<br>R,/L = L: $S_{3n-2}$<br>(1) When MODE = H (simultaneous sampling)<br>$CLK_1$: $S_{3n-2}$, $S_{3n-1}$, $S_{3n}$ (n = 1, 2,·····160)<br>$CLK_2$: Connect $V_{DD1}$ or $V_{SS1}$<br>$CLK_3$: Connect $V_{DD1}$ or $V_{SS1}$ |
| MODE | Mode select signal input | I | This pin is used to select whether the three analog input signals, $C_1$, $C_2$, and $C_3$ are sampled simultaneously or sequentially (This pin is pulled down in the IC).<br>MODE = H: Simultaneous sampling<br>MODE = L or open: Sequential sampling |
| CX | Hold capacitance control input | I | Two Sample & hold circuits are switched.<br>CX = H S&H1: Sampling, S&H2: Output<br>CX = L S&H1: Output, S&H2: Sampling |
| TEST | Test | I | Fix this pin to the L level. |
| $V_{DD1}$ | Logic power supply | – | 3.0 to 5.5 V |
| $V_{DD2}$ | Driver power supply | – | 5.0 ± 0.5 V |
| $V_{SS1}$ | Logic ground | – | Grounding |
| $V_{SS2}$ | Driver ground | – | Grounding |
| $V_{SS3}$ | Sample & hold ground | – | It is ground of Sample & hold capacitance. Supply this terminal with the stable GND. |

**Cautions 1. To prevent latch-up-breakdown, the power should be turned on in order $V_{DD1}$, Logic input $V_{DD2}$, video signal input. It should be turned off in the opposite order. This relationship should be followed during transition periods as well.**

**2. The sampling of the video signal of this IC is only the simultaneous 3 output sampling of $C_1$ to $C_3$. Incidentally, it is designing abound of the input of the video signal in 10 MHz MAX. If a video signal with a higher frequency is input, the data may not be correctly displayed.**

★ **3. Recommend a bypass capacitor of about 0.1 μF with good high-frequency characteristics between $V_{DD1}$ and $V_{SS1}$, and $V_{DD2}$ and $V_{SS2}$ in each driver IC. Unless the power supply is reinforced, the supply voltage may fluctuate, making the sampling voltage abnormal.**

**4. If noise is superimposed on the start pulse pin, the data may not be displayed. For this reason, be sure to input CX signal during the vertical blanking period.**

**5. If the start pulse width is extended by half the clock or longer, the sampling start timing SHP1 does not change from normal timing; therefore, the sampling operation is performed normally.**

## 5. FUNCTION DESCRIPTION

### 5.1 Switching of Sample & Hold Circuits

Two sample-and-hold circuits are switched.

| CX | Output | Sample & hold operation |
|---|---|---|
| L | Sample & Hold Circuit 1 ($S\&H_1$) | Sample & Hold Circuit 2 ($S\&H_2$) |
| H | Sample & Hold Circuit 2 ($S\&H_2$) | Sample & Hold Circuit 1 ($S\&H_1$) |

### 5.2 Sample & Hold and Output

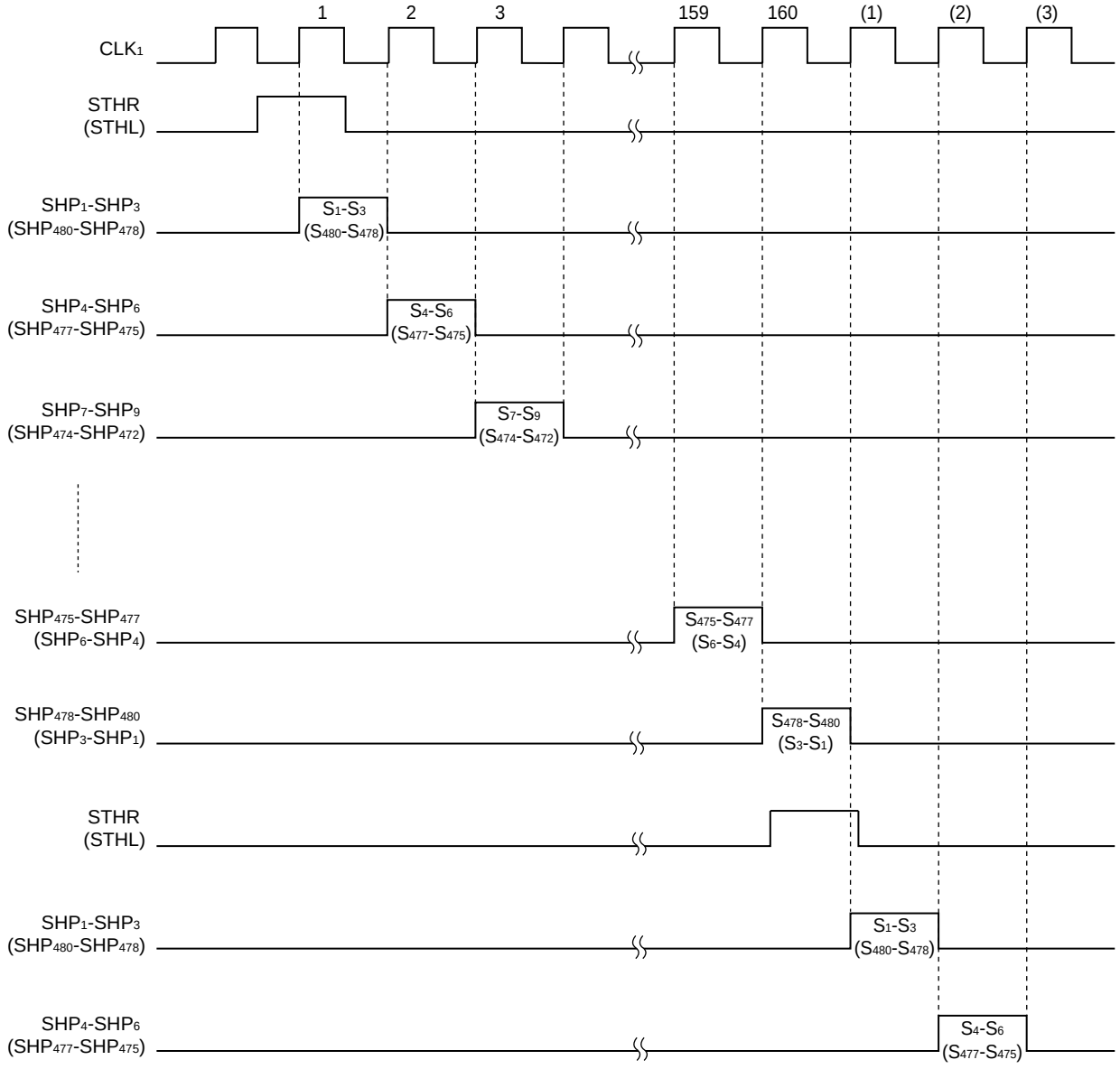
Relation between video signals $C_1$, $C_2$ and $C_3$ and output pins and two sample & hold circuits.

| CX | | $S_1$ ($S_{480}$) | $S_2$ ($S_{479}$) | $S_3$ ($S_{478}$) | $S_4$ ($S_{477}$) | ··· | $S_{479}$ ($S_2$) | $S_{480}$ ($S_1$) |
|---|---|---|---|---|---|---|---|---|
| L | Sampling | $C_{1\text{-}2}$ ($C_{3\text{-}2}$) | $C_{2\text{-}2}$ ($C_{2\text{-}2}$) | $C_{3\text{-}2}$ ($C_{1\text{-}2}$) | $C_{1\text{-}2}$ ($C_{3\text{-}2}$) | ··· | $C_{2\text{-}2}$ ($C_{2\text{-}2}$) | $C_{3\text{-}2}$ ($C_{1\text{-}2}$) |
| | Output | $C_{1\text{-}1}$ ($C_{3\text{-}1}$) | $C_{2\text{-}1}$ ($C_{2\text{-}1}$) | $C_{3\text{-}1}$ ($C_{1\text{-}1}$) | $C_{1\text{-}1}$ ($C_{3\text{-}1}$) | ··· | $C_{2\text{-}1}$ ($C_{2\text{-}1}$) | $C_{3\text{-}1}$ ($C_{1\text{-}1}$) |
| H | Sampling | $C_{1\text{-}1}$ ($C_{3\text{-}1}$) | $C_{2\text{-}1}$ ($C_{2\text{-}1}$) | $C_{3\text{-}1}$ ($C_{1\text{-}1}$) | $C_{1\text{-}1}$ ($C_{3\text{-}1}$) | ··· | $C_{2\text{-}1}$ ($C_{2\text{-}1}$) | $C_{3\text{-}1}$ ($C_{1\text{-}1}$) |
| | Output | $C_{1\text{-}2}$ ($C_{3\text{-}2}$) | $C_{2\text{-}2}$ ($C_{2\text{-}2}$) | $C_{3\text{-}2}$ ($C_{1\text{-}2}$) | $C_{1\text{-}2}$ ($C_{3\text{-}2}$) | ··· | $C_{2\text{-}2}$ ($C_{2\text{-}2}$) | $C_{3\text{-}2}$ ($C_{1\text{-}2}$) |

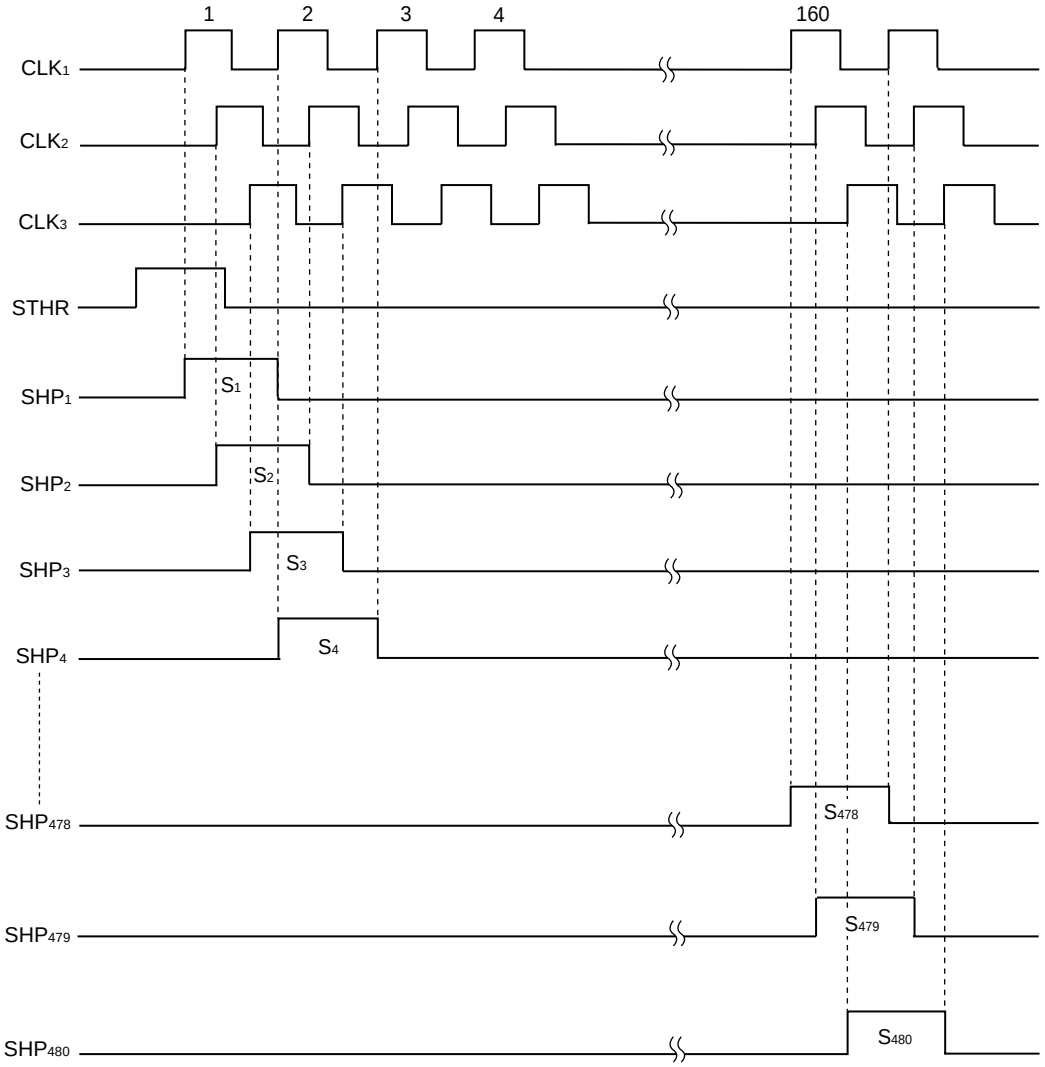
**Remark** $C_{m\text{-}n}$ = m: Video input, n: Sample & Hold

## 6. TIMING CHART

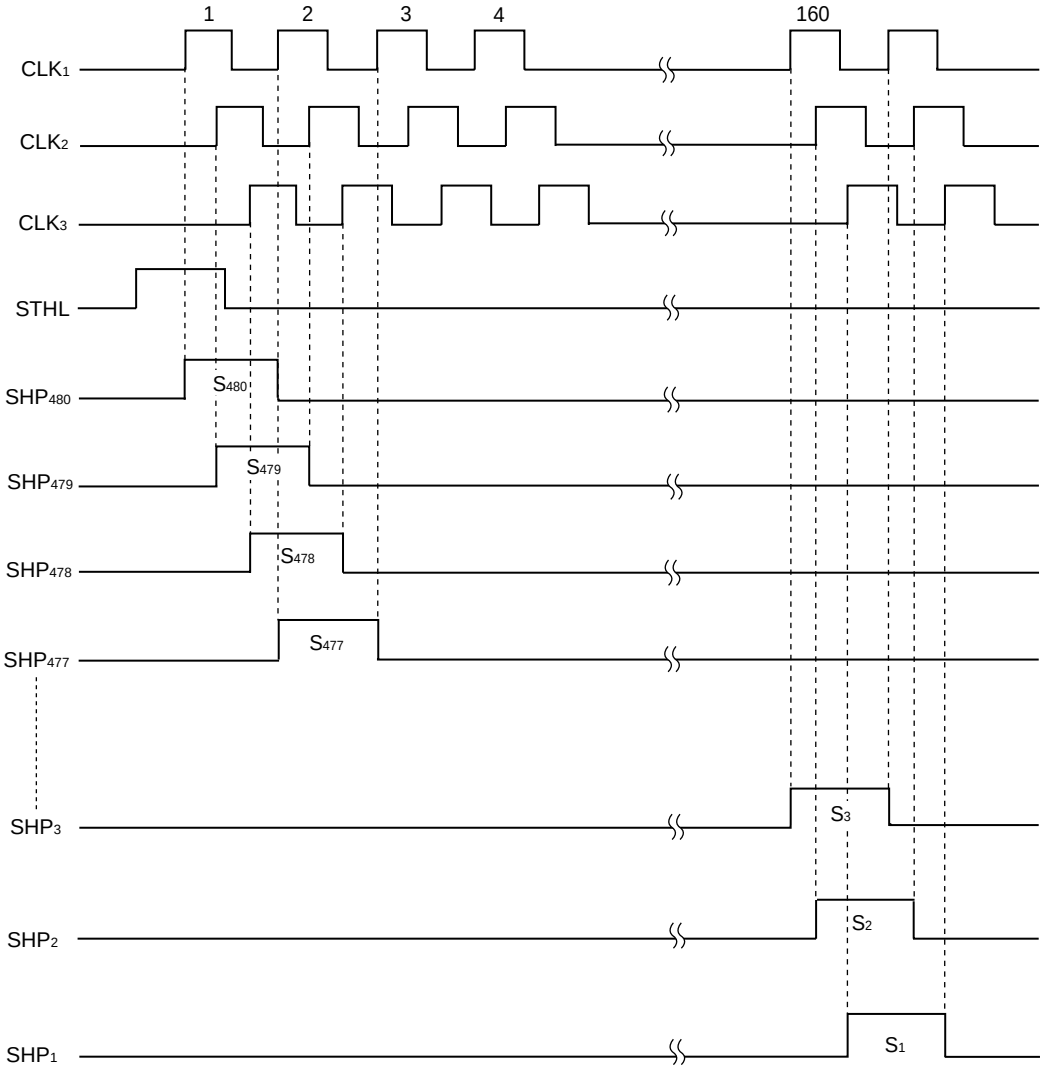
### 6.1 1-Phase Simultaneous Sampling



### 6.2 3-phase Sequential Sampling, Right Shift



### 6.3 3-phase Sequential Sampling, Left Shift



## 7. ELECTRICAL SPECIFICATIONS

**Absolute Maximum Ratings ($T_A$ = +25°C, $V_{SS1}$ = $V_{SS2}$ = 0 V)**

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Logic Part Supply Voltage | $V_{DD1}$ | –0.3 to +7.0 | V |
| Driver Part Supply Voltage | $V_{DD2}$ | –0.3 to +7.0 | V |
| Input Voltage | $V_I$ | –0.3 to $V_{DD1/2}$ + 0.3 | V |
| Output Voltage | $V_O$ | –0.3 to $V_{DD1/2}$ + 0.3 | V |
| Operating Ambient Temperature | $T_A$ | –30 to +85 | °C |
| Storage Temperature | $T_{stg}$ | –55 to +125 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Recommended Operating Range ($T_A$ = –30 to +85°C, $V_{DD2} \geq V_{DD1}$, $V_{SS1}$ = $V_{SS2}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Logic Part Supply Voltage | $V_{DD1}$ | | 3.0 | | 5.5 | V |
| Driver Part Supply Voltage | $V_{DD2}$ | | 4.5 | 5.0 | 5.5 | V |
| Video Input Voltage | $V_{VI}$ | | $V_{SS2}$ + 0.2 | | $V_{DD2}$ – 0.2 | V |
| Driver Part Output Voltage | $V_{O2}$ | | $V_{SS2}$ + 0.2 | | $V_{DD2}$ – 0.2 | V |
| Clock Frequency | $f_{CLK}$ | $CLK_1$ to $CLK_3$ | | | 20 | MHz |
| Output Load Capacitance | $C_L$ | 1 output | | | 50 | pF |

**Electrical Characteristics ($T_A$ = –30 to +85°C, $V_{DD1}$ = 3.0 to 5.5 V, $V_{DD2}$ = 5.0 V ± 0.5 V, $V_{DD2} \geq V_{DD1}$, $V_{SS1} = V_{SS2}$ = 0 V)**

| | Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| | Low-Level Driver Part Output Voltage | $V_{VOL}$ | $S_1$ to $S_{480}$ | | | $V_{SS2}$ + 0.2 | V |
| | High-Level Driver Part Output Voltage | $V_{VOH}$ | | $V_{DD2}$ – 0.2 | | | V |
| | High-Level Input Voltage | $V_{IH}$ | CLK, STHR (L), R,/L, $O_{sel}$, CX | 0.7 $V_{DD1}$ | | $V_{DD1}$ | V |
| | Low-Level Input Voltage | $V_{IL}$ | | $V_{SS1}$ | | 0.3 $V_{DD1}$ | V |
| | Input Leak Current | $I_{IL}$ | Except for MODE pin | –1.0 | | +1.0 | μA |
| | | | MODE pin, $V_I$ = 0 V | –10 | | +10 | μA |
| | | | MODE pin, $V_I = V_{DD1}$ = 5 V | 30 | | 300 | μA |
| | High-Level Output Voltage | $V_{LOH}$ | STHR (STHL), $I_{OH}$ = –1.0 mA | 0.85 $V_{DD1}$ | | | V |
| | Low-Level Output Voltage | $V_{LOH}$ | STHR (STHL), $I_{OL}$ = +1.0 mA | | | 0.15 $V_{DD1}$ | V |
| | Reference Voltage | $V_{REF1}$ | $V_{DD2}$ = 5.0 V, $V_{VI}$ = 0.5 V, $T_A$ = 25°C | | 0.5 | | V |
| | | $V_{REF2}$ | $V_{DD2}$ = 5.0 V, $V_{VI}$ = 2.5 V, $T_A$ = 25°C | | 2.5 | | V |
| | | $V_{REF3}$ | $V_{DD2}$ = 5.0 V, $V_{VI}$ = 4.5 V, $T_A$ = 25°C | | 4.5 | | V |
| ★ | Output Voltage Deviation | $\Delta V_{VO1}$ | $V_{DD2}$ = 5.0 V, $V_{VI}$ = 0.5 V, $T_A$ = 25°C | | | ±20 | mV |
| ★ | | $\Delta V_{VO2}$ | $V_{DD2}$ = 5.0 V, $V_{VI}$ = 2.5 V, $T_A$ = 25°C | | | ±20 | mV |
| ★ | | $\Delta V_{VO3}$ | $V_{DD2}$ = 5.0 V, $V_{VI}$ = 4.5 V, $T_A$ = 25°C | | | ±20 | mV |
| ★ | Logic Dynamic Current Consumption | $I_{DD1}$ | $V_{DD1}$ = 5.0 V, no load **Note** | | 1.6 | 5.6 | mA |
| ★ | Driver Dynamic Current Consumption | $I_{DD2}$ | $V_{DD2}$ = 5.0 V, no load **Note** | | 12.0 | 16.0 | mA |

**Note** $f_{CLK}$ = 15 MHz, $f_{CX}$ = 17 kHz.

**Switching Characteristics ($T_A$ = –30 to +85°C, $V_{DD1}$ = 3.0 to 5.5 V, $V_{DD2}$ = 5.0 V ± 0.5 V, $V_{DD2} \geq V_{DD1}$, $V_{SS1} = V_{SS2}$ = 0 V)**

| | Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| | Start Pulse Delay Time | $t_{PHL1}$ | $C_L$ = 20 pF | 7 | | 43 | ns |
| | | $t_{PLH1}$ | CLK → STHL (STHR) | 7 | | 43 | ns |
| | Driver Output Delay Time | $t_{PLH2}$ | $V_{DD2}$ = 5.0 V | | | 8 | μs |
| | | $t_{PLH3}$ | $R_L$ = 2 kΩ | | | 16 | μs |
| | | $t_{PHL2}$ | $C_L$ = 25 pF x 2 | | | 8 | μs |
| | | $t_{PHL3}$ | | | | 16 | μs |
| ★ | Input Capacitance | $C_{I1}$ | STHR(STHL), $T_A$=25°C | | 10 | 20 | pF |
| ★ | | $C_{I2}$ | $C_1$ to $C_3$, $T_A$=25°C | | 40 | 60 | pF |
| ★ | | $C_{I3}$ | STHR (STHL), $C_1$ to $C_3$ excluded input, $T_A$=25°C | | 7 | 15 | pF |

**Timing Requirement ($T_A$ = –30 to +85°C, $V_{DD1}$ = 3.0 to 5.5 V, $V_{SS1}$ = 0 V)**

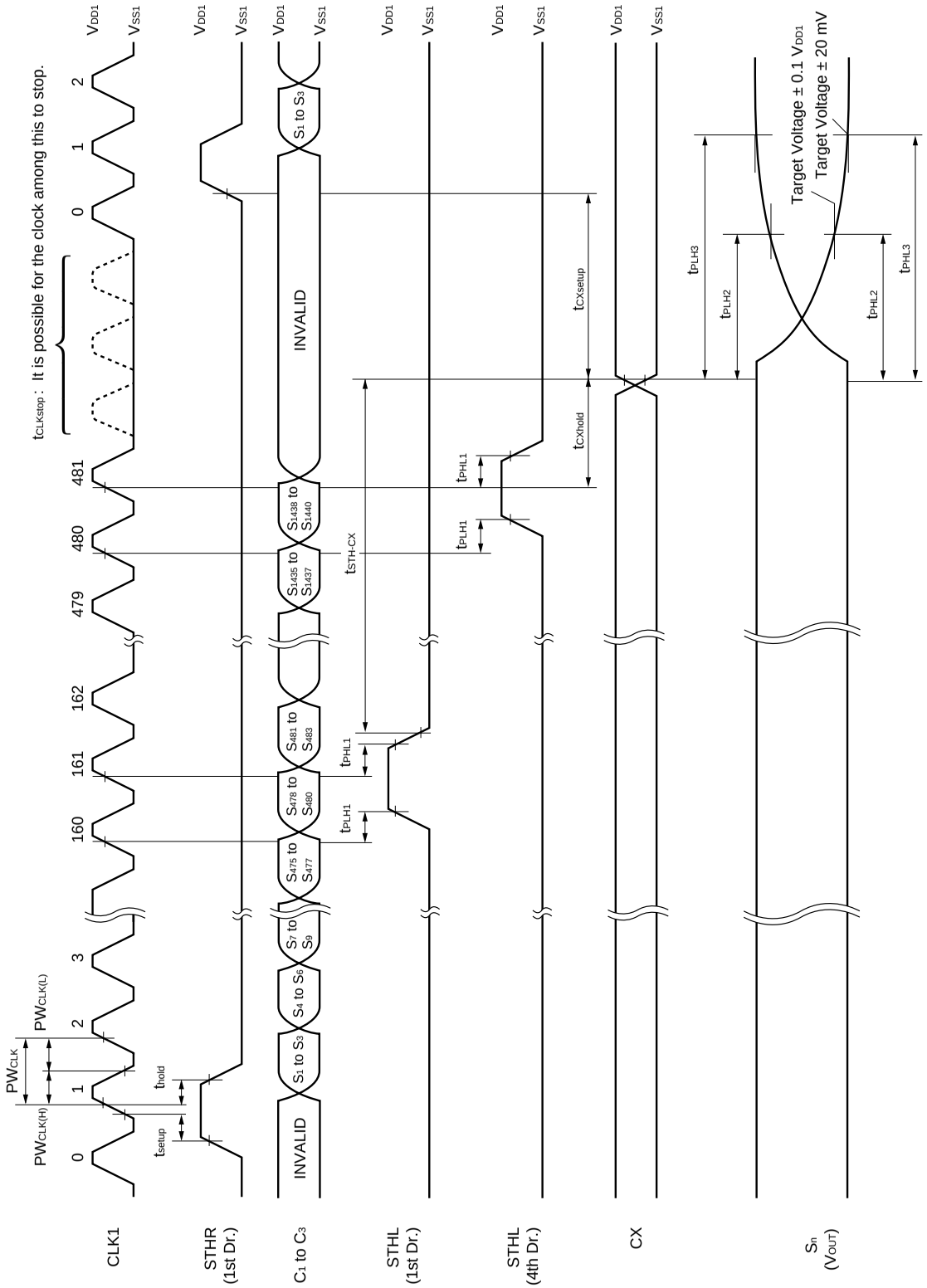
| | Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| | Clock Pulse Width | $PW_{CLK}$ | $CLK_1$ to $CLK_3$ | 50 | | | ns |
| | Clock Pulse High Period | $PW_{CLK(H)}$ | | 15 | | | ns |
| | Clock Pulse Low Period | $PW_{CLK(L)}$ | | 15 | | | ns |
| ★ | CLK-CLK time | $t_{CL1-2}$ | | 16.6 | | $\frac{PW_{CLK}}{2}$ | ns |
| | | $t_{CL2-3}$ | | | | | |
| | Start Pulse Setup Time | $t_{setup}$ | | 7 | | | ns |
| | Start Pulse Setup Time | $t_{hold}$ | | 7 | | | ns |
| | Start Pulse-CX Time | $t_{STH-CX}$ | | 50 | | | ns |
| | CX Setup Time | $t_{CXsetup}$ | | 1.0 | | | μs |
| | CX Hold Time | $t_{CXhold}$ | | 50 | | | ns |
| | CLK Stop Period | $t_{CLKstop}$ | | Refer to **8. SWITHING CHARACTERISTICS WAVEFORM.** | | | |

**Remark** Unless otherwise specified, the input level is defined to be $V_{IH}$ = 0.7 $V_{DD1}$, $V_{IL}$ = 0.3 $V_{DD1}$.

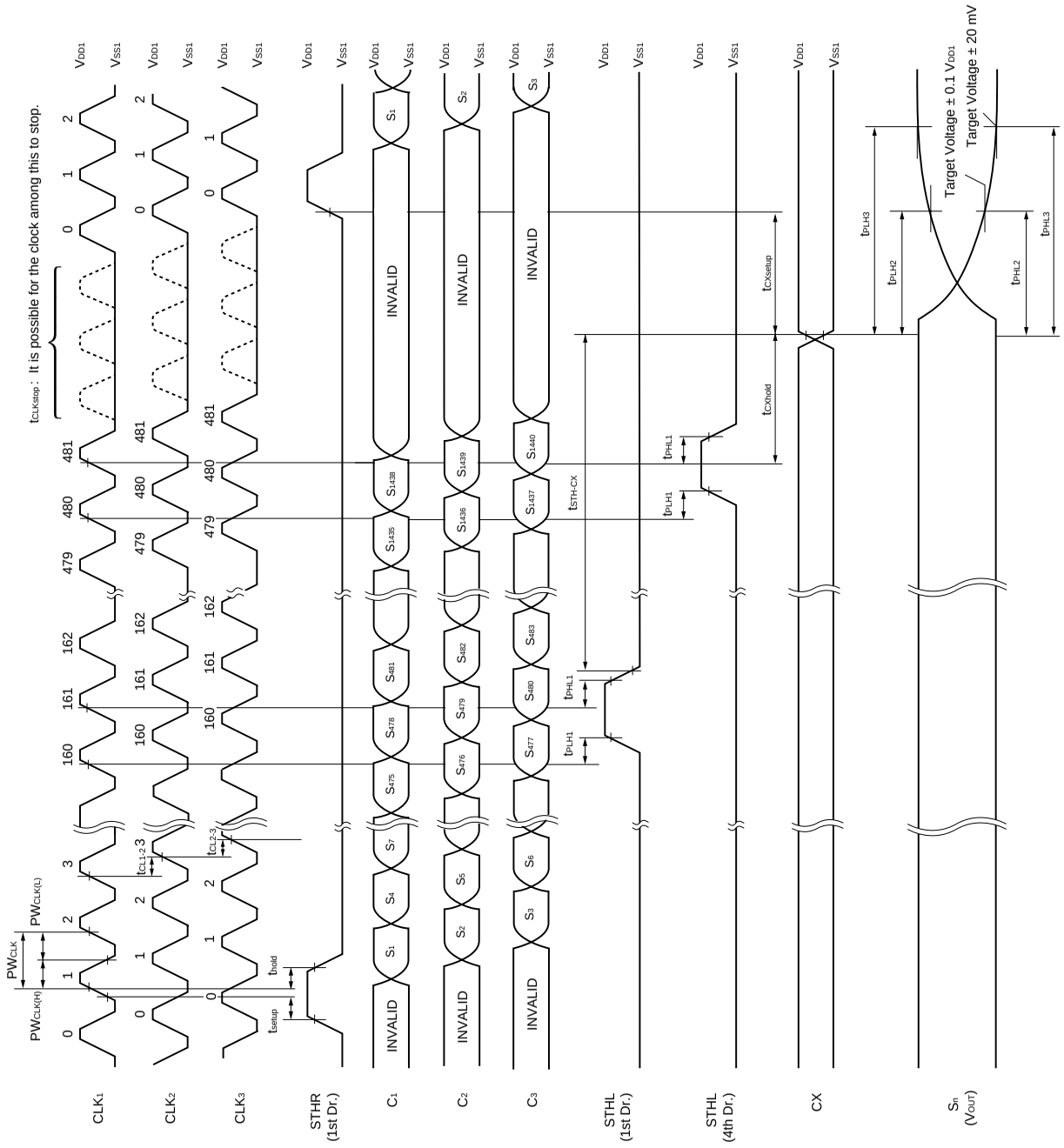
## 8. SWITCHING CHARACTERISTICS WAVEFORM (R,/L=H)

Unless otherwise specified, the input level is defined to be $V_{IH}$ = 0.7 $V_{DD1}$, $V_{IL}$ = 0.3 $V_{DD1}$.

### 8.1 1-Phase Simultaneous Sampling



## ★ 8.2 3-phase Sequential Sampling



## 9. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the μPD16781.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E).**

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD16781N-xxx: TCP (TAB Package)

| Mounting Condition | Mounting Method | Condition |
|---|---|---|
| Thermocompression | Soldering | Heating tool 300 to 350°C, heating for 2 to 3 sec, pressure 100g (per solder). |
| | ACF (Adhesive Conductive Film) | Temporaly bonding 70 to 100°C, pressure 3 to 8 kg/cm$^2$, time 3 to 5 sec. Real bonding 165 to 180°C, pressure 25 to 45 kg/cm$^2$, time 30 to 40 sec (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd). |

**Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.**

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

**Reference Documents**

**NEC Semiconductor Device Reliability/Quality Control System (C10983E)**

**Quality Grades On NEC Semiconductor Devices (C11531E)**

- **The information in this document is current as of February, 2002. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
- No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this document.
- NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC semiconductor products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
- NEC semiconductor products are classified into the following three quality grades:
  "Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.

  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

  The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.

  (Note)

  (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.

  (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).

M8E 00.4