RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD16652

200/192-OUTPUT TFT-LCD GATE DRIVER

The μPD16652 is a TFT-LCD gate driver. Because this gate driver has a level shift circuit for logic input, it can output a high gate scanning voltage in response to a CMOS-level input.

Moreover, it can also drive both the VGA/XGA/SXGA panel (192 output mode) and SVGA panel (200 output mode) by changing the number of outputs over between 200 and 192.

FEATURES

- High breakdown voltage output (ON/OFF range: V_{DD}-V_{EE} = 31 V MAX.)
- 3.3 V CMOS level input
- Number of output select function (200/192 outputs)

ORDERING INFORMATION

Parts Number	Package
μPD16652N-×××	TCP (TAB package)

Because the TCP is a custom model, consult NEC for details.

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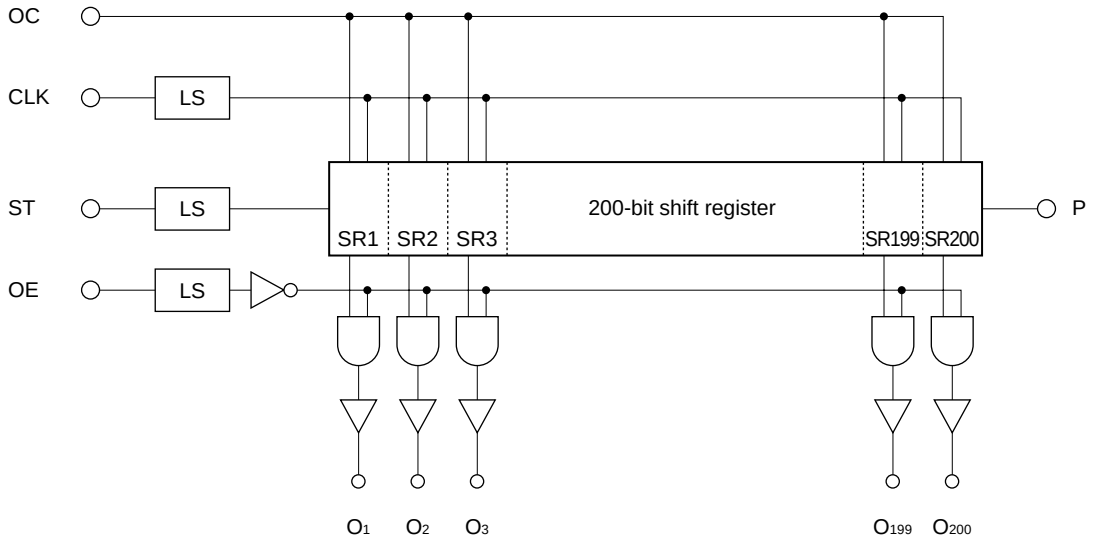
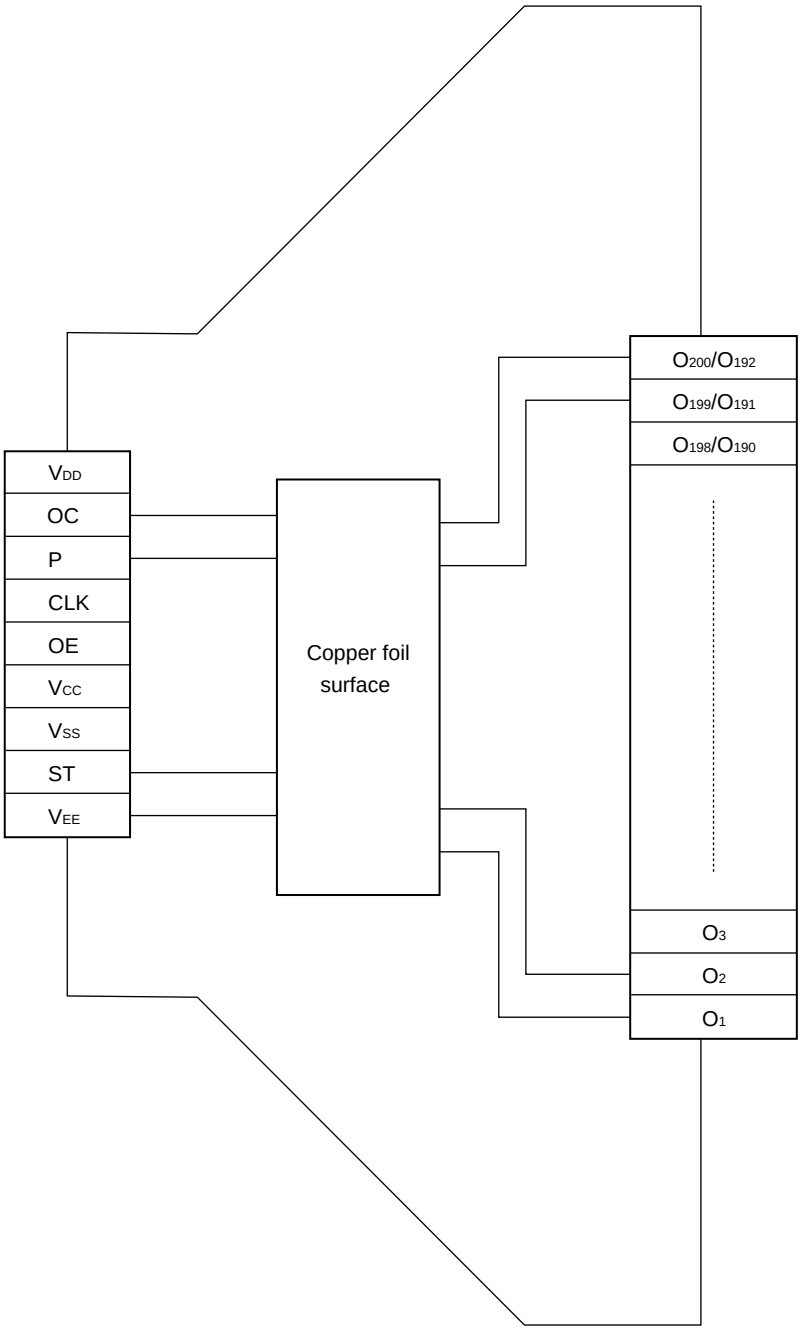
1. BLOCK DIAGRAM



LS (level shift): Interfaces between 3.3-V CMOS level and V_{DD}-V_{EE} level.

2. PIN CONFIGURATION (μPD16652n-xxx)



Caution This figure does not specify the TCP package.
It is recommended to connect OC to V_{DD} or V_{EE} on the TCP.

3. PIN DESCRIPTION

Symbol	Pin Name	Description
O_1 to O_{200}	Driver output pins	Scan signal output pins that drive the gate electrode of a TFT-LCD. The output level of each output pin changes in synchronization with the rising edge of shift clock CLK. The output voltage of the driver is V_{DD} to V_{EE} and the shift direction is only from O_1 to O_{200}.
ST	Start pulse input pin	Input pin of the internal shift register. The input data is read at the rising edge of shift clock CLK, and a scan signal is output from the driver pin. The input level is 3.3 V CMOS level.
P	Cascade output pin	This pin works as output terminal of the start pulse to the next stage when two or more μPD16652's are connected in cascade. The output pulse is output at the falling edge of the 199th clock CLK when OC = L, and cleared at the falling edge of the 200th clock. When OC = H, the pulse is output at the falling edge if the 191st clock and cleared at the falling edge of the 192nd clock. The output level is V_{DD}-V_{EE} level.
CLK	Shift clock input	Shift clock input to the internal shift register. The internal shift register shifts its contents at the rising edge of CLK.
OE	Enable input	This pin fixes the driver output to the L level when it is high. However, the shift register is not cleared. Because the OE operation is not synchronous with the clock, the internal logic operates even when OE = H.
OC	Input to select number of outputs	Selects the number of outputs. OC = L: 200 outputs (SVGA) OC = H: 192 outputs (VGA, XGA, SXGA) When OC = H (192 outputs), O_{97} through O_{104} outputs of the register are fixed to the V_{EE} level. Fix this terminal to V_{DD} or V_{EE} on TCP.
V_{DD}	Positive power supply for driver	Shared with internal logic and driver.
V_{CC}	Reference power supply	3.3 V ± 0.3 V. Reference power supply for level shifter: LS
V_{SS}	Ground	Connect this pin to the system ground.

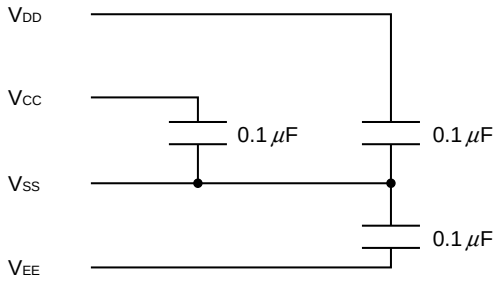
4. NOTES ON CORRECT USE

(1) Power ON/OFF sequence

To prevent the μPD16652 from damage due to latchup, turn on power in the order $V_{CC} \rightarrow V_{EE}$ and $V_{DD} \rightarrow$ logic input. Turn off power in the reverse order. Observe these power sequences even during transition period.

(2) Inserting bypass capacitor

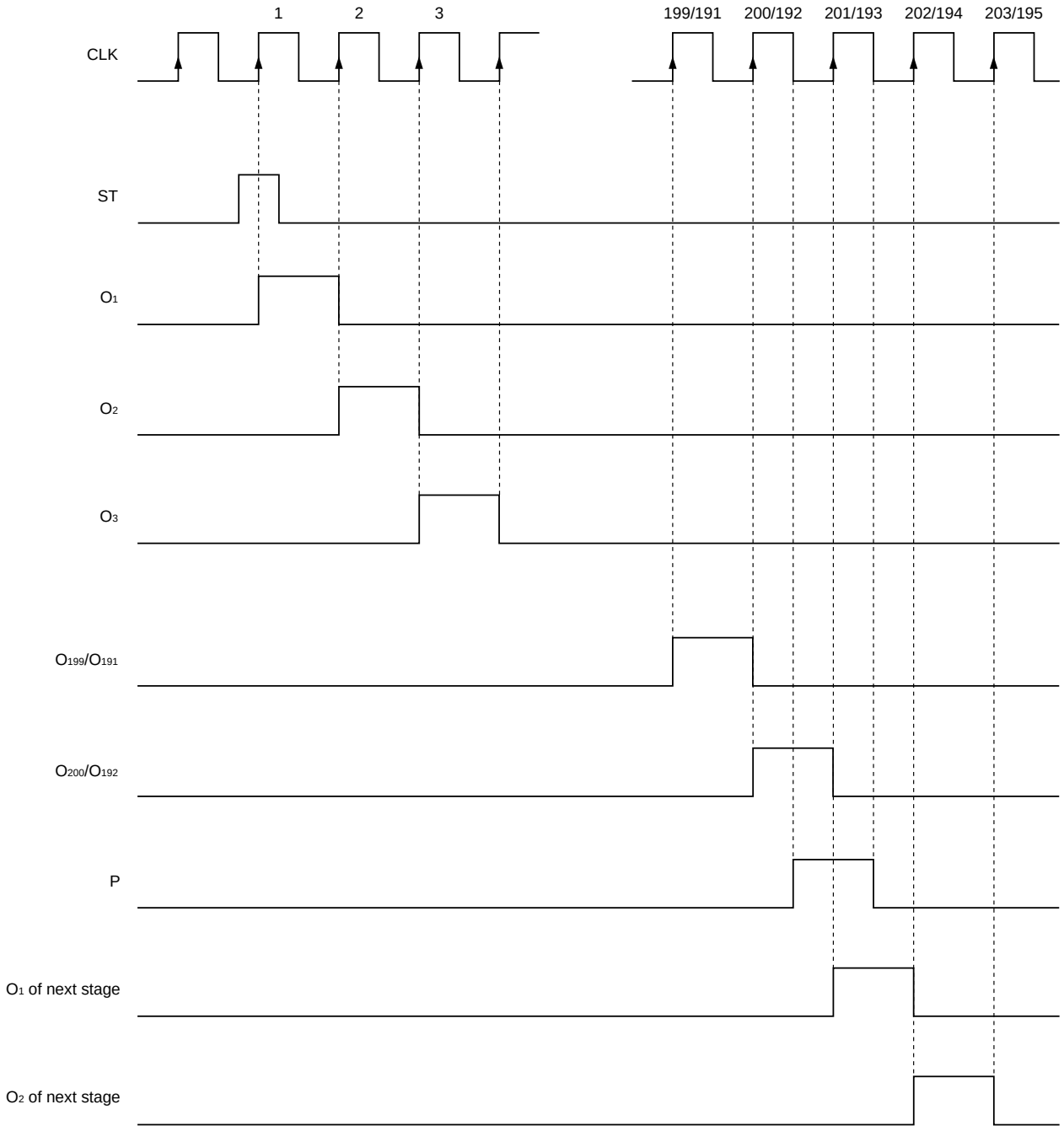
Because the internal logic operates at a high voltage (V_{DD}-V_{EE}), insert a bypass capacitor of about 0.1 μF between the respective power pins as shown below to secure the noise margin of V_{IH} and V_{IL}.



(3) Processing of OC pin

Do not input a switching signal to the OC pin that selects the number of outputs. Connect this pin to V_{DD} or V_{EE}.

5. TIMING CHART (200/192 OUTPUTS)



O_{97} through O_{104} are fixed to L (V_{EE}) level for 192-output.

6. ELECTRIC SPECIFICATION

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5 to +28	V
Supply voltage	V_{CC}	–0.5 to +7.0	V
Supply voltage	V_{DD}-V_{EE}	–0.5 to +33	V
Supply voltage	V_{EE}	–23 to +0.5	V
Input voltage	V_I	V_{EE} – 0.5 to V_{DD} + 0.5	V
Input current	I_I	±10	mA
Output current	I_O	±10	mA
Operating ambient temperature	T_A	–20 to +85	°C
Storage temperature	T_{stg}.	–55 to +125	°C

Recommended Operating Range (T_A = –20 to 70°C, V_{SS} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	10		25	V
Supply voltage	V_{EE}	–21		–5	V
Supply voltage	V_{DD}-V_{EE}	15		31	V
Supply voltage	V_{CC}	3.0	3.3	3.6	V

Electrical Specifications (T_A = –20 to +70°C, V_{DD} = 22 V, V_{EE} = –9 V, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	CLK, ST	0.7 V_{CC}		V_{CC}	V
Input voltage, low	V_{IL}	CLK, ST	V_{EE}		0.3 V_{CC}	V
Output voltage, high	V_{OH}	P, I_{OH} = –40 μA	V_{DD} – 0.4[Note]		V_{DD}[Note]	V
Output voltage, low	V_{OL}	P, I_{OH} = 40 μA	V_{EE}[Note]		V_{EE} + 0.4[Note]	V
Output current, high	I_{nOH}	O_n, V_n = V_{DD} – 1.0 V			–1.0	mA
Output current, low	I_{nOL}	O_n, V_n = V_{EE} + 1.0 V	1.0			mA
Output ON resistance	R_{on}	V_n = V_{EE} + 1.0 V or V_{DD} – 1.0 V			1.0	kΩ
Input leakage current	I_{IL}	V_I = 0 V or 3.3 V			±1.0	μA
Dynamic current consumption	I_{DD}	V_{DD}, f_{CLK} = 60 kHz		500	1000	μA
	I_{EE}	V_{EE}, f_{CLK} = 60 kHz	–1000	–500		μA
	I_{CC}	V_{CC}, f_{CLK} = 60 kHz		13	50	μA

Note The cascade output is at the driver level (V_{DD}-V_{EE}).

Switching Characteristics (T_A = –20 to +70°C, V_{DD} = 22 V, V_{EE} = –9 V, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
STVL output delay time	t_{PHL1}	C_L = 20 pF			600	ns
	t_{PLH1}	CLK → P			600	ns
Driver output delay time	t_{PHL2}	C_L = 220 pF			700	ns
	t_{PLH2}	CLK → O_n			700	ns
Output rise time	t_{TLH}	C_L = 220 pF			400	ns
Output fall time	t_{THL}	C_L = 220 pF			400	ns
Input capacitance	C_I	T_A = 25°C			15	pF
Maximum clock frequency	$f_{max.}$	When connected in cascade	300			kHz

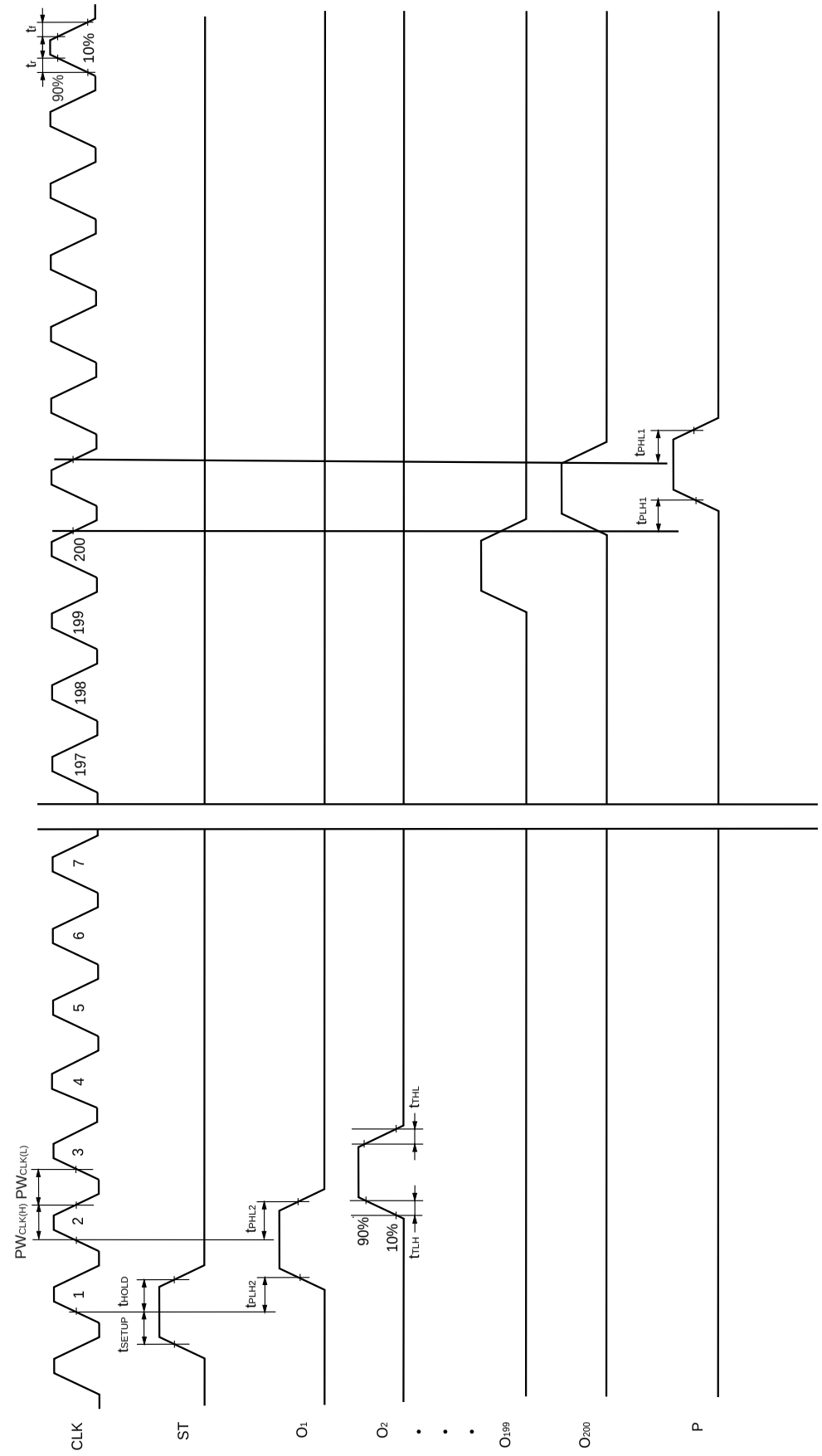
Timing Requirement (T_A = –20 to +70°C, V_{DD} = 22 V, V_{EE} = –9 V, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock pulse high period	PW_{CLK} (H)		500			ns
Clock pulse low period	PW_{CLK} (L)		500			ns
Data setup time	t_{setup}	ST ↑ → CLK ↑	200			ns
Data hold time	t_{hold}	CLK ↑ → ST ↓	200			ns

The rise and fall times of logic input must be t_r = t_f = 20 ns (10% to 90%).

Phase-out/Discontinued

7. SWITCHING CHARACTERISTICS WAVE



8. RECOMMENDED MOUNTING CONDITIONS

When mounting this product, please make sure that the following recommended conditions are satisfied.

For packaging methods and conditions other than those recommended below, please contact NEC sales personnel.

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 sec; pressure 100 g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C; pressure 3 to 8 kg/cm^2; time 3 to 5 sec. Real bonding 165 to 180°C; pressure 25 to 45 kg/cm^2, time 30 to 40 secs. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.

Reference

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades to NEC's Semiconductor Devices (C11531E)

[MEMO]