RELIMINARY PRODUCT INFORMATION

MOS INTEGRATED CIRCUIT

μPD161802

240 OUTPUTS TFT-LCD SOURCE DRIVER WITH RAM

DESCRIPTION

The μPD161802 is a TFT-LCD source driver that includes display RAM

This driver has 240 outputs, a display RAM capacity of 172.8 K bytes (240 pixels x 18 bits x 320 lines) and can provide a 262,144-color display.

FEATURES

- TFT-LCD driver with on-chip display RAM
- Logic power supply voltage: 1.6 to 2.0 V (Can also be generated within chip from power IC interface's power supply)
- CPU/RGB interface voltage: 1.8 to V_{DD}
- Power supply IC interface power supply voltage: 2.5 to 3.3 V
- Driver power supply voltage: 4.0 to 5.5 V
- Display RAM: 240 x 18 x 320 bits
- Driver outputs: 240 outputs
- CPU interface: Three types of interfaces selectable
  - 6-bit/16-bit/18-bit RGB interface (through mode, capture mode)
  - i80/M68 parallel interface (selectable from 8/16/18-bit)
  - 8-bit serial interface
- Colors: 262,144 colors/pixel
- On-chip timing generator
- On-chip oscillator
- E^2PROM interface (Micro Wire)

ORDERING INFORMATION

Part Number	Package
μPD161802P	Chip

Remark Purchasing the above chip entails the exchange of documents such as a separate memorandum on product quality, so please contact one of our sales representatives.

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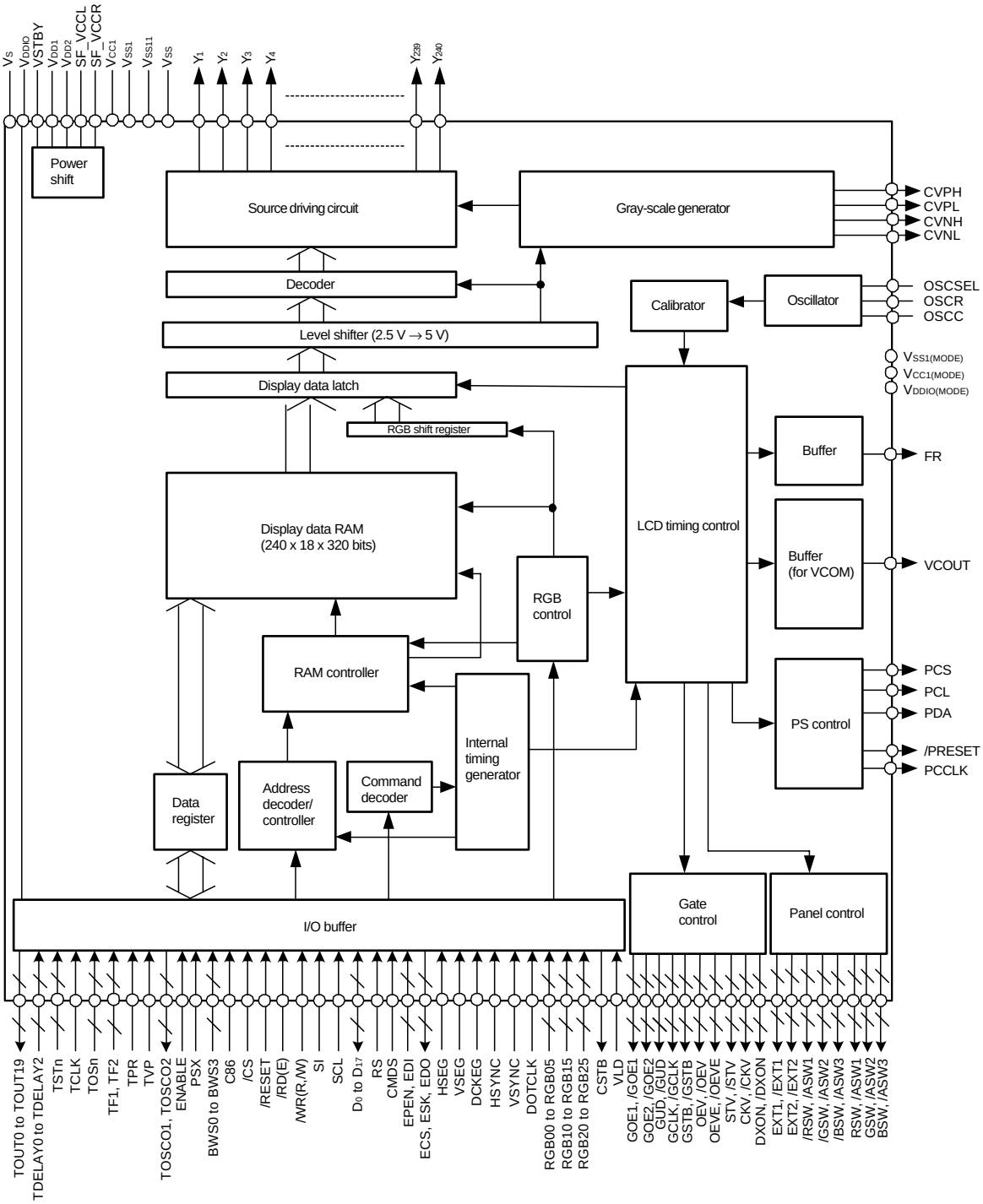
CONTENTS

HITACHI MODE

1. BLOCK DIAGRAM



Remark /xxx indicates active low signal.

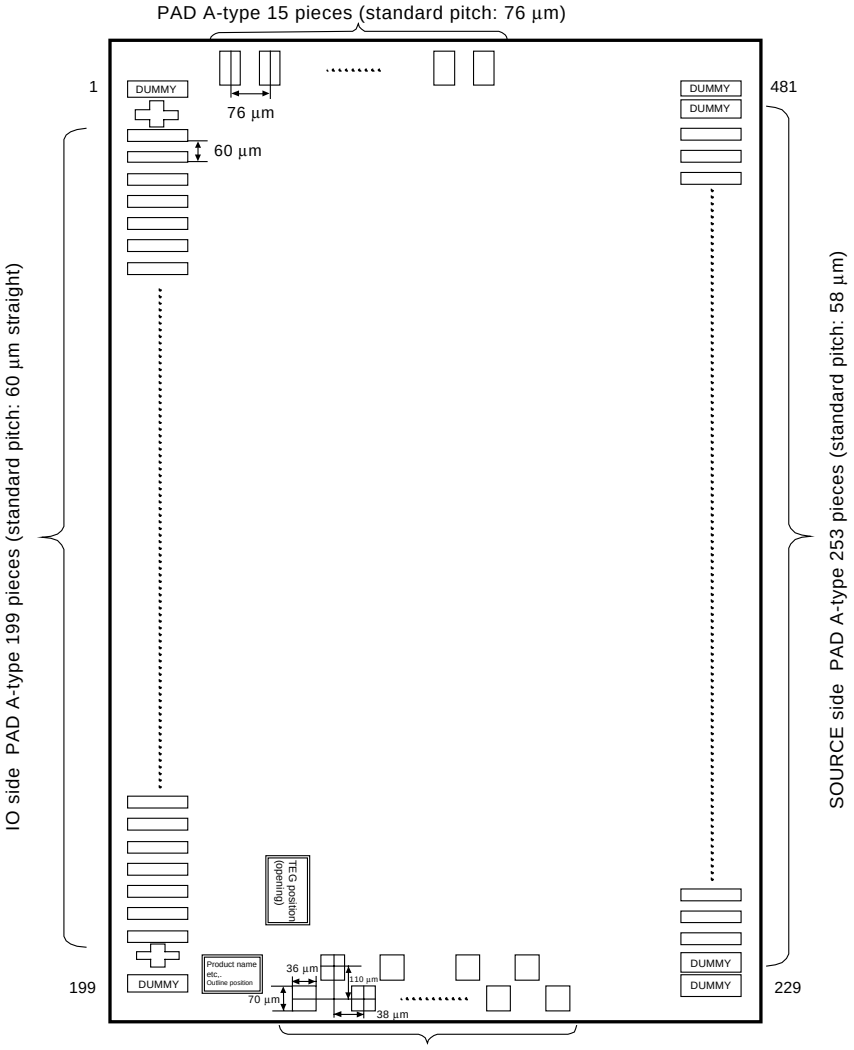
2. PIN CONFIGURATION (Pad Layout)

Chip size: 2.60 x 15.06 mm^2 (Target value)

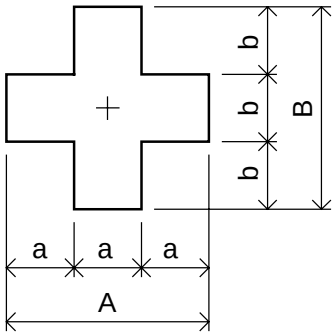
Bump size:

PAD A-type: 30 x 100 μm^2

PAD B-type: 36 x 70 μm^2



<Alignment Mark>



Alignment shape of mark (unit: μm)

A	a	B	b
90	30	90	30

Table 2–1. Pad Coordinate (1/5)

No.	Pin Name	I/O	Power	Pad coordinate [μm]	
				X	Y
1	DUMMY	–	–	-1152.00	7310.00
2	/PRESET	OUT	VCC1	-1152.00	7110.00
3	ASW3,BSW	OUT	VCC1	-1152.00	7050.00
4	/ASW3,/BSW	OUT	VCC1	-1152.00	6990.00
5	ASW2,GSW	OUT	VCC1	-1152.00	6930.00
6	/ASW2,/GSW	OUT	VCC1	-1152.00	6870.00
7	ASW1,RSW	OUT	VCC1	-1152.00	6810.00
8	/ASW1,/RSW	OUT	VCC1	-1152.00	6750.00
9	STV,GSTB	OUT	VCC1	-1152.00	6690.00
10	/STV,/GSTB	OUT	VCC1	-1152.00	6630.00
11	CKV,GCLK	OUT	VCC1	-1152.00	6570.00
12	/CKV,/GCLK	OUT	VCC1	-1152.00	6510.00
13	OEV,GOE2	OUT	VCC1	-1152.00	6450.00
14	/OEV,/GOE2	OUT	VCC1	-1152.00	6390.00
15	OEVE,GOE1	OUT	VCC1	-1152.00	6330.00
16	/OEVE,/GOE1	OUT	VCC1	-1152.00	6270.00
17	XDON,GUD	OUT	VCC1	-1152.00	6210.00
18	/XDON,/GUD	OUT	VCC1	-1152.00	6150.00
19	VCOUT	OUT	VCC1	-1152.00	6090.00
20	FR	OUT	VCC1	-1152.00	6030.00
21	PDA	OUT	VCC1	-1152.00	5970.00
22	PCS	OUT	VCC1	-1152.00	5910.00
23	PCL	OUT	VCC1	-1152.00	5850.00
24	PCCLK	OUT	VCC1	-1152.00	5790.00
25	EXT1	OUT	VCC1	-1152.00	5730.00
26	/EXT1	OUT	VCC1	-1152.00	5670.00
27	EXT2	OUT	VCC1	-1152.00	5610.00
28	/EXT2	OUT	VCC1	-1152.00	5550.00
29	VDDIO(MODE)	–	–	-1152.00	5490.00
30	CSTB	OUT	VDDIO	-1152.00	5390.00
31	/RESET	IN	VDDIO	-1152.00	5290.00
32	D17	IO	VDDIO	-1152.00	5190.00
33	D16	IO	VDDIO	-1152.00	5090.00
34	D15	IO	VDDIO	-1152.00	4990.00
35	D14	IO	VDDIO	-1152.00	4890.00
36	D13	IO	VDDIO	-1152.00	4790.00
37	D12	IO	VDDIO	-1152.00	4690.00
38	D11	IO	VDDIO	-1152.00	4590.00
39	D10	IO	VDDIO	-1152.00	4490.00
40	D9	IO	VDDIO	-1152.00	4390.00
41	D8	IO	VDDIO	-1152.00	4290.00
42	D7	IO	VDDIO	-1152.00	4190.00
43	D6	IO	VDDIO	-1152.00	4090.00
44	D5	IO	VDDIO	-1152.00	3990.00
45	D4	IO	VDDIO	-1152.00	3890.00
46	D3	IO	VDDIO	-1152.00	3790.00
47	D2	IO	VDDIO	-1152.00	3690.00
48	D1	IO	VDDIO	-1152.00	3590.00
49	D0	IO	VDDIO	-1152.00	3490.00
50	VSS1(MODE)	–	–	-1152.00	3390.00
51	/RD	IN	VDDIO	-1152.00	3290.00
52	/WR	IN	VDDIO	-1152.00	3190.00
53	RS	IN	VDDIO	-1152.00	3090.00
54	/CS	IN	VDDIO	-1152.00	2990.00
55	VDDIO(MODE)	–	–	-1152.00	2890.00
56	SI	IN	VDDIO	-1152.00	2790.00
57	SCL	IN	VDDIO	-1152.00	2690.00
58	VSS1(MODE)	–	–	-1152.00	2590.00
59	VLD	IN	VDDIO	-1152.00	2490.00
60	VDDIO(MODE)	–	–	-1152.00	2390.00
61	VSYNC	IN	VDDIO	-1152.00	2290.00
62	HSYNC	IN	VDDIO	-1152.00	2190.00
63	DOTCLK	IN	VDDIO	-1152.00	2090.00
64	ENABLE		VDDIO	-1152.00	1990.00
65	VSS1(MODE)	–	–	-1152.00	1890.00
66	RGB00	IN	VDDIO	-1152.00	1790.00
67	RGB01	IN	VDDIO	-1152.00	1690.00
68	RGB02	IN	VDDIO	-1152.00	1590.00
69	RGB03	IN	VDDIO	-1152.00	1490.00
70	RGB04	IN	VDDIO	-1152.00	1390.00
71	RGB05	IN	VDDIO	-1152.00	1290.00
72	RGB10	IN	VDDIO	-1152.00	1190.00
73	RGB11	IN	VDDIO	-1152.00	1090.00
74	RGB12	IN	VDDIO	-1152.00	990.00
75	RGB13	IN	VDDIO	-1152.00	890.00
76	RGB14	IN	VDDIO	-1152.00	790.00
77	RGB15	IN	VDDIO	-1152.00	690.00
78	RGB20	IN	VDDIO	-1152.00	590.00
79	RGB21	IN	VDDIO	-1152.00	490.00
80	RGB22	IN	VDDIO	-1152.00	390.00
81	RGB23	IN	VDDIO	-1152.00	290.00
82	RGB24	IN	VDDIO	-1152.00	190.00
83	RGB25	IN	VDDIO	-1152.00	90.00
84	VDDIO	–	–	-1152.00	-60.00
85	VDDIO	–	–	-1152.00	-120.00
86	VDDIO	–	–	-1152.00	-180.00
87	VDDIO	–	–	-1152.00	-240.00
88	VDDIO	–	–	-1152.00	-300.00
89	VDDIO	–	–	-1152.00	-360.00
90	VCC1	–	–	-1152.00	-420.00
91	VCC1	–	–	-1152.00	-480.00
92	VCC1	–	–	-1152.00	-540.00
93	VCC1	–	–	-1152.00	-600.00
94	VCC1	–	–	-1152.00	-660.00
95	VCC1	–	–	-1152.00	-720.00
96	SF_VCCL	OUT	VCC1	-1152.00	-780.00
97	SF_VCCL	OUT	VCC1	-1152.00	-840.00
98	SF_VCCL	OUT	VCC1	-1152.00	-900.00
99	SF_VCCL	OUT	VCC1	-1152.00	-960.00
100	SF_VCCL	OUT	VCC1	-1152.00	-1020.00
101	SF_VCCL	OUT	VCC1	-1152.00	-1080.00
102	VDD1	–	–	-1152.00	-1140.00
103	VDD1	–	–	-1152.00	-1200.00
104	VDD1	–	–	-1152.00	-1260.00
105	VDD1	–	–	-1152.00	-1320.00
106	VDD1	–	–	-1152.00	-1380.00
107	VDD1	–	–	-1152.00	-1440.00
108	VDD1	–	–	-1152.00	-1500.00
109	VDD1	–	–	-1152.00	-1560.00
110	SF_VCCR	OUT	VCC1	-1152.00	-1620.00
111	SF_VCCR	OUT	VCC1	-1152.00	-1680.00
112	SF_VCCR	OUT	VCC1	-1152.00	-1740.00
113	SF_VCCR	OUT	VCC1	-1152.00	-1800.00
114	SF_VCCR	OUT	VCC1	-1152.00	-1860.00
115	SF_VCCR	OUT	VCC1	-1152.00	-1920.00
116	VDD2	–	–	-1152.00	-1980.00
117	VDD2	–	–	-1152.00	-2040.00
118	VDD2	–	–	-1152.00	-2100.00
119	VDD2	–	–	-1152.00	-2160.00
120	VDD2	–	–	-1152.00	-2220.00

PAD A TYPE

Table 2–1. Pad Coordinate (2/5)

No.	Pin Name	I/O	Power	Pad coordinate [μm]	
				X	Y
121	VDD2	–	–	-1152.00	-2280.00
122	VDD2	–	–	-1152.00	-2340.00
123	VDD2	–	–	-1152.00	-2400.00
124	VSS1	–	–	-1152.00	-2460.00
125	VSS1	–	–	-1152.00	-2520.00
126	VSS1	–	–	-1152.00	-2580.00
127	VSS1	–	–	-1152.00	-2640.00
128	VSS1	–	–	-1152.00	-2700.00
129	VSS1	–	–	-1152.00	-2760.00
130	VSS11	–	–	-1152.00	-2820.00
131	VSS11	–	–	-1152.00	-2880.00
132	VSS11	–	–	-1152.00	-2940.00
133	VSS11	–	–	-1152.00	-3000.00
134	VSS11	–	–	-1152.00	-3060.00
135	VSS11	–	–	-1152.00	-3120.00
136	VSS	–	–	-1152.00	-3180.00
137	VSS	–	–	-1152.00	-3240.00
138	VSS	–	–	-1152.00	-3300.00
139	VSS	–	–	-1152.00	-3360.00
140	VSS	–	–	-1152.00	-3420.00
141	VSS	–	–	-1152.00	-3480.00
142	CVNL	IO	VS	-1152.00	-3540.00
143	CVNL	IO	VS	-1152.00	-3600.00
144	CVNL	IO	VS	-1152.00	-3660.00
145	CVNH	IO	VS	-1152.00	-3720.00
146	CVNH	IO	VS	-1152.00	-3780.00
147	CVNH	IO	VS	-1152.00	-3840.00
148	CVPL	IO	VS	-1152.00	-3900.00
149	CVPL	IO	VS	-1152.00	-3960.00
150	CVPL	IO	VS	-1152.00	-4020.00
151	CVPH	IO	VS	-1152.00	-4080.00
152	CVPH	IO	VS	-1152.00	-4140.00
153	CVPH	IO	VS	-1152.00	-4200.00
154	VS	–	–	-1152.00	-4390.00
155	VS	–	–	-1152.00	-4450.00
156	VS	–	–	-1152.00	-4510.00
157	VS	–	–	-1152.00	-4570.00
158	VS	–	–	-1152.00	-4630.00
159	VS	–	–	-1152.00	-4690.00
160	OSCC	IN	VDD1	-1152.00	-4790.00
161	OSCR	OUT	VDD1	-1152.00	-4850.00
162	EDI	IN	VCC1	-1152.00	-4950.00
163	ECS	OUT	VCC1	-1152.00	-5010.00
164	ESK	OUT	VCC1	-1152.00	-5070.00
165	EDO	OUT	VCC1	-1152.00	-5130.00
166	VSS1(MODE)	–	–	-1152.00	-5190.00
167	EPEN	–	VCC1	-1152.00	-5250.00
168	OSCSEL	IN	VCC1	-1152.00	-5310.00
169	VCC1(MODE)	–	–	-1152.00	-5370.00
170	CMDS	IN	VCC1	-1152.00	-5430.00
171	HSEG	IN	VCC1	-1152.00	-5490.00
172	VSEG	IN	VCC1	-1152.00	-5550.00
173	VCC1(MODE)	–	–	-1152.00	-5610.00
174	DCKEG	IN	VCC1	-1152.00	-5670.00
175	PSX	IN	VCC1	-1152.00	-5730.00
176	C86	IN	VCC1	-1152.00	-5790.00
177	VCC1(MODE)	–	–	-1152.00	-5850.00
178	BWS0	IN	VCC1	-1152.00	-5910.00
179	BWS1	IN	VCC1	-1152.00	-5970.00
180	BWS2	IN	VCC1	-1152.00	-6030.00

No.	Pin Name	I/O	Power	Pad coordinate [μm]	
				X	Y
181	VCC1(MODE)	–	–	-1152.00	-6090.00
182	BWS3	IN	VCC1	-1152.00	-6150.00
183	VSTBY	IN	VCC1	-1152.00	-6210.00
184	TDELAY0	IN	VCC1	-1152.00	-6270.00
185	TDELAY1	IN	VCC1	-1152.00	-6330.00
186	TDELAY2	IN	VCC1	-1152.00	-6390.00
187	TCLK	IN	VCC1	-1152.00	-6450.00
188	TSTVIHL	IN	VCC1	-1152.00	-6510.00
189	TSTRTST	IN	VCC1	-1152.00	-6570.00
190	TOSCSEO1	IN	VCC1	-1152.00	-6630.00
191	TOSCSEO2	IN	VCC1	-1152.00	-6690.00
192	TOSCSEI1	IN	VCC1	-1152.00	-6750.00
193	TOSCSEI2	IN	VCC1	-1152.00	-6810.00
194	TOSCI1	IN	VCC1	-1152.00	-6870.00
195	TOSCI2	IN	VCC1	-1152.00	-6930.00
196	TOSCO1	OUT	VCC1	-1152.00	-6990.00
197	TOSCO2	OUT	VCC1	-1152.00	-7050.00
198	VSS1(MODE)	–	–	-1152.00	-7110.00
199	DUMMY	–	–	-1152.00	-7310.00
200	DUMMY	–	–	-785.00	-7397.00
201	DUMMY	–	–	-747.00	-7287.00
202	TOUT19	OUT	VCC1	-709.00	-7397.00
203	TOUT18	OUT	VCC1	-671.00	-7280.00
204	TOUT17	OUT	VCC1	-633.00	-7397.00
205	TOUT16	OUT	VCC1	-595.00	-7280.00
206	TOUT15	OUT	VCC1	-557.00	-7397.00
207	TOUT14	OUT	VCC1	-519.00	-7280.00
208	TOUT13	OUT	VCC1	-481.00	-7397.00
209	TOUT12	OUT	VCC1	-443.00	-7280.00
210	TOUT11	OUT	VCC1	-405.00	-7397.00
211	TOUT10	OUT	VCC1	-367.00	-7280.00
212	TOUT9	OUT	VCC1	-329.00	-7397.00
213	TOUT8	OUT	VCC1	-291.00	-7280.00
214	TOUT7	OUT	VCC1	-253.00	-7397.00
215	TOUT6	OUT	VCC1	-215.00	-7280.00
216	TOUT5	OUT	VCC1	-177.00	-7397.00
217	TOUT4	OUT	VCC1	-139.00	-7280.00
218	TOUT3	OUT	VCC1	-101.00	-7397.00
219	TOUT2	OUT	VCC1	-63.00	-7280.00
220	TOUT1	OUT	VCC1	-25.00	-7397.00
221	TOUT0	OUT	VCC1	13.00	-7280.00
222	TF1	IN	–	51.00	-7397.00
223	TF2	IN	–	89.00	-7280.00
224	TPR	IN	–	127.00	-7397.00
225	TVP	IN	–	165.00	-7280.00
226	VSS1(MODE)	–	–	203.00	-7397.00
227	VDD1(MODE)	–	–	241.00	-7280.00
228	DUMMY	–	–	279.00	-7390.00
229	DUMMY	–	–	1152.00	-7308.00
230	DUMMY	–	–	1152.00	-7250.00
231	Y1	OUT	VS	1152.00	-7192.00
232	Y2	OUT	VS	1152.00	-7134.00
233	Y3	OUT	VS	1152.00	-7076.00
234	Y4	OUT	VS	1152.00	-7018.00
235	Y5	OUT	VS	1152.00	-6960.00
236	Y6	OUT	VS	1152.00	-6902.00
237	Y7	OUT	VS	1152.00	-6844.00
238	Y8	OUT	VS	1152.00	-6786.00
239	Y9	OUT	VS	1152.00	-6728.00
240	Y10	OUT	VS	1152.00	-6670.00

PAD A TYPE

PAD B TYPE

Table 2–1. Pad Coordinate (3/5)

No.	Pin Name	I/O	Power	Pad coordinate [μm]	
				X	Y
241	Y11	OUT	VS	1152.00	-6612.00
242	Y12	OUT	VS	1152.00	-6554.00
243	Y13	OUT	VS	1152.00	-6496.00
244	Y14	OUT	VS	1152.00	-6438.00
245	Y15	OUT	VS	1152.00	-6380.00
246	Y16	OUT	VS	1152.00	-6322.00
247	Y17	OUT	VS	1152.00	-6264.00
248	Y18	OUT	VS	1152.00	-6206.00
249	Y19	OUT	VS	1152.00	-6148.00
250	Y20	OUT	VS	1152.00	-6090.00
251	Y21	OUT	VS	1152.00	-6032.00
252	Y22	OUT	VS	1152.00	-5974.00
253	Y23	OUT	VS	1152.00	-5916.00
254	Y24	OUT	VS	1152.00	-5858.00
255	Y25	OUT	VS	1152.00	-5800.00
256	Y26	OUT	VS	1152.00	-5742.00
257	Y27	OUT	VS	1152.00	-5684.00
258	Y28	OUT	VS	1152.00	-5626.00
259	Y29	OUT	VS	1152.00	-5568.00
260	Y30	OUT	VS	1152.00	-5510.00
261	Y31	OUT	VS	1152.00	-5452.00
262	Y32	OUT	VS	1152.00	-5394.00
263	Y33	OUT	VS	1152.00	-5336.00
264	Y34	OUT	VS	1152.00	-5278.00
265	Y35	OUT	VS	1152.00	-5220.00
266	Y36	OUT	VS	1152.00	-5162.00
267	Y37	OUT	VS	1152.00	-5104.00
268	Y38	OUT	VS	1152.00	-5046.00
269	Y39	OUT	VS	1152.00	-4988.00
270	Y40	OUT	VS	1152.00	-4930.00
271	Y41	OUT	VS	1152.00	-4872.00
272	Y42	OUT	VS	1152.00	-4814.00
273	Y43	OUT	VS	1152.00	-4756.00
274	Y44	OUT	VS	1152.00	-4698.00
275	Y45	OUT	VS	1152.00	-4640.00
276	Y46	OUT	VS	1152.00	-4582.00
277	Y47	OUT	VS	1152.00	-4524.00
278	Y48	OUT	VS	1152.00	-4466.00
279	Y49	OUT	VS	1152.00	-4408.00
280	Y50	OUT	VS	1152.00	-4350.00
281	Y51	OUT	VS	1152.00	-4292.00
282	Y52	OUT	VS	1152.00	-4234.00
283	Y53	OUT	VS	1152.00	-4176.00
284	Y54	OUT	VS	1152.00	-4118.00
285	Y55	OUT	VS	1152.00	-4060.00
286	Y56	OUT	VS	1152.00	-4002.00
287	Y57	OUT	VS	1152.00	-3944.00
288	Y58	OUT	VS	1152.00	-3886.00
289	Y59	OUT	VS	1152.00	-3828.00
290	Y60	OUT	VS	1152.00	-3770.00
291	Y61	OUT	VS	1152.00	-3712.00
292	Y62	OUT	VS	1152.00	-3654.00
293	Y63	OUT	VS	1152.00	-3596.00
294	Y64	OUT	VS	1152.00	-3538.00
295	Y65	OUT	VS	1152.00	-3480.00
296	Y66	OUT	VS	1152.00	-3422.00
297	Y67	OUT	VS	1152.00	-3364.00
298	Y68	OUT	VS	1152.00	-3306.00
299	Y69	OUT	VS	1152.00	-3248.00
300	Y70	OUT	VS	1152.00	-3190.00
301	Y71	OUT	VS	1152.00	-3132.00
302	Y72	OUT	VS	1152.00	-3074.00
303	Y73	OUT	VS	1152.00	-3016.00
304	Y74	OUT	VS	1152.00	-2958.00
305	Y75	OUT	VS	1152.00	-2900.00
306	Y76	OUT	VS	1152.00	-2842.00
307	Y77	OUT	VS	1152.00	-2784.00
308	Y78	OUT	VS	1152.00	-2726.00
309	Y79	OUT	VS	1152.00	-2668.00
310	Y80	OUT	VS	1152.00	-2610.00
311	Y81	OUT	VS	1152.00	-2552.00
312	Y82	OUT	VS	1152.00	-2494.00
313	Y83	OUT	VS	1152.00	-2436.00
314	Y84	OUT	VS	1152.00	-2378.00
315	Y85	OUT	VS	1152.00	-2320.00
316	Y86	OUT	VS	1152.00	-2262.00
317	Y87	OUT	VS	1152.00	-2204.00
318	Y88	OUT	VS	1152.00	-2146.00
319	Y89	OUT	VS	1152.00	-2088.00
320	Y90	OUT	VS	1152.00	-2030.00
321	Y91	OUT	VS	1152.00	-1972.00
322	Y92	OUT	VS	1152.00	-1914.00
323	Y93	OUT	VS	1152.00	-1856.00
324	Y94	OUT	VS	1152.00	-1798.00
325	Y95	OUT	VS	1152.00	-1740.00
326	Y96	OUT	VS	1152.00	-1682.00
327	Y97	OUT	VS	1152.00	-1624.00
328	Y98	OUT	VS	1152.00	-1566.00
329	Y99	OUT	VS	1152.00	-1508.00
330	Y100	OUT	VS	1152.00	-1450.00
331	Y101	OUT	VS	1152.00	-1392.00
332	Y102	OUT	VS	1152.00	-1334.00
333	Y103	OUT	VS	1152.00	-1276.00
334	Y104	OUT	VS	1152.00	-1218.00
335	Y105	OUT	VS	1152.00	-1160.00
336	Y106	OUT	VS	1152.00	-1102.00
337	Y107	OUT	VS	1152.00	-1044.00
338	Y108	OUT	VS	1152.00	-986.00
339	Y109	OUT	VS	1152.00	-928.00
340	Y110	OUT	VS	1152.00	-870.00
341	Y111	OUT	VS	1152.00	-812.00
342	Y112	OUT	VS	1152.00	-754.00
343	Y113	OUT	VS	1152.00	-696.00
344	Y114	OUT	VS	1152.00	-638.00
345	Y115	OUT	VS	1152.00	-580.00
346	Y116	OUT	VS	1152.00	-522.00
347	Y117	OUT	VS	1152.00	-464.00
348	Y118	OUT	VS	1152.00	-406.00
349	Y119	OUT	VS	1152.00	-348.00
350	Y120	OUT	VS	1152.00	-290.00
351	Y121	OUT	VS	1152.00	-232.00
352	Y122	OUT	VS	1152.00	-174.00
353	Y123	OUT	VS	1152.00	-116.00
354	Y124	OUT	VS	1152.00	-58.00
355	Y125	OUT	VS	1152.00	0.00
356	Y126	OUT	VS	1152.00	58.00
357	Y127	OUT	VS	1152.00	116.00
358	Y128	OUT	VS	1152.00	174.00
359	DUMMY	–	–	1152.00	232.00
360	DUMMY	–	–	1152.00	290.00

PAD A TYPE

Table 2–1. Pad Coordinate (4/5)

No.	Pin Name	I/O	Power	Pad coordinate [μm]	
				X	Y
361	DUMMY	–	–	1152.00	348.00
362	DUMMY	–	–	1152.00	406.00
363	DUMMY	–	–	1152.00	464.00
364	DUMMY	–	–	1152.00	522.00
365	DUMMY	–	–	1152.00	580.00
366	DUMMY	–	–	1152.00	638.00
367	DUMMY	–	–	1152.00	696.00
368	Y129	OUT	VS	1152.00	754.00
369	Y130	OUT	VS	1152.00	812.00
370	Y131	OUT	VS	1152.00	870.00
371	Y132	OUT	VS	1152.00	928.00
372	Y133	OUT	VS	1152.00	986.00
373	Y134	OUT	VS	1152.00	1044.00
374	Y135	OUT	VS	1152.00	1102.00
375	Y136	OUT	VS	1152.00	1160.00
376	Y137	OUT	VS	1152.00	1218.00
377	Y138	OUT	VS	1152.00	1276.00
378	Y139	OUT	VS	1152.00	1334.00
379	Y140	OUT	VS	1152.00	1392.00
380	Y141	OUT	VS	1152.00	1450.00
381	Y142	OUT	VS	1152.00	1508.00
382	Y143	OUT	VS	1152.00	1566.00
383	Y144	OUT	VS	1152.00	1624.00
384	Y145	OUT	VS	1152.00	1682.00
385	Y146	OUT	VS	1152.00	1740.00
386	Y147	OUT	VS	1152.00	1798.00
387	Y148	OUT	VS	1152.00	1856.00
388	Y149	OUT	VS	1152.00	1914.00
389	Y150	OUT	VS	1152.00	1972.00
390	Y151	OUT	VS	1152.00	2030.00
391	Y152	OUT	VS	1152.00	2088.00
392	Y153	OUT	VS	1152.00	2146.00
393	Y154	OUT	VS	1152.00	2204.00
394	Y155	OUT	VS	1152.00	2262.00
395	Y156	OUT	VS	1152.00	2320.00
396	Y157	OUT	VS	1152.00	2378.00
397	Y158	OUT	VS	1152.00	2436.00
398	Y159	OUT	VS	1152.00	2494.00
399	Y160	OUT	VS	1152.00	2552.00
400	Y161	OUT	VS	1152.00	2610.00
401	Y162	OUT	VS	1152.00	2668.00
402	Y163	OUT	VS	1152.00	2726.00
403	Y164	OUT	VS	1152.00	2784.00
404	Y165	OUT	VS	1152.00	2842.00
405	Y166	OUT	VS	1152.00	2900.00
406	Y167	OUT	VS	1152.00	2958.00
407	Y168	OUT	VS	1152.00	3016.00
408	Y169	OUT	VS	1152.00	3074.00
409	Y170	OUT	VS	1152.00	3132.00
410	Y171	OUT	VS	1152.00	3190.00
411	Y172	OUT	VS	1152.00	3248.00
412	Y173	OUT	VS	1152.00	3306.00
413	Y174	OUT	VS	1152.00	3364.00
414	Y175	OUT	VS	1152.00	3422.00
415	Y176	OUT	VS	1152.00	3480.00
416	Y177	OUT	VS	1152.00	3538.00
417	Y178	OUT	VS	1152.00	3596.00
418	Y179	OUT	VS	1152.00	3654.00
419	Y180	OUT	VS	1152.00	3712.00
420	Y181	OUT	VS	1152.00	3770.00

No.	Pin Name	I/O	Power	Pad coordinate [μm]	
				X	Y
421	Y182	OUT	VS	1152.00	3828.00
422	Y183	OUT	VS	1152.00	3886.00
423	Y184	OUT	VS	1152.00	3944.00
424	Y185	OUT	VS	1152.00	4002.00
425	Y186	OUT	VS	1152.00	4060.00
426	Y187	OUT	VS	1152.00	4118.00
427	Y188	OUT	VS	1152.00	4176.00
428	Y189	OUT	VS	1152.00	4234.00
429	Y190	OUT	VS	1152.00	4292.00
430	Y191	OUT	VS	1152.00	4350.00
431	Y192	OUT	VS	1152.00	4408.00
432	Y193	OUT	VS	1152.00	4466.00
433	Y194	OUT	VS	1152.00	4524.00
434	Y195	OUT	VS	1152.00	4582.00
435	Y196	OUT	VS	1152.00	4640.00
436	Y197	OUT	VS	1152.00	4698.00
437	Y198	OUT	VS	1152.00	4756.00
438	Y199	OUT	VS	1152.00	4814.00
439	Y200	OUT	VS	1152.00	4872.00
440	Y201	OUT	VS	1152.00	4930.00
441	Y202	OUT	VS	1152.00	4988.00
442	Y203	OUT	VS	1152.00	5046.00
443	Y204	OUT	VS	1152.00	5104.00
444	Y205	OUT	VS	1152.00	5162.00
445	Y206	OUT	VS	1152.00	5220.00
446	Y207	OUT	VS	1152.00	5278.00
447	Y208	OUT	VS	1152.00	5336.00
448	Y209	OUT	VS	1152.00	5394.00
449	Y210	OUT	VS	1152.00	5452.00
450	Y211	OUT	VS	1152.00	5510.00
451	Y212	OUT	VS	1152.00	5568.00
452	Y213	OUT	VS	1152.00	5626.00
453	Y214	OUT	VS	1152.00	5684.00
454	Y215	OUT	VS	1152.00	5742.00
455	Y216	OUT	VS	1152.00	5800.00
456	Y217	OUT	VS	1152.00	5858.00
457	Y218	OUT	VS	1152.00	5916.00
458	Y219	OUT	VS	1152.00	5974.00
459	Y220	OUT	VS	1152.00	6032.00
460	Y221	OUT	VS	1152.00	6090.00
461	Y222	OUT	VS	1152.00	6148.00
462	Y223	OUT	VS	1152.00	6206.00
463	Y224	OUT	VS	1152.00	6264.00
464	Y225	OUT	VS	1152.00	6322.00
465	Y226	OUT	VS	1152.00	6380.00
466	Y227	OUT	VS	1152.00	6438.00
467	Y228	OUT	VS	1152.00	6496.00
468	Y229	OUT	VS	1152.00	6554.00
469	Y230	OUT	VS	1152.00	6612.00
470	Y231	OUT	VS	1152.00	6670.00
471	Y232	OUT	VS	1152.00	6728.00
472	Y233	OUT	VS	1152.00	6786.00
473	Y234	OUT	VS	1152.00	6844.00
474	Y235	OUT	VS	1152.00	6902.00
475	Y236	OUT	VS	1152.00	6960.00
476	Y237	OUT	VS	1152.00	7018.00
477	Y238	OUT	VS	1152.00	7076.00
478	Y239	OUT	VS	1152.00	7134.00
479	Y240	OUT	VS	1152.00	7192.00
480	DUMMY	–	–	1152.00	7250.00

PAD A TYPE

Table 2–1. Pad Coordinate (5/5)

No.	Pin Name	I/O	Power	Pad coordinate [μm]	
				X	Y
481	DUMMY	–	–	1152.00	7308.00
482	DUMMY	–	–	124.00	7382.00
483	DUMMY	–	–	48.00	7382.00
484	DUMMY	–	–	-28.00	7382.00
485	DUMMY	–	–	-104.00	7382.00
486	DUMMY	–	–	-180.00	7382.00
487	DUMMY	–	–	-256.00	7382.00
488	DUMMY	–	–	-332.00	7382.00
489	DUMMY	–	–	-408.00	7382.00
490	DUMMY	–	–	-484.00	7382.00
491	DUMMY	–	–	-560.00	7382.00
492	DUMMY	–	–	-636.00	7382.00
493	DUMMY	–	–	-712.00	7382.00
494	DUMMY	–	–	-788.00	7382.00
495	DUMMY	–	–	-864.00	7382.00
496	DUMMY	–	–	-940.00	7382.00

PAD A TYPE

	X [μm]	Y [μm]
Alignment Mark (M1)	-1152.00	7210.00
Alignment Mark (M2)	-1152.00	-7210.00

3. PIN FUNCTIONS

3.1 Power Supply System Pins (1/2)

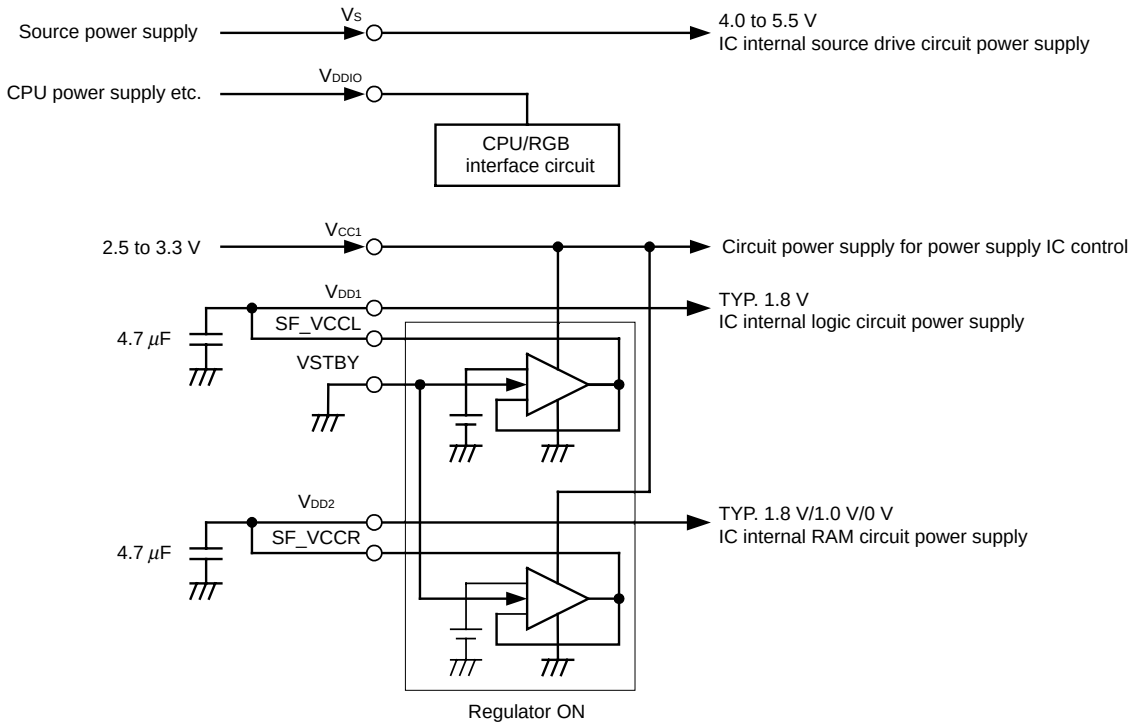
Symbol	Pin Name	Pad No.	I/O	Function
V_{DD1}	Power supply for logic	102 to 109	–	This is the power supply pin for the logic. When VSTBY = L, there is no need to apply a power supply voltage. The voltage that is input from the power supply control pin (V_{CC1}) is used to generate the logic's power supply voltage within the chip. However, the interface with the CPU must be implemented using V_{DDIO}. Also, no power is supplied to the V_{DD1} pin, but it should be connected to the SF_VCCL pin and a 4.7 μF capacitor should be connected between it and the GND pin. Refer to **Figure 3–1**.
SF_VCCL	Internal logic power supply generation amplifier output	96 to 101	Output	If using 3 power supplies (VSTBY = L), be sure to connect a capacitor between this pin and a GND connection. For details, refer to **Figure 3–1**. If using 4 power supplies (VSTBY = H), leave this pin open.
V_{DD2}	Power supply for display RAM	116 to 123	–	This power supply pin is used for the display RAM circuits. When VSTBY = L, there is no need to apply a power supply voltage. The voltage that is input from the power supply control pin (V_{CC1}) is used to generate the logic's power supply voltage within the chip. Also, no power is supplied to the V_{DD2} pin, but it should be connected to the SF_VCCR pin and a 4.7 μF capacitor should be connected between it and the GND pin. For details, refer to **Figure 3–1**.
SF_VCCR	Display RAM circuit power supply generation amplifier output	110 to 115	Output	In the case of 3 power-supply supply system (VSTBY = L), connect a capacitor between grounds. For details, refer to **Figure 3–1**. In the case of 4 power-supply supply system (VSTBY = H), leave it open.
V_{DDIO}	CPU/RGB interface power supply	84 to 89	–	This is the CPU/RGB interface's power supply pin. Be sure to input a power supply that has the same potential as the IC connected to the CPU/RGB interface.
V_{CC1}	Interface and power supply pin for power supply IC control	90 to 95	–	This is the power supply pin for the power IC control circuit. Be sure to input a power supply that has the same potential as the connected IC.
V_S	Driver and gate control for power supply	154 to 159	–	Power supply pin for driver circuit.
V_{SS11}	Ground pin for logic	130 to 135	–	Ground pin for logic circuit
V_{SS1}	Ground pin for interface and power supply IC	124 to 129	–	Ground pin for power supply IC of control circuit and logic interface circuit.
V_{SS}	Ground pin for driver and gate control	136 to 141	–	Ground pin for driver circuit power supply IC control circuit
VSTBY	Logic power supply generation control	183	Input	This pin is used to select whether or not to supply voltage to the logic's power supply. VSTBY = L: Supply voltage to V_{DD1}, V_{DD2}, SF_VCCL, and SF_VCCR is not required. VSTBY = H: Supply voltage to V_{DD1} and V_{DD2} is required.

(2/2)

Symbol	Pin Name	Pad No.	I/O	Function
$V_{DD1(MODE)}$	Mode setting pull-up power supply	227	–	Pull-up power supply pin for mode setting
$V_{DDIO(MODE)}$	Mode setting pull-up power supply	29, 55, 60, 84 to 88	–	Pull-up power supply pin for mode setting
$V_{CC1\ (MODE)}$	Mode setting pull-up power supply	169, 173, 177, 181	–	Pull-up power supply pin for mode setting
$V_{SS1\ (MODE)}$	Mode setting pull-down power supply	50, 58, 65, 166, 198, 226	–	Pull-down power supply pin for mode setting

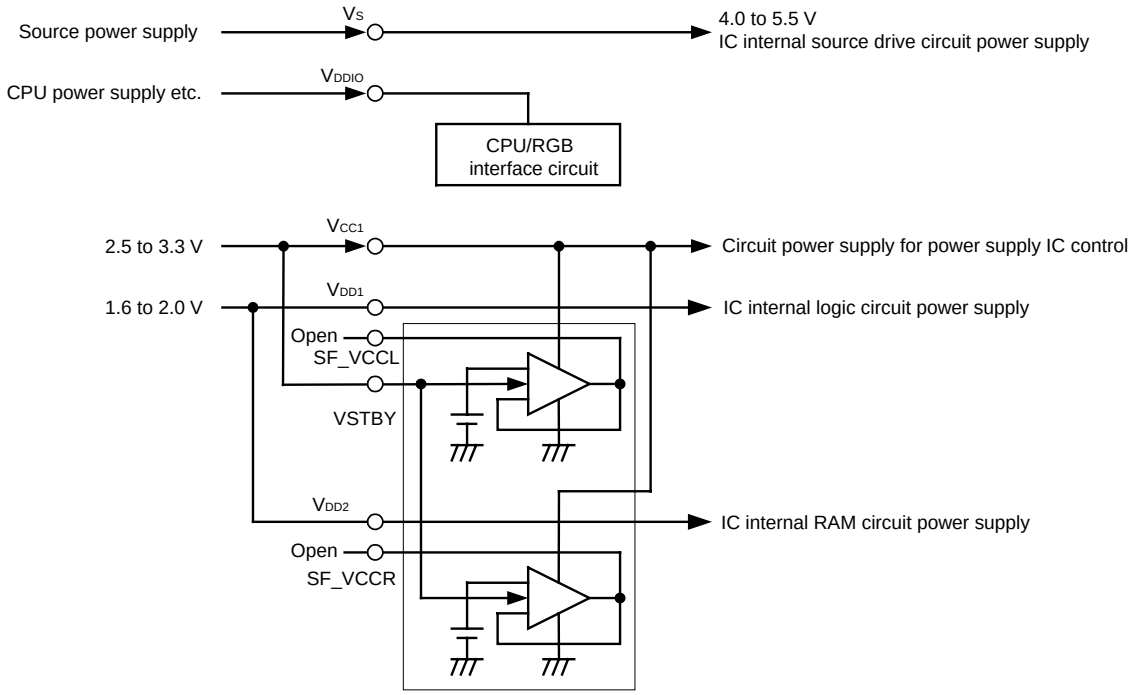
Figure 3–1. Supplies for Power Supply

[At the time of IC regulator circuit use for logic circuits: V_{CC1} = 2.5 to 3.3 V single power supply input]



Regulator ON

[At the time of IC regulator circuit unused for logic circuits: V_{DD1}, V_{DD2} = 1.6 to 2.0 V, V_{CC1} = 2.5 to 3.3 V]



Regulator OFF

3.2 Logic System Pins

(1/2)

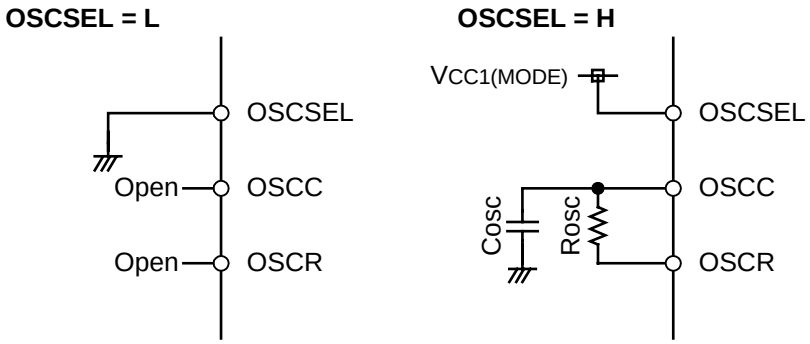
<table>
<tr><th>Symbol</th><th>Pin Name</th><th>Pad No.</th><th>I/O</th><th>Function</th></tr>
<tr><td>BWS0</td><td>CPU interface bus width selection</td><td>178</td><td>Input</td><td rowspan="2">This pin selects the bus width of the i80/M68 interface (it is invalid for the RGB interface).
<table><tr><th>BWS0</th><th>BWS1</th><th>i80/M68, Serial Interface Bus Width</th></tr><tr><td>L</td><td>L</td><td>18 bits</td></tr><tr><td>L</td><td>H</td><td>16 bits</td></tr><tr><td>H</td><td>L</td><td>Prohibited</td></tr><tr><td>H</td><td>H</td><td>8 bits parallel or serial interface</td></tr></table></td></tr>
<tr><td>BWS1</td><td>CPU interface bus width selection</td><td>179</td><td>Input</td></tr>
<tr><td>BWS2</td><td>RGB interface bus width selection</td><td>180</td><td>Input</td><td rowspan="2">This pin selects the bus width of the RGB interface (it is invalid for the CPU interface).
<table><tr><th>BWS2</th><th>BWS3</th><th>RGB Interface Bus Width</th></tr><tr><td>L</td><td>L</td><td>18 bits</td></tr><tr><td>L</td><td>H</td><td>16 bits</td></tr><tr><td>H</td><td>L</td><td>6 bits</td></tr><tr><td>H</td><td>H</td><td>Prohibited</td></tr></table></td></tr>
<tr><td>BWS3</td><td>RGB interface bus width selection</td><td>182</td><td>Input</td></tr>
<tr><td>PSX</td><td>CPU interface mode selection</td><td>175</td><td>Input</td><td>This pin selects the mode of the CPU interface.
L: i80/M68 interface only, H: Serial interface only</td></tr>
<tr><td>/CS</td><td>Chip select</td><td>54</td><td>Input</td><td>This pin is used for chip select signals. When /CS = L, the chip is active and can perform data I/O operations including command and data I/O.</td></tr>
<tr><td>/RESET</td><td>Reset</td><td>31</td><td>Input</td><td>When /RESET is L, an internal reset is initialized. The reset operation is executed at the /RESET signal level. Be sure to perform reset via this pin at power application.</td></tr>
<tr><td>/RD
(E)</td><td>Read
(Enable)</td><td>51</td><td>Input</td><td>When i80 series parallel data transfer (/RD) has been selected, the signal at this pin is used to enable read operations. Data is output to the data bus only when this pin is low.
When M68 series parallel data transfer (E) has been selected, the signal at this pin is used to enable read/write operations.</td></tr>
<tr><td>/WR
(R,/W)</td><td>Write
(Read/write)</td><td>52</td><td>Input</td><td>When i80 series parallel data transfer (/WR) has been selected, the signal at this pin is used to enable write operations.
When M68 series parallel data transfer (R,/W) has been selected, this pin is used to determine the direction of data transfer.
L: Write, H: Read</td></tr>
<tr><td>C86</td><td>Select interface</td><td>178</td><td>Input</td><td>This pin is used to switch between interface modes (i80 series CPU or M68 series CPU).
L: Selects i80 series CPU mode, H: Selects M68 series CPU mode</td></tr>
<tr><td>D_0 to D_{17}</td><td>Data bus</td><td>49 to 32</td><td>I/O</td><td>These pins comprise 18-bit bi-directional data.
When the chip is not selected, D_0 to D_{17} are in Hi-Z (high impedance) mode.</td></tr>
<tr><td>SI</td><td>Serial input</td><td>56</td><td>Input</td><td>This pin is data input of serial interface.</td></tr>
<tr><td>SCL</td><td>Serial clock</td><td>57</td><td>Input</td><td>This pin is clock input of serial interface.</td></tr>
<tr><td>RS</td><td>Data/command selection</td><td>53</td><td>Input</td><td>When parallel data transfer has been selected, this pin is usually connected to the least significant bit of the standard CPU address bus and is used to distinguish between data from display data and commands.
RS = L: Indicates that data from D_0 to D_{17} is commands.
RS = H: Indicates that data from D_0 to D_{17} is display data.</td></tr>
<tr><td>HSYNC</td><td>Horizontal sync signal</td><td>62</td><td>Input</td><td>This is the horizontal sync signal of the RGB interface.</td></tr>
<tr><td>VSYNC</td><td>Vertical sync signal</td><td>61</td><td>Input</td><td>This is the vertical sync signal of the RGB interface.</td></tr>
<tr><td>DOTCLK</td><td>Dot clock</td><td>63</td><td>Input</td><td>This is the dot clock signal of the RGB interface.</td></tr>
</table>

(2/2)

Symbol	Pin Name	Pad No.	I/O	Function
HSEG	HSYNC polarity selection	171	Input	This selects polarity of the horizontal sync signal of the RGB interface. HSEG = L: Low active HSEG = H: High active
VSEG	VSYNC polarity selection	172	Input	This selects polarity of the vertical sync signal of the RGB interface. VSEG = L: Low active VSEG = H: High active
DCKEG	DOTCLK polarity selection	174	Input	This selects polarity of the dot clock signal of the RGB interface. DCKEG = L: High active (this pin is latched up at rising edge) DCKEG = H: High level (this pin is latched up at falling edge)
RGB_{00} to RGB_{05}, RGB_{10} to RGB_{15}, RGB_{20} to RGB_{25}	Data bus	66 to 71, 72 to 77, 78 to 83	Input	These pins are RGB interface data signal.
CSTB	GSTB logic signal	30	Output	This pin outputs STB signal for gate driver leveled by interface power supply voltage (V_{DDIO}). This output signal is reverse signal of GSTB.
VLD	RAM write enable signal	59	Input	This is the data valid signal of CPU I/F display RAM write and RGB I/F capture write. VLD = L: Write data is valid (write to RAM) VLD = H: Write data is invalid (no write to RAM)
OSCSEL	Oscillator circuit selection	168	Input	The oscillation circuit of the inside reference clock for liquid crystal drive of IC is selected. OSCSEL = L: Internal oscillation circuit selection OSCSEL = H: External oscillation circuit selection
OSCR	Resistance Connection for Oscillator	161	Output	Resistance of T.B.D. Ω is connected between OSCC pins at the time (OSCSEL = H) of external oscillation circuit selection. Leave it open at the time (OSCSEL = L) of internal oscillation circuit selection.
OSCC	Capacitor connection for oscillator	160	Input	At the time (OSCSEL = H) of external oscillation circuit selection, resistance of T.B.D. Ω is connected between OSCR pins, and the capacitor of T.B.D. μF is connected between grounds. Leave it open at the time (OSCSEL = L) of internal oscillation circuit selection.
CMDS	CMDS	170	Input	Connect to V_{SS1}.
EPEN	External E^2PROM valid pin	167	Input	This selects whether external E^2PROM is valid or invalid. L: External E^2PROM is valid. H: External E^2PROM is invalid.
EDI	Data input for E^2PROM interfaces	162	Input	This is the data input for E^2PROM interfaces. This is used for data read out of E^2PROM or the check of BUSY/REDY. This connects with DOUT (data out pin) of E^2PROM.
ECS	CS for E^2PROM interfaces	163	Output	This is the chip selection for E^2PROM interfaces. By outputting ECS = High, data is transmitted, after changing E^2PROM into an active state.
ESK	CLK for E^2PROM interfaces	164	Output	This is the CLK for E^2PROM interfaces. The data is outputted from EDO to E^2PROM in the falling of ESK.. It connects with CLK (shift clock pin) of E^2PROM.
EDO	The data output for E^2PROM interfaces	165	Output	This is the data output for E^2PROM interfaces. The data output is carried out at ROM. This connects with DIN (data in pin) of ROM.

Remark T.B.D. (To be determined.)

[Example of the oscillator circuit connection]



3.3 Gate Driver Control Pins

Symbol	Pin Name	Pad No.	I/O	Function
OEVE, GOE1	OE1 output for gate control	15	Output	This pin is output enable pin for gate control. Signal is outputted to the timing set as R79 and R80. For details, refer to **5.4 Display Timing Generator.**
/OEVE, /GOE1	OE1 output for gate control	16	Output	This pin outputs inverted OEV, GOE1 signal.
OEV, GOE2	OE2 output for gate control	13	Output	This pin is output enable pin for gate control. For details, refer to **5.4 Display Timing Generator.**
/OEV, /GOE2	OE2 output for gate control	14	Output	This pin outputs inverted OEV, GOE2 signal.
STV, GSTB	STB output for gate control	9	Output	This pin is output strove pin for gate control. Timing signal for output, refer to **5.4 Display Timing Generator.**
/STV, /GSTB	STB output for gate control	10	Output	This pin outputs inverted STV, GSTB signal.
CKV, GCLK	CLK output for gate control	11	Output	This pin is the CLK output for the gate control. Timing signal for output, refer to **5.4 Display Timing Generator.**
/CKV, /GCLK	CLK output for gate control	12	Output	This pin outputs inverted CKV, GCLK signal.
GUD	Control signal for gate scan direction	17	Output	This pin is gate scan direction control signal. Timing signal for output, refer to **5.4 Display Timing Generator**.
/GUD	Control signal for gate scan direction	18	Output	This pin outputs inverted GUD signal.
XDON	Panel control output	17	Output	This pin is control output pin for panel. Signal is outputted by setup of RXDON [R77 (HITACHI mode: R017H)].
/XDON	Panel control output	18	Output	This pin outputs inverted XDON signal.
EXT1	Panel control signal	25	Output	This pin is the signal for panel control.
/EXT1	Panel control signal	26	Output	This pin outputs inverted EXT1 signal.
EXT2	Panel control signal	27	Output	This pin is the signal for panel control.
/EXT2	Panel control signal	28	Output	This pin outputs inverted EXT2 signal.

3.4 RGB Multi-plectra Switch Control Pins

Symbol	Pin Name	Pad No.	I/O	Function
ASW1, RSW	Multi-plectra control signal	7	Output	This pin is panel of multi-plectra control signal. Signal is outputted to the timing set as R83 and R84. For details, refer to **5.4 Display timing generator**.
/ASW1, /RSW	Multi-plectra control signal	8	Output	This pin outputs inverted ASW1, RSW signal.
ASW2, GSW	Multi-plectra control signal	5	Output	This pin is panel of multi-plectra control signal. Signal is outputted to the timing set as R85 and R86. For details, refer to **5.4 Display timing generator**.
/ASW2, /GSW	Multi-plectra control signal	6	Output	This pin outputs inverted ASW2, GSW signal.
ASW3, BSW	Multi-plectra control signal	3	Output	This pin is panel of multi-plectra control signal. Signal is outputted to the timing set as R87 and R88. For details, refer to **5.4 Display timing generator**.
/ASW3, /BSW	Multi-plectra control signal	4	Output	This pin outputs inverted ASW3, BSW signal.

3.5 External IC (μPD161862, etc.) Control Pins

Symbol	Pin Name	Pad No.	I/O	Function
PCS	Chip select signal output	22	Output	This is a chip selection output pin for serial interfaces for power supply IC control. Connect with chip selection input pins, such as the external power supply IC. Set-up of R38 to R42, and R60 to R65 starts an output. For details, refer to **5.1.8 Serial interface for power supply IC control**.
PCL	Serial clock signal output	23	Output	This is a serial clock output pin for serial interfaces for power supply IC control. Connect with serial clock input pins, such as the external power supply IC. Setup of R38 to R42, and R60 to R65 starts an output. For details, refer to **5.1.8 Serial interface for power supply IC control**.
PDA	Serial data output	21	Output	This is a serial data pin for serial interfaces for power supply IC control. Connect with serial data input pins, such as the external power supply IC. Setup of R38 to R42, and R60 to R65 starts an output. For details, refer to **5.1.8 Serial interface for power supply IC control**.
/PRESET	Reset output	2	Output	This is a reset signal output pin for power supplies IC. The reset signal inputted from RESET pin is outputted on the input signal level (V_{CC1}) of the external power supply IC. Connect with reset input pins, such as the external power supply IC.
PCCLK	Power supply IC DC/DC converter clock output	24	Output	The reference clock for the DC/DC converter circuits of a power supply IC is outputted. Oscillation frequency is divided cycle and outputted by the divided cycle ratio set up by DC4 and DC3 (R72). Use this pin, connecting with reference clock inputs for DC/DC converter circuits, such as power supply IC.

3.6 Driver Pins

Symbol	Pin Name	Pad No.	I/O	Function
Y_1 to Y_{240}	Source output	231 to 358, 368 to 479	Output	These pins are source output pins
VCOUT	Common timing output	19	Output	Common timing signal is outputted from V_{CC1} -V_{SS}, V_{P-P}. Usually, it is used such as shifting this timing output signal to the voltage level to need.
FR	Frame signal output	20	Output	This pin outputs frame polarity signal. With VCOUT, the signal of inversion polarity is outputted in V_{CC1} to V_{SS} when RXDON (R77 • D_2) = 0 setup. When RXDON = 1 setup, operation set as DSCGn (R72 • D_5 to D_0) is performed.
CVPH, CVPL, CVNH, CVNL	Basis power supply pin for γ-corrected power supplies	151 to 153, 148 to 150, 145 to 147, 142 to 144	Output	This is operational amplifier output pin for the γ-corrected power supplies. Normally, this pin connects capacitor of T.B.D. μF. When unused the amplifier for γ-correction, leave it open.

3.7 Test or Other Pins

Symbol	Pin Name	Pad No.	I/O	Function
$TOUT_0$ to $TOUT_{19}$, TOSCO1, TOSCO2,	Test output	221 to 202, 196, 197	Output	This is output pin when IC is in test mode. Normally, leave it open.
$TDELAY_0$ to $TDELAY_2$ ENABLE	Test input	184 to 186, 64	Input	This is input pin when IC is in test mode. Normally, connected it to V_{SS1}.
TSTRTST, TSTVIHL, TOSCI1, TOSCI2, TOSCSEI1, TOSCSEI2, TOSCSEO1, TOSCSEO2, TCLK TF1, TF2 TPR TVP	Test input	189, 188, 194, 195, 192, 193, 190, 191, 187, 222, 223, 224, 225	Input	These input pins are to set up test mode of IC. Normally, fixed it to V_{SS}.
DUMMY	Dummy	1, 199 to 201, 228 to 230, 359 to 367, 480 to 496	–	Dummy pin

4. PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The I/O circuit types of each pin and recommended connection of unused pins are described below.

(1/2)

Pin Name	I/O	Power Supply	Recommended Connection of Unused Pins		Note
			Parallel Interface	Serial Interface	
PSX	Input	V_{CC1}	Mode setting pin		O
BWS0 to BWS3	Input	V_{CC1}	Mode setting pin		O
VSTBY	Input	V_{CC1}	Mode setting pin		O
/RESET	Input	V_{DDIO}	Always reset on power application		–
/CS	Input	V_{DDIO}	Connect to V_{DDIO}		–
/RD (E), /WR	Input	V_{DDIO}	Connect to V_{DDIO} (when i80 series interface)	Connect to V_{DDIO} or V_{SS1}	–
C86	Input	V_{CC1}	Mode setting pin	Connect to V_{CC1} or V_{SS1}	O
D_0 to D_{17}	I/O	V_{DDIO}	–	Connect to V_{SS1}	–
SI, SCL	Input	V_{DDIO}	Connect to V_{DDIO}	–	–
HSYNC	Input	V_{DDIO}	Connect to V_{DDIO} or V_{SS1}		–
VSYNC	Input	V_{DDIO}	Connect to V_{DDIO} or V_{SS1}		–
DOTCLK	Input	V_{DDIO}	Connect to V_{DDIO} or V_{SS1}		O
HSEG	Input	V_{CC1}	Mode setting pin		O
VSEG	Input	V_{CC1}	Mode setting pin		O
DCKEG	Input	V_{CC1}	Mode setting pin		–
RGB_{00} to RGB_{05}, RGB_{10} to RGB_{15}, RGB_{20} to RGB_{25}	Input	V_{DDIO}	Connect to V_{DDIO} or V_{SS1}		O
RS	Input	V_{DDIO}	Register setting pin		–
VLD	Input	V_{DDIO}	Connect to V_{ss1}		–
CSTB	Output	V_{DDIO}	Leave open		–
OSCSEL	Input	V_{CC1}	Mode setting pin		O
OSCR	–	V_{DD1}	Leave open		
OSCC	–	V_{DD1}	Leave open or connect to V_{ss1}		
OEV, GOE_1	Output	V_{CC1}	Leave open		–
/OEV, $/GOE_1$	Output	V_{CC1}	Leave open		–
OEVE, GOE_2	Output	V_{CC1}	Leave open		–
/OEVE, $/GOE_2$	Output	V_{CC1}	Leave open		–
STV, GSTB	Output	V_{CC1}	Leave open		–
EPEN	Input	V_{CC1}	Mode setting pin		O
EDI	Input	V_{CC1}	Connect to V_{CC1} or V_{SS1}		–
ECS	Output	V_{CC1}	Leave open		–
ESK	Output	V_{CC1}	Leave open		–
EDO	Output	V_{CC1}	Leave open		–
/STV, /GSTB	Output	V_{CC1}	Leave open		–
CKV, GCLK	Output	V_{CC1}	Leave open		–
/CKV, /GCLK	Output	V_{CC1}	Leave open		–

(2/2)

Pin Name	I/O	Power Supply	Recommended Connection of Unused Pins		Note
			Parallel Interface	Serial Interface	
EXT1	Output	V_{CC1}	Leave open		–
/EXT1	Output	V_{CC1}	Leave open		–
EXT2	Output	V_{CC1}	Leave open		–
/EXT2	Output	V_{CC1}	Leave open		–
ASW1, RSW	Output	V_{CC1}	Leave open		–
/ASW1, /RSW	Output	V_{CC1}	Leave open		–
ASW2, GSW	Output	V_{CC1}	Leave open		–
/ASW2, /GSW	Output	V_{CC1}	Leave open		–
ASW3, BSW	Output	V_{CC1}	Leave open		–
/ASW3, /BSW	Output	V_{CC1}	Leave open		–
GUD	Output	V_{CC1}	Leave open		–
/GUD	Output	V_{CC1}	Leave open		–
XDON	Output	V_{CC1}	Leave open		–
/XDON	Output	V_{CC1}	Leave open		–
PCS	Output	V_{CC1}	Connect power supply IC etc. with exterior IC. Leave it open when in unused.		–
PCL	Output	V_{CC1}	Connect power supply IC etc. with exterior IC. Leave it open when in unused.		–
PDA	Output	V_{CC1}	Connect power supply IC etc. with exterior IC. Leave it open when in unused.		–
PCCLK	Output	V_{CC1}	Connect power supply IC etc. with exterior IC. Leave it open when in unused.		–
/PRESET	Output	V_{CC1}	Connect power supply IC etc. with exterior IC. Leave it open when in unused.		–
VCOUT	Output	V_{CC1}	Leave open		–
FR	Output	V_{CC1}	Leave open		–
CVNL, CVNH, CVPL, CVPH	Output	V_S	Always connect to the capacitor of T.B.D. μF. However, this pin can be left open if not using any amplifier for γ-correction.		–
TVP	Input	V_{CC1}	Connect to V_{SS1}		–
TPR	Input	V_{CC1}	Connect to V_{SS1}		–
TF1, TF2	Input	V_{CC1}	Connect to V_{SS1}		–
$TOUT_0$ to $TOUT_{19}$	Output	V_{CC1}	Leave open		–
TOSCO1, TOSCO2	Output	V_{CC1}	Leave open		–
TSTRTST	Input	V_{CC1}	Connect to V_{SS1}		–
TSTVIHL	Input	V_{CC1}	Connect to V_{SS1}		–
TOSCI1, TOSCI2	Input	V_{CC1}	Connect to V_{SS1}		–
TOSCSEO1, TOSCSEO2	Input	V_{CC1}	Connect to V_{SS1}		–
TOSCSEI1, TOSCSEI2	Input	V_{CC1}	Connect to V_{SS1}		–
$TDELAY_0$ to $TDELAY_2$	Input	V_{CC1}	Connect to V_{SS1}		–
TCLK	Input	V_{CC1}	Connect to V_{SS1}		–

Note O: Connect to V_{CC1} or V_{SS1}, depending on the mode selected.

5. DESCRIPTION OF FUNCTIONS

5.1 CPU Interface

5.1.1 Selection of interface type

The μPD161802 is able to transfer data via an RGB interface (18-/16-/6-bit) or via either of two CPU interfaces: the i80/M68 parallel interface (18-/16-/8-bit) or a serial interface (8-bit). The following modes can be selected for these CPU interfaces, as set via the PSX, BSW0, and BSW1 pins. Also, the RGB interface becomes valid when NWRGB (R25:D_2) = 1, at which time the bus width is selected according to the BWS2 and BSW3 pin settings.

Although the i80/M68 parallel interface and the serial interface allow writing to both the display data RAM and the registers, the RGB interface can be used only to overwrite the display data RAM.

Table 5–1. CPU Interface Bus Width Selection

PSX	BWS0	BWS1	Mode	/CS	RS	/RD (E)	/WR (R, /W)	C86	D_{17}, D_{16}	D_{15} to D_8	D_7 to D_0	SI, SCL
L	L	L	18-bit parallel	/CS	RS	/RD (E)	/WR (R, /W)	C86	D_{17}, D_{16}	D_{15} to D_8	D_7 to D_0	Hi-Z Note
	L	H	16-bit parallel	/CS	RS	/RD (E)	/WR (R, /W)	C86	Hi-Z Note	D_{15} to D_8	D_7 to D_0	Hi-Z Note
	H	H	8-bit parallel	/CS	RS	/RD (E)	/WR (R, /W)	C86	Hi-Z Note	Hi-Z Note	D_7 to D_0	Hi-Z Note
H	H	H	8-bit serial	/CS	RS	X	Hi-Z Note	X	Hi-Z Note	Hi-Z Note	Hi-Z Note	SI, SCL
Other than above			Setting prohibited									

Remark X: Don't care

Note Hi-Z: High impedance

Table 5–2. RGB Interface Bus Width Selection

BWS2	BWS3	Mode	RGB_{01} to RGB_{05}	RGB_{00}	RGB_{10} to RGB_{15}	RGB_{21} to RGB_{25}	RGB_{20}
L	L	18-bit parallel	RGB_{01} to RGB_{05}	RGB_{00}	RGB_{10} to RGB_{15}	RGB_{21} to RGB_{25}	RGB_{20}
L	H	16-bit parallel	RGB_{01} to RGB_{05}	Hi-Z Note	RGB_{10} to RGB_{15}	RGB_{21} to RGB_{25}	Hi-Z Note
H	L	6-bit parallel	Hi-Z Note	Hi-Z Note	Hi-Z Note	RGB_{21} to RGB_{25}	RGB_{20}
H	H	Setting prohibited					

Note Hi-Z: High impedance

5.1.2 Selection of data transfer mode

When the 18-bit parallel interface is selected, the length of 1 pixel is fixed to 18 bits. With the 16-bit or 8-bit parallel interface, however, the length of 1 pixel can be selected from 18 or 16 bits (1 pixel = 16 bits when DTX1 = 0, and 1 pixel = 18 bits when DTX1 = 1).

If the 16-bit or 8-bit parallel interface is selected, therefore, several modes of transferring data to the display RAM are selectable. The mode is selected by using the DTX1 register.

[16-bit parallel interface]

<When 1 pixel = 18 bits (DTX1 = 1)>

<1> 16-bit data transfer + 2-bit data transfer

1 pixel = 18-bit data is divided into 16-bit data and 2-bit data for transfer, as shown in Figure 5–3.

<When 1 pixel = 16 bits (DTX1 = 0)>

<2> 16-bit data transfer

Display data of 1 pixel is transferred by one transmission as shown in Figure 5–4. Because 1 pixel is 16 bits long, the number of display colors is limited to 65,536.

[8-bit parallel interface]

< When 1 pixel = 18 bits (DTX1 = 1)>

<1> Transferring 6-bit data three times

1 pixel = 18-bit data is divided into three 6-bit data for transfer, as shown in Figure 5–6.

<When 1 pixel = 16 bits (DTX1 = 0)>

<2> Transferring 8-bit twice

1 pixel is divided into two 8-bit data for transfer, as shown in Figure 5–7. Because 1 pixel is 16 bits long, the number of display colors is limited to 65,536.

1 pixel of the μPD161802 display RAM consists of 18 bits. If the 16-bit parallel interface is used to transfer 16 bits as 1 pixel (DTX1 = 0), therefore, the data transferred by the CPU (16 bits) runs short by 2 bits, and these 2 bits must be made up for.

For how to do this, refer to **Figures 5–4**, **5–5** and **5–7**.

Table 5–3. Interfaces and Data Transfer Modes

PSX	BWS0	BWS1	BWS2	BWS3	Interface Mode		DTX1	Number of Data of 1 Pixel	Mode of Transferring 1-Pixel Data
L	L	L	L/H Note1	L/H Note1	18-bit parallel		X	18-bit	18-bit transfer
		H			16-bit parallel		1		16-bit + 2-bit transfer
							0	16-bit	16-bit transfer
	H	H			8-bit parallel		1	18-bit	Transferring 6 bits three times
							0	16-bit	Transferring 8 bits twice
H	X	X			8-bit serial		X	16-bit	Transferring 8 bits twice
L/H Note2	H	H	L	L	RGB	18-bit	0/1 Note2	18-bit	18-bit transfer
			L	H		16-bit		16-bit	16-bit transfer
			H	L		6-bit		18-bit	Transferring 6 bits three times

Remark X: Don't care (H or L)

Notes 1. The RGB interface that is shared with the i80/M68 parallel interface or serial interface is selected by inputting low or high level to this pin.

2. The i80/M68 parallel interface or serial interface that is shared with the RGB interface is selected by inputting low or high level to this pin.

Figure 5–1. Relationship between Bus Data and Display RAM Data (18-bit parallel interface)

Data bus side

18-bit data																	
D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					
1 pixel																	

Display RAM side

Figure 5–2. Relationship between Bus Data and Display RAM Data (18-bit RGB interface)

Data bus side

18-bit data																	
RGB_{25}	RGB_{24}	RGB_{23}	RGB_{22}	RGB_{21}	RGB_{20}	RGB_{15}	RGB_{14}	RGB_{13}	RGB_{12}	RGB_{11}	RGB_{10}	RGB_{05}	RGB_{04}	RGB_{03}	RGB_{02}	RGB_{01}	RGB_{00}
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					
1 pixel																	

Display RAM side

Figure 5–3. Relationship between Bus Data and Display RAM Data (1-pixel/18-bit mode [DTX1 = 1], 16-bit parallel interface)

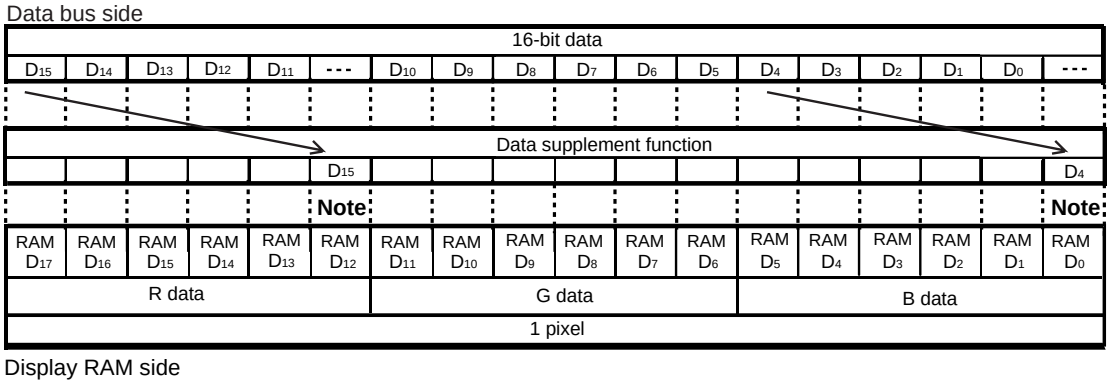
Data bus side

16-bit data																2-bit data	
D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_1	D_0
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					
1 pixel																	

Display RAM side

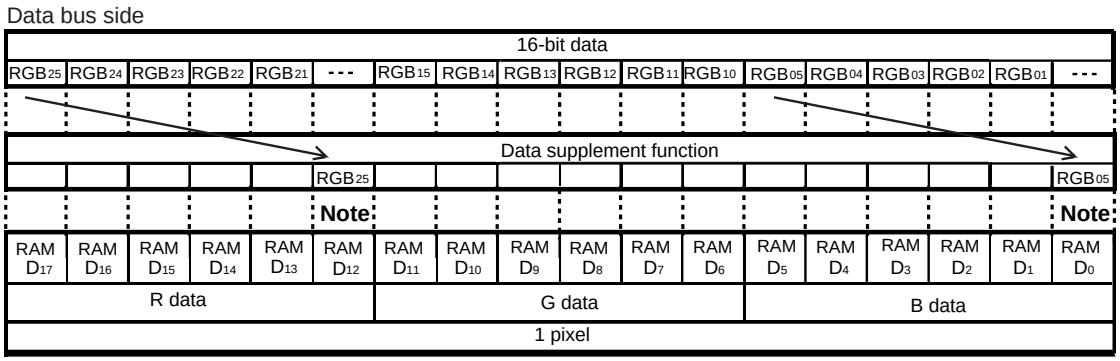
Caution Data D_2 to D_{15} of the second word are treated as invalid data when the 16-bit parallel interface is used.

Figure 5–4. Relationship between Bus Data and Display RAM Data
(1-pixel/16-bit mode [DTX1 = 0], 16-bit parallel interface)



Note When In used 16-bit parallel interface, display RAM data D_{12} and D_0 are supplemented by D_{15} and D_4 of bus data respectively, and written to the display RAM as 18-bit data.

Figure 5–5. Relationship between Bus Data and Display RAM Data (16-bit RGB interface)



Note When In used 16-bit parallel interface, display RAM data D_{12} and D_0 are supplemented by RGB_{25} and RGB_{05} of bus data respectively, and written to the display RAM as 18-bit data.

Figure 5–6. Relationship between Bus Data and Display RAM Data
(1-pixel/18-bit mode [DTX1 = 1], 8-bit parallel interface)

Data bus side

6-bit data						6-bit data						6-bit data					
D_5	D_4	D_3	D_2	D_1	D_0	D_5	D_4	D_3	D_2	D_1	D_0	D_5	D_4	D_3	D_2	D_1	D_0
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					
1 pixel																	

Display RAM side

Caution Display data D_6 and D_7 of the 8-bit parallel interface are treated as invalid data.

Figure 5–7. Relationship between Bus Data and Display RAM Data
(1-pixel/16-bit mode [DTX1 = 0], 8-bit parallel interface, 8-bit serial interface)

Data bus side

8-bit data									8-bit data								
D_7	D_6	D_5	D_4	D_3	---	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	---
Data supplement function																	
					D_7												D_4
					Note												**Note**
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					
1 pixel																	

Display RAM side

Note When In used 8-bit parallel interface mode, display RAM data D_0 and D_{12} are supplemented by bit D_7 of the first byte of the bus data and bit D_4 of the second byte of the bus data, and written to the display RAM as 18-bit data.

Figure 5–8. Relationship between Bus Data and Display RAM Data (6-bit RGB interface)

Data bus side

6-bit data						6-bit data						6-bit data					
RGB_{25}	RGB_{24}	RGB_{23}	RGB_{22}	RGB_{21}	RGB_{20}	RGB_{25}	RGB_{24}	RGB_{23}	RGB_{22}	RGB_{21}	RGB_{20}	RGB_{25}	RGB_{24}	RGB_{23}	RGB_{22}	RGB_{21}	RGB_{20}
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					
1 pixel																	

Display RAM side

Figure 5–9. 16-bit Parallel Interface Data Transfer (1-pixel/18-bit mode [DTX1 = 1])

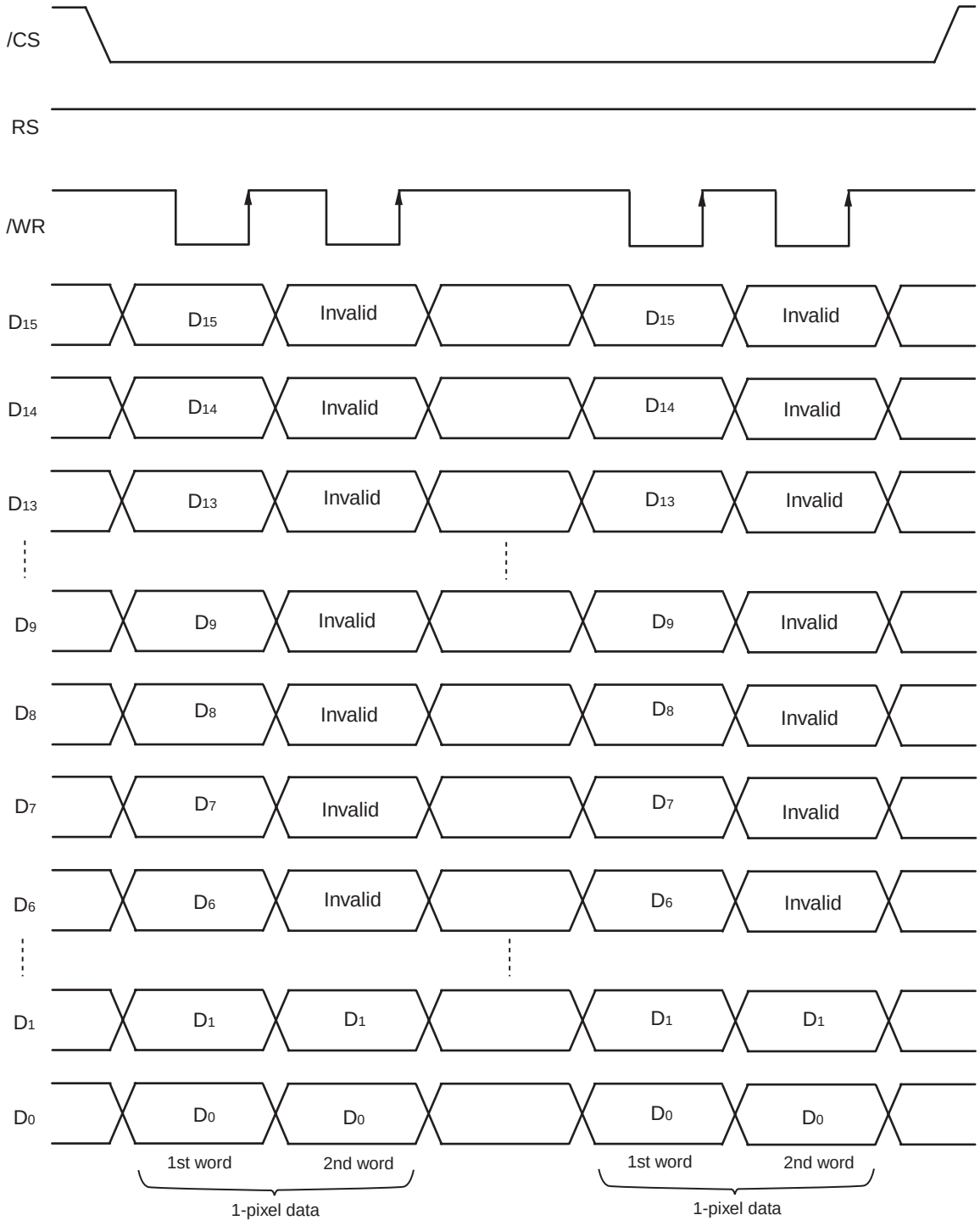


Figure 5–10. 8-bit Parallel Interface Data Transfer (1-pixel/16-bit mode [DTX1 = 0])

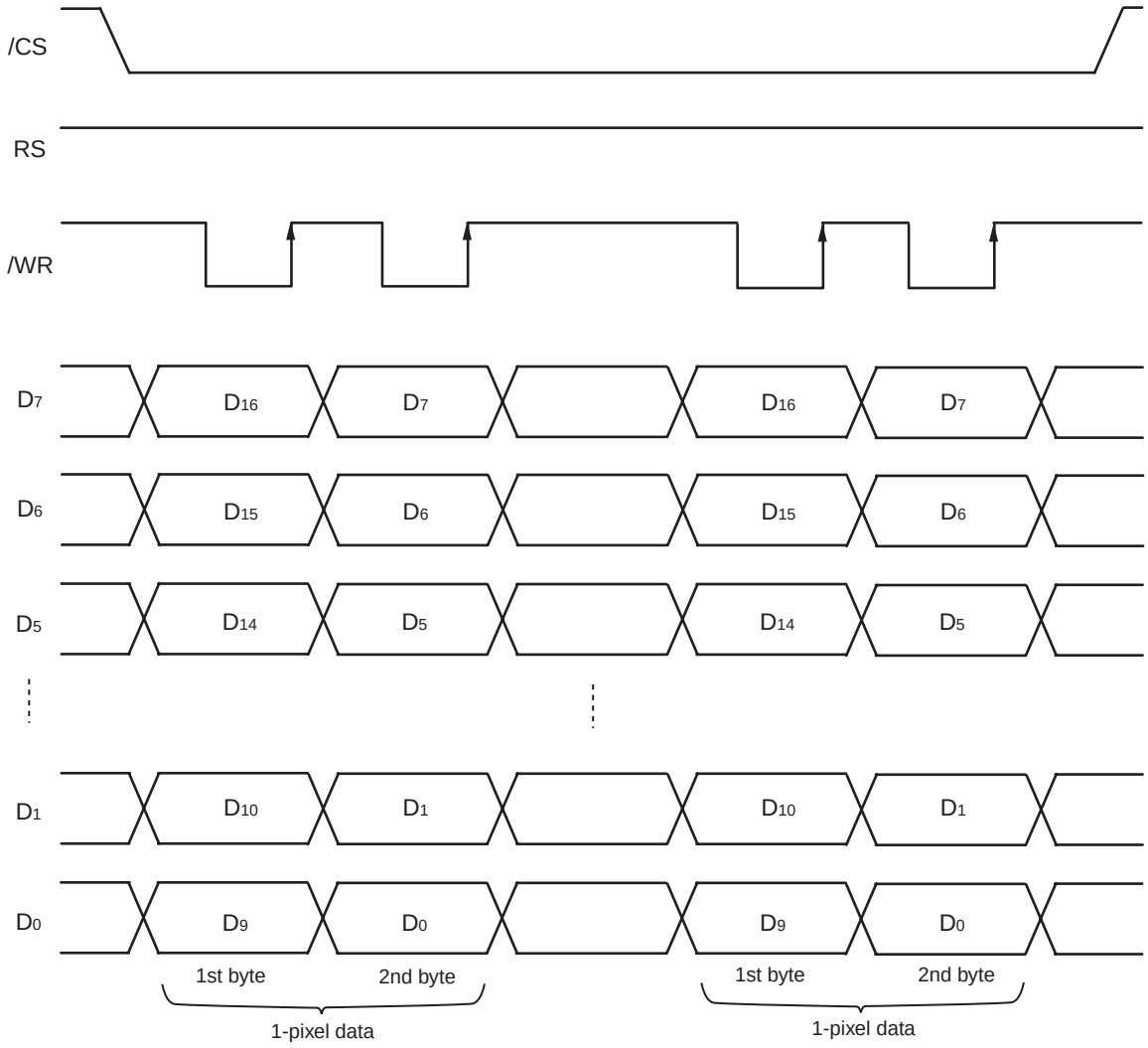
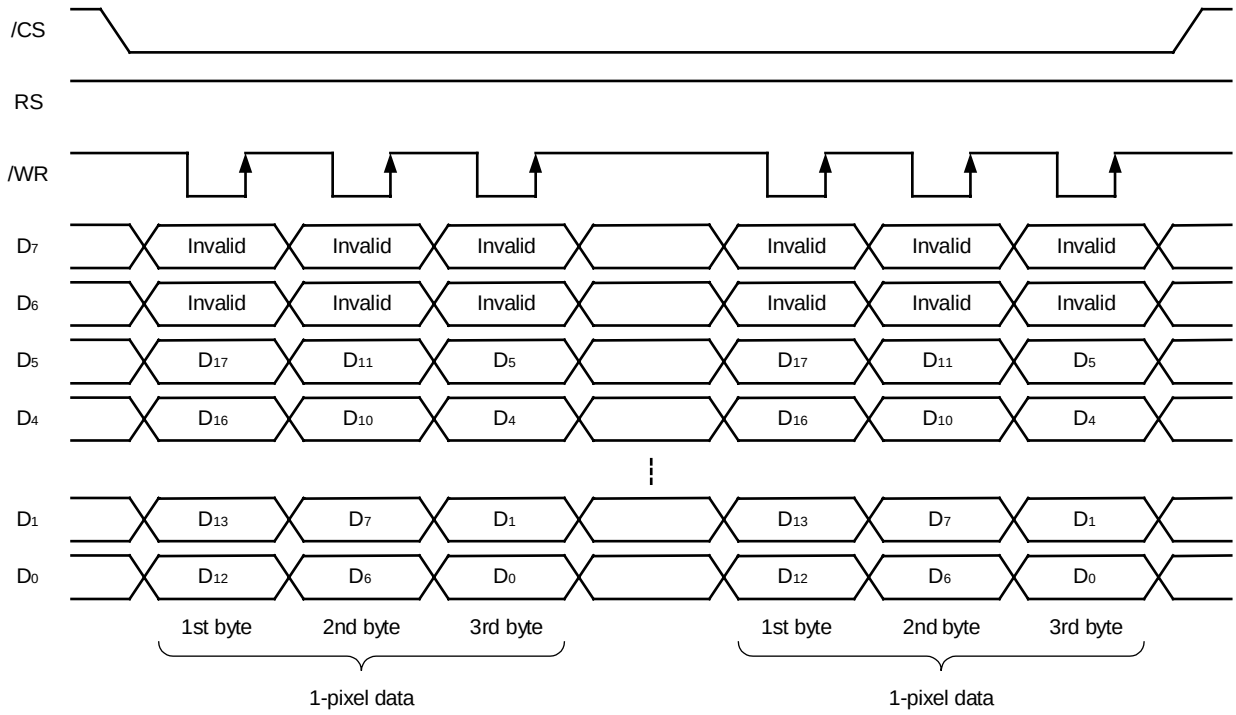


Figure 5–11. 8-bit Parallel Interface Data Transfer (1-pixel/18-bit mode [DTX1 = 1])



5.1.3 RGB interface

The μPD161802 can be directly connected to the RGB interface when bit D_2 of the RGB interface control register (R25 of NWRGB (D_2 bit)) is set to 1.

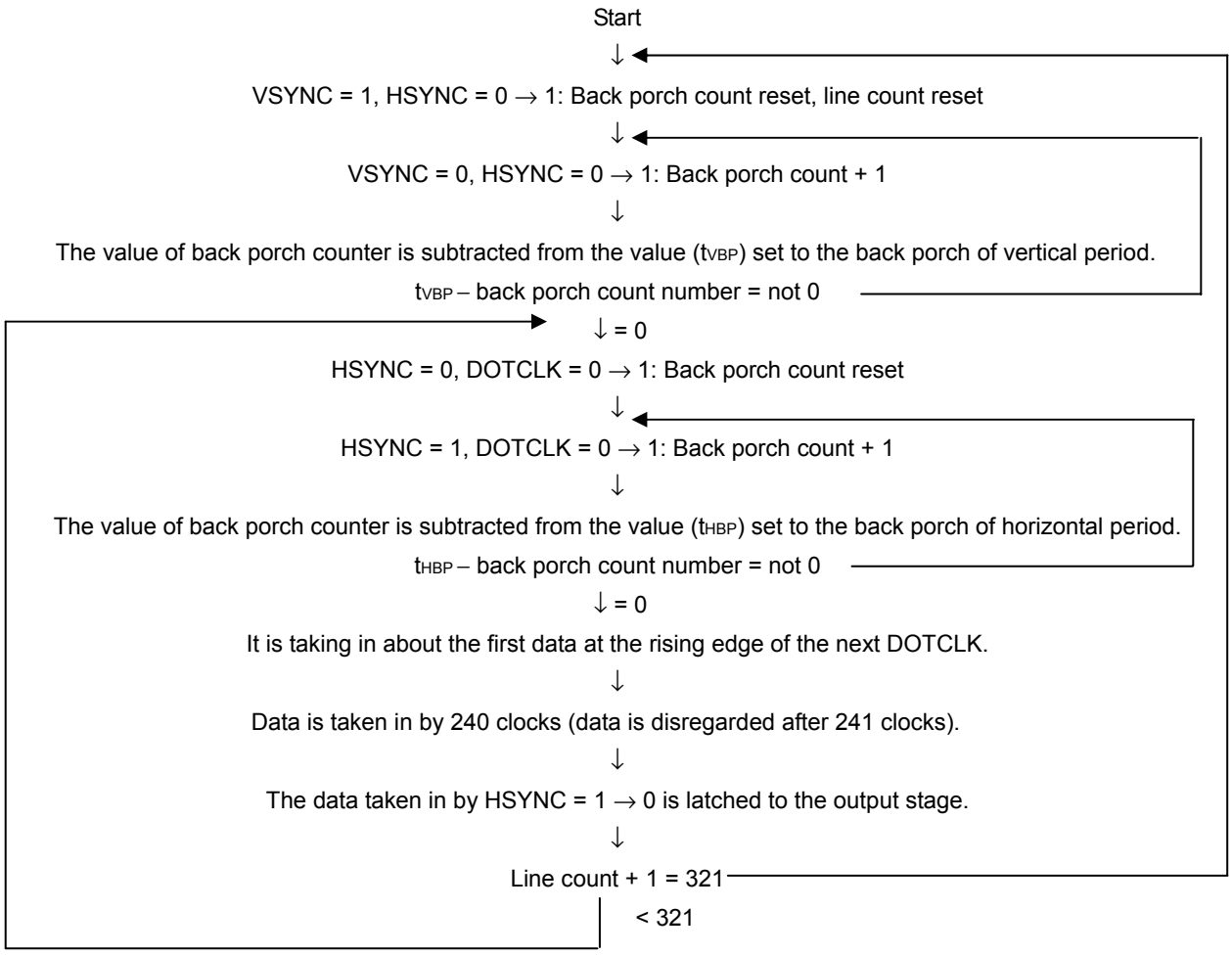
The HSYNC and VSYNC signals establish synchronization in the horizontal and vertical direction, respectively, and data input to the data bus (RGB_{00} to RBG_{05}, RGB_{10} to RGB_{15}, and RGB_{20} to RGB_{25}) is latched in synchronization with DOTCLK. For the electrical specifications, refer to **9. ELECTRICAL SPECIFICATIONS**.

When the RGB interface is selected, the display output timing can be selected from <HSYNC/VSYNC/DOTCLK> or <internal oscillation clock>. It can also be selected whether the data input from the RGB interface is to be written to the display RAM or not.

The mode in which the data input from the RGB interface is not written to the display data RAM and is used for display output is called the through mode (the display output timing is generated by HSYNC/VSYNC/DOTCLK).

The mode in which the data input from the RGB interface is written to the display data RAM for display output is called the capture mode. In the capture mode, the display output timing can be selected from <HSYNC/VSYNC/DOTCLK > or <internal oscillation clock>.

The operation of the μPD161802 when making display output timing into <HSYNC/VSYNC/DOTCLK> is as follows.



Remark VSYNC and HSYNC are both active low and DOTCLK latches data at the rising edge.

In addition, an RGB data invalid mode is also available. In this mode, data input from a video chip via the RGB interface is ignored. Note that only data input from the RGB interface is ignored in this mode and that access from the i80/M68 parallel interface and serial interface is possible.

However, mode selection operates D_0 to D_2 bits of RGB interface control register (R25) on shown as follows.

Table 5–4. RGB Interface Mode Selection

R25			RGB Interface		
D_2	D_1	D_0	Mode Name	Display Output Timing Clock	Writing from RGB Interface to Display Data RAM
1	0	0/1	Through mode	HSYNC/VSYNC/DOTCLK	No
1	1	1	Capture mode	HSYNC/VSYNC/DOTCLK	Yes
1	1	0		Internal oscillation clock	
0	X	1	RGB data invalid mode	HSYNC/VSYNC/DOTCLK	No
		0		Internal oscillation clock	

Remark X: Don't care

When capture mode is selected, DOTCLK is used as a write-in signal to a display data RAM. In addition, X addresses of an address pointer are reset by the HSYNC signal, and an increment is carried out by DOTCLK. Y address is reset by the VSYNC signal and an increment is carried out by the level synchronized signal.

The blanking period can be set by the horizontal back porch register and vertical back porch register. The active levels of HSYNC and VSYNC can be set. In addition, the active level of DOTCLK can also be set. In the through mode, however, the scroll function, partial function, and window access mode cannot be used.

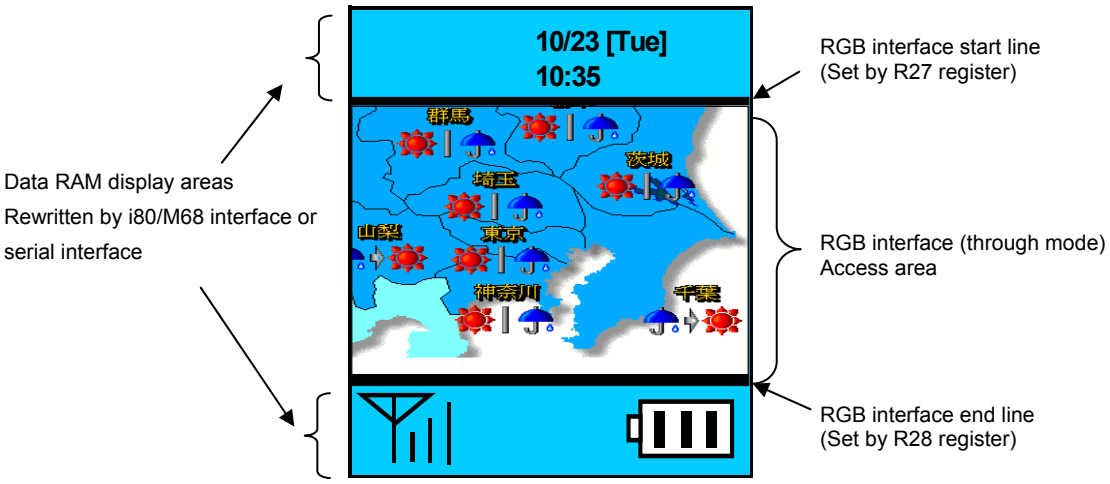
[Example of using RGB interface]

<Through mode>

In the through mode, the area to be displayed by the RGB interface is specified by the RGB interface start line register (R27) and RGB interface end line register (R28). The data written to the display data RAM are displayed in areas other than the RGB interface area.

In the through mode, the display data RAM and registers can be accessed (written or read) by the i80/M68 interface or serial interface when an access is made by the RGB interface.

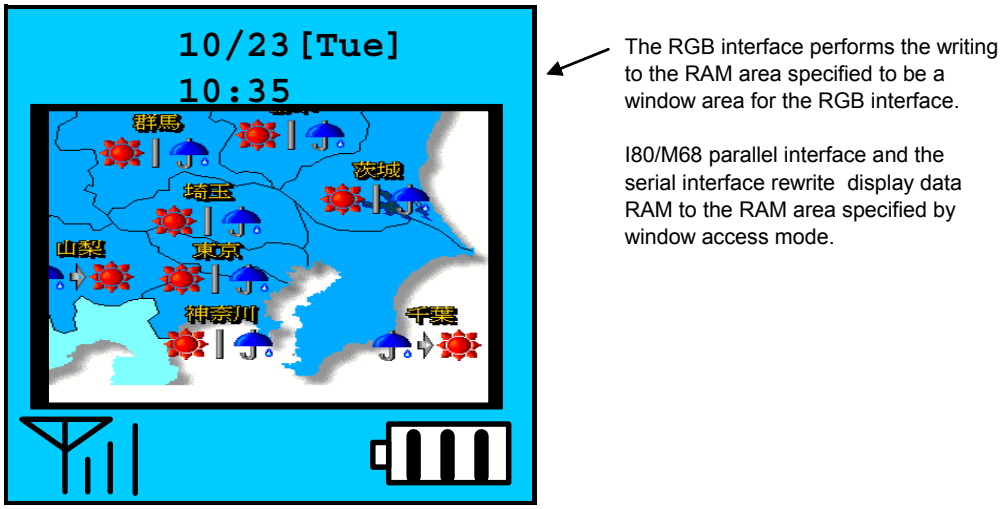
Therefore, an operation such as rewriting the time or antenna by a base band IC while inputting video data from a DSP via the RGB interface can be performed.



<Capture mode>

In the capture mode, the area set in the window access mode is written by the RGB interface (R29 to R32), and a domain which became active with the VLD pin (However, a register setup is confirmed when a register setup and a VLD pin set both up.).

Even in this mode, the i80/M68 parallel interface or serial interface, which are shared with the RGB interface, can be used. Note, however, that data can be written to a register while the RGB interface is accessed, but that the RAM cannot be accessed. Make sure that only one of these accesses is made (shift to the RGB data invalid mode so that video data is not input).

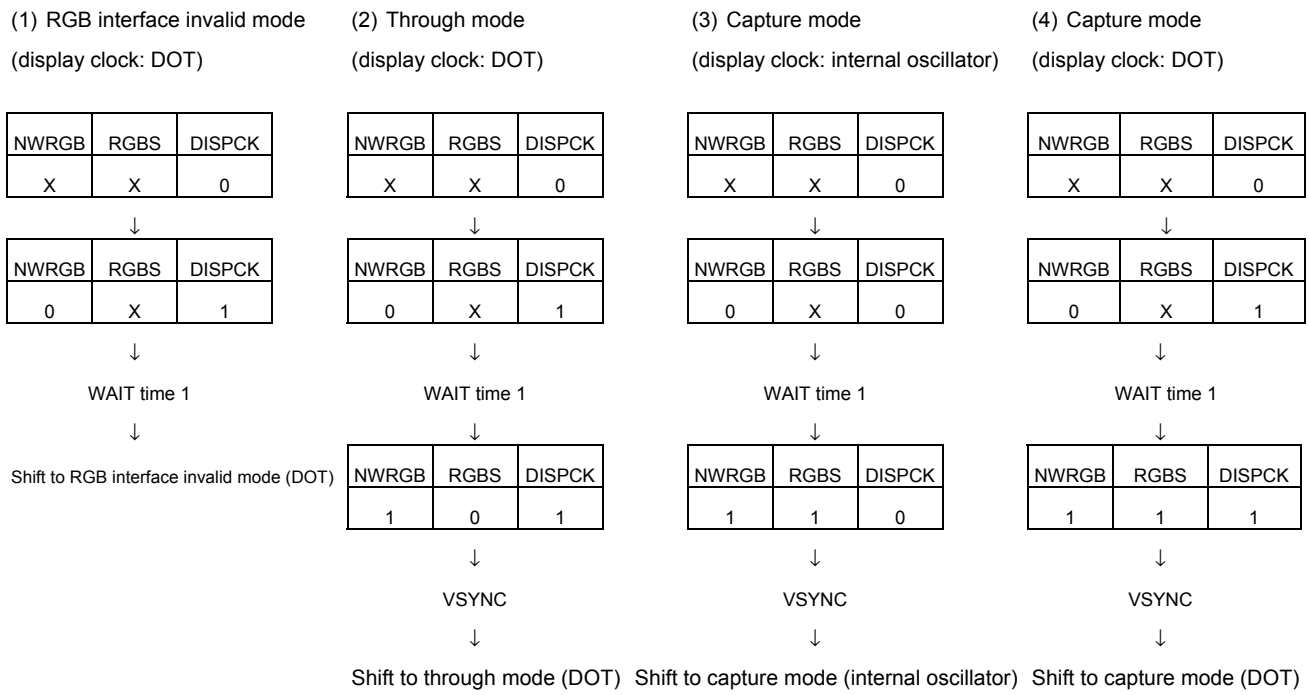


<Notes on using RGB interface>

<1> Be sure to input data from the RGB interface every frame.

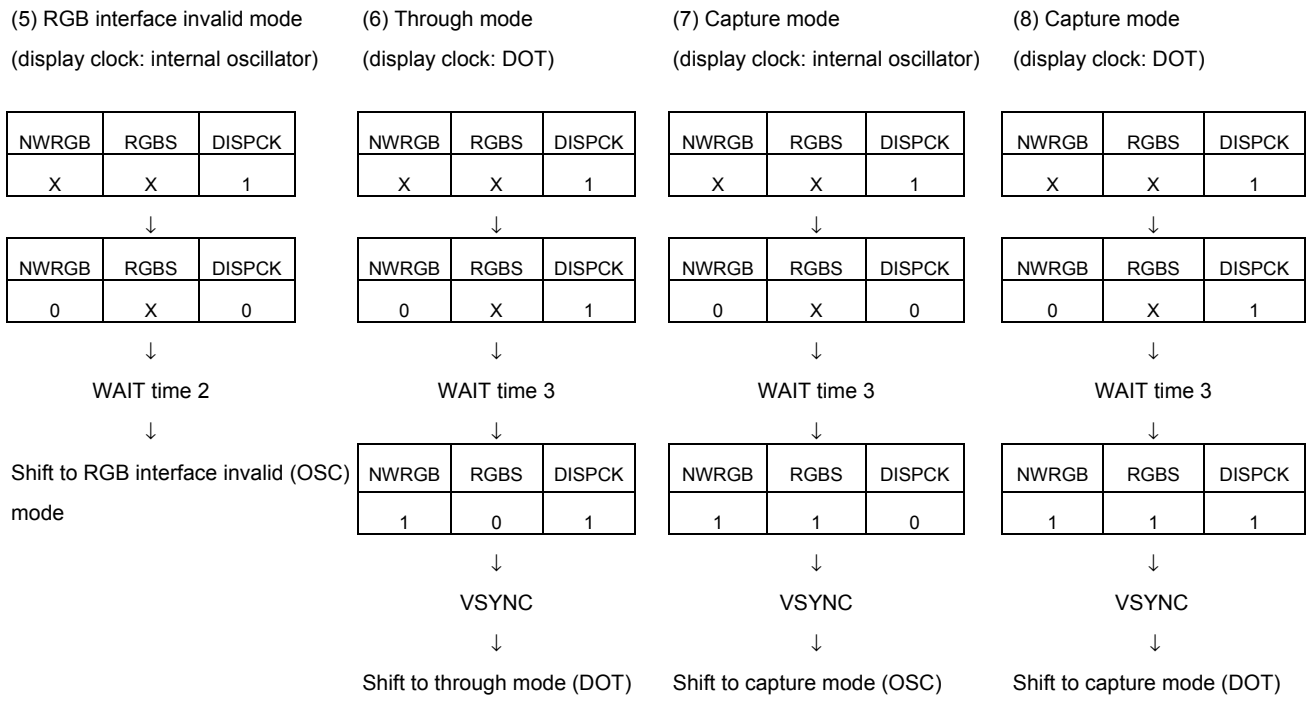
<2> When changing the mode (e.g., from the through mode to the capture mode, and vice versa), issue defined mode of selection command after once always setting RGB invalid mode. For more details, refer to sequence in the below.

<3> It is a shift flow from the time of internal oscillation use (DISPCK = 0) to each mode as a display clock.



Remark WAIT time 1: Set sufficient time of one or more frames.

<4> It is a shift flow from the time of DOTCLK use (DISPCK = 1) to each mode as a display clock.



Remarks 1. WAIT time 2: External clock for two frames is required.

2. WAIT time 3: External clock + VSYNC for one frame is required.

<5> Data (back porch period is included) of one line should be set within the period of HSYNC to HSYNC.

<6> Data (back porch period is included) of one frame should be set within the period of VSYNC to VSYNC.

<7> Do not set access to R25 register into stand-by mode.

<8> High-speed RAM write mode cannot be used.

<9> INC (D_2 bit of R5) function cannot be used about the writing to the display data RAM at the time of capture mode. However, ADX and an ADR function can be used.

<10> A setup of R6 to R11 is invalid at the time of RGB interface mode (since these are set up of CPU interface).

<11> The period from "the DOTCLK rising after falling of HSYNC" to "the rising of DOTCLK after a HSYNC rising" should not start VSYNC. For more details, refer to the next **Figure 5–12**, **5–13**.

Figure 5–12. Example of HSYNC, VSYNC, DOTCLK Input Timing (both HSYNC and VSYNC are low active)

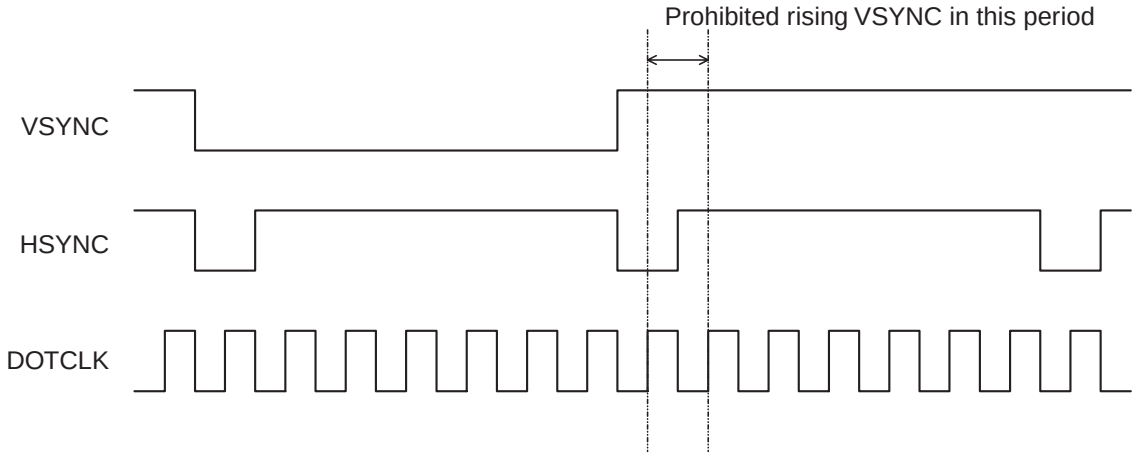
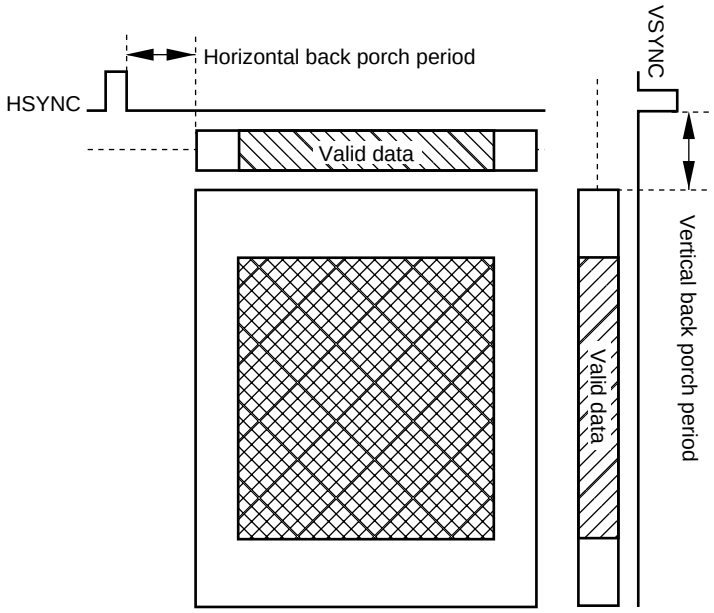


Figure 5–13. HSYNC and VSYNC Input Image Figure (when both HSYNC and VSYNC are high active)



5.1.4 i80/M68 Parallel interface

When the parallel interface has been selected, setting the C86 pin as either H or L enables a direct connection to an i80 series or M68 series CPU (see Table 5–5 below).

Table 5–5.

C86	Mode	/RD (E)	/WR (R, /W)	BWS0	BWS1	D_{17}, D_{16}	D_{15} to D_8	D_7 to D_0
H	M68 series CPU	E	R, /W	L	L	D_{17}, D_{16}	D_{15} to D_8	D_7 to D_0
				L	H	Hi-Z **Note**	D_{15} to D_8	D_7 to D_0
				H	H	Hi-Z **Note**	Hi-Z **Note**	D_7 to D_0
				H	L	Setting prohibited		
L	i80 series CPU	/RD	/WR	L	L	D_{17}, D_{16}	D_{15} to D_8	D_7 to D_0
				L	H	Hi-Z **Note**	D_{15} to D_8	D_7 to D_0
				H	H	Hi-Z **Note**	Hi-Z **Note**	D_7 to D_0
				H	L	Setting prohibited		

Note Hi-Z: High impedance. Leave it open.

The data bus signal is identified according to the combination of the RS, /RD (E), and /WR (R, /W) signals, as shown in the following Table 5–6.

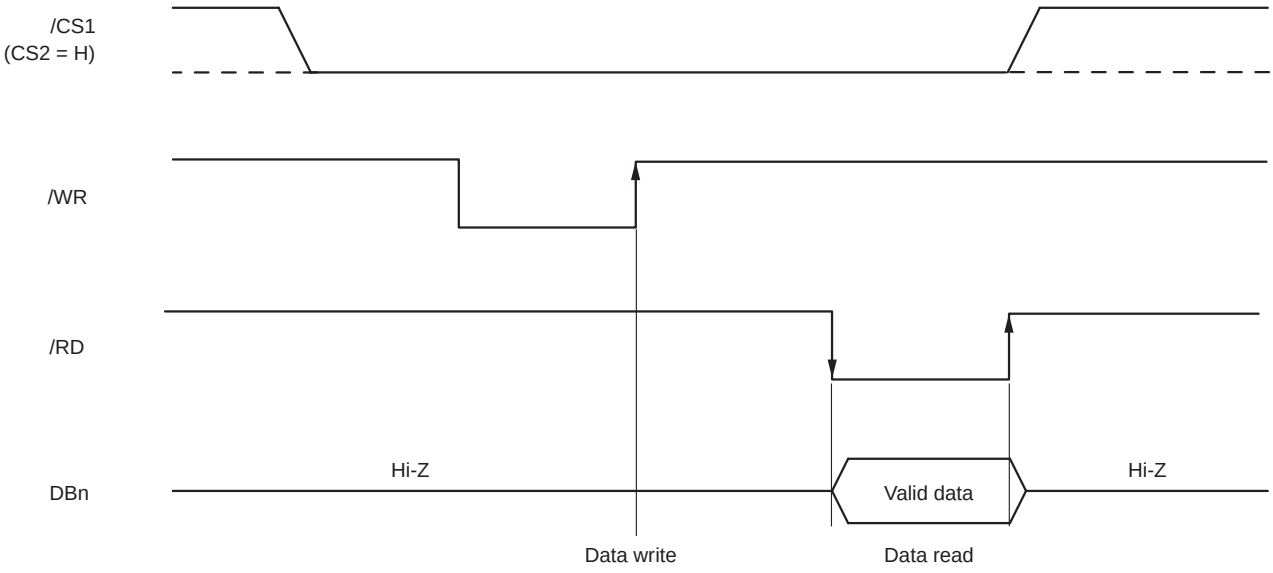
Table 5–6.

Common	M68 series CPU	i80 series CPU		Function
RS	R, /W	/RD	/WR	
H	H	L	H	Read display data
H	L	H	L	Write display data
L	H	L	H	Prohibited
L	L	H	L	Write command

(1) i80 Series Parallel Interface

When i80 series parallel data transfer has been selected, data is written to the μPD161802 at L period of the /WR signal. The data is output to the data bus when the /RD signal is L.

Figure 5–14. i80 Series Interface Data Bus Status

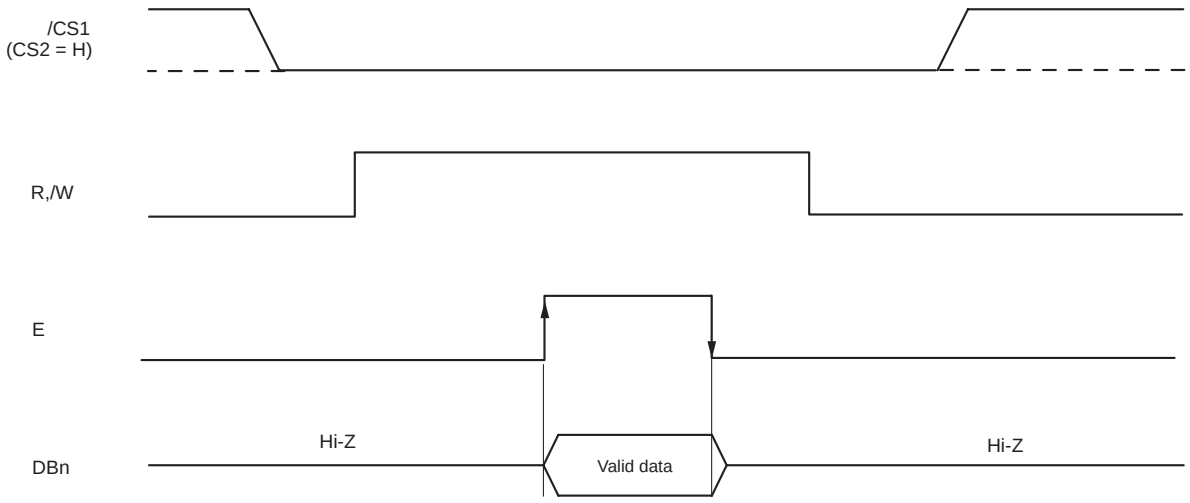


Remark Hi-Z: High impedance

(2) M68 Series Parallel Interface

When M68 series parallel data transfer has been selected, data is written at the H period of the E signal when the R,/W signal is L. In a data read operation, data is output at the rising edge of the E signal in a period when the R,/W signal is H. The data bus is released (Hi-Z) at the falling edge of the E signal.

Figure 5–15. M68 Series Interface Data Bus Status (when data read)



Remark Hi-Z: High impedance

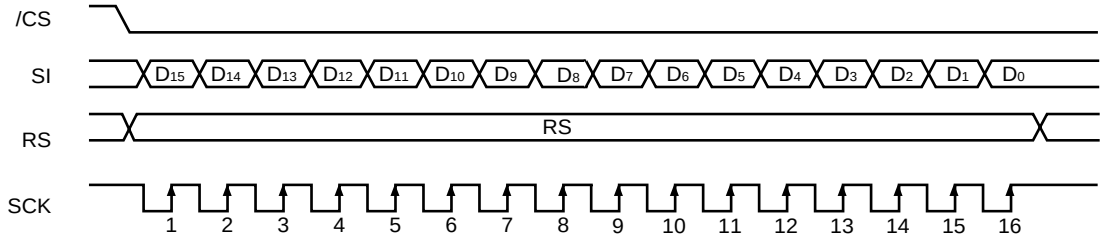
5.1.5 Serial interface

When the serial interface has been selected, if the chip is active (/CS = L), serial data input (SI) and serial clock input (SCL) can be received. Serial data is read from D_{15} and then from D_{14} to D_0 on the rising edge of the serial clock, via the serial input pin. This data is synchronized on the sixteenth serial clock's rising edge and is then converted to parallel data for processing.

RS input is used to judge serial input data as display data when RS = H the data is display data and when RS = L the data is command data. When the chip enters active mode, RS input is read at the rising edge after every sixteenth serial clock and is then used to judge the serial input data.

The serial interface signal chart is shown below.

Figure 5–16. Serial Interface Signal Chart



Remarks 1. If the chip is not active, the shift register and counter are reset to their initial settings.

2. The data read function is disabled during serial interface mode.

3. When using SCL wiring, take care concerning the possible effects of terminating reflection and noise from external sources. Our recommends checking operation with the actual device.

5.1.6 Chip select

The μPD161802 has a chip select pin (/CS). The CPU parallel interface and serial interface can be used only when /CS = L. When the chip select pin is inactive, D_0 to D_{17} are set to high impedance (invalid) and input of RS, /RD, or /WR is not active.

Therefore, keep the chip select pin active for 1 cycle period of data transfer (until a read/write operation has been completed once in the parallel interface mode).

It is not necessary to keep the chip select signal active when successively transferring data. It may be non-active between data transfer operations.

However, note that it is necessary to continue making chip selection active during "a register specification + register value setup" and transmission of "higher rank 8-bit+ low rank 8-bit of RAM" of 16-bit in the case of a serial interface.

5.1.7 Access to display data RAM and internal registers

Figures 5–17 to 5–19 show read/write accesses to the display data RAM and write accesses to internal registers 8-bit, 16-bit and 18-bit parallel interface modes and serial interface mode.

Note that the both display data RAM and registers are not read in the serial interface mode.

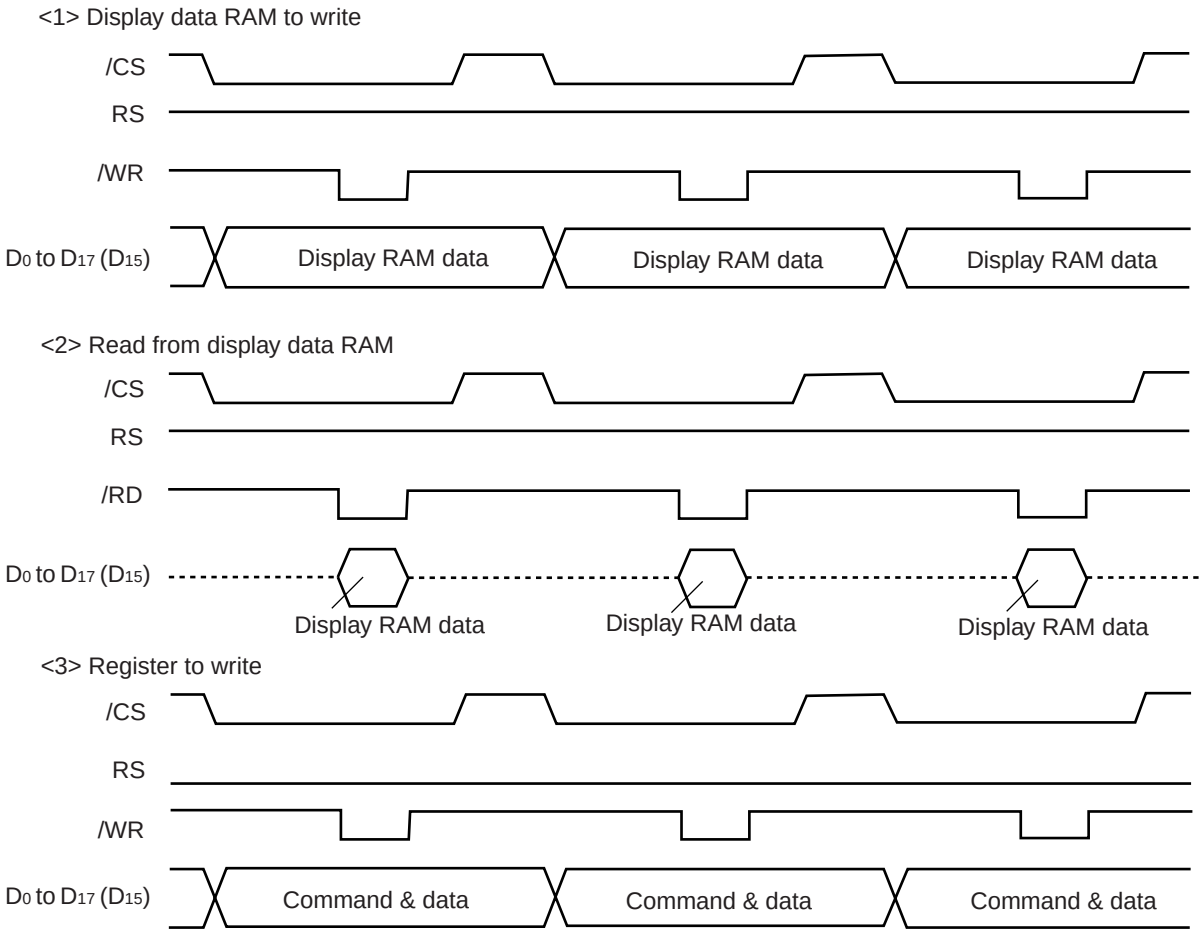
When the CPU accessed the μPD161802, the CPU only has to satisfy the standard requirement of the cycle time (t_{CYC}) and can transfer data at high speeds. Usually, it is not necessary for the CPU to take WAIT time into consideration.

In parallel interface, a high-speed RAM write function, as well as the ordinary RAM write function, is provided for writing data to the display data RAM. By using the high-speed write function, data can be written to the display RAM at an access speed two times faster than that of the ordinary RAM write function. Therefore, applications, such as video display where the display data must be rewritten at high speeds, can be supported. For details, refer to **5.2.4 High-speed RAM write mode**.

No dummy data is necessary for writing data. Dummy data is necessary only when display data is read. This relationship is shown in Figure 5–20.

However, note that even when in write mode of data at high speed for data read mode of read cycle time, this mode equals to normal mode.

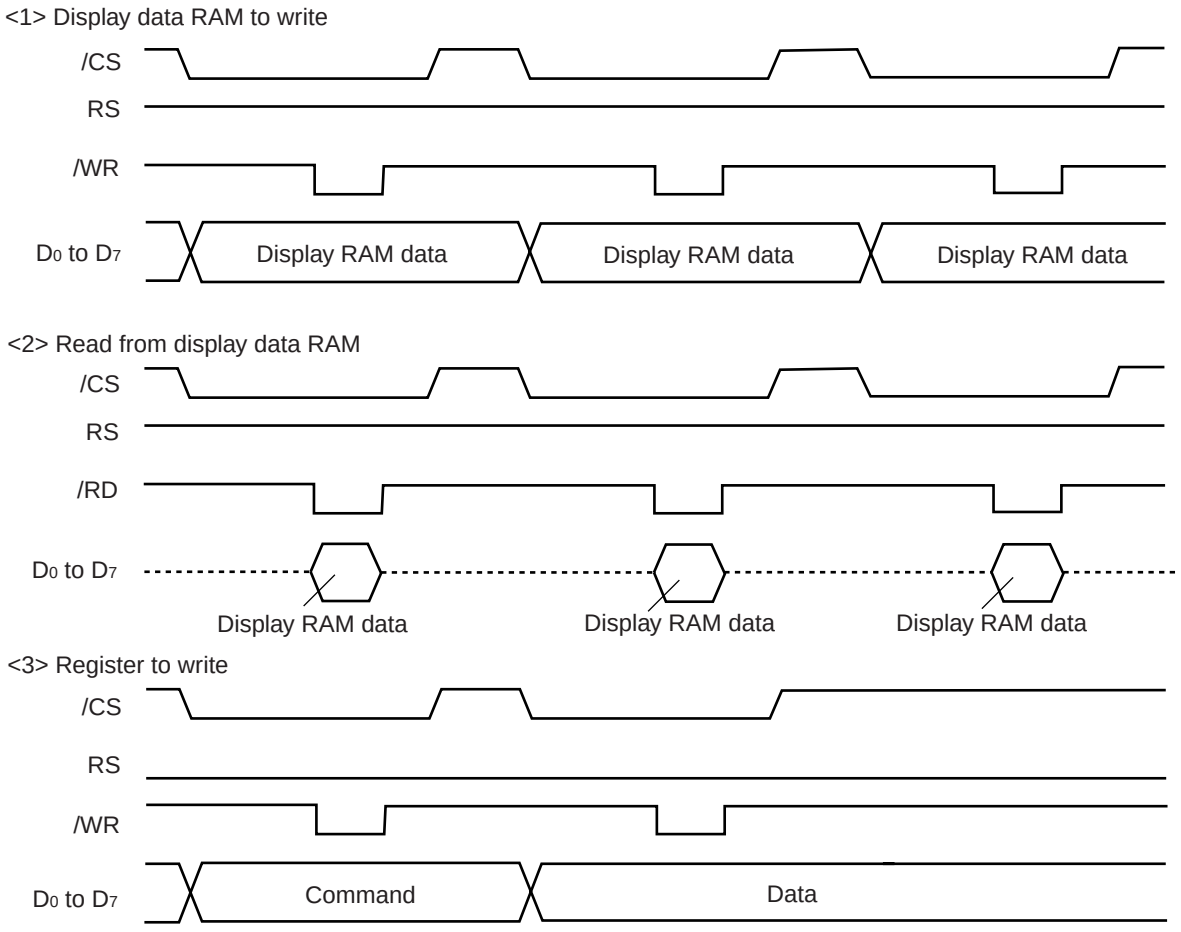
Figure 5–17. Read/Write in 16-/18-Bit Parallel Interface Mode



Cautions 1. While setting the writing to a register, set it the fixed input of the low level to RS pin. While setting the writing to a register, in the case of 16/18-bit parallel interface, 1 cycle period of write cycle is pointed out.

2. While setting the writing to a display data RAM, set it the fixed input of the high level to RS pin. While setting the writing to a display data RAM, in the case of 16/18-bit parallel interface, 1 cycle period of write cycle is pointed out. However, input signal to RS pin fix up to high level until 2-pixel data transfer ends the writing to a display data RAM at the time of high-speed RAM write mode use.

Figure 5–18. Read/Write in 8-Bit Parallel Interface Mode

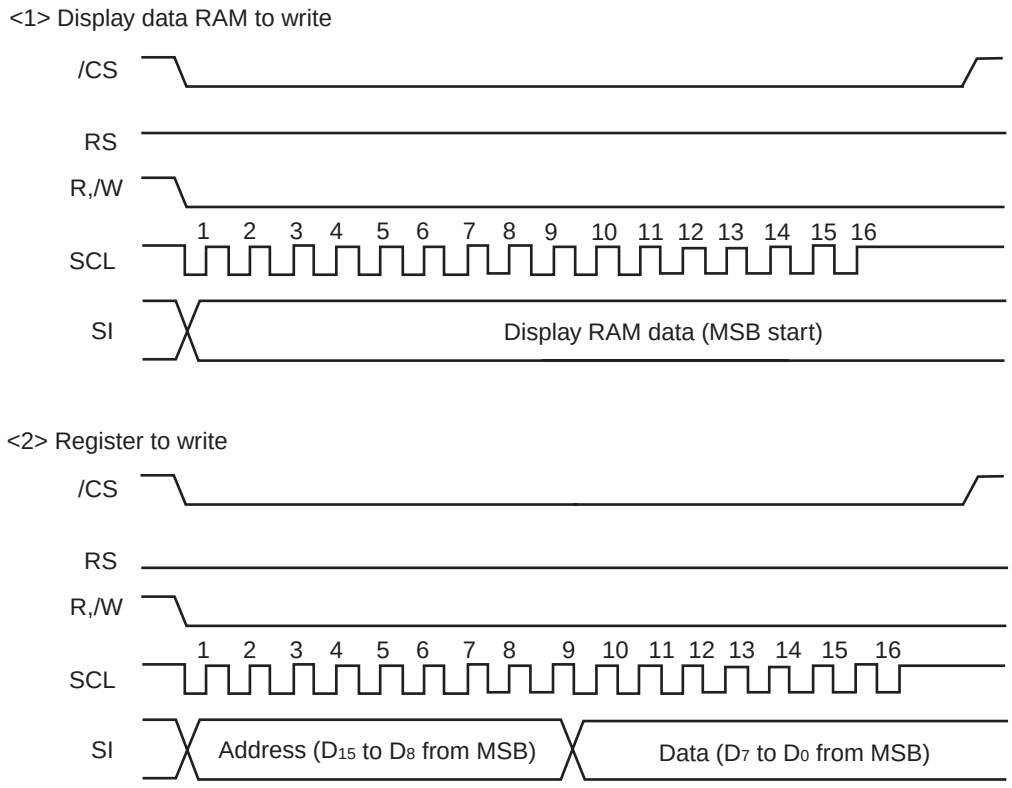


Cautions 1. While setting the writing to a register, set it the fixed input of the low level to RS pin. While setting the writing to a register, "register address specification " + "register data setup" is pointed out.

2. While setting the writing to display data RAM, set it the fixed input of the high level to RS pin. While setting the writing to display data RAM, a "data transfer for 1 pixel" period is pointed out.

3. When use 8-bit parallel interface, RS pin always start transfer after hard reset release, after set up 100 ns MIN. input of high level.

Figure 5–19. Write in Serial Interface Mode

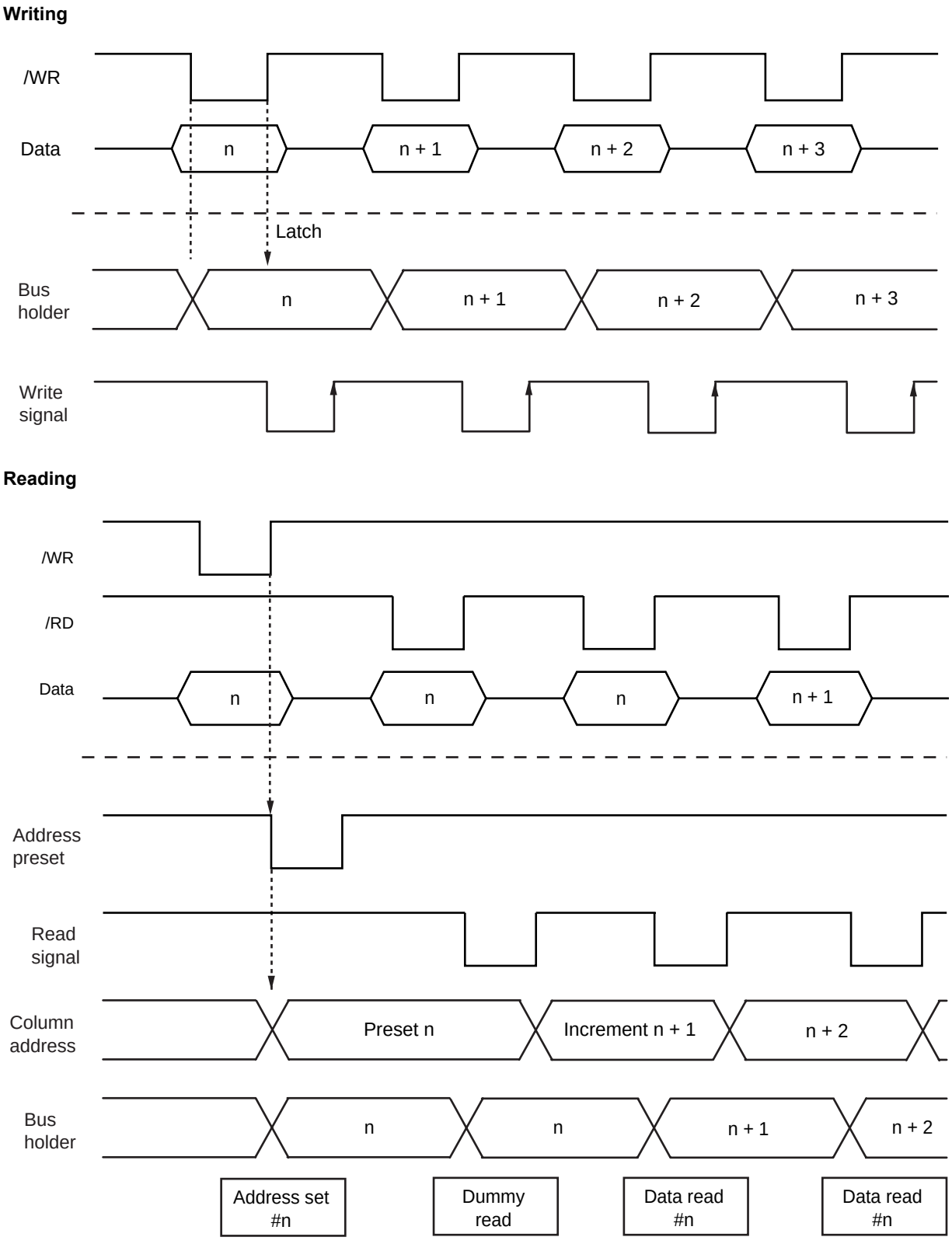


Cautions 1. It is necessary to continue making a tip selection active during "register address specification + register data setting" and transmission of "higher rank 8-bit+ low rank 8-bit of RAM" of 16-bit.

2. The period of "register address" + "register data" fix the output to RS pin to low level at the time of the writing to a register.

3. Fix it to the output to RS pin to high level during a 1-pixel data transferring period at the time of the writing to display data RAM.

Figure 5–20. Image of Internal Access to Display RAM



5.1.8 Serial interface for power supply IC control

The μPD161802 builds in the 16-bit serial interface function, in order to perform control for the external connection IC of a power supply IC etc. The following registers and pins are assigned as an object for this function.

Transfer operation is as follows.

Pin Name		Pin Function
PCS	Chip select	When data is written in the register for power supply control, it will become active "L" and the output of data will be started. Moreover, after data transfer is completed, it returns to inactive "H".
PCL	Serial clock	Serial clock output pin
PDA	Serial data	Serial data output pin. Data is outputted in falling of PCL clock signal.

Power supply IC control register list

Rn	Register	RS	R,/W	Data Bit							
				DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8
				DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
R38	Power supply IC control register 1	0	0	0	0	1	0	0	1	1	0
				PSD17	PSD16	PSD15	PSD14	PSD13	PSD12	PSD11	PSD10
R39	Power supply IC control register 2	0	0	0	0	1	0	0	1	1	1
				PSD27	PSD26	PSD25	PSD24	PSD23	PSD22	PSD21	PSD20
R40	Power supply IC control register 3	0	0	0	0	1	0	1	0	0	0
				PSD37	PSD36	PSD35	PSD34	PSD33	PSD32	PSD31	PSD30
R41	Power supply IC control register 4	0	0	0	0	1	0	1	0	0	1
							DC1	DC0			
R42	Power supply IC control register 5	0	0	0	0	1	0	1	0	1	0
				PSD57	PSD56	PSD55	PSD54	PSD53	PSD52	PSD51	PSD50
R60	Power supply IC control register 6	0	0	0	0	1	1	1	1	0	0
				PSD67	PSD66	PSD65	PSD64	PSD63	PSD62	PSD61	PSD60
R61	Power supply IC control register 7	0	0	0	0	1	1	1	1	0	1
				PSD77	PSD76	PSD75	PSD74	PSD73	PSD72	PSD71	PSD70
R62	Power supply IC control register 8	0	0	0	0	1	1	1	1	1	0
				PSD87	PSD86	PSD85	PSD84	PSD83	PSD82	PSD81	PSD80
R63	Power supply IC control register 9	0	0	0	0	1	1	1	1	1	1
				PSD97	PSD96	PSD95	PSD94	PSD93	PSD92	PSD91	PSD90
R64	Power supply IC control register 10	0	0	0	1	0	0	0	0	0	0
				PSDA7	PSDA6	PSDA5	PSDA4	PSDA3	PSDA2	PSDA1	PSDA0
R65	Power supply IC control register 11	0	0	0	1	0	0	0	0	0	1
				PSDB7	PSDB6	PSDB5	PSDB4	PSDB3	PSDB2	PSDB1	PSDB0

<Transfer operation>

By 3-line serial interface, data is transferred per 16 bits. Shift operation of serial interface is performed after chip select signal output (PCS = L) synchronizing with falling of a serial clock (PCL). The data format to the external connection IC serves as data which is set the 1st byte of transfer data as a command (register number), and is set as a command the 2nd byte. Transfer is performed at MSB first.

The start trigger of serial data transfer is the writing of the data to above-mentioned "power supply IC control" each control register. Writing of the data to each control register starts an output from PCS, PCL, and PDA automatically.

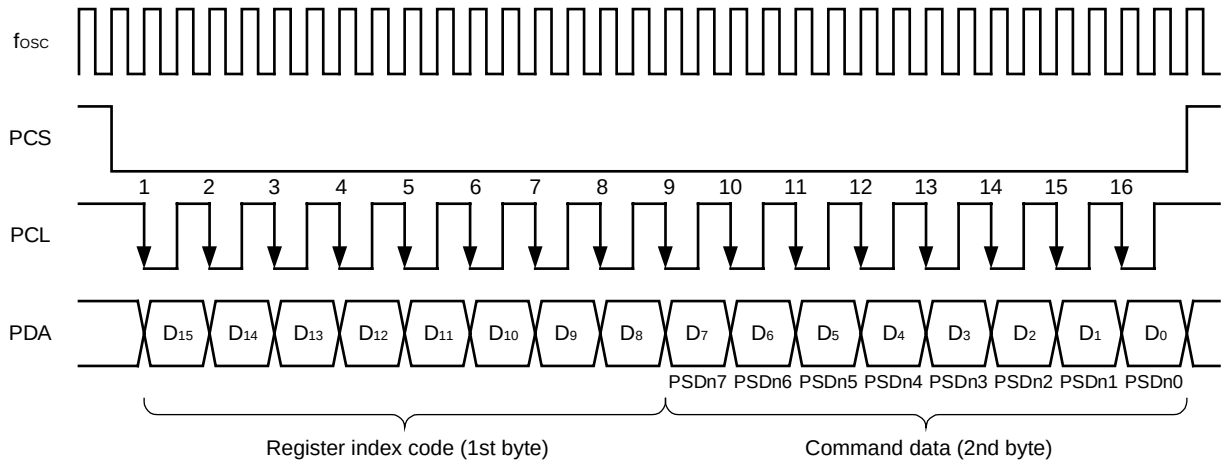
After reset command is inputted, IC connected to the μPD161802, such as a power supply IC, needs to recognize the 1st byte of data transferred to be a command (index register), and needs to recognize the 2nd byte of data to be data (data register) to a command.

In addition, when performing the writing to the register for power supply control continuously, after pre-serial data transmission is completed, it is necessary to perform.

The continuation writing to a power supply control register should set and perform wait time of minimum 250 μs.

When the data to the register for power supply control is written in during serial data transfer, the data transfer written in data and the register during transfer is not guaranteed.

Figure 5–21. Serial Interface Timing Chart for Power Supply IC Control



5.2 Display Data RAM

This RAM stores dot data for display and consists of 4,320 bits (240 x 18) x 320 bits. Any address of this RAM can be accessed by specifying an X address and an Y address.

Display data RAM construction refers to **Figure 5–22**.

Figure 5–22. Display Data RAM

D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
R data						G data						B data					
Pixel 1 (= 1 X address)																	

LCD panel	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8	
	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8	
	000H	001H	002H	003H	004H	005H	006H	007H	

5.2.1 X address circuit

The X address of the display data RAM is specified by using the X address register (R6) as shown in Figure 5–24. The specified X address is incremented by one each time display data is written or read.

In the X address increment mode, the X address is incremented up to 0EFH. If more display data is written or read, the Y address is incremented, and the X address returns to 000H.

The relationship between the X address and source output can be inverted by the ADX flag of control register 1 as shown in Figure 5–23. After switched ADX, the input data can be rotated 90 degrees and displayed by changing the ADR function and address increment direction between X and Y.

5.2.2 Y address circuit

The Y address of the display data RAM is specified by using the Y address register (R7) as shown in Figure 5–24.

The Y address is incremented each by one when one each time display is written or read and X address is incremented to last address.

When the Y address has been incremented up to 13FH and the X address up to the final address, if further display data is read or written, the X and Y addresses return to 000H.

As shown in Figure 5–23, the relationship between the Y address and gate output can be inverted by the ADR flag of the control register. The data written to the display can be rotated 90 degrees and output by changing the ADX function and address increment direction between X and Y.

Table 5–7. Data Access Control (R5) Setting

INC	Setting
0	Time of data access X directions an address continuing an increment or a decrement is carried out.
1	Time of data access Y directions an address continuing an increment or a decrement is carried out.

Caution When the access direction is changed, be sure to access Display RAM from INC after setting up X address register (R6) and Y address register (R7).

Figure 5–23. Example of 90-Degree Rotation

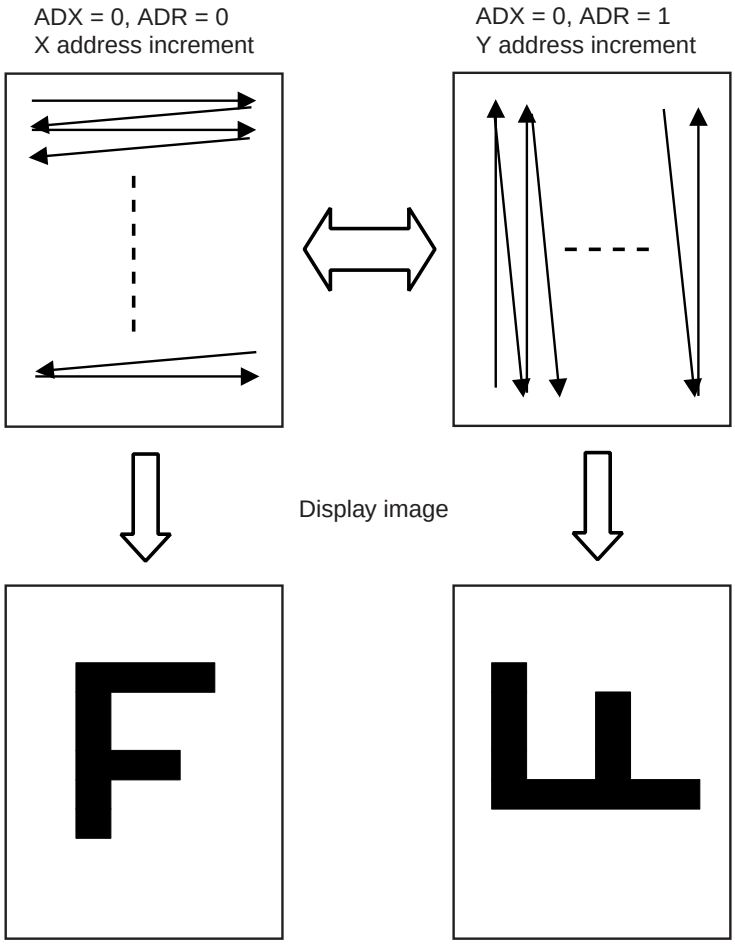
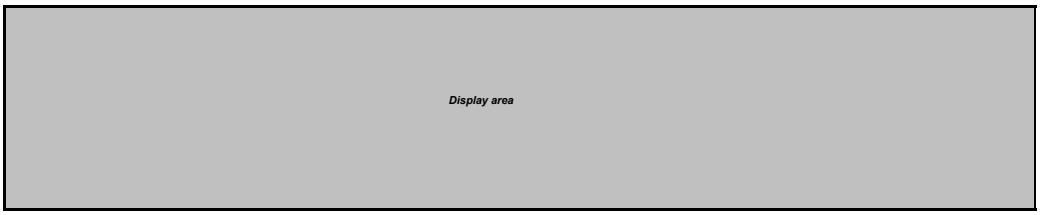


Figure 5–24. The μPD161802 RAM Addressing

(1) ADX = 0

Source output	Y_1			Y_2			---	---	Y_{239}			Y_{240}		
X-address	000H			001H			---	---	0EEH			0EFH		
	D_{17} to D_{12}	D_{11} to D_6	D_5 to D_0	D_{17} to D_{12}	D_{11} to D_6	D_5 to D_0			D_{17} to D_{12}	D_{11} to D_6	D_5 to D_0	D_{17} to D_{12}	D_{11} to D_6	D_5 to D_0

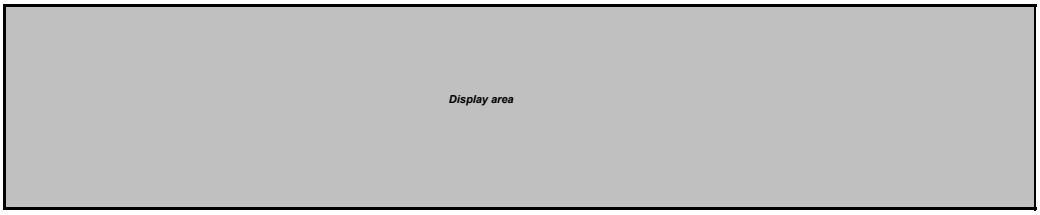
Y-address	
ADR = 0	ADR = 1
000H	13FH
001H	13EH
078H	07BH
079H	07AH
07AH	079H
07BH	078H
13EH	001H
13FH	000H



(2) ADX = 1

Source output	Y_1			Y_2			---	---	Y_{239}			Y_{240}		
X-address	0EFH			0EEH			---	---	001H			000H		
	D_{17} to D_{12}	D_{11} to D_6	D_5 to D_0	D_{17} to D_{12}	D_{11} to D_6	D_5 to D_0			D_{17} to D_{12}	D_{11} to D_6	D_5 to D_0	D_{17} to D_{12}	D_{11} to D_6	D_5 to D_0

Y-address	
ADR = 0	ADR = 1
000H	13FH
001H	13EH
078H	07BH
079H	07AH
07AH	079H
07BH	078H
13EH	001H
13FH	000H



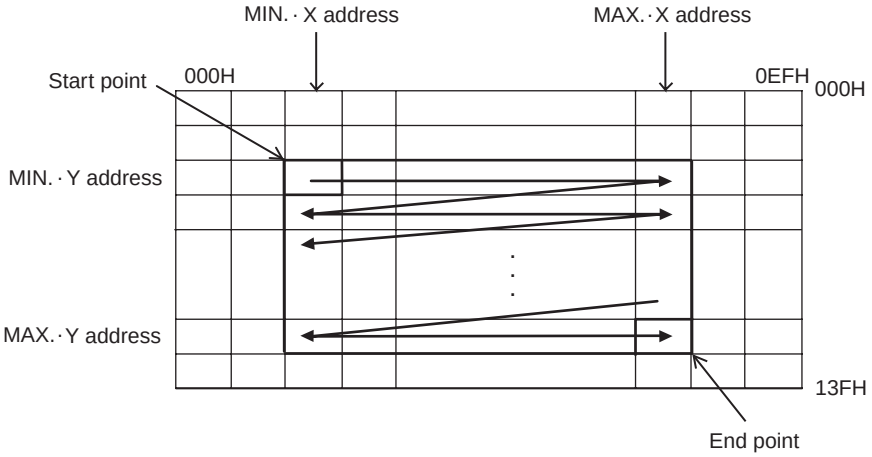
5.2.3 Arbitrary address area access (window access mode (WAS))

With the μPD161802, any area of the display RAM selected by the MIN.·X/Y address registers (R8 and R10) and MAX.·X/Y address registers (R9 and R11) can be accessed.

First, select the area to be accessed by using the MIN.·X/Y address registers and MAX.·X/Y address registers. When WAS of data access control register (R5) is set to 1, the window access mode is then selected. The address scanning setting is also valid in this mode, in the same manner as when data is normally written to the display RAM. In addition, data can be written from any address by specifying the X address register (R6) and Y address register (R7).

The data input from the RGB interface in the through mode of the RGB interface cannot be used in the window access mode.

Figure 5–25. Example of Incrementing Address when in Window Access Mode



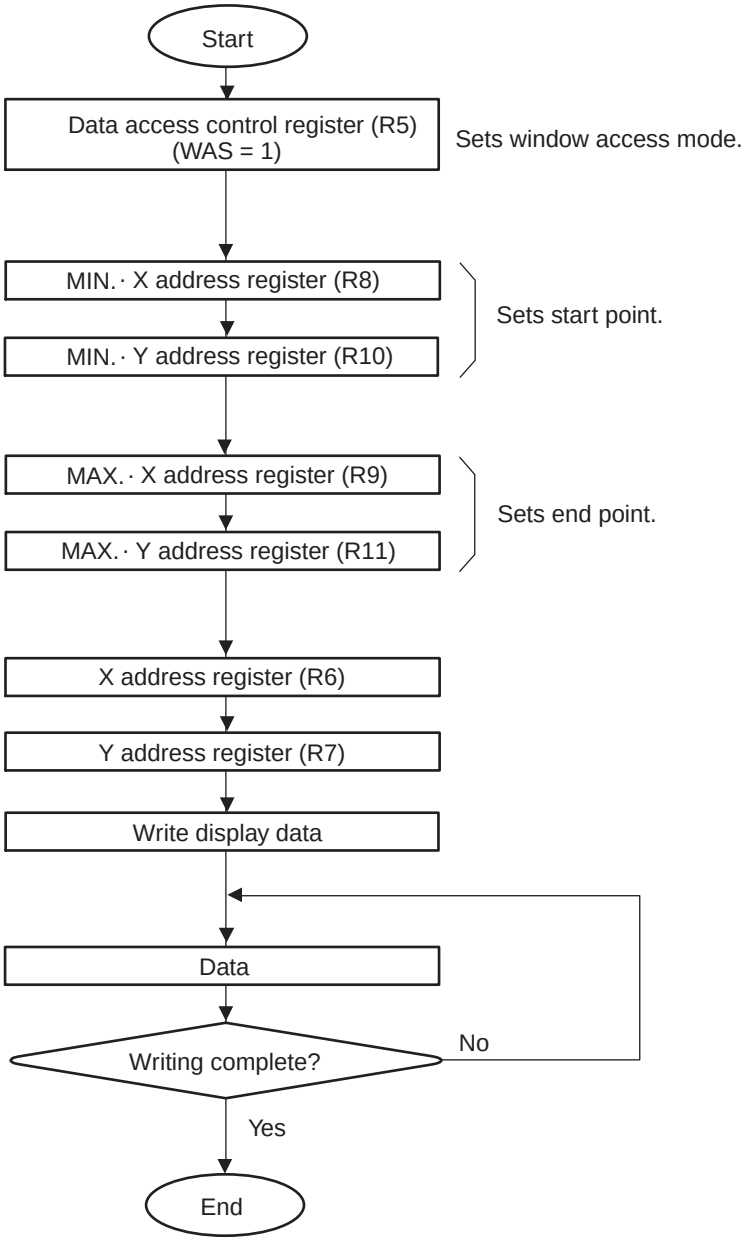
Cautions 1. When using the window access mode, the relationship between the start point and end point shown in the table below must be established.

Item	Address Relationship
X address	000H ≤ MIN.·X address ≤ X address (R6) MAX.·X address ≤ 0EFH
Y address	000H ≤ MIN.·Y address ≤ Y address (R7) MAX.·Y address ≤ 13FH

2. If invalid address data is set as the MIN./MAX.· address, operation is not guaranteed.

3. Do not specify any value other than the address value 2n – 2 (n = 1 to 120) for the X address in the high-speed RAM access mode. The operation is not guaranteed if invalid address data is set.

Figure 5–26. Example of Sequence in Window Access Mode



5.2.4 High-speed RAM write mode

With the μPD161802, two types of access modes can be selected for accessing the display RAM.

The μPD161802 has a high-speed RAM write function, as well as an ordinary RAM write function. By using the high-speed write function, data can be written to the display RAM at an access speed two times faster than that of the ordinary RAM write function. Therefore, applications, such as video display where the display data must be rewritten at high speeds, can be supported.

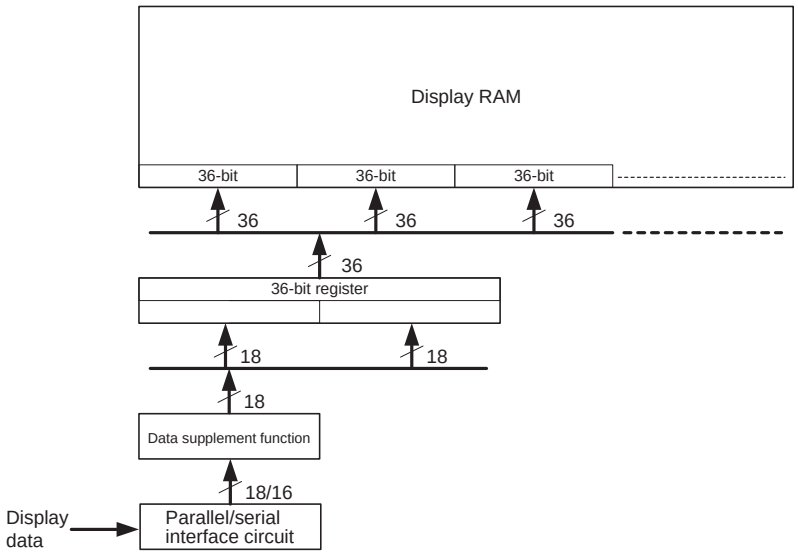
When the high-speed RAM write mode is selected by using BSTR of the data access control register (R5), data is temporarily stored in an internal register of the μPD161802. When data of 36 bits (18 bits x 2) has been stored in the register, it is written to the display RAM. It is also possible to write the next data to the internal register while the first data is being written to the RAM.

In the high-speed RAM write mode, however, the CPU must transmit data in units of 2 pixel data (1-pixel/18-bit mode: 36-bit, 1-pixel/16-bit mode: 32-bit) have been written to the internal register. If data of less than 2-pixel data is transmitted in the high-speed RAM write mode, this data is not written to the display RAM. Therefore, CPU data is not reflected on the LCD display even if it is transmitted. In this case, the data that is not reflected remains stored in the register. When the next data is transferred, it is written to the register from where the preceding data is stored.

However, if the RS signal is changed (RS = L) in the middle of data transfer, and then asserted active again and when the display data write is set, the register is initialized. Consequently, the data stored in the register is lost.

It is therefore recommended to transmit display data in 2-pixel units when using the high-speed RAM write mode.

Figure 5–27. Image of Operation in High-speed RAM Write Mode



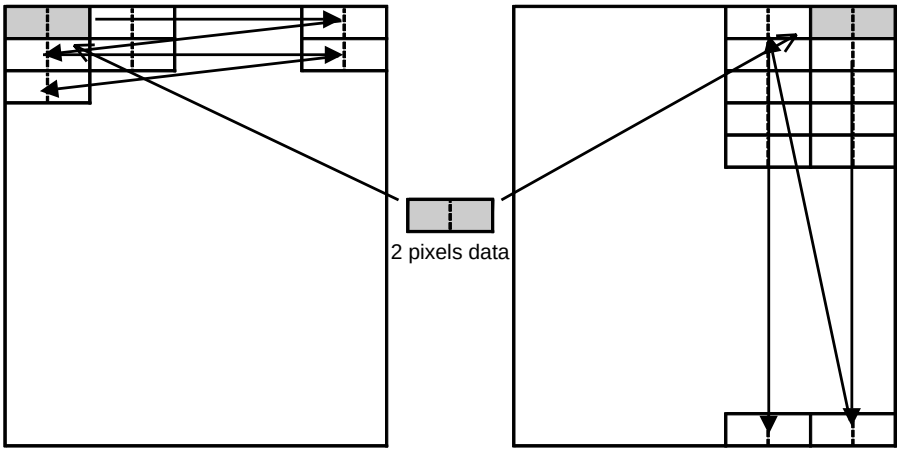
Cautions 1. Do not specify any value other than the address value 2n – 2 (n = 1 to 120) for the X address register (R6) in the high-speed RAM access mode. The operation is not guaranteed if invalid address data is set.

2. Burst mode cannot be used about each mode of 8-bit parallel interface, serial interface, and RGB interface.

3. This write-in mode is valid only at the time of 16-/18-bit parallel interface package data transfer mode.

Note that it writes in 2 pixels at a time perpendicularly at the time of Y address increment mode as shown in Figure. 5–28.

Figure 5–28. Image of Operation Accompanying Difference in the Direction of an Address Increment at the Time of High-speed RAM Write Mode



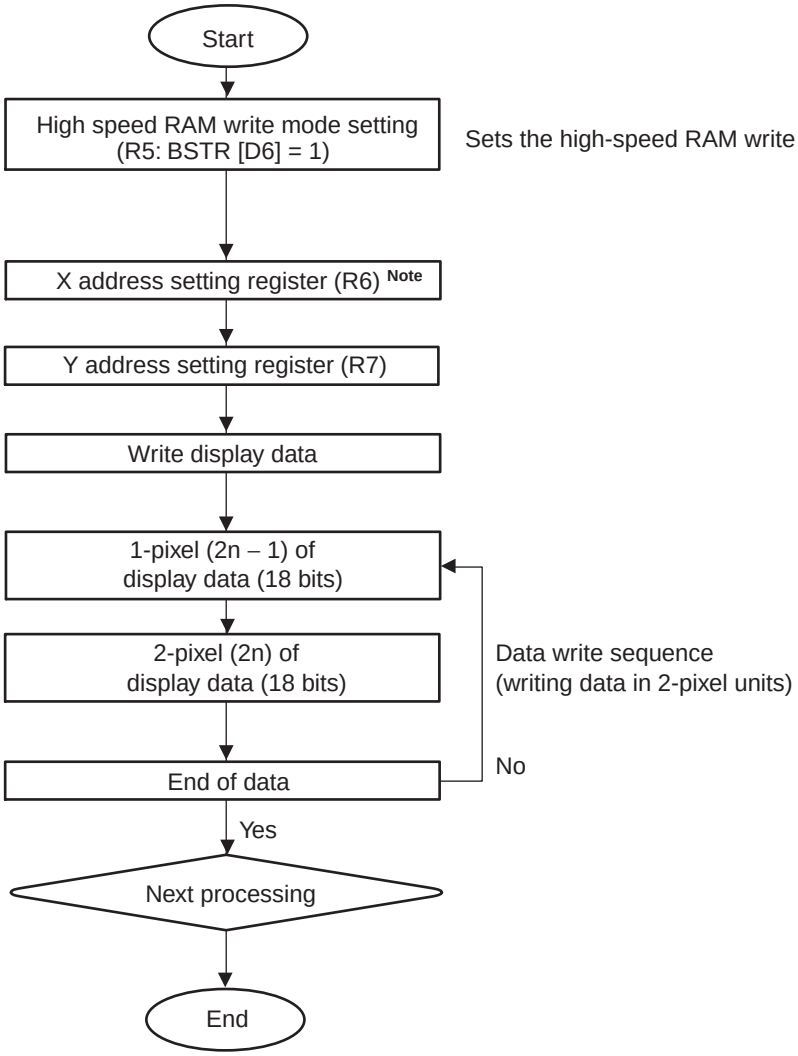
X address increment mode
(D_2 of R5 = 0)

Writing is set in the direction of
X address every 2 pixels.

Y address increment mode
(D_2 of R5 = 1)

Writing is set in the direction of
Y address every 2 pixels.

Figure 5–29. Example of Sequence in High-Speed RAM Write Mode (when 18-Bit Parallel Interface)



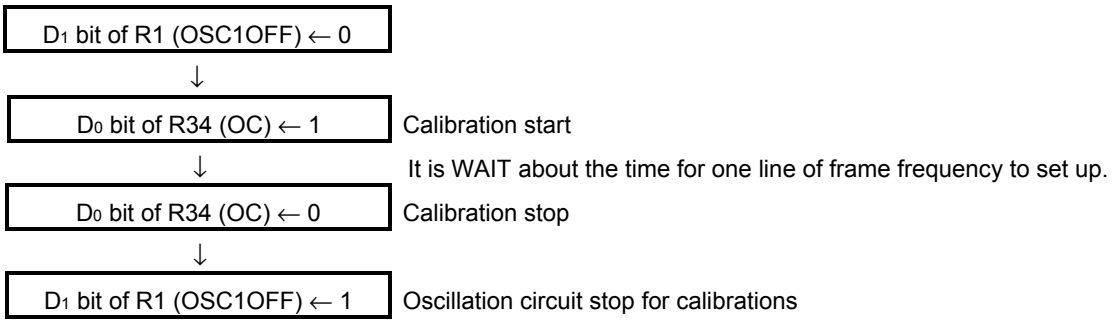
Remark n: n ≥ 1

Note Do not specify any value other than the address value 2n – 2 (n = 1 to 120) for the X address (R6) in the high-speed RAM access mode. The operation is not guaranteed if invalid address data is set.

5.3 Oscillator

The μPD161802 can select from built-in oscillation circuit (OSCSEL = L: type with built-in CR), or an external oscillation circuit (OSCSEL = H: CR external) the oscillation circuit which generates display clock by setup of an OSCSEL pin.

The μPD161802 also has two CR oscillators (with external R), which generate the display clock. One oscillation circuit (OSC2) is used in order to generate liquid crystal display output timing, and another oscillation circuit (OSC1) is used for it at the time of calibration execution of frame frequency. A calibration execution flow is shown below.



Since the oscillation circuit for calibrations comes to unnecessary after calibration execution, in order to lower power consumption, suspend an oscillation ("1" is set to OSC1OFF of D_1 bit of R1). In addition, when set calibration again once performing a calibration, start oscillation operation again.

Moreover, the frame frequency by which the calibration was carried out is eliminated by command reset. Therefore, when command reset is input, set a calibration again.

Be sure to connect the capacitor of T.B.D. μF to an OSCR pin with resistance of T.B.D. μF at an OSCC pin at the time (OSCSEL = H) of external oscillation circuit selection. When internal oscillator has been selected, leave both pins open. (or please make an OSCR pin leave open or make an fixed OSCC pin to low)

5.4 Display Timing Generator

The display timing generator generates the timing signals for the internal timing of the source driver and for the panel gate.

5.4.1 1-line period timing

The μPD161802 has two drive system timing output circuits. Following preparation of these drive system timing output is carried out, and a usually different timing signal at the time of a drive and a partialness drive is generated.

	Timing Circuit 1	Timing Circuit 2	Remark
Gate circuit clock signal	GCLK	CKV	Fixed timing
Gate circuit start pulse signal	GSTB	STV	Fixed timing
Multi-plectra switch signal 1	RSW	ASW1	R83, R84
Multi-plectra switch signal 2	GSW	ASW2	R85, R86
Multi-plectra switch signal 3	BSW	ASW3	R87, R88
Gate output enable signal 1	GOE_1	OEV	R79, R80
Gate output enable signal 2	GOE_2	OEVE	RGOE2, ROEVE [R77]
Field selection signal 1	EXT1		R66 D [4:3]
Field selection signal 2	EXT2		
Extended timing signal 1		EXT1	R89, R90
Extended timing signal 2		EXT2	R91, R92

The clock set up by the calibration function is being used for the clock of one-line period, and it is generating all timing by using 40 clocks as a base.

Calibration function is assigning 40 clocks and is adjusting frame frequency to within a time of the one line period set up by calibration time (t_{cal}).

Moreover, the number of clocks of one-line period can be set up by the one-line period clock setting register (R76). The number of clocks set up by R76 is inserted as dummy clock from one-line period 38 clock.

Figure 5–30. 1-line Driving Period (timing circuit 1)

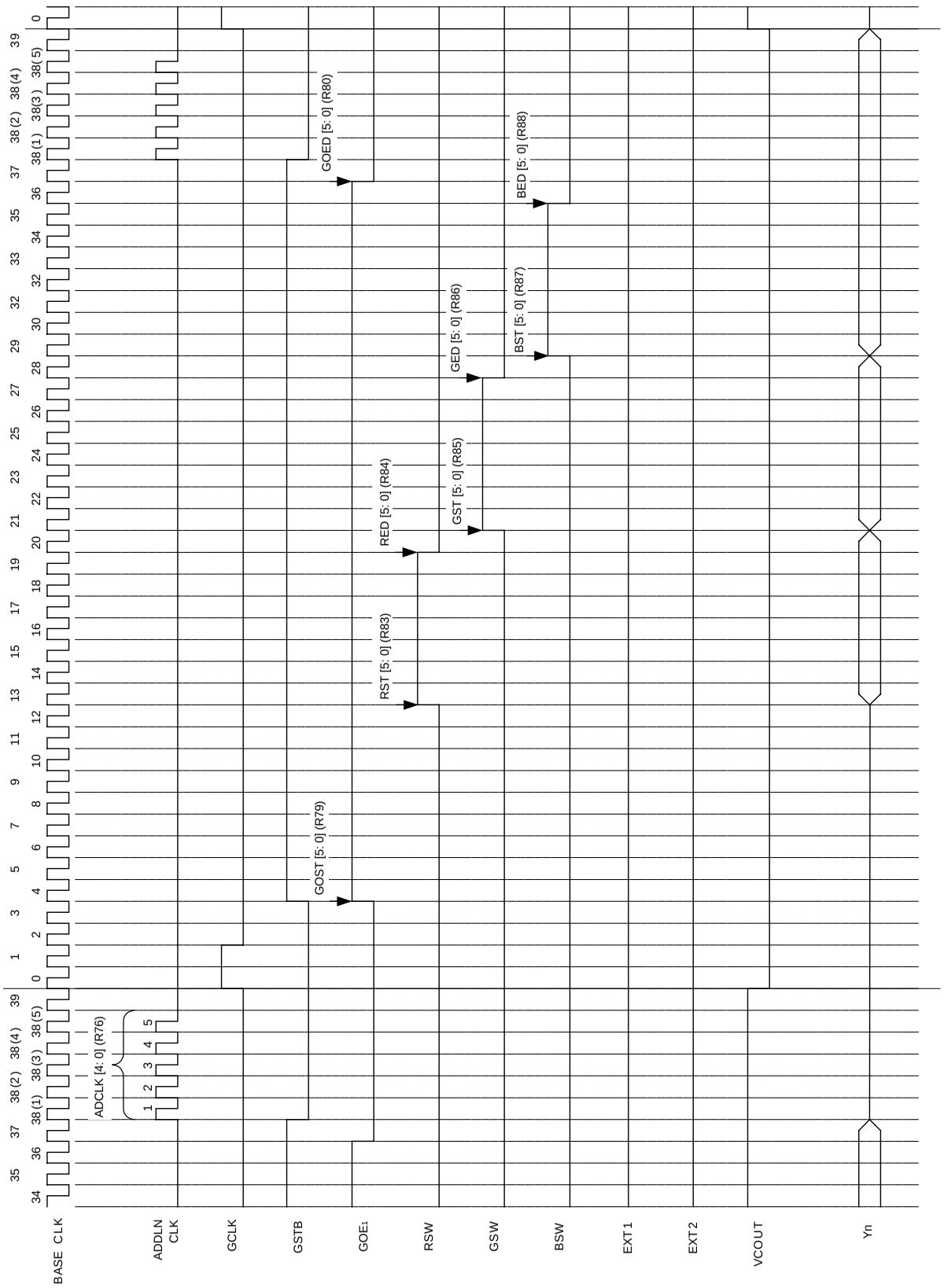
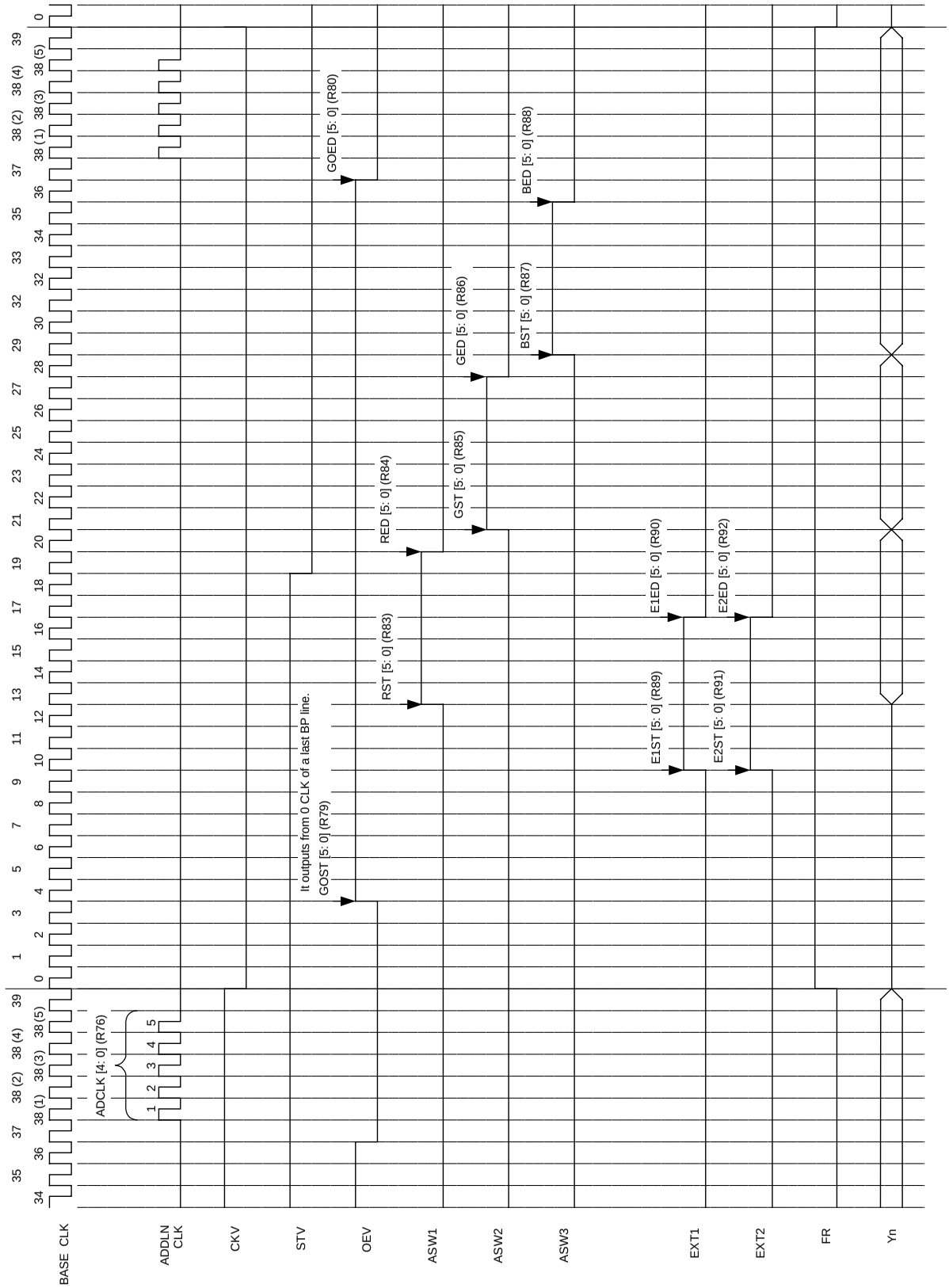


Figure 5–31. 1-line Driving Period (timing circuit 2)

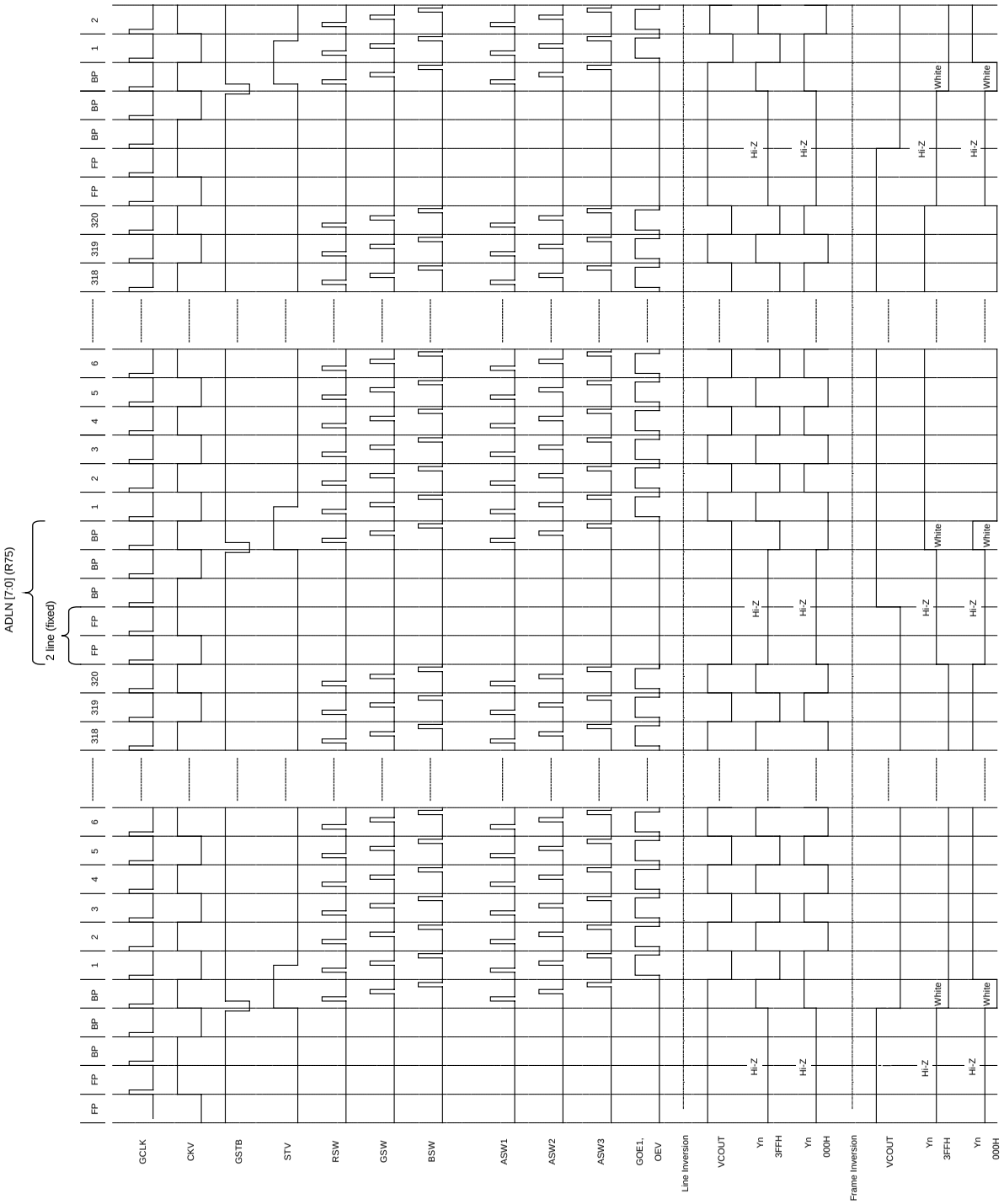


5.4.2 1-frame period timing

The μPD161802 has two driving system timing output circuits. For details, refer to the **5.4.1 1-line period timing**.

Those signals are the timing at the time of ON/OFF and a standby setup etc., and are controlled by different timing control flag. Refer to **5.8 Power Supply Sequence** and **5.9 Standby and Power Supply OFF Sequence**.

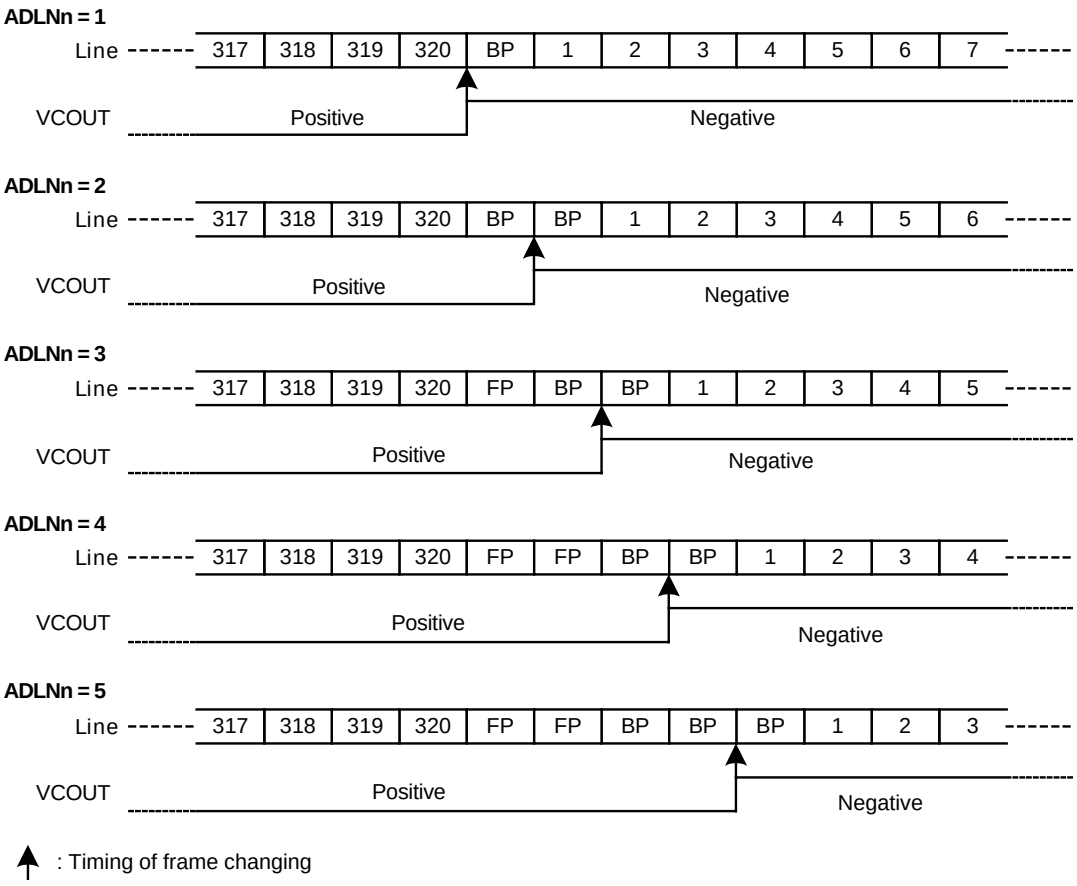
Figure 5–32. 1- frame Driving Period



Moreover, the one-frame period is constituted by 320 line + front porch period (FP) + back porch (BP), and the number of lines of a FP + BP period can be set up by the blanking period line setting register (R75: ADLNn). At this time, a frame changes and timing is performed during the back porch of the 1st line. Refer to the following Table and Figure 5–33.

ADLN7	ADLN6	ADLN5	ADLN4	ADLN3	ADLN2	ADLN1	ADLN0	Setting Line Number	
								FP	BP
0	0	0	0	0	0	0	0	Prohibited	
0	0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	1	0	0	2
0	0	0	0	0	0	1	1	2	1
0	0	0	0	0	1	0	0	2	2
0	0	0	0	0	1	0	1	2	3
				⋮				⋮	⋮
1	1	1	1	1	1	1	0	2	252
1	1	1	1	1	1	1	1	2	253

Figure 5–33. ADLNn Setting and Frame Change Rate



5.4.3 3-line interlace

The μPD161802 has 3-line interlace function.

EXT1, EXT2 pin performs the change of normal mode and 3-line interlace mode.

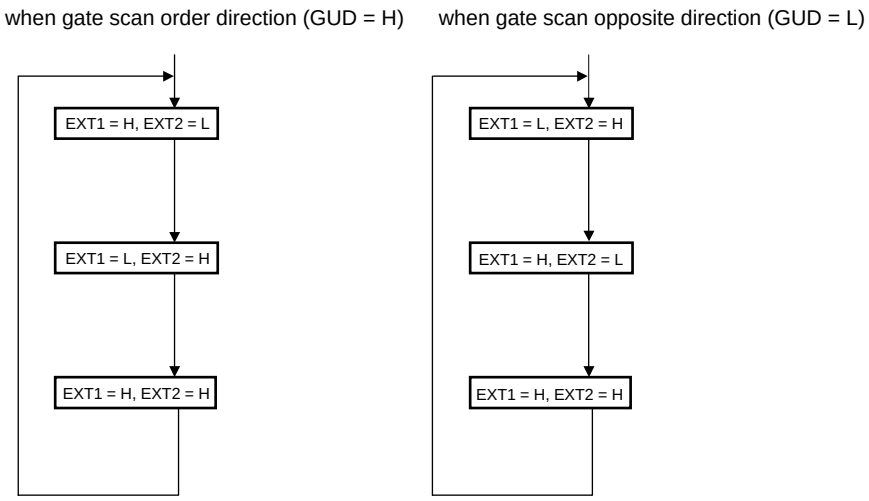
Normal mode: EXT1 = L, EXT2 = L

3-line interlace mode:

The 1st field Source output: 0 → 3 → 6 → …… → 315 → 318

The 2nd field Source output: 1 → 4 → 7 → …… → 316 → 319

The 3rd field Source output: 2 → 5 → 8 → …… → 314 → 317



Cautions 1. When use 3-line interlace function, set 4 over to ALNn.

2. 3-line interlace function should set up TCKSEL (R78 [D_7] = 0), and should select the timing circuit 1.

The timing at the time of 3-line interlace mode comes to be shown in the following figures.

Figure 5–34. Display timing (Blanking period = 4 line (ADLNn = 4), the dummy line between the fields = 1 line)

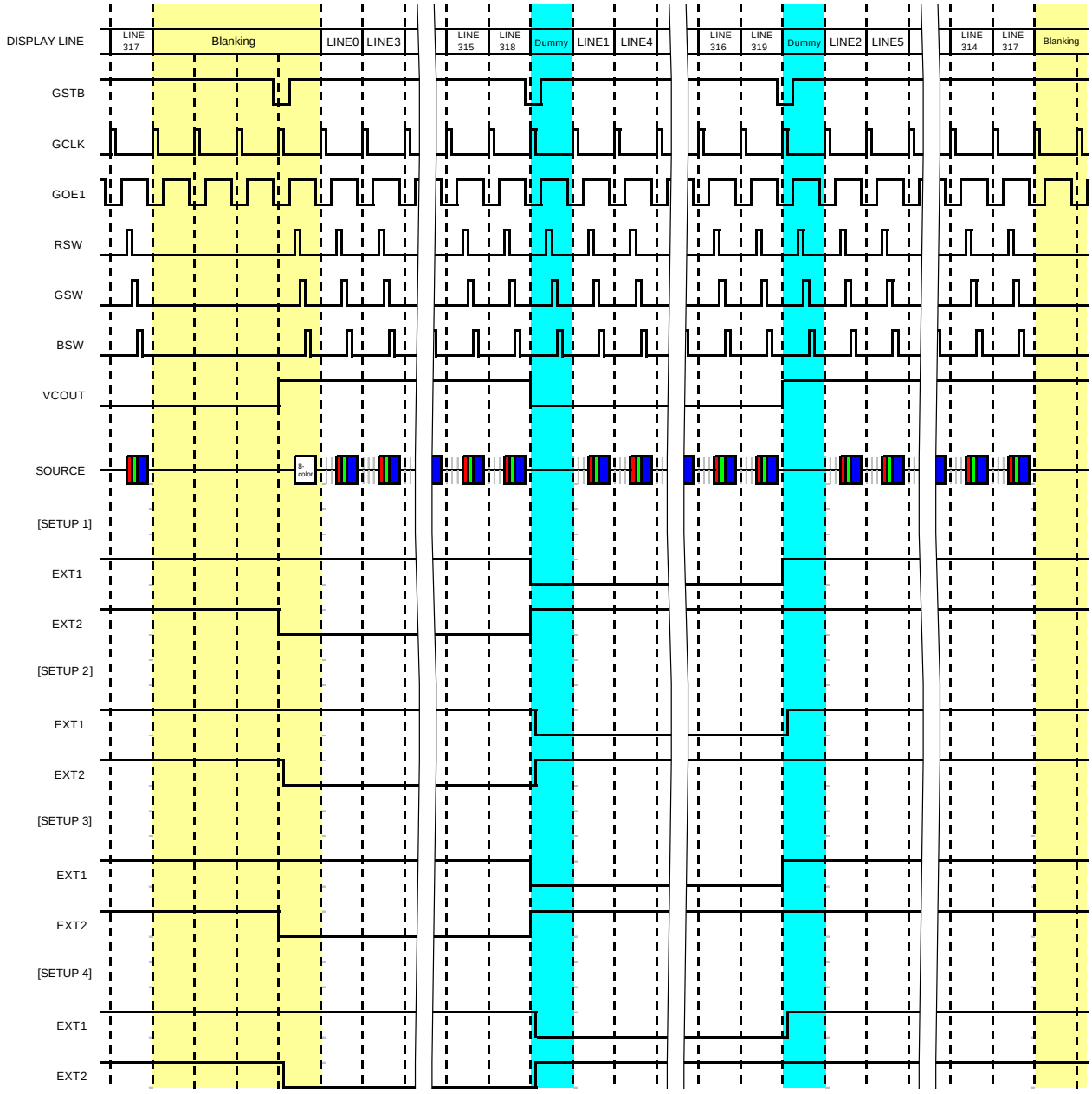


Figure 5–35. Display timing (Blanking period = 4 line (ADLNn = 4), the dummy line between the fields = 2 line)

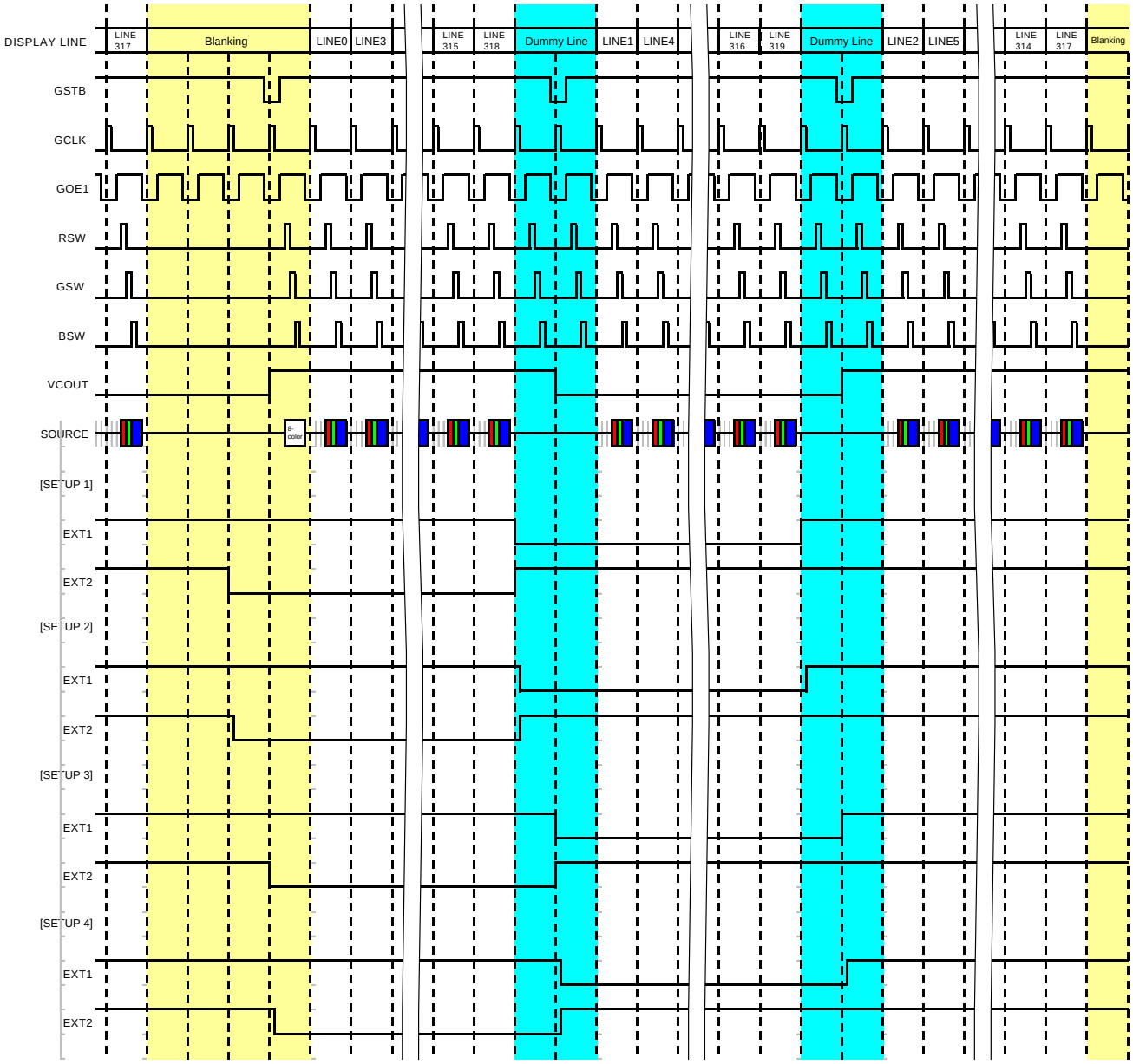


Figure 5–36. Mode change timing (Blanking period = 3-line (ADLNn = 3), the dummy line between the fields = 2 line)

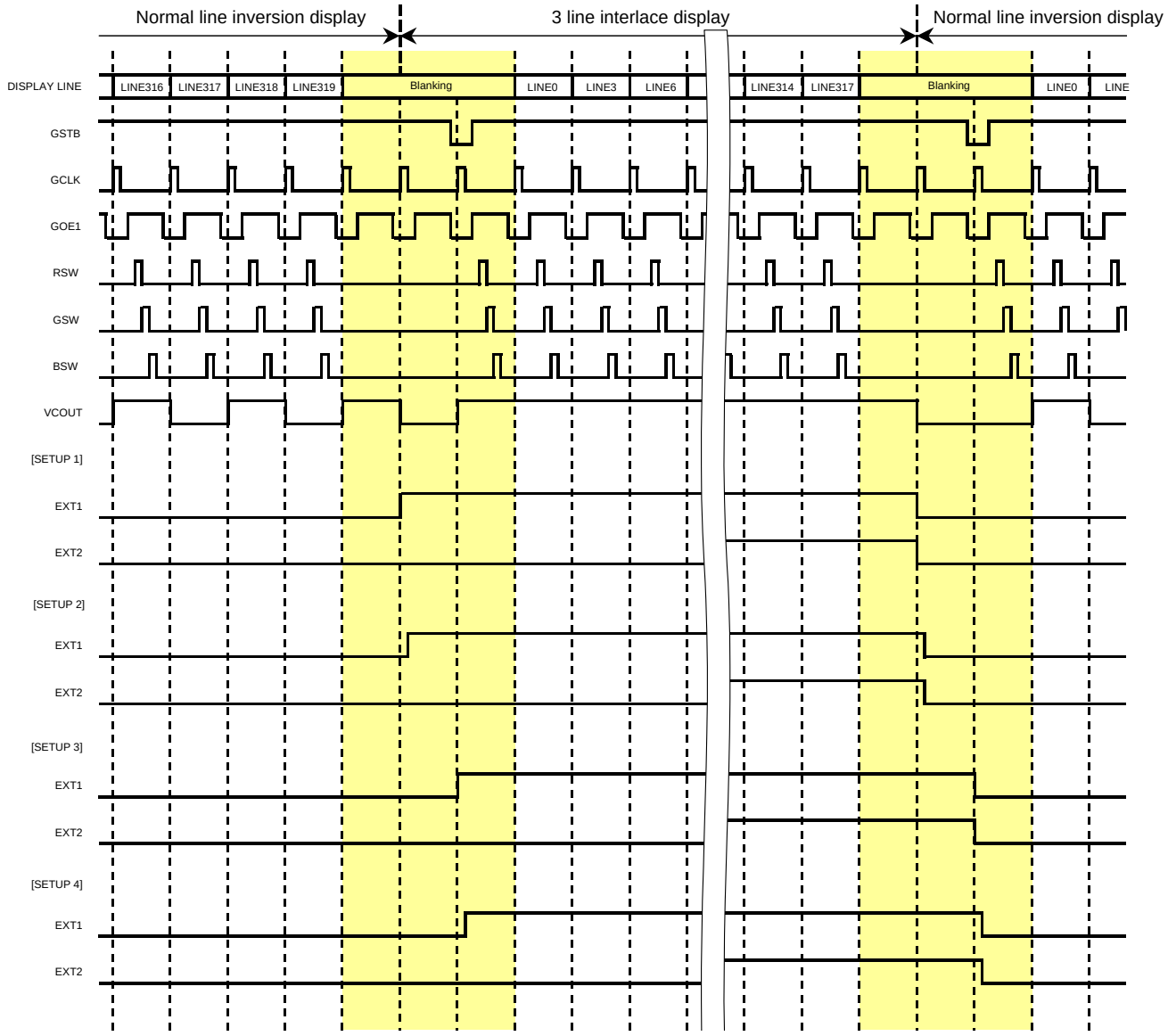


Figure 5–37. Change timing (Blanking period = 4 line (ADLNn = 4), the dummy line between the fields = 2 line)

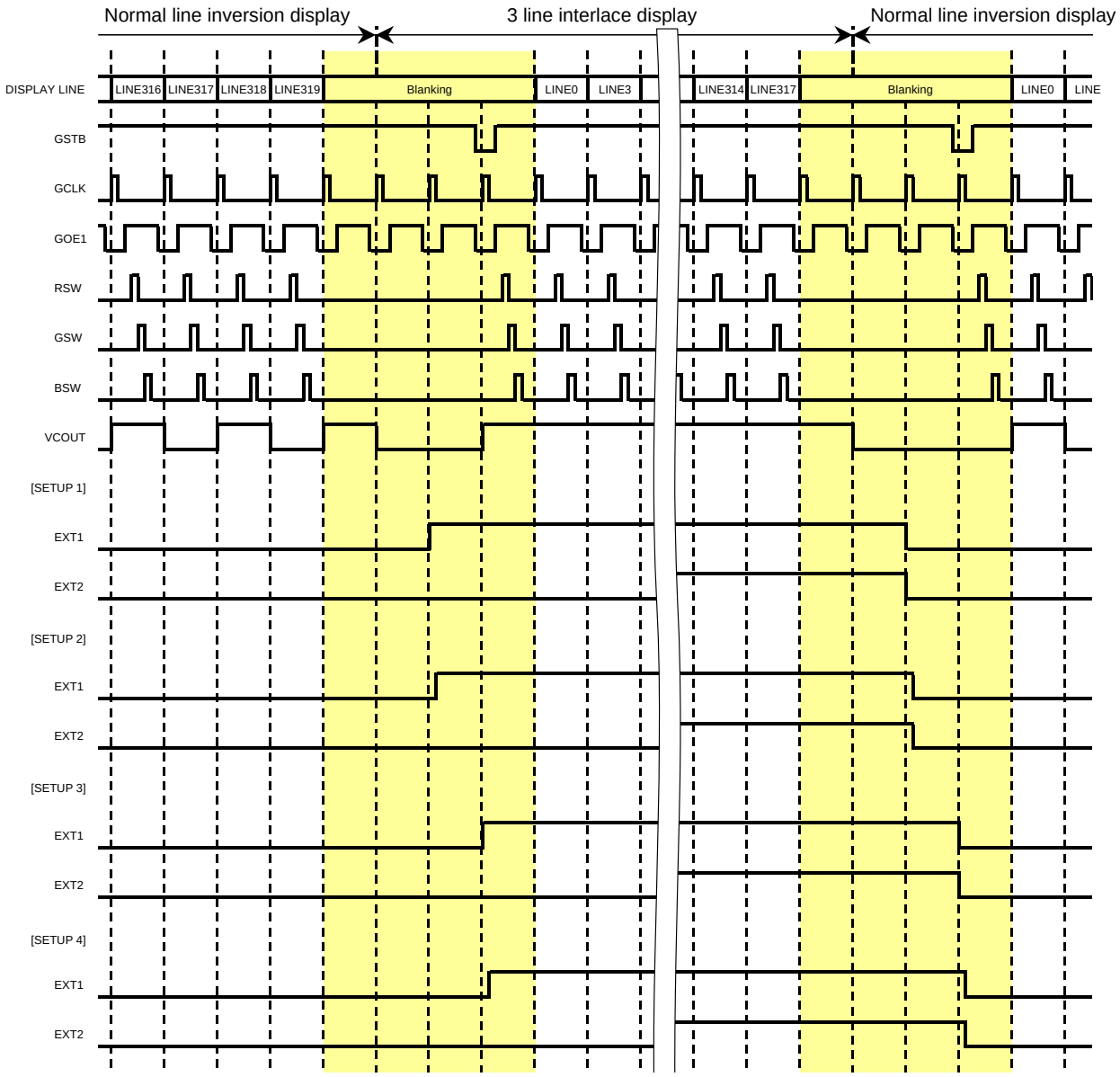


Figure 5–38. Mode change timing (Blanking period = 5 line (ADLNn = 5), the dummy line between the fields = 2 line)

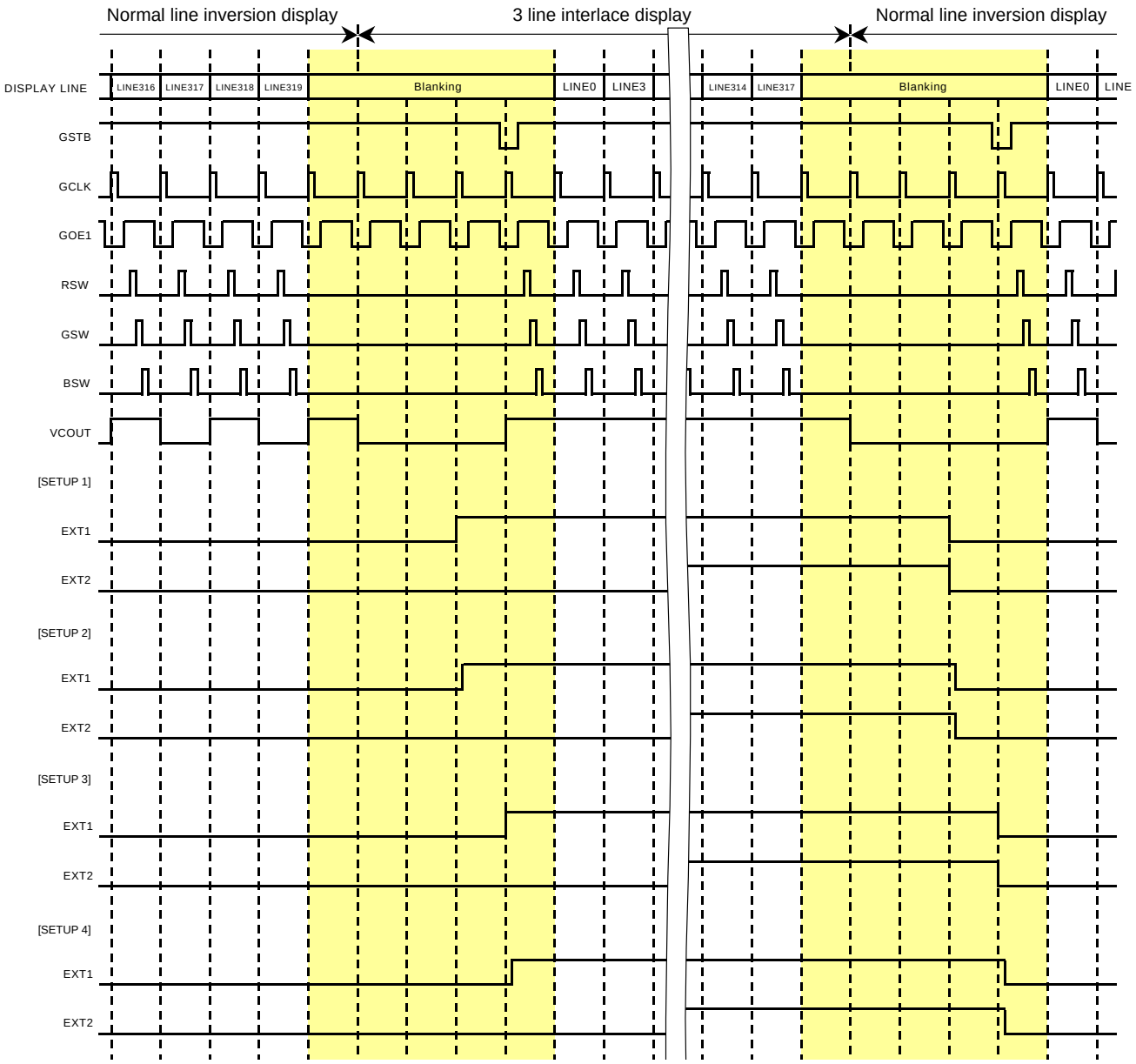
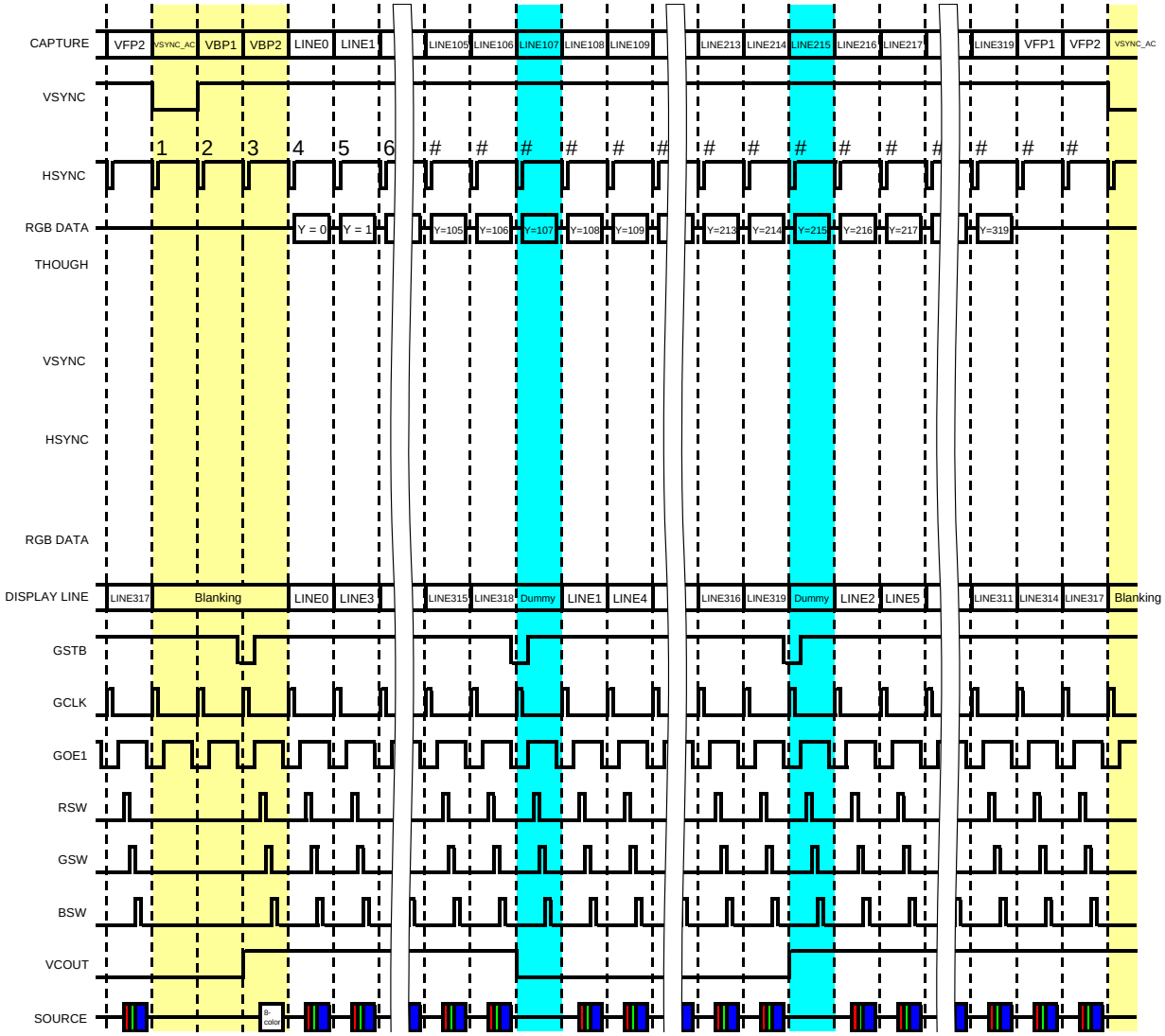


Figure 5–39. RGB interface timing (Blanking period = 3-line, the dummy line between the fields = 1 line)



Remarks 1. Capture mode: VFP = 2, VSYNC_ACT =1, VBP = 2

Through mode: Setting impossible

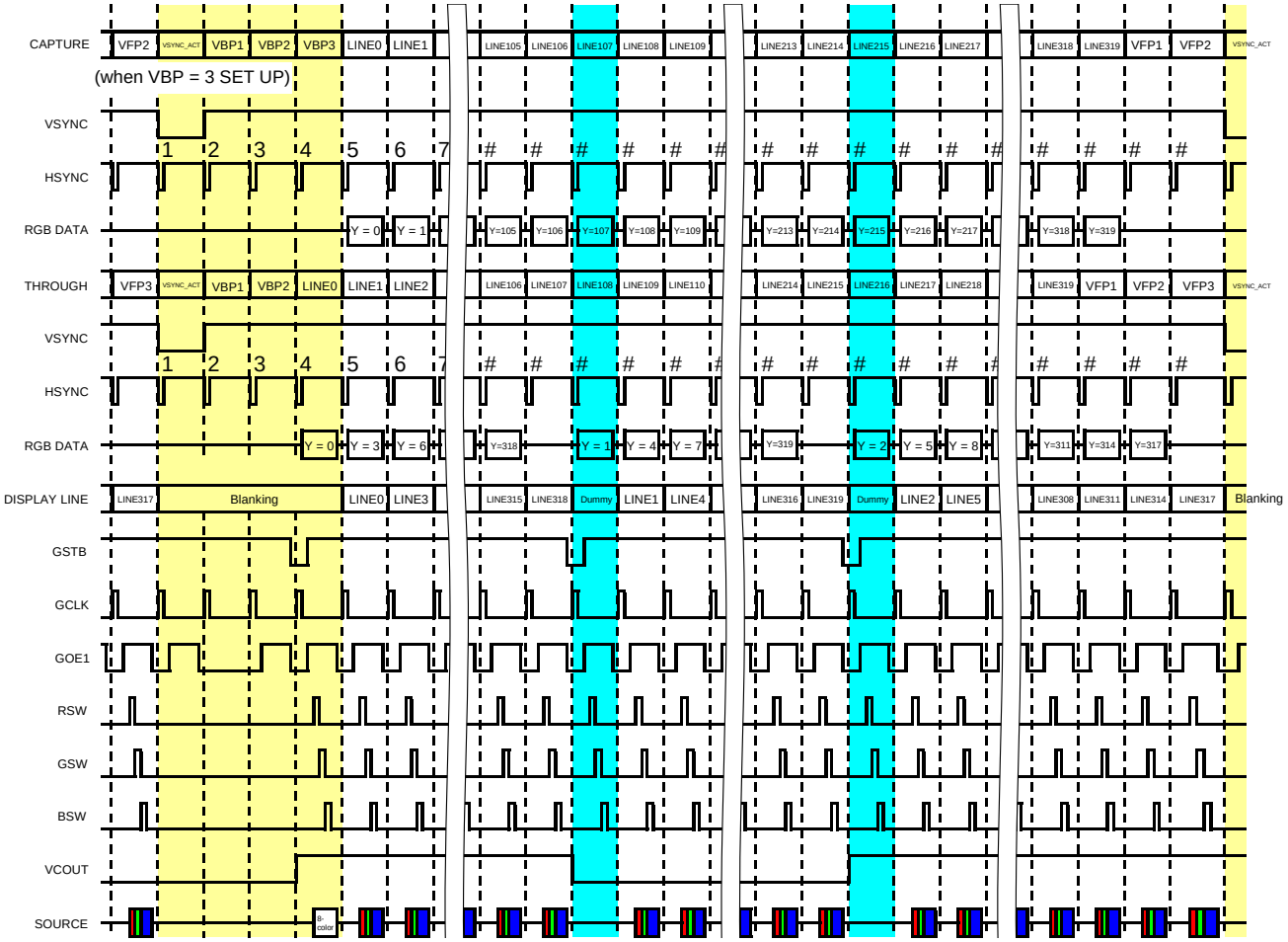
2. VBP is setting by the register.

3. VFP is setting by the number of times of HSYNC input

[VFP] = [the number of times of an 1 frame HSYNC input] – [VSYNC_ACT] – [VBP setting value] – 320

4. VSYNC_ACT (VSYNC active period) needs the input beyond 1H.

Figure 5–40. RGB interface timing (Blanking period = 4 line, the dummy line between the fields = 1 line)



Remarks 1. Capture mode: VFP = 2, VSYNC_ACT = 1, VBP = 3 or VFP = 2, VSYNC_ACT = 2, VBP = 2 or VFP = 3, VSYNC_ACT = 1, VBP = 2

Through mode: VFP = 3, VSYNC_ACT = 1, and VBP = 2

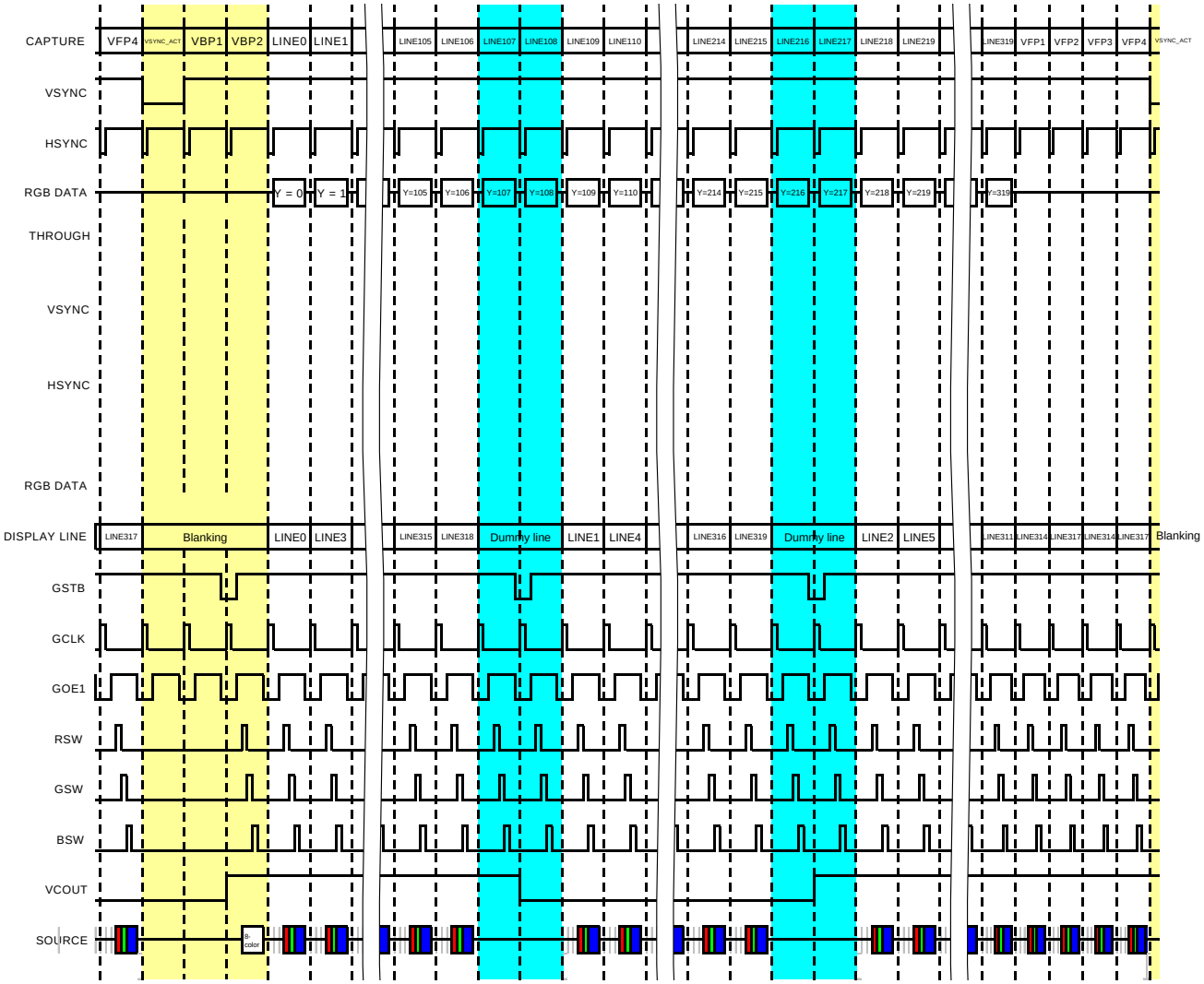
2. VBP is setting by the register.

3. VFP is setting by the number of times of HSYNC input

[VFP] = [the number of times of an 1 frame HSYNC input] – [VSYNC_ACT] – [VBP setting value] – 320

4. VSYNC_ACT (VSYNC active period) needs the input beyond 1H.

Figure 5–41. RGB interface timing (Blanking period = 3-line, the dummy line between the fields = 2 line)



Remarks 1. Capture mode: VFP = 4, VSYNC_ACT = 1, VBP = 2

Through mode: Setting impossible

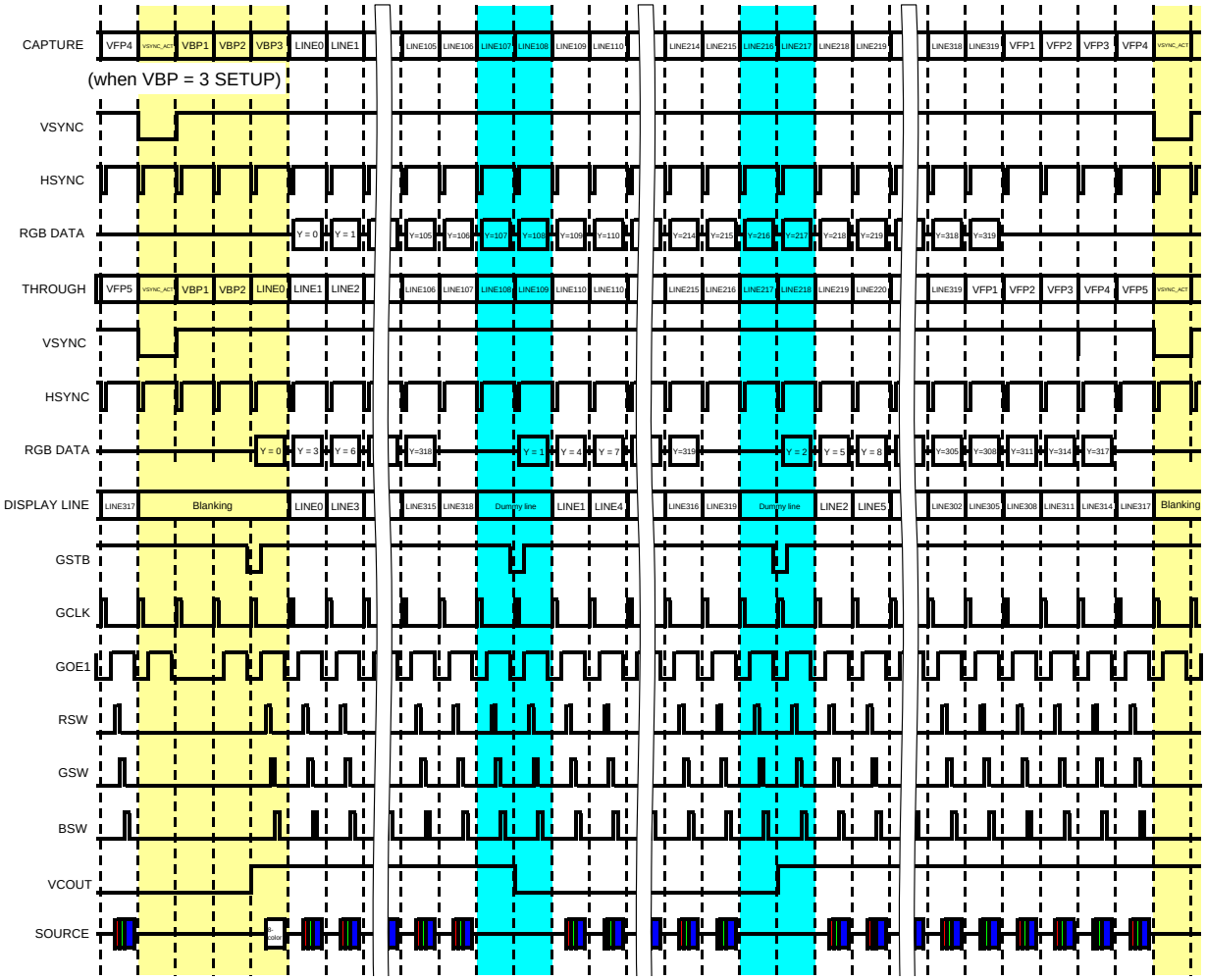
2. VBP is setting by the register.

3. VFP is setting by the number of times of HSYNC input

[VFP] = [the number of times of an 1 frame HSYNC input] – [VSYNC_ACT] – [VBP setting value] – 320

4. VSYNC_ACT (VSYNC active period) needs the input beyond 1H.

Figure 5–42. RGB interface timing (Blanking period = 4 line, the dummy line between the fields = 2 line)



Remarks 1. Capture mode: VFP = 4, VSYNC_ACT = 1, VBP = 3 or VFP = 4, VSYNC_ACT = 2, VBP = 2 or VFP = 5, VSYNC_ACT = 1, VBP = 2

Through mode: VFP = 5, VSYNC_ACT = 1, and VBP = 2

2. VBP is setting by the register.

3. VFP is setting by the number of times of HSYNC input

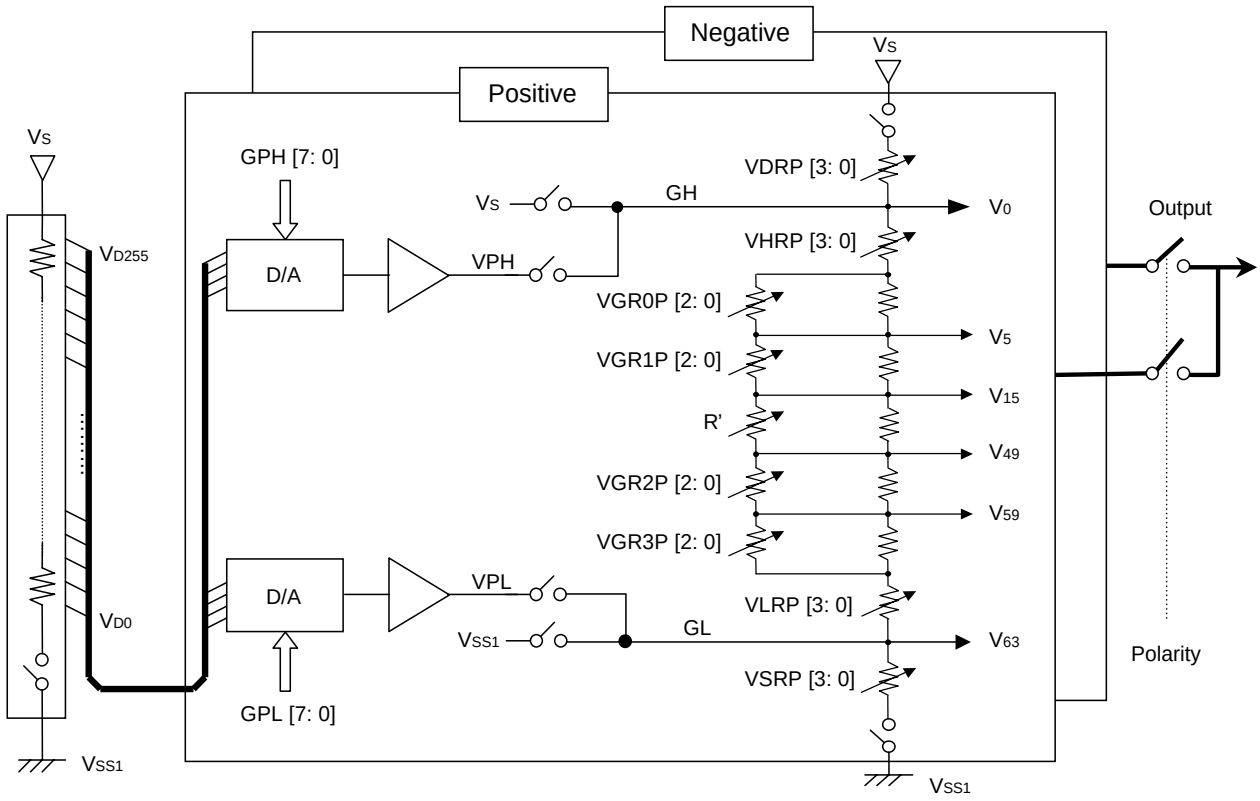
[VFP] = [the number of times of an 1 frame HSYNC input] – [VSYNC_ACT] – [VBP setting value] – 320

4. VSYNC_ACT (VSYNC active period) needs the input beyond 1H.

5.5 γ- Curve Correction Power Supply Circuit

The μPD161802 includes a γ-curve correction power supply circuit. If the internal γ-curve correction matches the LCD characteristics, no external components are necessary. In addition, this circuit can adjust inclination of γ- and amplitude by register setup while building in each γ-correction resistance by the side of a positive polarity and negative polarity.

Figure 5–43. γ- Curve Correction Power Supply Block Diagram
(The following circuit is in each by the side of positive-/negative-polarity)



5.5.1 Amplitude adjustment with internal amplifier

Amplitude adjustment can select two ways, the method of adjusting with internal amplifier, and the method of adjusting by internal resistance. Each register of R44 (GPH [7:0]), R45 (GNH [7:0]), R46 (GPL [7:0]), and R47 (GNL [7:0]) performs adjustment with amplifier. Refer to **Figure 5–44**.

Figure 5–44. Amplitude Adjustment

(This figure is a circuit by the side of positive-polarity. Use GPH reading it as GNH, GPL to GNL, VPH to VNH, and VPL to VNL if negative-polarity side's reading)

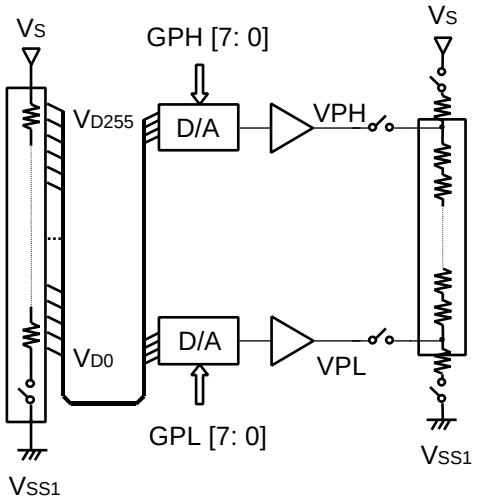
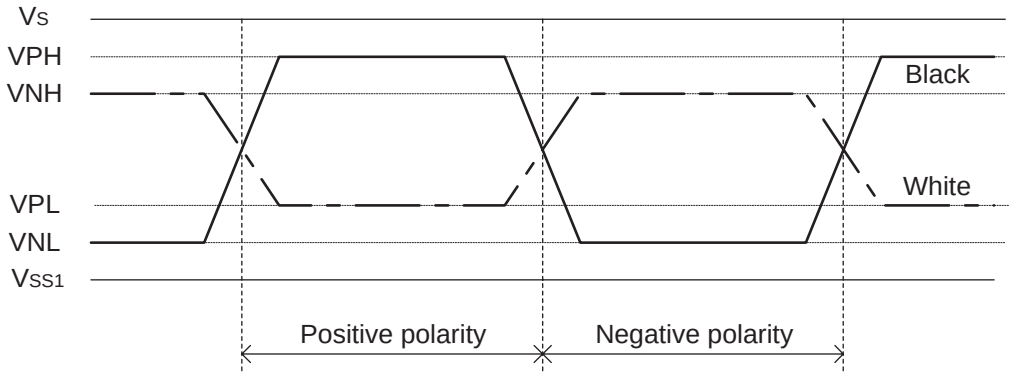


Figure 5–45. Relationship of TFT Drive Voltage (normally white)



	Drive Level	Setting Register	
VPH	Positive polarity, black	Contrast value setting register 1	R44
VNH	Negative polarity, white	Contrast value setting register 2	R45
VPL	Positive polarity, white	Contrast value setting register 3	R46
VNL	Negative polarity, black	Contrast value setting register 4	R47

The value of each amplifier output can be expressed as follows and the value of β can be set as shown in Table 5–9 and 5–10 by using the contrast value registers (R44, R45, R46, and R47)

VNL, VPL, VNH, VPH = (β ÷ 256) x V_S

Caution The usable range in which each output level of VPH, VNH, VPL, and VNL can be set depends on the γ-curve.

Table 5–8. γ- Contrast Value Setting and Electronic Volume Register β Setting 1 (VPH, VNL)

R44	GPH7	GPH6	GPH5	GPH4	GPH3	GPH2	GPH1	GPH0	β value Setting or
R45	GNH7	GNH6	GNH5	GNH4	GNH3	GNH2	GNH1	GNH0	Status Setting
000H	0	0	0	0	0	0	0	0	Fixed to V_S (amplifier OFF)
001H	0	0	0	0	0	0	0	1	255
002H	0	0	0	0	0	0	1	0	254
003H	0	0	0	0	0	0	1	1	253
⋮				⋮					⋮
0FEH	1	1	1	1	1	1	1	0	2
0FFH	1	1	1	1	1	1	1	1	1

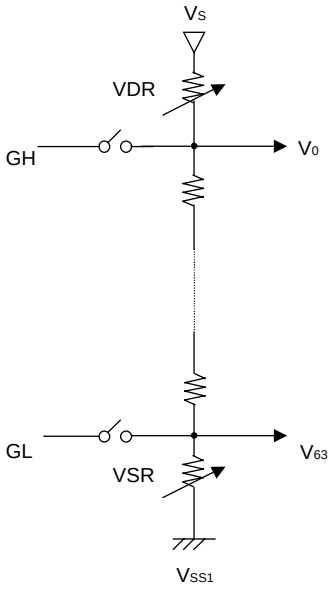
Table 5–9. γ- Contrast Value Setting and Electronic Volume Register β Setting 2 (VPL, VNL)

R46	GPL7	GPL6	GPL5	GPL4	GPL3	GPL2	GPL1	GPL0	β value Setting or
R47	GNL7	GNL6	GNL5	GNL4	GNL3	GNL2	GNL1	GNL0	Statement Setting
000H	0	0	0	0	0	0	0	0	Fixed to V_{SS1} (amplifier OFF)
001H	0	0	0	0	0	0	0	1	1
002H	0	0	0	0	0	0	1	0	2
003H	0	0	0	0	0	0	1	1	3
⋮				⋮					⋮
0FEH	1	1	1	1	1	1	1	0	254
0FFH	1	1	1	1	1	1	1	1	255

5.5.2 Amplitude adjustment by built-in resistance

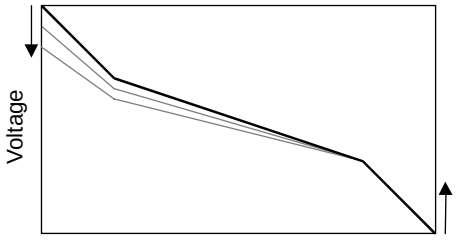
The 4-bit data set as registers R48 and R52 sets amplitude adjustment by built-in resistance. Refer to **Figure 5–46**.

Figure 5–46. Amplitude Adjustment



VDRP [3: 0] (VSRP [3: 0])				VDRP
0	0	0	0	Short (0)
0	0	0	1	4R
0	0	1	0	8R
0	0	1	1	12R
0	1	0	0	16R
0	1	0	1	20R
0	1	1	0	24R
0	1	1	1	28R
1	0	0	0	32R
1	0	0	1	36R
1	0	1	0	40R
1	0	1	1	44R
1	1	0	0	48R
1	1	0	1	52R
1	1	1	0	56R
1	1	1	1	60R

VDRN [3: 0] (VSRN [3: 0])				VDRN
0	0	0	0	Short (0)
0	0	0	1	4R
0	0	1	0	8R
0	0	1	1	12R
0	1	0	0	16R
0	1	0	1	20R
0	1	1	0	24R
0	1	1	1	28R
1	0	0	0	32R
1	0	0	1	36R
1	0	1	0	40R
1	0	1	1	44R
1	1	0	0	48R
1	1	0	1	52R
1	1	1	0	56R
1	1	1	1	60R

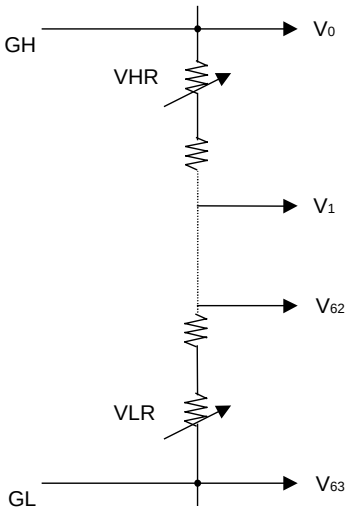


Scale data

5.5.3 Inclination adjustment

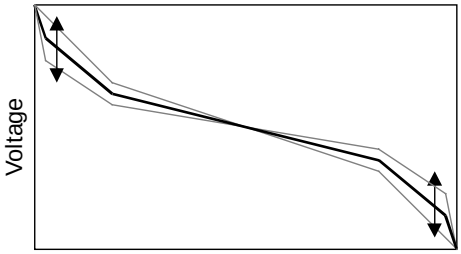
Internal resistance also adjusts inclination adjustment. R49 and R53 registers set adjustment. Refer to **Figure 5–47**.

Figure 5–47. Inclination Adjustment



VHRP [3: 0] (VLRP [3: 0])				VHRP
0	0	0	0	0R
0	0	0	1	4R
0	0	1	0	8R
0	0	1	1	12R
0	1	0	0	16R
0	1	0	1	20R
0	1	1	0	24R
0	1	1	1	28R
1	0	0	0	32R
1	0	0	1	36R
1	0	1	0	40R
1	0	1	1	44R
1	1	0	0	48R
1	1	0	1	52R
1	1	1	0	56R
1	1	1	1	60R

VHRN [3: 0] (VLRN [3: 0])				VHRN
0	0	0	0	0R
0	0	0	1	4R
0	0	1	0	8R
0	0	1	1	12R
0	1	0	0	16R
0	1	0	1	20R
0	1	1	0	24R
0	1	1	1	28R
1	0	0	0	32R
1	0	0	1	36R
1	0	1	0	40R
1	0	1	1	44R
1	1	0	0	48R
1	1	0	1	52R
1	1	1	0	56R
1	1	1	1	60R

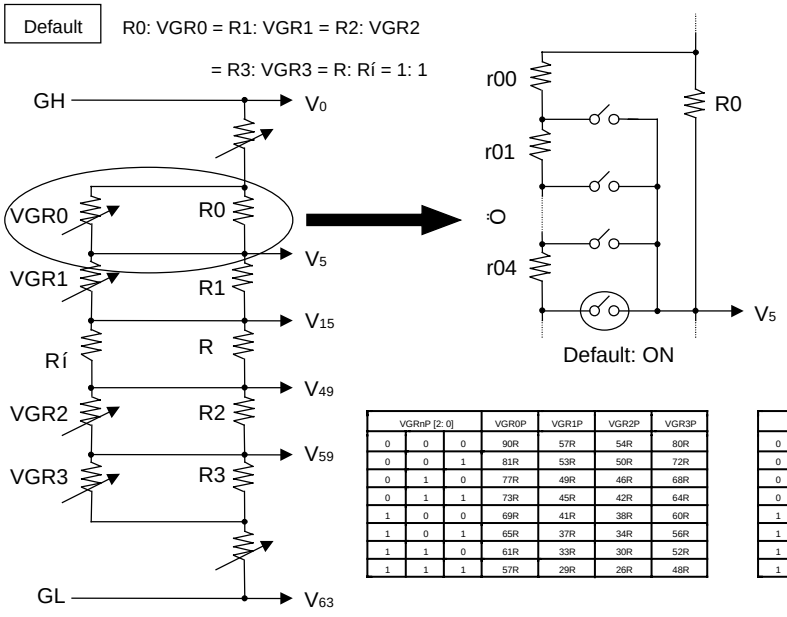


Scale data

5.5.4 Fine tuning adjustment

Internal resistance also sets fine tuning. Please adjust by R50, R51, R54 and R55 register. Refer to **Figure 5–48**.

Figure 5–48. Fine Tuning



VGRnP [2: 0]			VGR0P	VGR1P	VGR2P	VGR3P
0	0	0	90R	57R	54R	80R
0	0	1	81R	53R	50R	72R
0	1	0	77R	49R	46R	68R
0	1	1	73R	45R	42R	64R
1	0	0	69R	41R	38R	60R
1	0	1	65R	37R	34R	56R
1	1	0	61R	33R	30R	52R
1	1	1	57R	29R	26R	48R

VGRnN [2: 0]			VGR0N	VGR1N	VGR2N	VGR3N
0	0	0	80R	54R	57R	90R
0	0	1	72R	50R	53R	81R
0	1	0	68R	46R	49R	77R
0	1	1	64R	42R	45R	73R
1	0	0	60R	38R	41R	69R
1	0	1	56R	34R	37R	65R
1	1	0	52R	30R	33R	61R
1	1	1	48R	26R	29R	57R

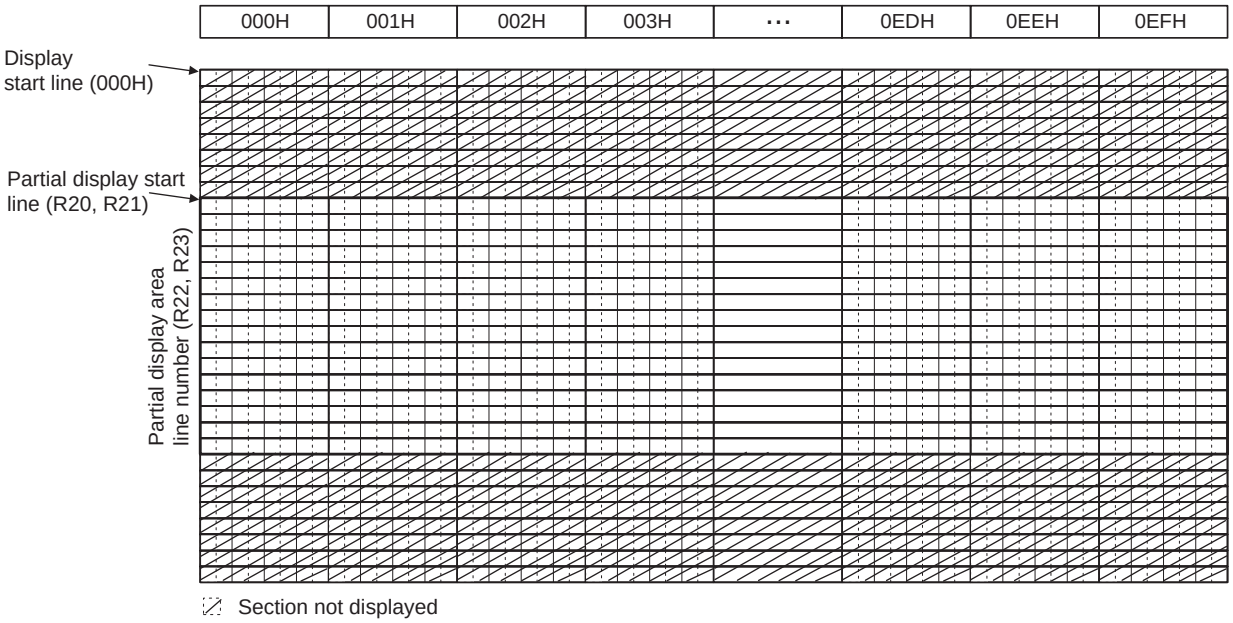
5.6 Partial Display Mode

The μPD161802 is provided with a function that allows sections within the panel to be displayed separately (partial display mode). The start line of the area to be displayed in partial display mode is set using the partial display area start line register (R20, R21), the number of lines in the area to be displayed is set using the partial non-display area line count register (R22, R23), and the color of the area not to be displayed is set using the partial non-display area setting register (R17). If "1" is set in the partial display area line count registers (R22, R23), the partial display areas each become 1 line. If "0" is set, there are no partial display areas but only normal display areas.

The non-display area indicated by R20 and R22 is called Partial 1, and the non-display area indicates by R21 and R23 is called Partial 2. The Partial 2 setting is enabled only when the Partial 1 setting has been performed (when R22 ≠ 0). Therefore, to set only one area as a non-display area, perform only the setting for Partial 1.

Low power consumption cannot be achieved if only the partial mode is set. If low power consumption is required, the mode must be switched to the 8-color mode.

Figure 5–49. Partial Display Mode



Cautions 1. The "scroll step count register (R16)" command is ignored in the partial display mode.

2. The specified partial areas must not directly overlap, and the partial 1 area and partial 2 area must be separated by at least one line. If the areas overlap, only the partial 1 setting are valid, and partial display is not performed for the partial 2 area. In addition, the last line (320 lines: 13FH) and the start line (1 line: 000H) have become continuously in address. Therefore, partial the non-displaying area for 1 line is required also among these lines.

3. When setting the partial display areas, be sure to observe the following relationship.

"000H" ≤ R20 (R21)

R22 (R23) ≤ "13FH"

4. By GSEL (R43:D_4) = 1 setup, it does not become low power consumption in 8-color mode when built-in γ- output adjustment circuit use.

5.6.1 Partial display, non-display area driving

The μPD161802 can select drive of a non-displaying area by setting of PT1, PT0 [R78] and GSM at the time of a partial display as follows.

Table 5–10. Driving Output Pin and State of Driving (1/2)

GSM	PT1	PT0	GOE1	R/G/BSW	Sn		Remark
					Non-display start 2 line	Other non-display line	
0	0	0	Normal output	Normal output	8-color specification color Note	←	Normal partial driving
	0	1	L level fixed	Normal output	8-color specification color Note	←	
	1	0	L level fixed	Normal output	V_{SS}	←	
	1	1	L level fixed	Normal output	8-color white display	Hi-Z	Non-refresh driving 1
1	0	0	L level fixed	Normal output	Hi-Z	Hi-Z	Non-refresh driving 2
	Except above		Prohibited setting				

Note The color specified by PSEL (R17:D_3), and RGR (R17:D_2), PGG (R17:D_1) and PGB (R17:D_0)

Table 5–11. Driving Output Pin and State of Driving (2/2)

GSM	PT1	PT0	OEV	ASW1 to ASW3		Sn		Remark
				Non-display start 2 line	Other non-display line	Non-display start 2 line	Other non-display line	
0	0	0	Normal output	Normal output	Normal output	8-color specification color Note	←	Normal partial driving
	0	1	L level fixed	Normal output	Normal output	8-color specification color Note	←	
	1	0	L level fixed	Normal output	Normal output	V_{SS}	←	
	1	1	L level fixed	Normal output	L level fixed	8-color white display	Hi-Z	Non-refresh driving 1
1	0	0	L level fixed	Normal output	Normal output	Hi-Z	Hi-Z	Non-refresh driving 2
	Except above		Prohibited setting					

Note The color specified by PSEL (R17:D_3), and RGR (R17:D_2), PGG (R17:D_1) and PGB (R17:D_0)

5.6.2 Partial display, non-display area, and normal partial driving

During partial display mode or when GSM = 0, the μPD161802 is set to normal partial drive mode whenever the settings for PT1 and PT0 are anything other than PT1 = 1 and PT0 = 1.

Normal partial drive mode is the output mode for non-display areas set via the PT1 and PT0 bits, and each frame is driven during this mode. When the settings for PT1 and PT0 are anything other than PT1 = 0 and PT0 = 0, the OEV signal is fixed at low level output so the displayed data in the panel's non-display area cannot be overwritten.

Figure 5–50. Normal Partial Driving Waveform (1/2)

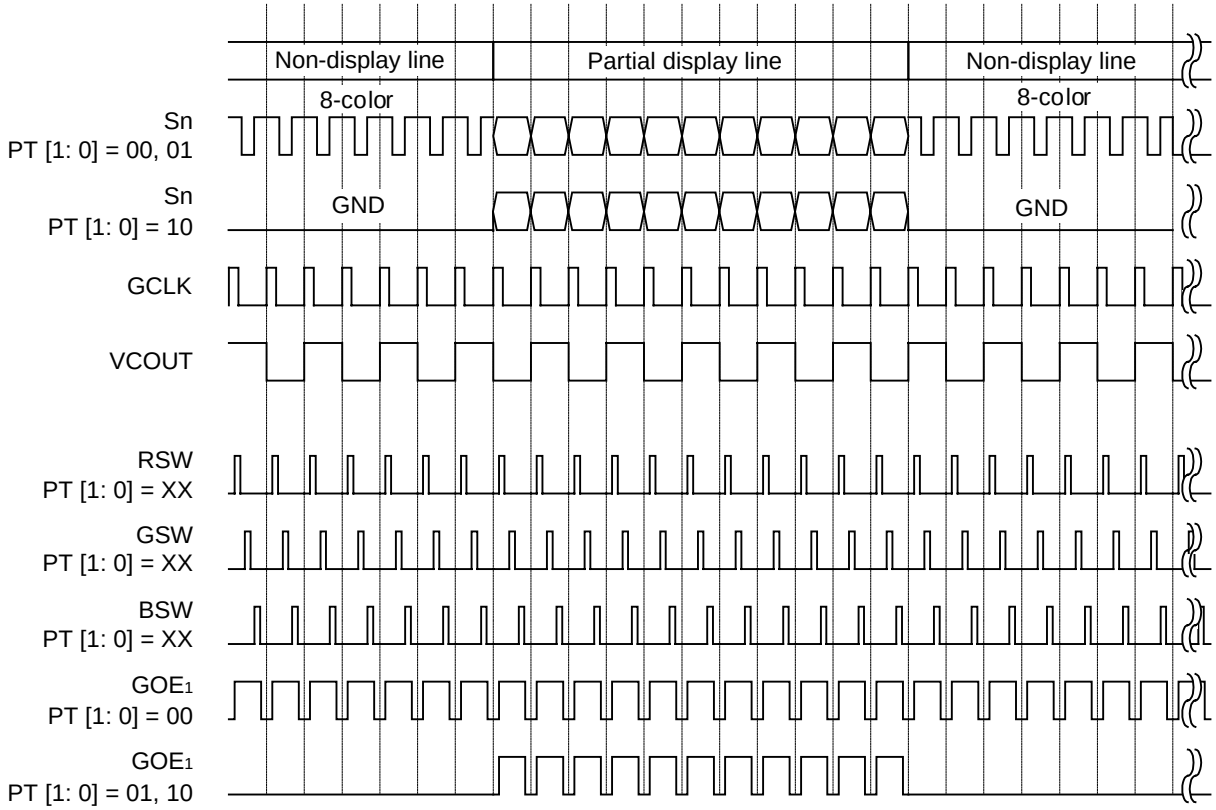
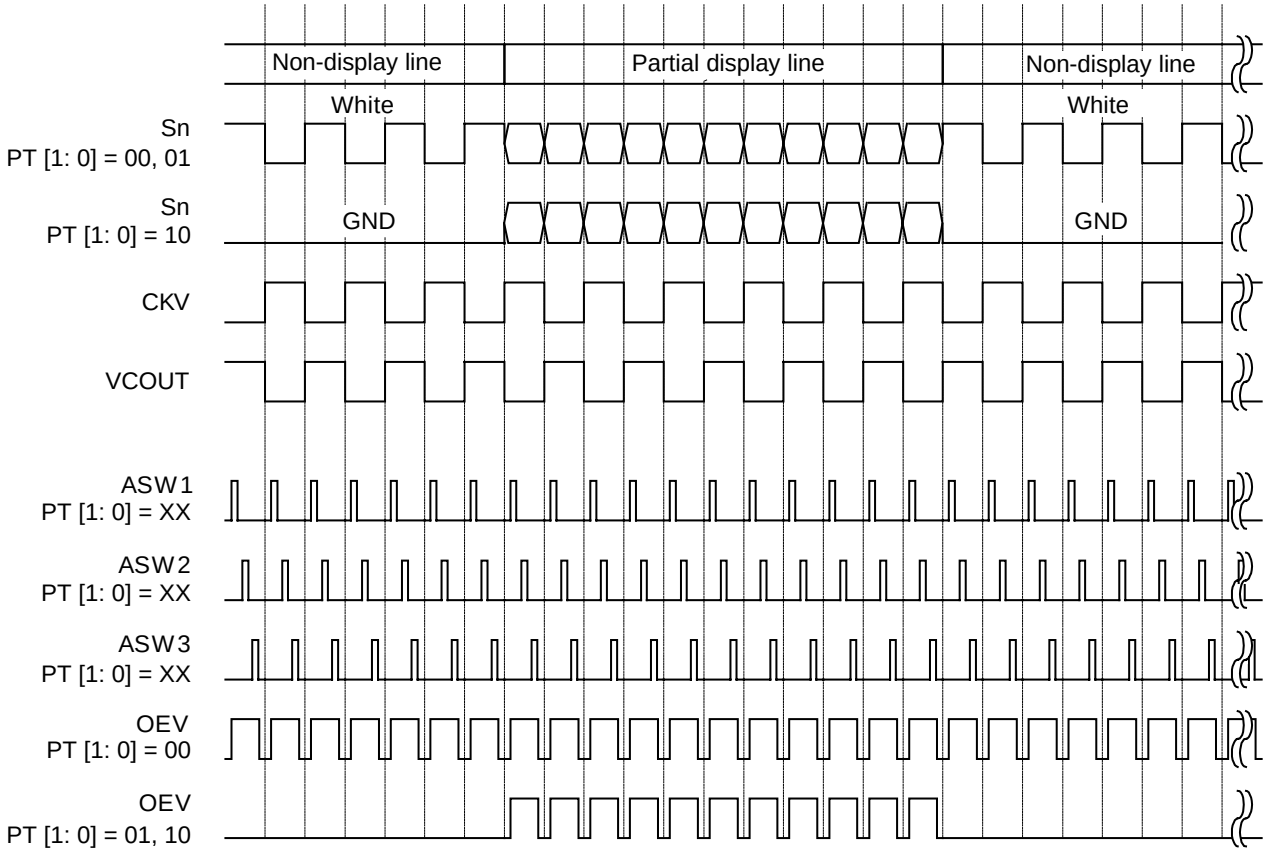


Figure 5–50. Normal Partial Driving Waveform (2/2)



5.6.3 Partial display, non-display area, and non-refresh driving

The μPD161802 can select the non-refreshing drive of a partial a non-displaying area by setting it as GSM = 0, PT1 = 1, PT0 = 1 or GSM = 1, PT1 = 0 and PT0 = 0 at the time of partial display.

This drive is the cycle set up by REFM [2:0] (R68: D_6 to D_4) with REFB [3:0] (R68: D_3 to D_0) in the non-refreshing frame which stops a source output and operation of a gate, and the refreshment frame which carries out a source white level output (normally white panel) and a gate normal scan, and drives partial a non-displaying area.

Figure 5–51. Non-refresh Driving, Frame Cycle Switching Timing

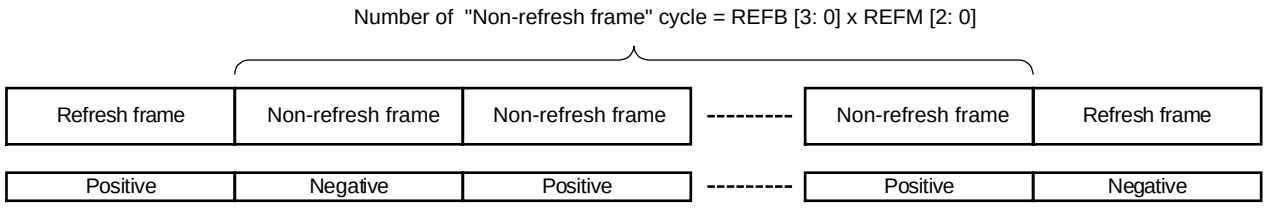


Table 5–12. Non-refresh Driving Frame Basic Cycle

REFB3	REFB2	REFB1	REFB0	Setting Value
0	0	0	0	Only non-refresh driving cycle
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
	⋮			⋮
1	1	1	0	14
1	1	1	1	15

Table 5–13. Non-refresh Driving Frame Basic Cycle Multiple Setting

REFM2	REFM1	REFM0	Setting Value
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

Figure 5–52. Example of Non-refresh Driving Output Waveform (PT1 = 0, PT0 = 0) (1/2)

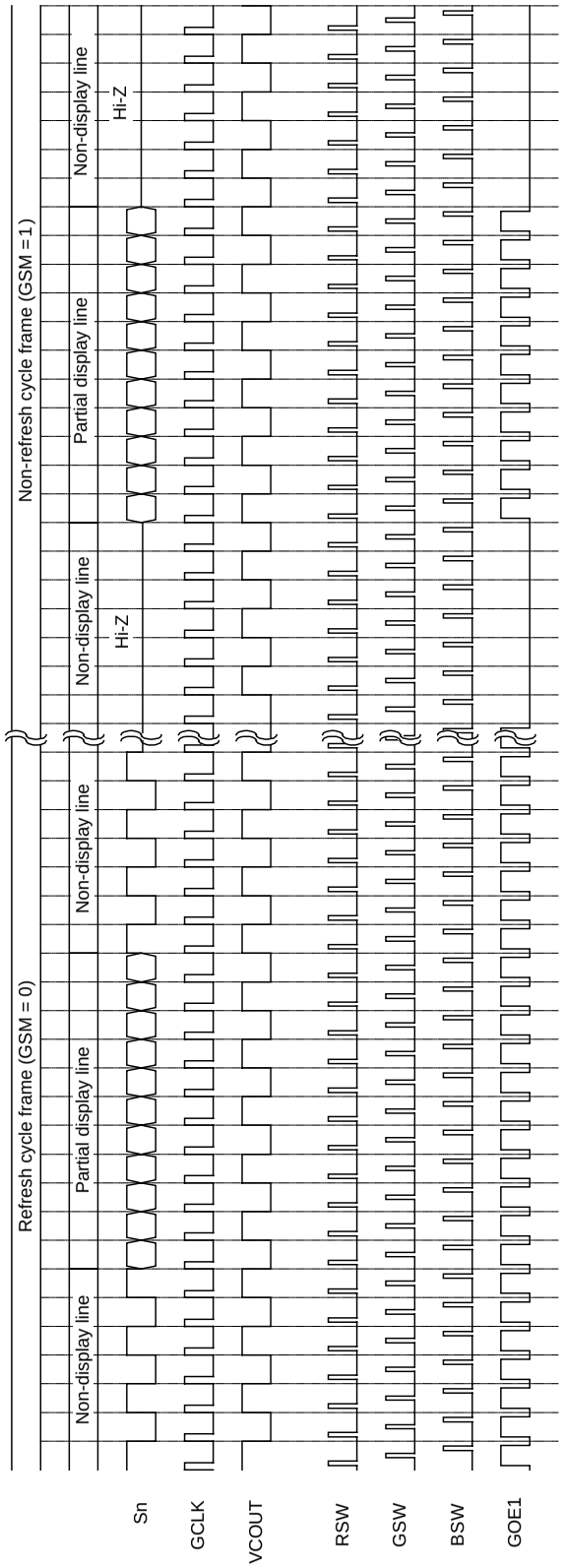


Figure 5–52. Example of Non-refresh Driving Output Waveform (PT1 = 0, PT0 = 0) (2/2)

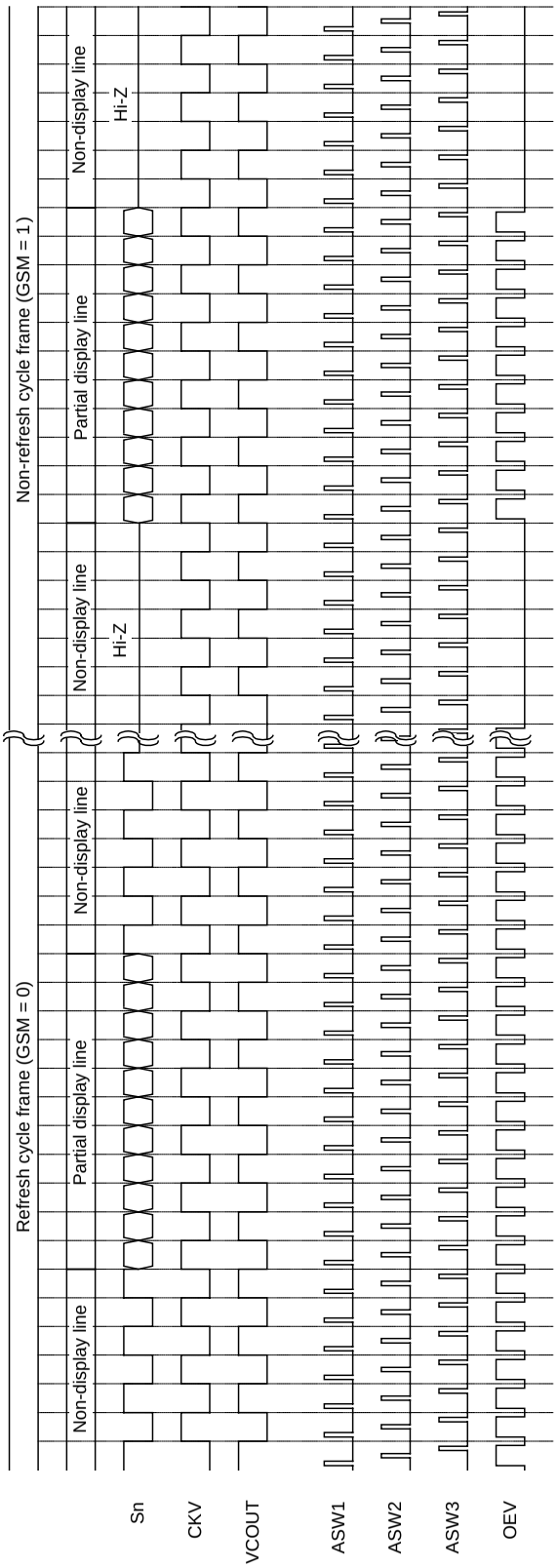


Figure 5–53. Example of Non-refresh Driving Output Waveform (GSM = 0, PT1 = 1, PT0 = 1) (1/2)

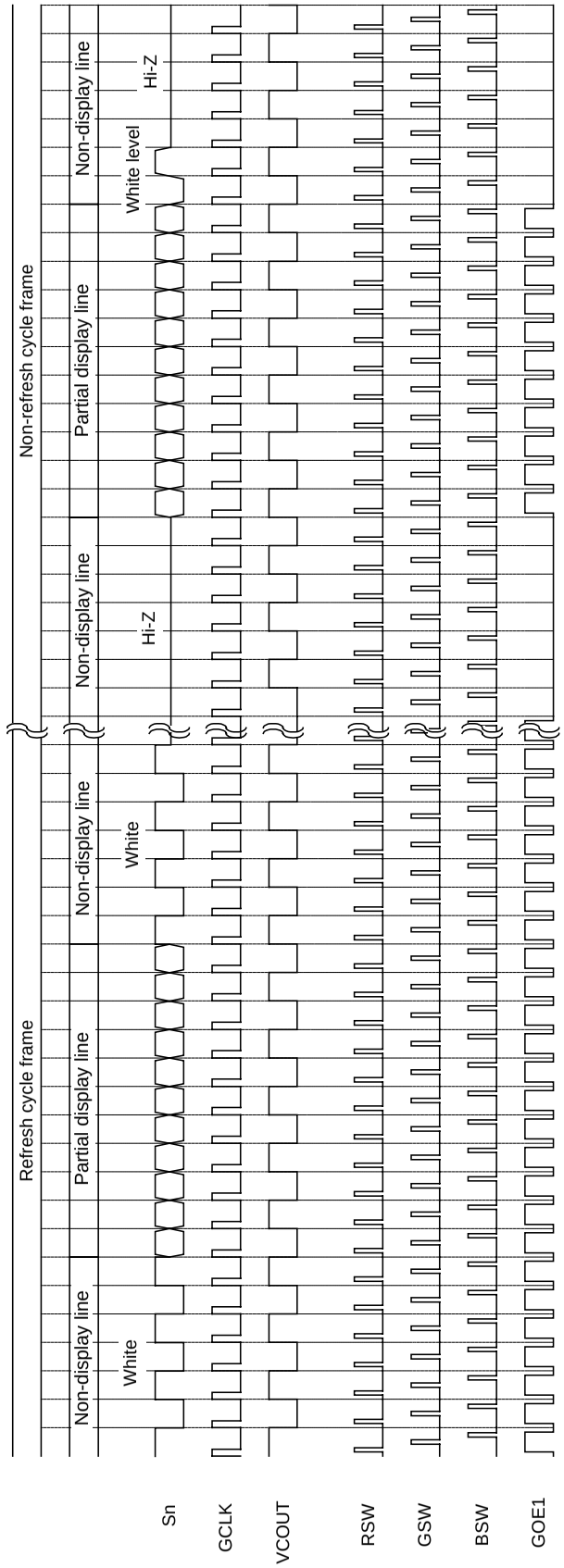
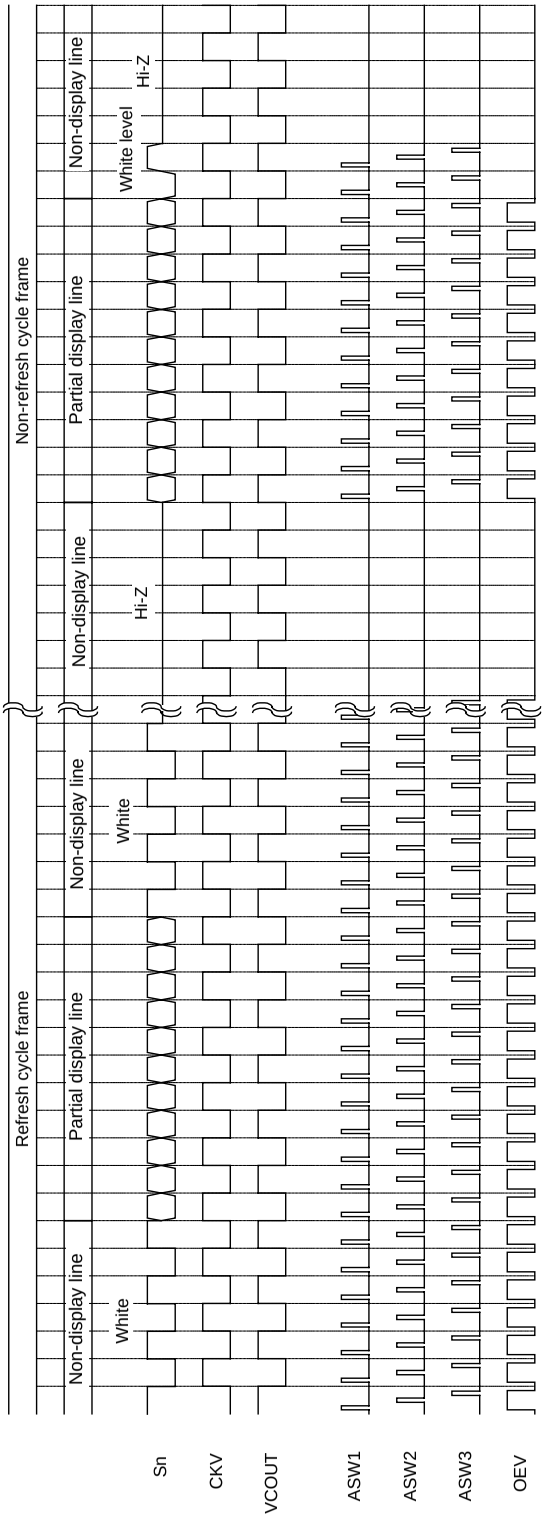


Figure 5–53. Example of Non-refresh Driving Output Waveform (GSM = 0, PT1 = 1, PT0 = 1) (2/2)



The following sequence is recommended to avoid display malfunction when switching from normal display mode to partial display mode and vice versa.

(1) Recommended sequence for switching from normal display mode to partial display mode

DISPn = 1	R0	D_7	<1> Display OFF
↓			
PGX setting	R17	D_2 ⋮ D_0	<2> Partial OFF area color register setting Note1
↓			
Display data overwrite (for partial display)			<3> Display data overwrite Note1
↓			
P1SLn, P2SLn setting	R20, R21	D_7 ⋮ D_0	<4> Partial display area start line setting Note1
↓			
P1AWn, P2AWn setting	R22, R23	D_7 ⋮ D_0	<5> Partial display area line count setting Note1
↓			
DTY = 1, COLOR = 1	R0	D_4, D_2	<6> Partial display mode, 8-color mode Note2
↓			
DISPn = 0	R0	D_7	<7> Display ON

Notes 1. <2> to <5> can be executed in any order.

2. <6> must be executed after <4> and <5> have been set.

(2) Recommended sequence for switching from partial display mode to normal display mode

DISPn = 1	R0	D_7	<1> Display OFF
↓			
Display data overwrite (for normal display)			<2> Display data overwrite [Note]
↓			
DTY = 0, COLOR = 0	R0	D_4, D_2	<3> Normal display mode, 260,000-color mode [Note]
↓			
DISPn = 0	R0	D_7	<4> Display ON

Note <2> to <3> can be executed in any order.

(3) Recommended sequence for switching from partial display mode to partial display mode (switching the partial display area)

DISPn = 1	R0	D_7	<1> Display OFF
↓			
(Display data overwrite)			<2> Display data overwrite [Note1, 2]
↓			
P1SLn, P2SLn setting	R20, R21	D_7 ⋮ D_0	<3> Partial display area start line setting [Note1]
↓			
P1AWn, P2AWn setting	R22, R23	D_7 ⋮ D_0	<4> Partial display area line count setting [Note1]
↓			
DTY = 1	R0	D_4	<5> Partial display mode [Note3]
↓			
DISPn = 0	R0	D_7	<6> Display ON

Notes 1. <2> to <4> can be executed in any order.

2. Execute <2> only when necessary.

3. <5> must be executed after <3> and <4> have been set.

(4) Partial display setting examples

Setting A-1

Register	Setting Value	Details of Setting Value
Partial display area start line register (R20, R21)	000H	Specifies Y address 000H
Partial display area line count register (R22, R23)	09FH	Sets an area of 160 lines

Setting A-2

Register	Setting Value	Details of Setting Value
Partial display area start line register (R20, R21)	0A0H	Specifies Y address 0A0H
Partial display area line count register (R22, R23)	09FH	Sets an area of 160 lines

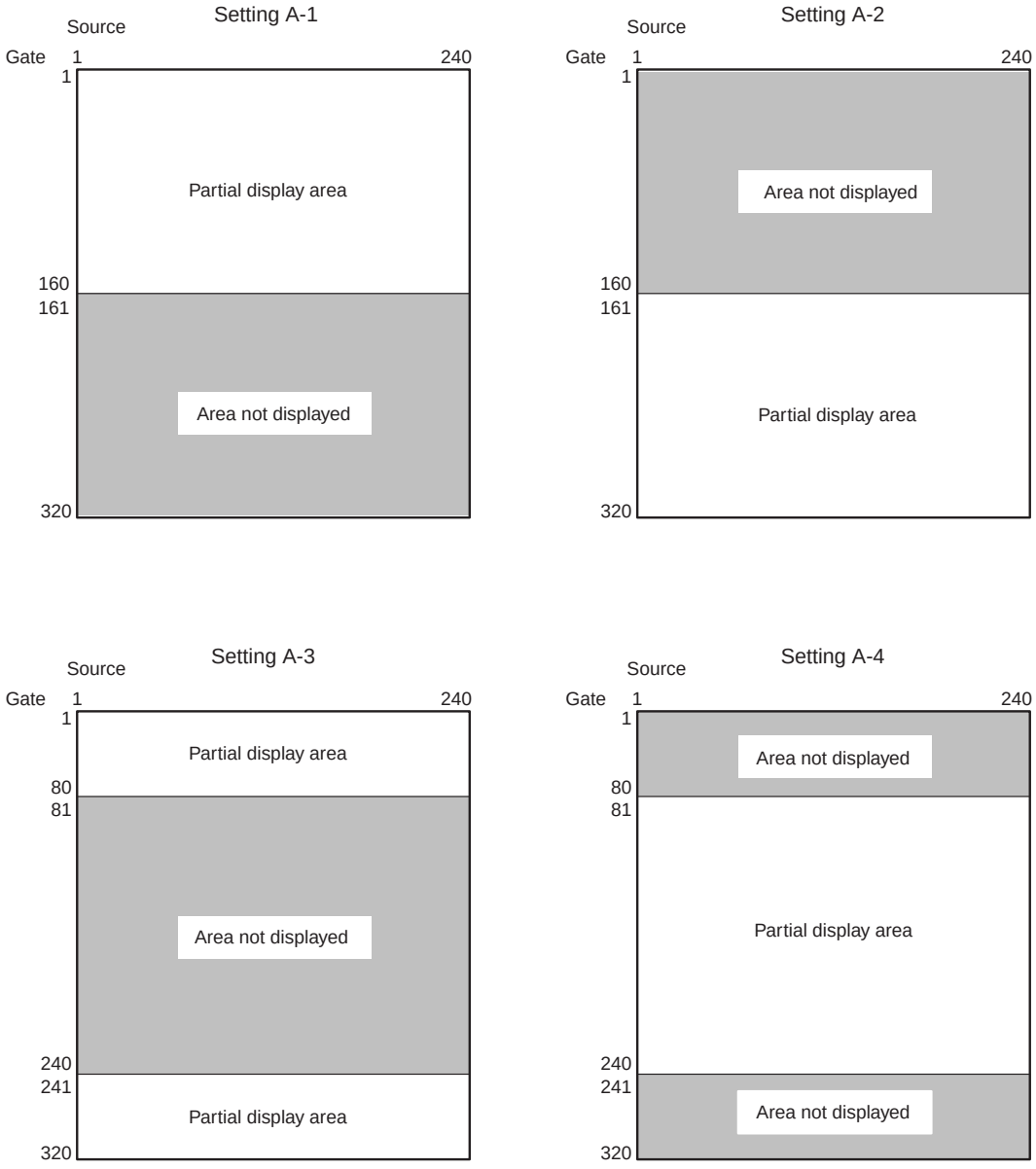
Setting A-3

Register	Setting Value	Details of Setting Value
Partial display area start line register (R20, R21)	0EFH	Specifies Y address 0EFH
Partial display area line count register (R22, R23)	09FH	Sets an area of 160 lines

Setting A-4

Register	Setting Value	Details of Setting Value
Partial display area start line register (R20, R21)	050H	Specifies Y address 050H
Partial display area line count register (R22, R23)	09FH	Sets an area of 160 lines

Figure 5–54. Partial Display Setting



5.7 Panel Scroll

The μPD161802 has a panel scroll function. Any area of the panel can be scrolled by using the scroll area start line register (R14), scroll area line count register (R15), and scroll step count register (R16) to set the Y address of the top line of the area to be scrolled, the count of lines of the area to be scrolled, and the scroll step number, respectively.

Note that in partial mode, the panel scroll function is disabled.

Table 5–14. Scroll Area Start Line Register (R14)

SSL8	SSL7	SSL6	SSL5	SSL4	SSL3	SSL2	SSL1	SSL0	Start Line Y Address
0	0	0	0	0	0	0	0	0	000H
0	0	0	0	0	0	0	0	1	001H
0	0	0	0	0	0	0	1	0	002H
0	0	0	0	0	0	0	1	1	003H
				↓					↓
1	0	0	1	1	1	1	0	1	13DH
1	0	0	1	1	1	1	1	0	13EH
1	0	0	1	1	1	1	1	1	13FH

Table 5–15. Scroll Area Line Count Register (R15)

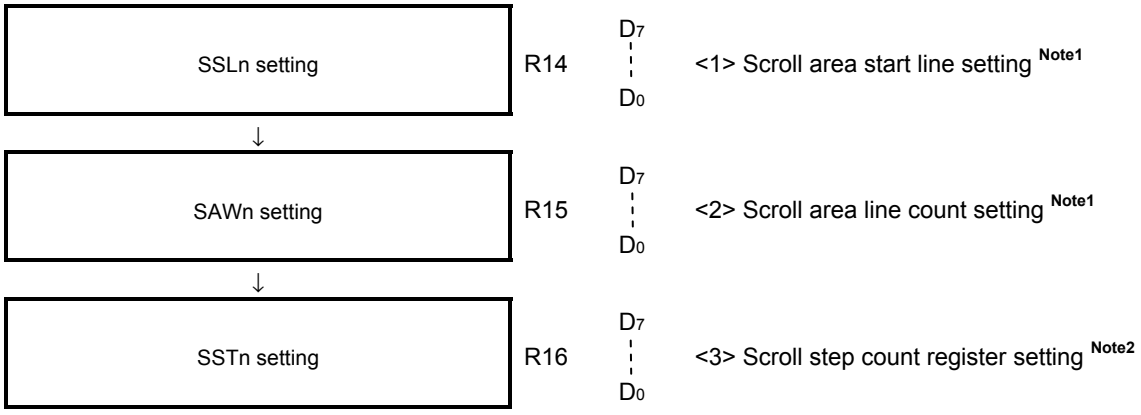
SAW8	SAW7	SAW6	SAW5	SAW4	SAW3	SAW2	SAW1	SAW0	Scroll Area Line Number
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	0	1	1	4
				↓					↓
1	0	0	1	1	1	1	0	1	318
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1	1	320

Table 5–16. Scroll Step Count Register (R16)

SST8	SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0	Scroll Area Line Number
0	0	0	0	0	0	0	0	0	0 (No scroll)
0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	1	1	3
				↓					↓
1	0	0	1	1	1	1	0	1	317
1	0	0	1	1	1	1	1	0	318
1	0	0	1	1	1	1	1	1	319

Scrolling must be set using the following sequence.

(1) Recommended scroll sequence



Notes 1. <1> to <2> can be executed in any order.

2. <3> must be executed after <1> and <2> have been set.

Remark Set SSTn to 000H to disable the scroll operation. No particular sequence is required for this.

Cautions 1. If the sum of the values of SSLn and SAWn is 320 (13FH) or over, it is invalid (no scroll operation).

2. Set the step number SSTn so that it does not exceed the line number SAWn. If a value exceeding SAWn is set, it will be invalid (no scroll operation).

(2) Scroll setting examples

Setting A-1

Register	Setting Value	Details of Setting Value
Scroll area start line register (R14)	000H	Sets Y address 000H
Scroll area line count register (R15)	13FH	Sets an area of 320 lines

Setting A-2

Register	Setting Value	Details of Setting Value
Scroll area start line register (R14)	000H	Sets Y address 000H
Scroll area line count register (R15)	09FH	Sets an area of 160 lines

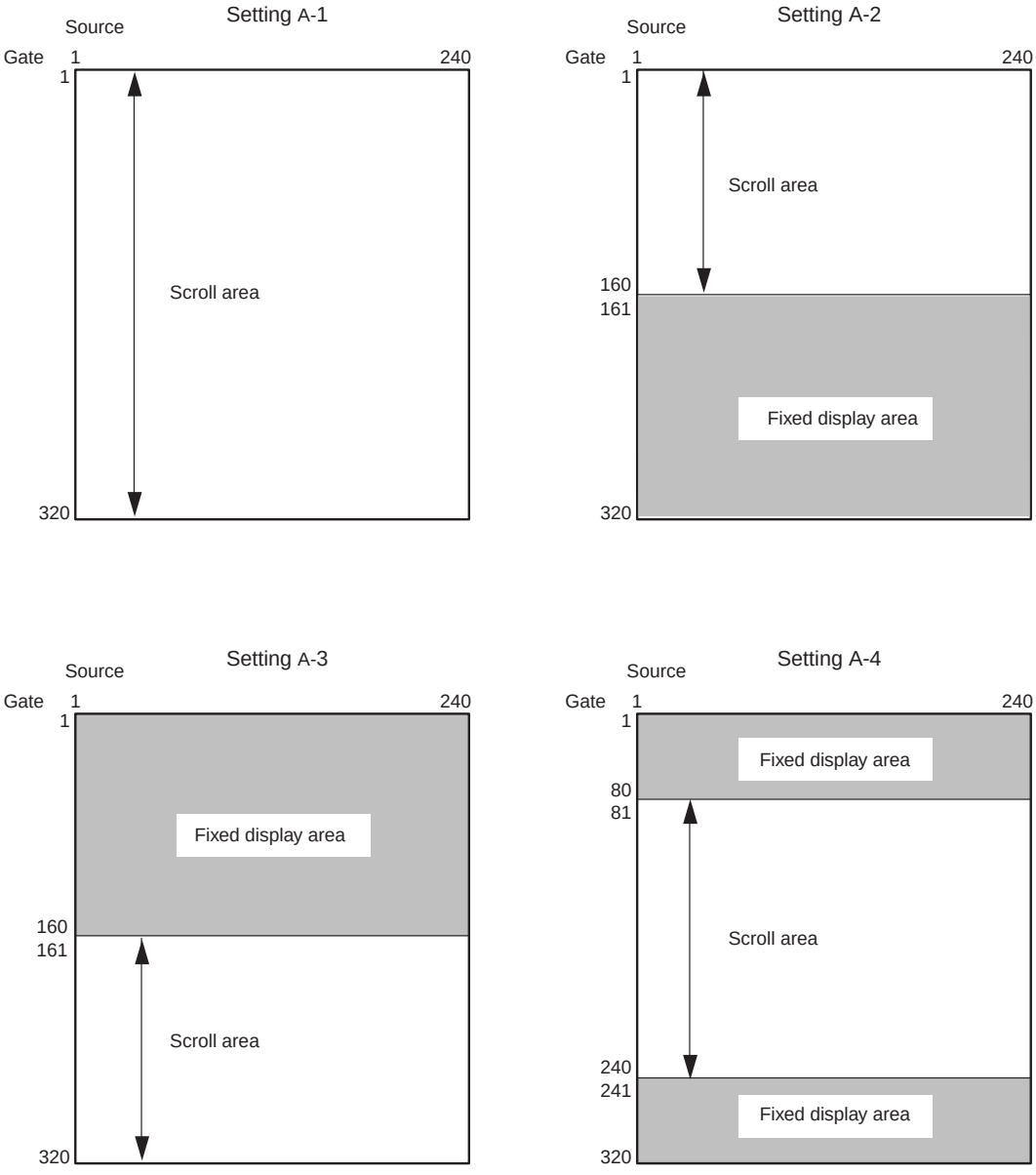
Setting A-3

Register	Setting Value	Details of Setting Value
Scroll area start line register (R14)	0A0H	Sets Y address 0A0H
Scroll area line count register (R15)	09FH	Sets an area of 160 lines

Setting A-4

Register	Setting Value	Details of Setting Value
Scroll area start line register (R14)	050H	Sets Y address 050H
Scroll area line count register (R15)	09FH	Sets an area of 160 lines

Figure 5–55. Display Scroll Setting



(3) Scroll setting flowchart example

Start

↓

Scroll area start line register setting (R14)

RS	D_{15} / D_7							D_8 / D_0
L	X	0	0	0	1	1	1	1
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_7 to D_0 are the data for scroll area start line.

↓

Scroll area line count register setting (R15)

RS	D_{15} / D_7							D_8 / D_0
L	X	0	0	1	0	0	0	0
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_7 to D_0 are the data for scroll area line count.

↓

Scroll step count register setting (1 step) (R16)

RS	D_{15} / D_7							D_8 / D_0
L	X	0	0	1	0	0	0	1
	0	0	0	0	0	0	0	1

↓

X address register (R6)

RS	D_{15} / D_7							D_8 / D_0
L	X	0	0	0	0	1	1	0
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_7 to D_0 depend on application condition.

↓

Y address register assignment (R7)

RS	D_{15} / D_7							D_8 / D_0
L	X	0	0	0	0	1	1	1
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_7 to D_0 depend on application condition.

↓

Display data Re-write scrolling area 1 (Start)

RS	D_{15} / D_7							D_8 / D_0
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} to D_0 are display memory data.

↓

Display data Re-write scrolling area 2

RS	D_{15} / D_7							D_8 / D_0
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} to D_0 are display memory data.

↓
↓
↓

Display data Re-write scrolling area n (End)

RS	D_{15} / D_7							D_8 / D_0
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} to D_0 are display memory data.

↓

↓

Scroll step count register setting (2 steps) — R16

RS	D15 / D7							D8 / D0
L	X	0	0	1	0	0	1	0
	0	0	0	0	0	0	0	1

↓

X address register — R6

RS	D15 / D7							D8 / D0
L	X	0	0	0	0	1	1	0
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_7 **to** D_0 **depend on application condition.**

↓

Y address register assignment — R7

RS	D15 / D7							D8 / D0
L	X	0	0	0	0	1	1	1
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_7 **to** D_0 **depend on application condition.**

↓

Display data Re-write scrolling area 1 (Start)

RS	D15 / D7							D8 / D0
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} **to** D_0 **are display memory data.**

↓

Display data Re-write scrolling area 2

RS	D15 / D7							D8 / D0
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} **to** D_0 **are display memory data.**

↓
↓
↓

Display data Re-write scrolling area n (End)

RS	D15 / D7							D8 / D0
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} **to** D_0 **are display memory data.**

(Repeat)

↓
↓
↓

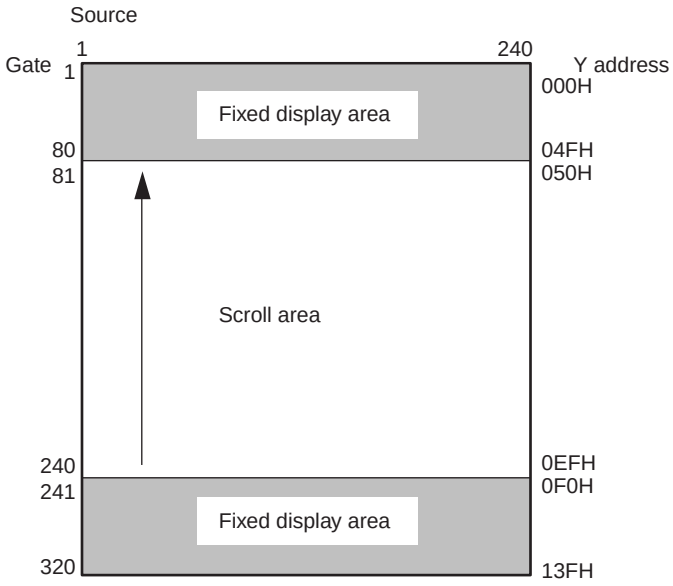
Next transaction

(4) Scroll function example

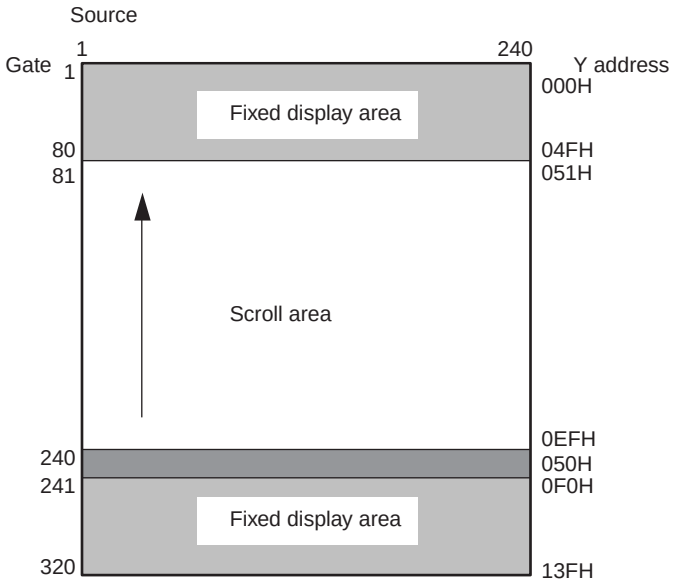
Scroll area start line register (R14): 03CH

Scroll area line count register (R15): 077H

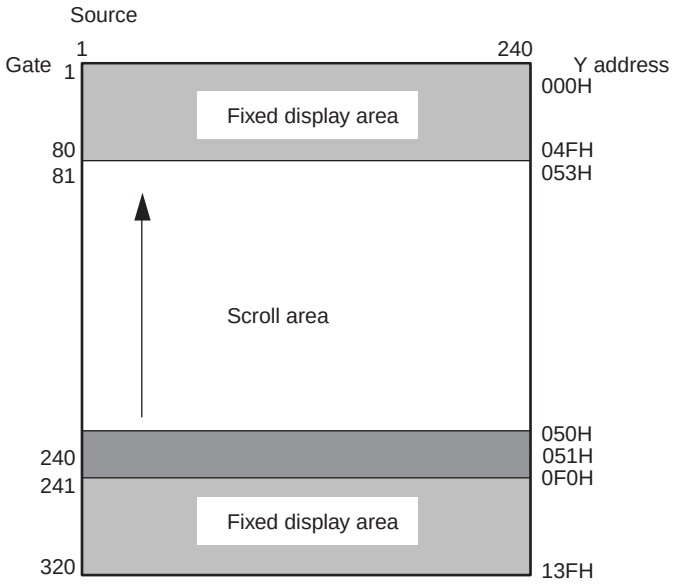
(a) Scroll step count register setting (R16): 000H



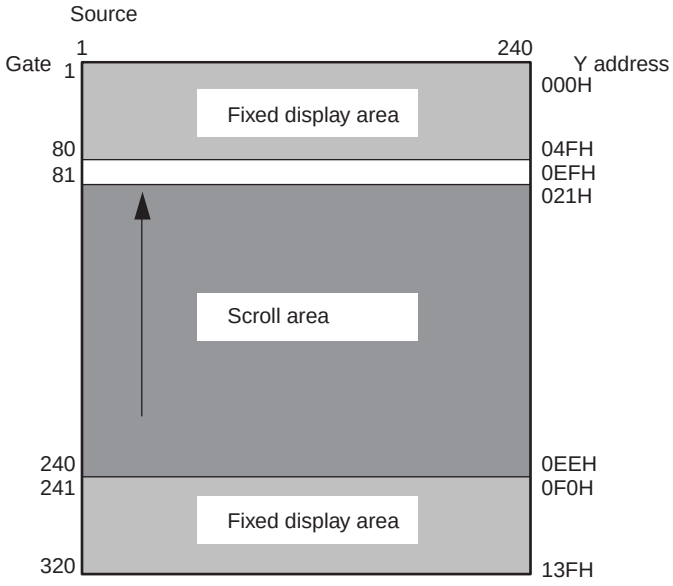
(b) Scroll step count register setting (R16): 001H



(c) Scroll step count register setting (R16): 002H



(d) Scroll step count register setting (R16): 076H

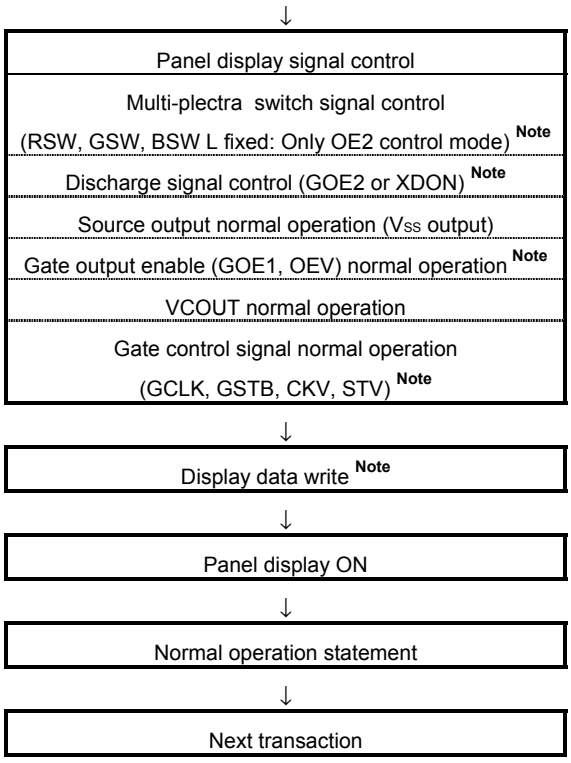


5.8 Power Supply Sequence

The power ON supply sequence of the μPD161802 recommends the sequence shown below.

Power ON	
↓	
WAIT	Power supply voltage stable time
↓	
Hard reset (/RESET ”L” pulse input)	
↓	
RAM address offset	RMODS (R2) = “1”
	By hard reset, the initial value is "0". When using it by "0" setup, it is not necessary to perform this processing.
↓	
Command reset	CRES (R3) = “1”
	All register setup except R2 is to a default state.
↓	
Stand-by mode	
↓	
SRAM power ON	R78 RMST [1:0] = 1, 0
↓	
WAIT time (10 ms)	SRAM power supply rising wait time
	It is SRAM power supply circuit rising wait time with built-in IC.
↓	
Display RAM data output "0" data mask release	R78 RMMSK = ”1”
↓	
Sleep mode state	Display OFF, oscillation stop, logic power supply ON, SRAM power supply ON
↓	
Oscillator circuit operation start	R1 OSC2OFF = ”0”
↓	
Power supply IC control (power supply ON)	R38 to R42, R60 to R65
	(Sequence changes with use power supply IC. Refer to the specifications of the power supply IC currently used.)
↓	
WAIT time Note	Power supply rising wait time
	It is the power supply rising wait time of the power supply IC to "Display ON".
↓	

Note Set up the control system register flag of the signal actually used on a panel.



Note Set up the control system register flag of the signal actually used on a panel.

5.9 Stand-by Power Supply OFF Sequence

The stand-by power supply OFF sequence is described below.

5.9.1 Stand-by controlled by STBY flag

The μPD161802 has a stand-by function. When the STBY bit of the control register 1 (R0) is set to 1 while changing the total output of a gate into an ON state in the dummy period of one frame, it is outputted to V_{SS}, and VCOUTn is outputted to V_{SS}, and discharge of the electric charge of a panel is carried out. After the output of gate is in ON state, automatically stopping oscillator (OSC2OFF = 1), regulator OFF for the μPD161802, DC/DC converter OFF (DCON control) and display RAM power supply OFF become perfect stand-by mode.

In addition, this function is valid only when the timing circuit 1 is chosen.

As for control of power supply IC, it is possible to use and control the serial interface pin for control for power supply IC (PCS, PCL and PDA). For details, refer to the specifications of IC used about the OFF sequence/ON sequence of power supply IC.

(1) Stand-by sequence

R0 of STBY bit = 1

↓

(WAIT in one frame period)

↓

Power supply IC control (controlling by serial interface for power supply IC control)

(regulator OFF, DC/DC converter OFF)

↓

OSC display stop OSC2OFF = 1 setting

↓

Sleep mode state

↓

Display RAM power supply OFF

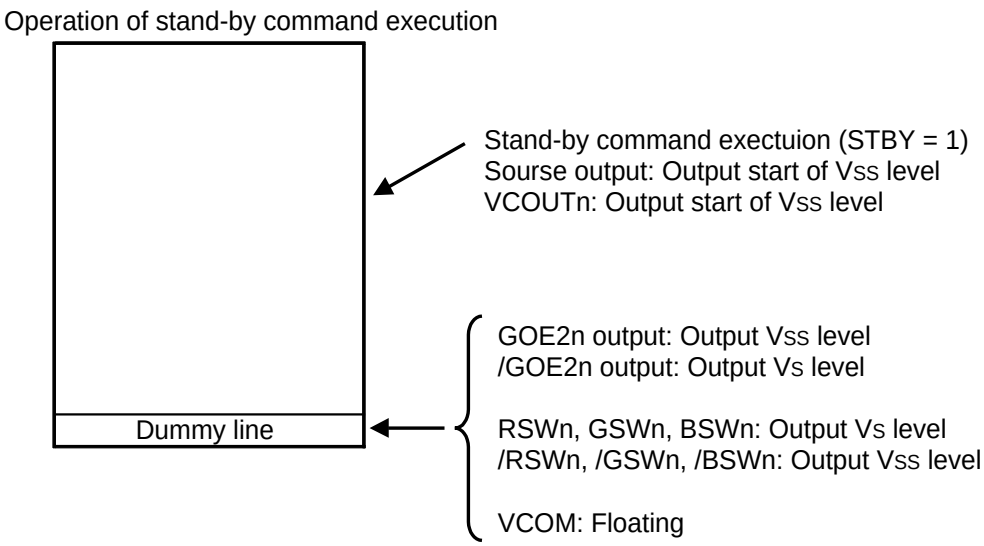
RAMMSK = 0 (R78:D_6)

RMST [1:0] = 00 (R78:D_5, D_4)

↓

Stand-by statement

Figure 5–56. Outline of Operation at the Time of Stand-by Execution



(2) Stand-by release sequence

In case of transfer normal mode from stand-by mode, against stand-by sequence, it executes in order.

Under stand-by

↓

Display RAM power supply ON

RMST [1:0] = 10 (R78:D_5, D_4)

↓

(Display RAM power supply rising WAIT time)

↓

Display RAM data mask release

RAMMSK = 1 (R78:D_6)

↓

OSC display oscillation start

OSC2OFF = “0”

↓

Power supply IC control (controlling by serial interface for power supply IC control)

(regulator ON, DC/DC converter ON)

↓

(power ON rising WAIT time)

↓

STBY = 0

5.9.2 Standby-by command input control

When VSTBY = low (power supply to V_{DD1} and V_{DD2} is from internal regulator), the μPD161802 can be freely switched (via input of a mode selection command) from the normal operation mode shown in Figure 5–48 to sleep mode, deep sleep mode, or stand-by mode.

These modes are organized as shown below to enable reduction of power consumption.

	State of Internal Operation the μPD161802				
	Logic Power Supply	Command Massage	SRAM Power Supply	SRAM State	Oscillation
Normal operation	O	Good	O	Normal operation	Operation
Sleep mode	O	Good	O	Normal operation	Stop
Deep sleep mode	O	Good	Δ	Data maintenance	Stop
Stand-by mode	O	Good	X	Data cancellation	Stop

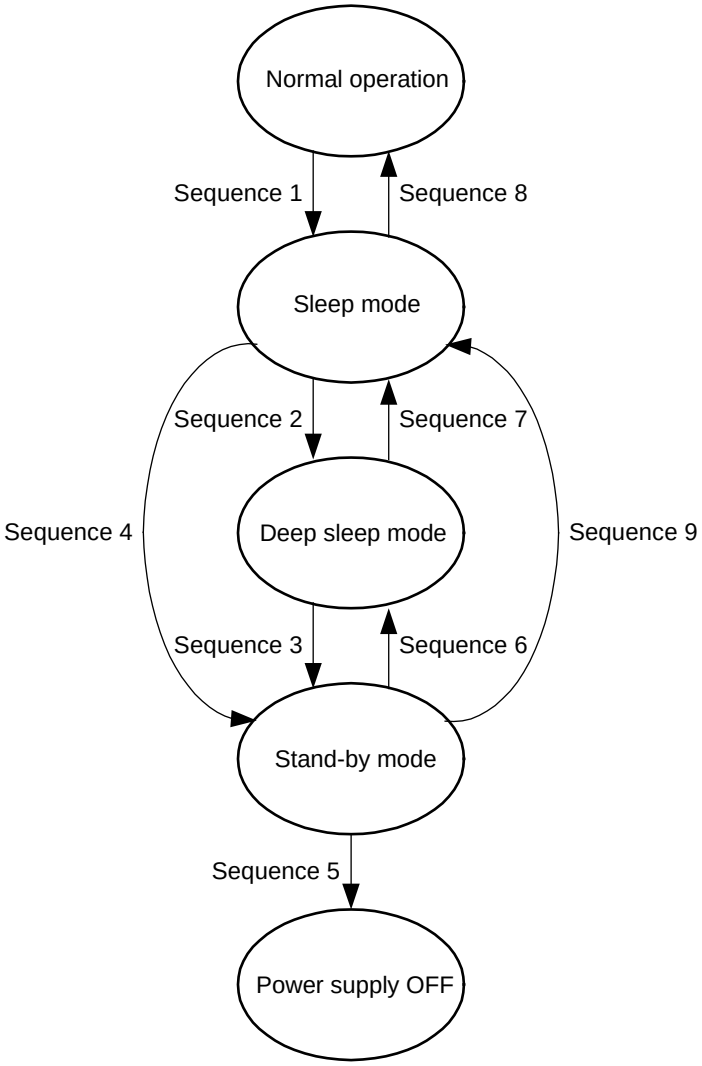
Remark O: Supply, Δ: Low power supply, X: Supply stop

Current consumption current: Normal operation > Sleep mode > Deep sleep mode > Stand-by mode

Setting a sequence, such as for stopping the power IC's power supply, enables module-based reduction of power consumption.

When VSTBY = High has been set, the SRAM power supply voltage supplied to V_{DD2} from an external source remains the same (whether in deep sleep mode or standby mode). Therefore, the amount of power consumed in deep sleep mode and stand-by mode is the same as in sleep mode.

Figure 5–57. IC State Changes



Caution When using the VSTBY = High setting, the settings at sequence 2, 3, 6 and 7 cannot be made.

<Sequence 1>

Normal operation statement	Display ON
↓	
Panel display OFF	R0 DISP1 = ”1”
↓	
WAIT time	Over 1-frame cycle time
↓	
Panel display signal control 1	
Source output stop (Vss output)	R77 RSOUT = ”0”
Gate output stop (GOE1, OEV) signal stop Note1	R77 RGOE1 = ”0” or ROEV = ”0”
VCOUT stop	R93 RVCOT = ”0”
Gate control signal stop (GCLK, GSTB, CKV, STV) Note1	R93 RGCLK = ”0”, RGSTB = ”0” or RCKV = ”0”, RSTV = ”0”
↓	
WAIT time	Over 1-frame cycle time Note2
↓	
Panel discharge control 1	
Discharge control signal (GOE2 or XDON) Note1	R77 RGOE2 = ”1” or RXDON = ”1”
↓	
WAIT time	**Note2**
↓	
Panel discharge control 2	
Multi-plectra switch signal control (RSW, GSW, BSW L fixed: Only OE2 control) Note1	R93 RGBW = ”0”
↓	
Power supply IC control (power supply OFF)	R38 to R42, R60 to R65 (sequence changes with use power supplies IC. Refer to the specifications of the power supply IC currently used.)
↓	
Oscillator stop	R1 OSC2OFF = ”1”
↓	
Sleep mode statement	Display OFF, oscillator stop, logic power supply ON, SRAM power supply ON
↓	
Next transaction	

This sequence is shown in illustration and changes with use panels. It is after checking the specification of the panel used about a sequence enough evaluation. It recommends as following condition after considering.

Notes 1. Set up the control system register flag of the signal actually used on a panel.

2. WAIT time is after checking the characteristic of a use panel, and specification enough evaluation.

<Sequence 2>

Sleep mode	Display OFF, oscillator stop, logic power supply ON, SRAM power supply ON
↓	
Display RAM data output ”0” data mask Note1	R78 RMMSK = ”0”
↓	
SRAM power supply low power mode	R78 RMST [1:0] = 0, 1
↓	
Deep sleep mode Note2	Display OFF, oscillator stop, logic power supply ON, SRAM power supply low power

Notes 1. When it set as a deep sleep mode state, be sure to input the following command. When this processing is not performed but it shifts to a deep sleep mode (RMST [1:0] = 0, 1), problems, such as an increase in penetration current, may occur.

2. Deep sleep mode state is operating the SRAM power supply for display data in the low power mode, and attains low power consumption. Although the data written to display RAM at this time is held, operation of write/read of display data cannot be performed. Note that no-guarantee about operation of IC at the time of accessing display RAM at the time of a deep sleep mode.

Caution Do not set this sequence when VSTB = High.

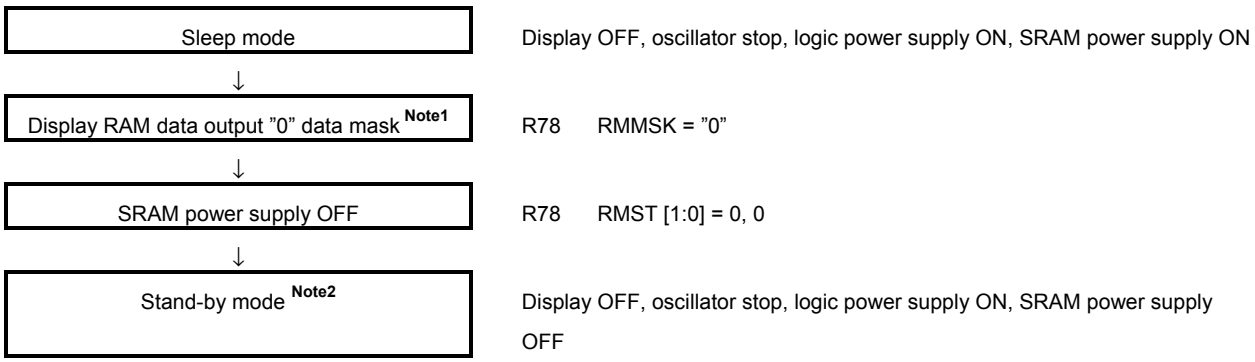
<Sequence 3>

Deep sleep mode	Display OFF, oscillator stop, logic power supply ON, SRAM power supply low power
↓	
SRAM power supply OFF	R78 RMST [1:0] = 0, 0
↓	
Stand-by mode Note	Display OFF, oscillator stop, logic power supply ON, SRAM power supply OFF

Note Stand-by mode state is stopping supply of the SRAM power supply for display data, and is attaining further low power consumption. The data written to display RAM at this time is canceled. After stand-by mode setup, when usually changing in operation again, it is necessary to write in display data again.

Caution Do not set this sequence when VSTB = High.

<Sequence 4>

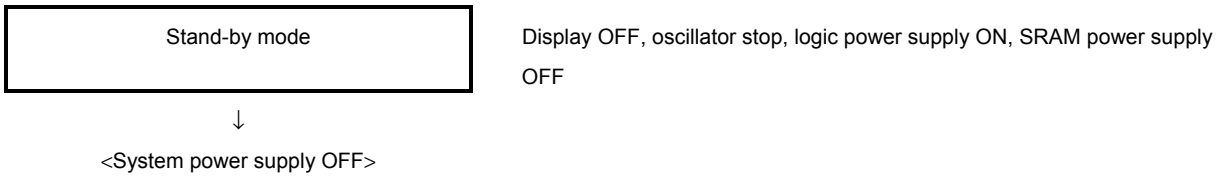


Notes 1. When it set as a deep sleep mode state, be sure to input the following command. When this processing is not performed but it shifts to a deep sleep mode (RMST [1:0] = 0, 1), problems, such as an increase in penetration current, may occur.

2. Stand-by mode state is stopping supply of the SRAM power supply for display data, and is attaining further low power consumption. The data written to display RAM at this time is canceled. After stand-by mode setup, when usually changing in operation again, it is necessary to write in display data again.

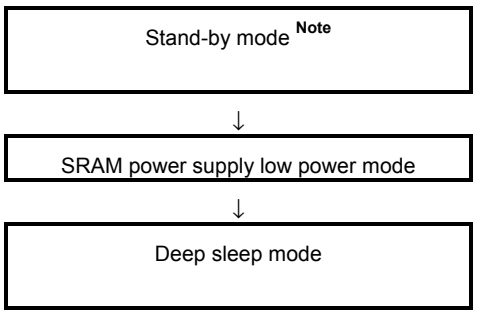
Caution When VSTBY = High has been set, the SRAM power supply voltage supplied to V_{DD2} from an external source remains the same (even in stand-by mode). Therefore, the amount of power consumed in stand-by mode is the same as in sleep mode.

<Sequence 5>



Safely, since system power supply is turned off, after setting it as stand-by mode, it recommends turning OFF system power supply.

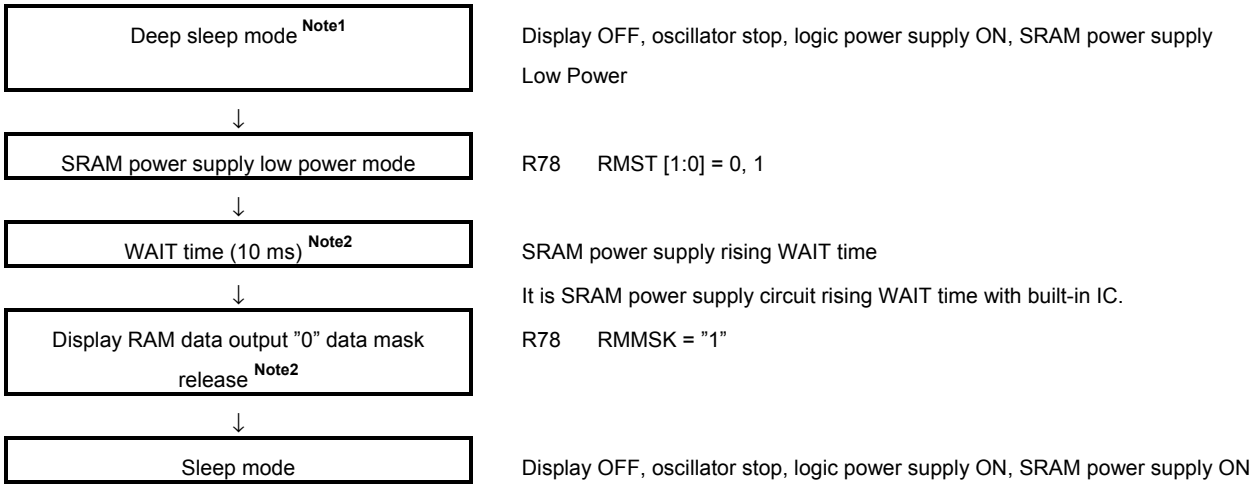
<Sequence 6>



Note Stand-by mode state is stopping supply of the SRAM power supply for display data, and is attaining further low power consumption. The data written to display RAM at this time is canceled. After stand-by mode setup, when usually changing in operation again, it is necessary to write in display data again.

Caution Do not set this sequence when VSTB = High.

<Sequence 7>

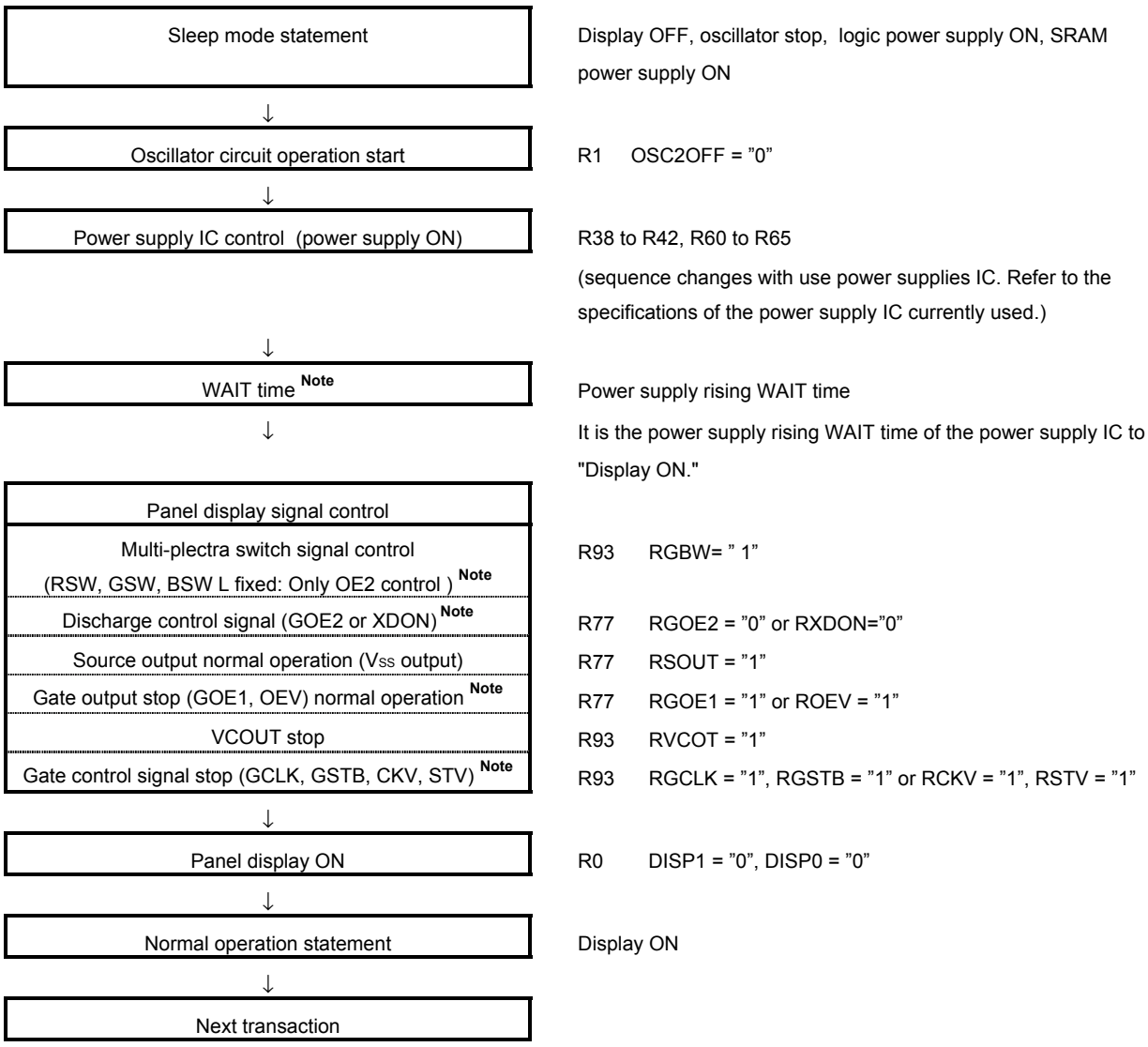


Notes 1. Deep sleep mode state is operating the SRAM power supply for display data in the low power mode, and attains low power consumption. Although the data written to display RAM at this time is held, operation of write/read of display data cannot be performed. Note that no-guarantee about operation of IC at the time of accessing display RAM at the time of a deep sleep mode.

2. From deep sleep mode, sleep mode or when it usually returns to operation, input the following command. When display ON is carried out, all LCD displays will be "0" data outputs, without canceling a setup of this command.

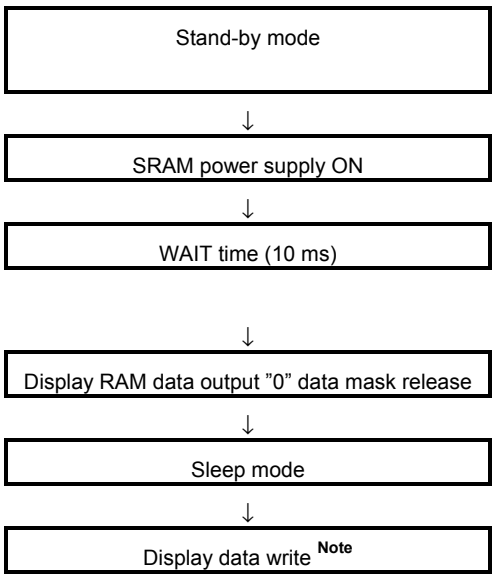
Caution Do not set this sequence when VSTB = High.

<Sequence 8>



Notes Set up the control system register flag of the signal actually used on a panel.

<Sequence 9>



Display OFF, oscillator stop, logic power supply ON, SRAM power supply OFF

R78 RMST [1:0] = 1, 0

SRAM power supply rising WAIT time

It is SRAM power supply circuit rising WAIT time with built-in IC.

R78 RMMSK = ”1”

Display OFF, oscillator stop, logic power supply ON, SRAM power supply ON

Note Stand-by mode state is stopping supply of the SRAM power supply for display data, and is attaining further low power consumption. The data written to display RAM at this time is canceled. After stand-by mode setup, when usually changing in operation again, it is necessary to write in display data again.

Caution When VSTBY = High has been set, the SRAM power supply voltage supplied to V_{DD2} from an external source remains the same (even in stand-by mode). Therefore, the amount of power consumed in stand-by mode is the same as in sleep mode.

6. E²PROM INTERFACE

The μPD161802 builds in the interface function to E²PROM corresponding to the Microwire interface. However, the capacity of E²PROM corresponds only to 2 K bits and 4 K bits article.

6.1 The μPD161802 and E²PROM Connection

Connection with E²PROM is made as shown in the following figure.

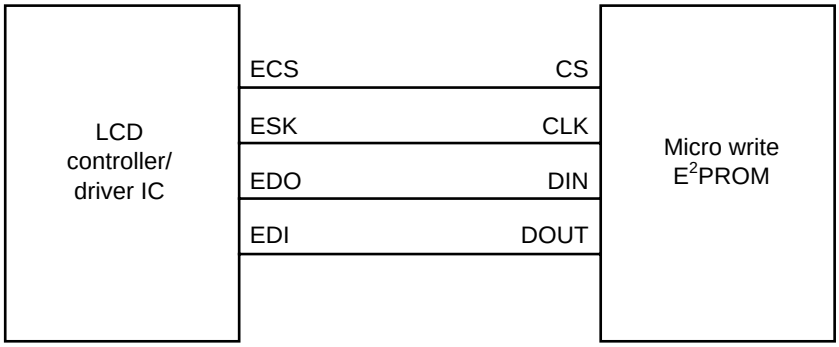


Table 6–1. LCD controller side signal

Pin	Function
ECS	Chip select signal over E²PROM. With outputting ECS = 1, E²PROM is made into an active state and data is transmitted after that. It connects with CS (chip select pin) of E²PROM.
ESK	Clock signal over E²PROM. In falling of ESK, data is outputted from EDO to E²PROM. It connects with CLK (shift clock pin) of E²PROM.
EDO	Data output pin. Data is outputted to E²PROM. It connects with DIN (data in pin) of E²PROM
EDI	Data input pin. It is used for reading of the data of E²PROM. It connects with DOUT (data out pin) of E²PROM.

6.2 Each Operation

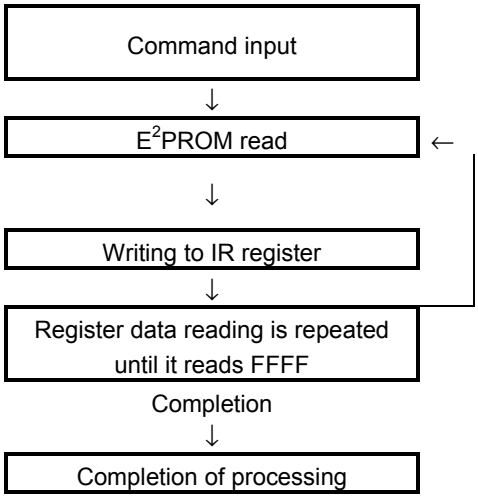
The μPD161802 can perform writing of register data, reading of a register date and elimination of E^2PROM data to E^2PROM. Selection of each operation is performed using R24 register.

R24 register			E^2PROM command
E2OPC2	E2OPC1	E2OPC0	
0	0	0	Setting prohibited
0	0	1	EPSAVE: Writing to E^2PROM
0	1	0	MASKON: Permission of the writing and elimination to E^2PROM
0	1	1	MASKOF: Prohibition of the writing and elimination to E^2PROM
1	0	0	EPCLR: All area elimination of E^2PROM
1	0	1	EPWALL: FFH is written in all the area of E^2PROM
1	1	0	EPREAD: Reading from E^2PROM
1	1	1	Setting prohibited

In addition, explain each operation below.

[E^2PROM read command: Reading from E^2PROM]

From the "E^2PROM address" set as "the E^2PROM reading start address register (R58)", it reads in order of "index" + "a register value" (a total of 16 bits) and the register data stored in E^2PROM is saved to the applicable index of the μPD161802. In addition, reading operation is continuously performed until it reads the reading end ID (R127 = 07FH).



R58: Setting of reading start address
R24: E^2PROM read execution (006H)

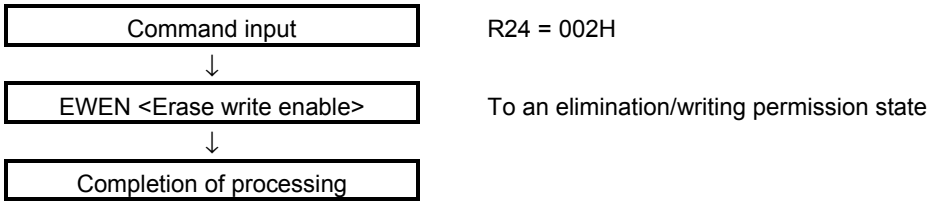
[EPSAVE command: Writing of the data to E^2PROM]

The data writing to E^2PROM writes IR data of R57, and register data set up by R57 in the E^2PROM address set up by R33.

Elimination/writing permission and command input	R24: Elimination/writing permission carry out (MASKON command = 002H)
↓	
EWEN issue	To elimination/writing permission state
↓	
E^2PROM writing address specification	It writes in R33 and is specification of address.
↓	**Caution Since increment is not carried out, it is required.**
Writing index specification of E^2PROM	The index which wants to write in R57 is set up.
↓	(As for the data of an index, the register value in μPD161802 is written in.)
The data transmission command input to E^2PROM	R24: Data transmission execution to E^2PROM (EPSAVE command = 001H)
↓	
Wait	It is wait time in order to write in ROM. It is needed. Insert wait time after confirming the specification of E^2PROM used.
Completion	
↓	
Elimination/writing protected and command input	R24: Elimination/writing protected execution (003H)
↓	
EWDS	It passes elimination/writing protected. About the data of E^2PROM, they are elimination or the disposal for making it not rewrite carelessly.
↓	
Completion of processing	

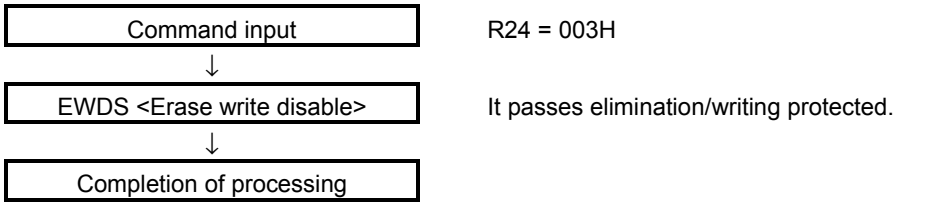
[MASKON command: Writing/elimination permission to E^2PROM]

Elimination/writing to E^2PROM are permitted.



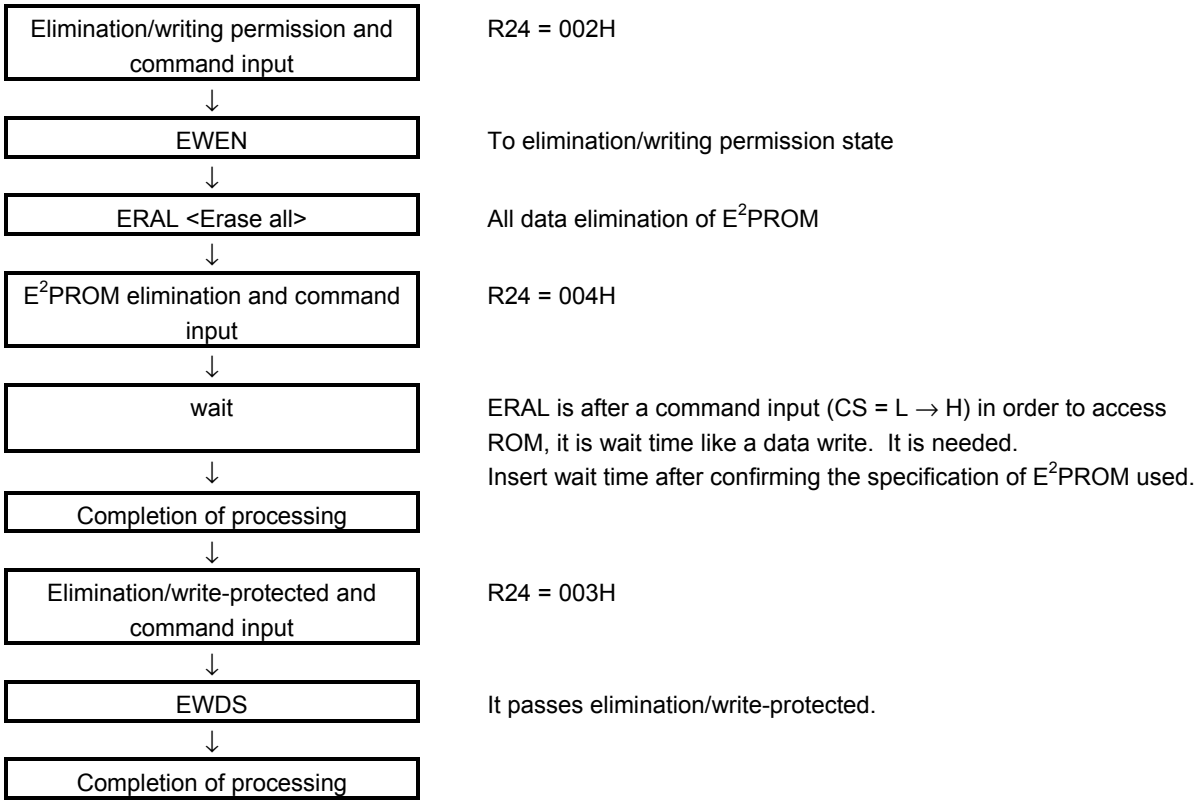
[MASKOF: Writing protected to E^2PROM]

Elimination/writing to E^2PROM are protected (Reading of data is possible).



[EPCLR command: E^2PROM elimination] :

The data of E^2PROM is initialized.



[EPWALL]

"index = 07FH"+ "Data = 1FFH" is written in all the data of E^2PROM.

At the time of E^2PROM initialization, it reads to all E^2PROM data, an end command (R127) is written and the infinite loop of reading by the noise etc. is prevented.

Elimination/writing permission and command input	R24 = 002H
↓	
EWEN	To elimination/writing permission state
↓	
EPWALL command input	R24 = 005H
↓	
WRAL <Erase all>	"Index = 07FH (R127) "+ "Data = 1FFH" is written in to all the data of E^2PROM.
↓	
wait	WRAL is after a command input (CS = L → H) in order to access ROM, it is wait time like a data write. It is needed. Insert wait time after confirming the specification of E^2PROM used.
↓	
Elimination/write-protected and command input	R24 = 003H
↓	
EWDS	It passes elimination/write-protected.
↓	
Completion of processing	

7. RESET

If the /RESET input becomes L or the reset command is input, the internal timing generator is initialized. The reset command will also initialize each register to its default value. These default values are listed in the table below (Register number is an estimate. Understand that there is a case where it changes later).

(1/2)

Register		/RESET Pin Note1	Reset Command	Default Value
Control register 1	R0	X	O	080H
Control register 2	R1	X	O	003H
RAM address offset register	R2	O	X	000H
Command reset register	R3	X	O	000H
Data access control register	R5	X	O	000H
X address register	R6	X	O	000H
Y address register	R7	X	O	000H
MIN. ·X address register	R8	X	O	000H
MAX. ·X address register	R9	X	O	0EFH
MIN. ·Y address register	R10	X	O	000H
MAX. ·Y address register	R11	X	O	13FH
VLD pin polarity inversion register	R13	X	O	000H
Scroll area start line register	R14	X	O	000H
Scroll area line count register	R15	X	O	000H
Scroll step count register	R16	X	O	000H
Partial non-display area setting register	R17	X	O	000H
Blanking period bias control register	R18	X	O	000H
Partial 1 display area start line register	R20	X	O	000H
Partial 2 display area start line register	R21	X	O	000H
Partial 1 display area line count register	R22	X	O	000H
Partial 2 display area line count register	R23	X	O	000H
The register for E^2PROM interface control	R24	O	O	000H
RGB interface control register	R25	X	O	000H
RGB interface back poach period register	R26	X	O	012H
RGB interface through mode start line register	R27	X	O	000H
RGB interface through mode end line register	R28	X	O	000H
RGB interface capture mode window access MIN. ·X address register	R29	X	O	000H or 10FH Note2
RGB interface capture mode window access MAX. ·X address register	R30	X	O	0EFH or 0FFH Note2
RGB interface capture mode window access MIN. ·Y address register	R31	X	O	000H
RGB interface capture mode window access MAX. ·Y address register	R32	X	O	13FH
E^2PROM write in address specification register	R33	X	O	000H
Calibration register Note3	R34	X	O	000H
Power supply IC control register 1 to 5	R38 to R42	X	O	000H
γ-resistance-connection changing register	R43	X	O	000H

Remark O: Default value set, X: Default value not set

(2/2)

Register		/RESET Pin Note1	Reset Command	Default Value
γ-amplitude adjustment register 1 to 4	R44 to R47	X	O	005H
γ-characteristic adjustment P1 register	R48	X	O	011H
γ-characteristic adjustment P2 register	R49	X	O	077H
γ-characteristic adjustment P3 register	R50	X	O	044H
γ-characteristic adjustment P4 register	R51	X	O	044H
γ-characteristic adjustment N1 register	R52	X	O	011H
γ-characteristic adjustment N2 register	R53	X	O	077H
γ-characteristic adjustment N3 register	R54	X	O	044H
γ-characteristic adjustment N4 register	R55	X	O	044H
Output amplitude power supply setup register for 8-color displays	R56	X	O	000H
E^2PROM write in index specification register	R57	X	O	000H
E^2PROM reading start address specification register	R58	X	O	000H
γ-reference voltage generator capability setting register	R59	X	O	044H
Power supply IC control register 6 to 11	R60 to R65	X	O	000H
AMP drive method change register	R66	X	O	000H
Partial display/non-display area refresh cycle register	R68	X	O	000H
RGB switch open timing register	R72	X	O	000H
The bias current setting register for the liquid crystal drive AMP	R73	X	O	004H
Blanking period line setting register	R75	X	O	001H
1 line period clock setting register	R76	X	O	001H
Panel signal control register 1	R77	X	O	000H
Pre-charge polarity select register	R78	X	O	000H
GOE1 start timing register	R79	X	O	004H
GOE1 end timing register	R80	X	O	025H
Pre-charge start timing register	R81	X	O	005H
Pre-charge end timing register	R82	X	O	005H
R switch start timing register	R83	X	O	00DH
R switch end timing register	R84	X	O	014H
G switch start timing register	R85	X	O	015H
G switch end timing register	R86	X	O	01CH
B switch start timing register	R87	X	O	01DH
B switch end timing register	R88	X	O	024H
Extended signal 1 start timing register	R89	X	O	009H
Extended signal 1 end timing register	R90	X	O	009H
Extended signal 2 start timing register	R91	X	O	009H
Extended signal 2 end timing register	R92	X	O	009H
Panel signal control register 2	R93	X	O	000H
Test mode		O	O	–

Remark O: Default value set, X: Default value not set

Notes 1. The internal counters are initialized only by a reset from the /RESET pin. Be sure to perform reset via the /RESET pin at power application.

2. With setting value of RAM address offset register (R2), a default value change as show in the below table.

R2 Setting Value	Default Value	
	R29	R30
000H	000H	0EFH
001H	010H	0FFH

3. The following value is set as the calibration setting time, t_{cal}, in a reset by reset command.

$t_{cal} = 1/f_{OSC2} \times 40$ (f_{OSC2} returns to initial frequency)

Caution The contents of RAM are saved in the case of both reset by /RESET pin and reset by reset command. Note that the RAM contents are unfixed immediately after the power is turned on.

The setting table at the time of /RESET = Low

Control Signal		All ON (default)	All OFF
Source Output		GND	Hi-Z
Gate Output Control Signal	GOE1	Normal	Low Fixation
	GOE2	Low Fixation	Normal [Note]
R/G/BSW Output		All High	All Low

Note The output of GOE2 changes with setup of RGON2 bit (R77 D_4).

RGON2 = 0: GOE2 = High RGON2 = 1: GOE2 = Low (R/G/BSW = High fixation)

Cautions 1. The timing circuit 1 is set up and only a case is valid.

2. The source output, a gate output control signal, and R/G/BSW output can be set up individually.

8. COMMAND

8.1 Command List

(Register number is an estimate. Understand that there is a case where it changes later).

Display data access

RAM Access	RS	R,/W	Data Bit								
			DB_{17}	DB_{16}	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9
			DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
18-bit parallel interface											
Display data read 1	1	1	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9
			D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display data write 1	1	0	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9
			D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
16-bit parallel interface (1-pixel/16-bit mode [DTX = 0])											
Display data read 2	1	1	**Hi-Z**	**Hi-Z**	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{11}	D_{10}
			D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1
Display data write 2	1	0	–	–	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{11}	D_{10}
			D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1
16-bit parallel interface (1-pixel/18-bit mode [DTX = 1])											
Display data read 3	1	1	**Hi-Z**	**Hi-Z**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
			D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9
			(D_8)	(D_7)	(D_6)	(D_5)	(D_4)	(D_3)	(D_2)	(D_1)	(D_0)
Display data write 3	1	0	**Hi-Z**	**Hi-Z**	**X**	**X**	**X**	**X**	**X**	**X**	**X**
			D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9
			(D_8)	(D_7)	(D_6)	(D_5)	(D_4)	(D_3)	(D_2)	(D_1)	(D_0)

Remark Hi-Z: High impedance, X: Invalid data

Caution When the 16-bit parallel interface is used in 1-pixel/18-bit mode (DTX = H), data access of two words per pixel is required.

18-bit parallel interface mode, DB_{17}, DB_{16} = 0 (1/5)

Rn	Register	RS	R,/W	Data Bit							
				DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8
				DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
R0	Control register 1	0	0	0	0	0	0	0	0	0	0
				DISP1	DISP0	INV	DTY	STBY	COLOR		GSM
R1	Control register 2	0	0	0	0	0	0	0	0	0	1
				ADX	ADR	0	GUD	LTS1	LTS0	OSC1OFF	OSC2OFF
R2	RAM address offset register	0	0	0	0	0	0	0	0	1	0
											RMOFS
R3	RESET	0	0	0	0	0	0	0	0	1	1
											CRES
R5	Data access control register	0	0	0	0	0	0	0	1	0	1
				DTX1	BSTR	0	WAS	0	INC	0	0
R6	X address register (1 word)	0	0	0	0	0	0	0	1	1	0
				0	0	0	0	0	0	0	0
	X address register (2 word)			X	X	X	X	X	X	X	X
				XA_7	XA_6	XA_5	XA_4	XA_3	XA_2	XA_1	XA_0
R7	Y address register (1 word)	0	0	0	0	0	0	0	1	1	1
				0	0	0	0	0	0	0	0
	Y address register (2 word)			X	X	X	X	X	X	X	YA_8
				YA_7	YA_6	YA_5	YA_4	YA_3	YA_2	YA_1	YA_0
R8	MIN. ·X address register (1 word)	0	0	0	0	0	0	1	0	0	0
				0	0	0	0	0	0	0	0
	MIN. ·X address register (2 word)			X	X	X	X	X	X	X	X
				XMIN7	XMIN6	XMIN5	XMIN4	XMIN3	XMIN2	XMIN1	XMIN0
R9	MAX. ·X address register (1 word)	0	0	0	0	0	0	1	0	0	1
				0	0	0	0	0	0	0	0
	MAX. ·X address register (2 word)			X	X	X	X	X	X	X	X
				XMAX7	XMAX6	XMAX5	XMAX4	XMAX3	XMAX2	XMAX1	XMAX0
R10	MIN. ·Y address register (1 word)	0	0	0	0	0	0	1	0	1	0
				0	0	0	0	0	0	0	0
	MIN. ·Y address register (2 word)			X	X	X	X	X	X	X	YMIN8
				YMIN7	YMIN6	YMIN5	YMIN4	YMIN3	YMIN2	YMIN1	YMIN0
R11	MAX. ·Y address register (1 word)	0	0	0	0	0	0	1	0	1	1
				0	0	0	0	0	0	0	0
	MAX. ·Y address register (2 word)			X	X	X	X	X	X	X	YMAX8
				YMAX7	YMAX6	YMAX5	YMAX4	YMAX3	YMAX2	YMAX1	YMAX0
R13	VLD pin polarity inversion register	0	0	0	0	0	0	1	1	0	1
				RESS0	RESGA	RESSW	0		VPL	0	
R14	Scroll area start line register (1 word)	0	0	0	0	0	0	1	1	1	0
				0	0	0	0	0	0	0	0
	Scroll area start line register (2 word)			X	X	X	X	X	X	X	SSL8
				SSL7	SSL6	SSL5	SSL4	SSL3	SSL2	SSL1	SSL0
R15	Scroll area line count register (1 word)	0	0	0	0	0	0	1	1	1	1
				0	0	0	0	0	0	0	0
	Scroll area line count register (2 word)			X	X	X	X	X	X	X	SAW8
				SAW7	SAW6	SAW5	SAW4	SAW3	SAW2	SAW1	SAW0

18-bit parallel interface mode, DB_{17}, DB_{16} = 0 (2/5)

Rn	Register	RS	R,/W	Data Bit							
				DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8
				DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
R16	Scroll step count register (1 word)	0	0	0	0	0	1	0	0	0	0
				0	0	0	0	0	0	0	0
	Scroll step count register (2 word)			X	X	X	X	X	X	X	SST8
				SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0
R17	Partial non-display area setting register	0	0	0	0	0	1	0	0	0	1
								PSEL	PGR	PGG	PGB
R18	Blanking period bias control register	0	0	0	0	0	1	0	0	1	0
				BSSP7	BSSP6	BSSP5	BSSP4	BSSP3	BSSP2	BSSP1	BSSP0
R20	Partial 1 display area start line register (1 word)	0	0	0	0	0	1	0	1	0	0
				0	0	0	0	0	0	0	0
	Partial 1 display area start line register (2 word)			X	X	X	X	X	X	X	P1SL8
				P1SL7	P1SL6	P1SL5	P1SL4	P1SL3	P1SL2	P1SL1	P1SL0
R21	Partial 2 display area start line register (1 word)	0	0	0	0	0	1	0	1	0	1
				0	0	0	0	0	0	0	0
	Partial 2 display area start line register (2 word)			X	X	X	X	X	X	X	P2SL8
				P2SL7	P2SL6	P2SL5	P2SL4	P2SL3	P2SL2	P2SL1	P2SL0
R22	Partial 1 display area line count register (1 word)	0	0	0	0	0	1	0	1	1	0
				0	0	0	0	0	0	0	0
	Partial 1 display area line count register (2 word)			X	X	X	X	X	X	X	P1AW8
				P1AW7	P1AW6	P1AW5	P1AW4	P1AW3	P1AW2	P1AW1	P1AW0
R23	Partial 2 display area line count register (1 word)	0	0	0	0	0	1	0	1	1	1
				0	0	0	0	0	0	0	0
	Partial 2 display area line count register (2 word)			X	X	X	X	X	X	X	P2AW8
				P2AW7	P2AW6	P2AW5	P2AW4	P2AW3	P2AW2	P2AW1	P2AW0
R24	E^2PROM interface control register	0	0	0	0	0	1	1	0	0	0
									E2OPC2	E2OPC1	E2OPC0
R25	RGB interface control register	0	0	0	0	0	1	1	0	0	1
					DCK2	DCK1	DCK0		NWRGB	RGBS	DISPCK
R26	RGB back poach period setting register	0	0	0	0	0	1	1	0	1	0
				HBP3	HBP2	HBP1	HBP0	VBP3	VBP2	VBP1	VBP0
R27	RGB through mode display start line register (1 word)	0	0	0	0	0	1	1	0	1	1
				0	0	0	0	0	0	0	0
	RGB through mode display start line register (2 word)			X	X	X	X	X	X	X	RGBST8
				RGBST7	RGBST6	RGBST5	RGBST4	RGBST3	RGBST2	RGBST1	RGBST0
R28	RGB through mode display end line register (1 word)	0	0	0	0	0	1	1	1	0	0
				0	0	0	0	0	0	0	0
	RGB through mode display end line register (2 word)			X	X	X	X	X	X	X	RGBED8
				RGBED7	RGBED6	RGBED5	RGBED4	RGBED3	RGBED2	RGBED1	RGBED0
R29	RGB capture mode window access MIN. X address register (1 word)	0	0	0	0	0	1	1	1	0	1
				0	0	0	0	0	0	0	0
	RGB capture mode window access MIN. X address register (2 word)			X	X	X	X	X	X	X	X
				CAPXMIN7	CAPXMIN6	CAPXMIN5	CAPXMIN4	CAPXMIN3	CAPXMIN2	CAPXMIN1	CAPXMIN0

18-bit parallel interface mode, DB_{17}, DB_{16} = 0 (3/5)

Rn	Register	RS	R,/W	Data Bit							
				DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8
				DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
R30	RGB capture mode window access MAX. X address register (1 word)	0	0	0	0	0	1	1	1	1	0
				0	0	0	0	0	0	0	0
	RGB capture mode window access MAX. X address register (2 word)			X	X	X	X	X	X	X	X
				CAPXMAX7	CAPXMAX6	CAPXMAX5	CAPXMAX4	CAPXMAX3	CAPXMAX2	CAPXMAX1	CAPXMAX0
R31	RGB capture mode window access MIN. Y address register (1 word)	0	0	0	0	0	1	1	1	1	1
				0	0	0	0	0	0	0	0
	RGB capture mode window access MIN. Y address register (2 word)			X	X	X	X	X	X	X	CAPYMIN8
				CAPYMIN7	CAPYMIN6	CAPYMIN5	CAPYMIN4	CAPYMIN3	CAPYMIN2	CAPYMIN1	CAPYMIN0
R32	RGB capture mode window access MAX. Y address register (1 word)	0	0	0	0	1	0	0	0	0	0
				0	0	0	0	0	0	0	0
	RGB capture mode window access MAX. Y address register (2 word)			X	X	X	X	X	X	X	CAPYMAX8
				CAPYMAX7	CAPYMAX6	CAPYMAX5	CAPYMAX4	CAPYMAX3	CAPYMAX2	CAPYMAX1	CAPYMAX0
R33	E^2PROM write in address specification register	0	0	0	0	1	0	0	0	0	1
				E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
R34	Calibration register	0	0	0	0	1	0	0	0	1	0
											OC
R38	Power supply IC control register 1	0	0	0	0	1	0	0	1	1	0
				PSD17	PSD16	PSD15	PSD14	PSD13	PSD12	PSD11	PSD10
R39	Power supply IC control register 2	0	0	0	0	1	0	0	1	1	1
				PSD27	PSD26	PSD25	PSD24	PSD23	PSD22	PSD21	PSD20
R40	Power supply IC control register 3	0	0	0	0	1	0	1	0	0	0
				PSD37	PSD36	PSD35	PSD34	PSD33	PSD32	PSD31	PSD30
R41	Power supply IC control register 4	0	0	0	0	1	0	1	0	0	1
				PSD47	PSD46	PSD45	PSD44	PSD43	PSD42	PSD41	PSD40
R42	Power supply IC control register 5	0	0	0	0	1	0	1	0	1	0
				PSD57	PSD56	PSD55	PSD54	PSD53	PSD52	PSD51	PSD50
R43	γ-resistance-connection changing register	0	0	0	0	1	0	1	0	1	1
							GSEL				GONSEL
R44	γ-amplitude adjustment register 1	0	0	0	0	1	0	1	1	0	0
				GPH7	GPH6	GPH5	GPH4	GPH3	GPH2	GPH1	GPH0
R45	γ-amplitude adjustment register 2	0	0	0	0	1	0	1	1	0	1
				GNH7	GNH6	GNH5	GNH4	GNH3	GNH2	GNH1	GNH0
R46	γ-amplitude adjustment register 3	0	0	0	0	1	0	1	1	1	0
				GPL7	GPL6	GPL5	GPL4	GPL3	GPL2	GPL1	GPL0
R47	γ-amplitude adjustment register 4	0	0	0	0	1	0	1	1	1	1
				GNL7	GNL6	GNL5	GNL4	GNL3	GNL2	GNL1	GNL0
R48	γ-characteristic adjustment P1 register	0	0	0	0	1	1	0	0	0	0
				VDRP3	VDRP2	VDRP1	VDRP0	VSRP3	VSRP2	VSRP1	VSRP0
R49	γ-characteristic adjustment P2 register	0	0	0	0	1	1	0	0	0	1
				VLRP3	VLRP2	VLRP1	VLRP0	VHRP3	VHRP2	VHRP1	VHRP0
R50	γ-characteristic adjustment P3 register	0	0	0	0	1	1	0	0	1	0
					VGR1P2	VGR1P1	VGR1P0		VGR0P2	VGR0P1	VGR0P0
R51	γ-characteristic adjustment P4 register	0	0	0	0	1	1	0	0	1	1
					VGR3P2	VGR3P1	VGR3P0		VGR2P2	VGR2P1	VGR2P0

18-bit parallel interface mode, DB_{17}, DB_{16} = 0 (4/5)

Rn	Register	RS	R,/W	Data Bit							
				DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8
				DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
R52	γ-characteristic adjustment N1 register	0	0	0	0	1	1	0	1	0	0
				VDRN3	VDRN2	VDRN1	VDRN0	VSRN3	VSRN2	VSRN1	VSRN0
R53	γ-characteristic adjustment N2 register	0	0	0	0	1	1	0	1	0	1
				VLRN3	VLRN2	VLRN1	VLRN0	VHRN3	VHRN2	VHRN1	VHRN0
R54	γ-characteristic adjustment N3 register	0	0	0	0	1	1	0	1	1	0
					VGR1N2	VGR1N1	VGR1N0		VGR0N2	VGR0N1	VGR0N0
R55	γ-characteristic adjustment N4 register	0	0	0	0	1	1	0	1	1	1
					VGR3N2	VGR3N1	VGR3N0		VGR2N2	VGR2N1	VGR2N0
R56	Output amplitude power supply setup register for 8-color displays	0	0	0	0	1	1	1	0	0	0
										GV8S1	0
R57	E^2PROM writing index specification register	0	0	0	0	1	1	1	0	0	1
				E2IR7	E2IR6	E2IR5	E2IR4	E2IR3	E2IR2	E2IR1	E2IR0
R58	E^2PROM reading start address specification register	0	0	0	0	1	1	1	0	1	0
				E2SA7	E2SA6	E2SA5	E2SA4	E2SA3	E2SA2	E2SA1	E2SA0
R59	γ-reference voltage generator capability setting register	0	0	0	0	1	1	1	0	1	1
				WHP	WI2	WI1	WI0	BHP	BI2	BI1	BI0
R60	Power supply IC control register 6	0	0	0	0	1	1	1	1	0	0
				PSD67	PSD66	PSD65	PSD64	PSD63	PSD62	PSD61	PSD60
R61	Power supply IC control register 7	0	0	0	0	1	1	1	1	0	1
				PSD77	PSD76	PSD75	PSD74	PSD73	PSD72	PSD71	PSD70
R62	Power supply IC control register 8	0	0	0	0	1	1	1	1	1	0
				PSD87	PSD86	PSD85	PSD84	PSD83	PSD82	PSD81	PSD80
R63	Power supply IC control register 9	0	0	0	0	1	1	1	1	1	1
				PSD97	PSD96	PSD95	PSD94	PSD93	PSD92	PSD91	PSD90
R64	Power supply IC control register 10	0	0	0	1	0	0	0	0	0	0
				PSDA7	PSDA6	PSDA5	PSDA4	PSDA3	PSDA2	PSDA1	PSDA0
R65	Power supply IC control register 11	0	0	0	1	0	0	0	0	0	1
				PSDB7	PSDB6	PSDB5	PSDB4	PSDB3	PSDB2	PSDB1	PSDB0
R66	The 3L interlace & AMP drive method change register	0	0	0	1	0	0	0	0	1	0
				0	LACE3	LACE2	LACE1	LACE0	LMD2	LMD1	0
R68	Partial display/non-display area refresh cycle register	0	0	0	1	0	0	0	1	0	0
					REFM2	REFM1	REFM0	REFB3	REFB2	REFB1	REFB0
R72	RGB switch open timing register	0	0	0	1	0	0	1	0	0	0
				DC4	DC3	DC2	DSCG4	DSCG3	DSCG2	DSCG1	DSCG0
R73	The bias setting register for the liquid crystal drive AMP	0	0	0	1	0	0	1	0	0	1
								BCONB3	BCONB2	BCONB1	BCONB0
R75	Blanking period line setting register	0	0	0	1	0	0	1	0	1	1
				ADLN7	ADLN6	ADLN5	ADLN4	ADLN3	ADLN2	ADLN1	ADLN0
R76	1 line period clock setting register	0	0	0	1	0	0	1	1	0	0
							ADCK4	ADCK3	ADCK2	ADCK1	ADCK0
R77	Panel signal control register 1	0	0	0	1	0	0	1	1	0	1
				RPCK1	RPCK0	RSOUT	RGOE2	RGOE1	RXDON	ROEVE	ROEV
R78	The 3L interlace & AMP drive method change register	0	0	0	1	0	0	1	1	1	0
				TCLSL	RMMSK	RMST1	RMST0	PT1	PT0	REV	0

18-bit parallel interface mode, DB_{17}, DB_{16} = 0 (5/5)

Rn	Register	RS	R,/W	Data Bit							
				DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8
				DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
R79	GOE1 start timing register	0	0	0	1	0	0	1	1	1	1
						GOST5	GOST4	GOST3	GOST2	GOST1	GOST0
R80	GOE1 end timing register	0	0	0	1	0	1	0	0	0	0
						GOED5	GOED4	GOED3	GOED2	GOED1	GOED0
R83	R switch start timing register	0	0	0	1	0	1	0	0	1	1
						RST5	RST4	RST3	RST2	RST1	RST0
R84	R switch end timing register	0	0	0	1	0	1	0	1	0	0
						RED5	RED4	RED3	RED2	RED1	RED0
R85	G switch start timing register	0	0	0	1	0	1	0	1	0	1
						GST5	GST4	GST3	GST2	GST1	GST0
R86	G switch end timing register	0	0	0	1	0	1	0	1	1	0
						GED5	GED4	GED3	GED2	GED1	GED0
R87	B switch start timing register	0	0	0	1	0	1	0	1	1	1
						BST5	BST4	BST3	BST2	BST1	BST0
R88	B switch end timing register	0	0	0	1	0	1	1	0	0	0
						BED5	BED4	BED3	BED2	BED1	BED0
R89	Extended signal 1 start timing register	0	0	0	1	0	1	1	0	0	1
						E1ST5	E1ST4	E1ST3	E1ST2	E1ST1	E1ST0
R90	Extended signal 1 end timing register	0	0	0	1	0	1	1	0	1	0
						E1ED5	E1ED4	E1ED3	E1ED2	E1ED1	E1ED0
R91	Extended signal 2 start timing register	0	0	0	1	0	1	1	0	1	1
						E2ST5	E2ST4	E2ST3	E2ST2	E2ST1	E2ST0
R92	Extended signal 2 end timing register	0	0	0	1	0	1	1	1	0	0
						E2ED5	E2ED4	E2ED3	E2ED2	E2ED1	E2ED0
R93	Panel signal control register 2	0	0	0	1	0	1	1	1	0	1
				0	RVCOT	RGBSW	RGSTB	RGCLK	RASW	RSTV	RCKV

Cautions 1. Input unfixed (0 or 1) in blank area.

2. Access is prohibited about the register is not in the above register.

8.2 Command Explanation

(Register number is an estimate. Understand that there is a case where it changes later).

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Register	Bit	Symbol	Function
R0	D_7	DISP1	This command performs the same output as when 8-color mode white, independently of the internal RAM data (case of normally white). This command is executed, after it has been transferred, when the next line is output. 0: Normal operation 1: Ignores data of RAM and outputs all display line 8-color mode whites. DISP1 takes precedence over DISP0. When DISP1 = 1, DISP0 = 1 is ignored.
	D_6	DISP0	This command performs the same output as when 8-color mode black, independently of the internal RAM data (case of normally white). This command is executed, after it has been transferred, when the next line is output. 0: Normal operation 1: Ignores data of RAM and outputs all display line 8-color mode black.
	D_5	INV	This command selects a line inversion function and a frame inversion function. Execution in the mode set by this command is from the timing outputs the following frame data. In addition, at the time of 3-line interlace display mode selection, this command setup is disregarded and serves as field inversion. 0: Line inversion 1: Frame inversion
	D_4	DTY	This pin selects the partial function. When the partial function s selected in the 260,000-color mode, set the partial OFF area color setting register (R17) to 000H. In the 8-color mode, the partial OFF area color can be set to any value from 000H to 007H. The power consumption cannot be reduced with the partial function. To reduce the power consumption, select the 8-color mode. This command is executed following transfer from the time the next frame. 0: Normal display mode 1: Partial display mode
	D_3	STBY	This bit selects the stand-by function. When the stand-by function is selected, a display OFF operation is executed, the amplifiers at each output are stopped. After executing the stand-by function using this bit, set the regulator for gate power supply IC to OFF and set the DC/DC converter to OFF. For the sequence, refer to the preliminary product information of the power supply IC etc. Note that when releasing stand-by, perform the opposite operation, the display RAM power supply ON and display RAM mask release after setting the DC/DC converter to ON and setting the regulators of the gate IC and power supply IC to ON, cancel this bit. 0: Normal operation 1: Stand-by function (Display read OFF from RAM, stop VCOM, display OFF = source output becomes V_{SS})
	D_2	COLOR	This pin switches the 260,000-color mode and the 8-color mode. When the 8-color mode is selected, low power supply can be selected in order to stop the amplifier at each output circuit. In the 8-color mode, the value of the MSB of the internal RAM data is used as the color data. This command is executed following transfer from the next frame. 0: 260,000-color mode (18-bit/pixels) 1: 8-color mode (3-bit/pixels) **Caution In 8-color mode, it does not become low power consumption at the time of built-in γ-output adjustment circuit use by GSEL(R43:D_4) =1 setup.**

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R0</td><td>D_0</td><td>GSM</td><td>Sets output of the gate scanning signal during partial display.
If this bit is set to 1, the gate scan of the lines set in the partial non-display area is stopped.
This command is executed following transfer from the next frame.
0: Normal mode
1: Stops gate scanning in partial non-display area</td></tr>
<tr><td rowspan="6">R1</td><td>D_7</td><td>ADX</td><td>Addressing of X address is inverted. For more details, refer to Figure 5–24.</td></tr>
<tr><td>D_6</td><td>ADR</td><td>Addressing of Y address is inverted. For more details, refer to Figure 5–24.</td></tr>
<tr><td>D_4</td><td>GUD</td><td>This pin can be used when changing the direction of gate scan of a panel.
A display is possible for a vertical contrary by changing the direction of gate scan of a panel also in the time of the through mode of RGB interface using the output signal from this pin.
This command is executed following transfer from the next frame.
0: GUD pin L output (at the time of 3-line interlace opposite direction)
1: GUD pin H output (at the time of 3-line interlace the direction of order)
The signal change timing is the same as frame change timing. About frame change timing, refer to 5.4.2 1-frame period timing.</td></tr>
<tr><td>D_3</td><td>LTS1</td><td rowspan="2">Selects set time of calibration.
The calibration function adjusts the frame frequency by setting time of one line. This command can select the set time of a line from the following:
<table><tr><th>LTS1</th><th>LTS0</th><th>1-line time</th><th>1-line frequency</th></tr><tr><td>0</td><td>0</td><td>t_{cal} x 1</td><td>Normal operation x 1</td></tr><tr><td>0</td><td>1</td><td>t_{cal} x 2</td><td>Normal operation x 2</td></tr><tr><td>1</td><td>0</td><td>t_{cal} x 4</td><td>Normal operation x 4</td></tr><tr><td>1</td><td>1</td><td>t_{cal} x 8</td><td>Normal operation x 8</td></tr></table>Remark t_{cal}: Calibration set time = 1 ÷ Frame frequency ÷ Number of displayed lines</td></tr>
<tr><td>D_2</td><td>LTS0</td></tr>
<tr><td>D_1</td><td>OSC1OFF</td><td>This is oscillator circuit stop bit for calibration. This command is stop when in stand-by mode.
0: Oscillator operation
1: Oscillator stop</td></tr>
<tr><td>D_0</td><td>OSC2OFF</td><td>This is oscillator circuit stop bit for LCD display. This command is stop when in stand-by mode.
0: Oscillator operation
1: Oscillator stop</td></tr>
<tr><td>R2</td><td>D_0</td><td>RMOFS</td><td>Offset is applied to the address value of X addresses of the display RAM. The relation between X addresses and an output is set up as follows.
0: Offset OFF, 000H (0) to 0EFH (239)
1: Offset ON, 020H (0) to 0FFH (239)</td></tr>
<tr><td>R3</td><td>D_0</td><td>CRES</td><td>Command reset function. Be sure to execute this bit after power ON.
Command reset automatically clears this bit following execution (RES = 1H). Therefore, it is not necessary to set 0 (select normal operation) again by software. Moreover, since the time required for the value of this bit to change (1 → 0) following command reset execution is extremely short, it is not necessary to secure time until the next command is set following command reset setting.
0: Normal operation
1: Command reset</td></tr>
</table>

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Register	Bit	Symbol	Function
R5	D_7	DTX1	The data bus of the display data at the time of 16-bit parallel data transfer inputted is set. DTX1 = L: 1-pixel/16-bit mode DTX1 = H: 1-pixel/18-bit mode
	D_6	BSTR	Sets the write mode for writing data to the display RAM. If the high-speed RAM write mode is selected, data is written to the display RAM in 2-pixel units inside the IC. When selecting the high-speed RAM write mode, be sure to write data to the display RAM in 2-pixel units. 0: Normal write mode (18-bit access) 1: High-speed RAM write mode (36-bit access)
	D_4	WAS	Window access mode setting When the window access mode is set, the address is increment/decrement only in the range set by the MIN. ·X address setting register (R8), MAX. ·X address setting register (R9), MIN. ·Y address setting register (R10), and MAX. ·Y address setting register (R11). 0: Normal operation 1: Window access mode
	D_2	INC	This bit selects the direction in which the address is to be increment. 0: Increments X address 1: Increments Y address
R6	D_7 to D_0	XAn	This register sets the X address of the display RAM. Set 000H to 0EFH.
R7	D_8 to D_0	YAn	This register sets the Y address of the display RAM. Set 000H to 13FH.
R8	D_7 to D_0	XMINn	Sets the minimum value of the X address in the window access mode. The X address is incremented up to the maximum value set by the MAX. ·X address register (R9), and then initialized to the address value set by this command. Set 000H to 0EFH.
R9	D_7 to D_0	XMAXn	Sets the maximum value of the X address in the window access mode. The X address is incremented up to the maximum value set by the MIN. ·X address register (R8), and then initialized to the address value set by this command. Set 000H to 0EFH.
R10	D_8 to D_0	YMINn	Sets the minimum value of the Y address in the window access mode. The Y address is incremented up to the maximum value set by the MAX. ·Y address register (R11), and then initialized to the address value set by this command. Set 000H to 13FH.
R11	D_8 to D_0	YMAXn	Sets the maximum value of the Y address in the window access mode. The Y address is incremented up to the address value set by this command, and then initialized to the minimum address value set by the MIN. ·Y address register (R10). Set 000H to 13FH.
R13	D_7	RESS0	The source output at the time of /RESET is set up. 0: It is a V_{SS} output at the time of /RESET 1: It is a Hi-Z output at the time of /RESET
	D_6	RESAG	The GOE1 and GOE2 output at the time of /RESET is set up. 0: at the time of /RESET, GOE1 = normal output, GOE2 = L level output 1: at the time of /RESET, GOE1 = L level output, GOE2 = normal output
	D_5	RESSW	The RSW, GSW and BSW output at the time of /RESET is set up. 0: at the time of /RESET, RSW = GSW = BSW = ALL High level output 1: at the time of /RESET, RSW = GSW = BSW = ALL Low level output
	D_2	VPL	The signal polarity of a V_{LD} pin is set up. 0: RAM writing becomes valid at the time of VLD = L. RAM writing becomes invalid at the time of VLD = H. 1: RAM writing becomes valid at the time of VLD = H. RAM writing becomes invalid at the time of VLD = L.

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R14</td><td>D8 to D0</td><td>SSLn</td><td>Scroll area start line register (000H to 13FH)
When the panel is scrolled, the panel of the number of lines set by the scroll area line count register (R15) is scrolled up by the number of steps set by the scroll step count register (R16), starting from the line set by this command.</td></tr>
<tr><td>R15</td><td>D8 to D0</td><td>SAWn</td><td>Scroll area line count register (000H to 13FH)
When the panel is scrolled, the panel of the number of lines set by this command is scrolled up by the number of steps set by the scroll step count register (R16), starting from the line set by the scroll area start line register (R14).</td></tr>
<tr><td>R16</td><td>D8 to D0</td><td>SSTn</td><td>Scroll step count register (000H to 13FH)
When the panel is scrolled, the panel of the number of lines set by the scroll area line count register (R15) and the scroll step count register (R16) is scrolled up by the number of steps set by this command.
Note that because this command is invalid in the partial display mode, the scroll function cannot be used.</td></tr>
<tr><td rowspan="4">R17</td><td>D3</td><td>PSEL</td><td>This bit selects whether the data specified the display color of partial non-display area in PGR, PGG and the PGB bit as color data, using MSB of a display data RAM is used as color data.
0: Use the data specified by PGR, PGG and PGB
1: Display data RAM, making it into color data for MSB of a use.</td></tr>
<tr><td>D2</td><td>PGR</td><td rowspan="3">Sets the color of the panel other than the partial display area during partial display (R0: DTY = 1).
One of eight colors can be selected (RGB: 1 bit each) as the OFF color.
The relationship between each color data and the bits of this register is as follows.
This relationship is not dependent upon the value of ADC.
PGR: R OFF= 0, ON = 1
PGG: G OFF= 0, ON = 1
PGB: B OFF= 0, ON = 1</td></tr>
<tr><td>D1</td><td>PGG</td></tr>
<tr><td>D0</td><td>PGB</td></tr>
<tr><td>R18</td><td>D7 to D0</td><td>BSSPn</td><td>The number of bias-off lines from the blanking period start is set up at the time of source output amplifier bias control register LMD = 1 setup.
<table>
<tr><th>Display Mode</th><th>BSSP = 0 Setting</th><th>It is more than BSSP = 1 at the setting time</th></tr>
<tr><td>Internal OSC display</td><td rowspan="2">It is all the blanking period bias ON.</td><td>The bias OFF between several lines of a setting value and henceforth are bias-turned ON from the blanking period start.</td></tr>
<tr><td>VSYNC/HSYNC/ DOTCLK display</td><td>VFP line number + VSYNV Bias is turned off from several lines which applied the BSSP value −1 to the number of ACT lines, and the blanking period start line, and it bias turns on henceforth.
At the time of through mode, it takes −1 from the above-mentioned calculation.
At the time of three-line interlace mode, several dummy line minutes are subtracted from the above-mentioned formula.
Dummy setup of 1 line: −2 line
Dummy setup of 2 line: −4 line</td></tr>
</table></td></tr>
<tr><td>R20</td><td>D8 to D0</td><td>P1SLn</td><td>Partial1 display area start line register (000H to 13FH)
During partial display (R0: DTY = 1), the area starting from the line set by this command and ending as set by the partial 1 display area line count register (R22) is the partial 1 display area.</td></tr>
</table>

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R21</td><td>D_8 to D_0</td><td>P2SLn</td><td>Partial2 display area start line register (000H to 13FH)
During partial display (R0: DTY = 1), the area starting from the line set by this command and ending as set by the partial 2 display area line count register (R23) is the partial 2 display area.</td></tr>
<tr><td>R22</td><td>D_8 to D_0</td><td>P1AWn</td><td>Partial1 display area line count register (000H to 13FH)
An area starting from the line set by the partial 1 display area start register (R20) and ending as set by this command is the partial 1 display area.
If this register is 0, the values of the partial 2 display area start line register (R21) and the partial 2 display area line count register (R23) are not valid.</td></tr>
<tr><td>R23</td><td>D_8 to D_0</td><td>P2AWn</td><td>Partial 2 display area line count register (000H to 13FH)
An area starting from the line set by the partial 2 display area start register (R21) and ending as set by this command is the partial 2 display area.
If the partial 1 display area line count register is 0, the values of the partial 2 display area start line register (R21) and partial 2 display area line count register (R23) are not valid.</td></tr>
<tr><td>R24</td><td>D_2
D_1
D_0</td><td>E2OPC2
E2OPC1
E2OPC0</td><td>E^2PROM interface is controlled.
<table>
<tr><th>E2OPC2</th><th>E2OPC1</th><th>E2OPC0</th><th>E^2PROM Control</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Setting prohibited</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>EPSAVE: Write in execution to E^2PROM</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>MASKON: Writing / elimination permission to E^2PROM</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>MASKOGF: Writing / elimination permission to E^2PROM</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>EPCLK: All area elimination of E^2PROM</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>EPWALL: It is the writing of FFH to all the area of E^2PROM.</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>EPREAD: Reading execution of E^2PROM</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Setting prohibited</td></tr>
</table></td></tr>
<tr><td>R25</td><td>D_6
D_5
D_4</td><td>DCK2
DCK1
DCK0</td><td>The divided cycle ratio of the external input DOTCLK and a display clock is set up.
<table>
<tr><th>DCK2</th><th>DCK1</th><th>DCK0</th><th>The Divided Cycle Ratio</th><th>1 line input DOTCLK number</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>6 divided cycle</td><td>[240] + [HBP] + [HSYNC ACT] over</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>7 divided cycle</td><td>[280] + [HBP] + [HSYNC ACT] over</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>8 divided cycle</td><td>[320] + [HBP] + [HSYNC ACT] over</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>9 divided cycle</td><td>[360] + [HBP] + [HSYNC ACT] over</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>10 divided cycle</td><td>[400] + [HBP] + [HSYNC ACT] over</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>11 divided cycle</td><td>[440] + [HBP] + [HSYNC ACT] over</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>12 divided cycle</td><td>[480] + [HBP] + [HSYNC ACT] over</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td colspan="2">Setting prohibited</td></tr>
</table></td></tr>
<tr><td></td><td>D_2</td><td>NWRGB</td><td>This bit commands invalid of RGB interface input.
0: Invalid for RGB interface input
1: Valid for RGB interface input</td></tr>
<tr><td></td><td>D_1</td><td>RGBS</td><td>This bit selects RGB interface mode.
0: Through mode
1: Capture mode</td></tr>
<tr><td></td><td>D_0</td><td>DISPCK</td><td>This bit selects timing clock for display output in RGB interface mode.
0: Internal oscillator clock
1: HSYNC/VSYNC/DOTCLK</td></tr>
</table>

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Register	Bit	Symbol	Function
R26	D_7 to D_4	HBPn	This bit sets horizontal back porch period of RGB interface. Horizontal back porch period = set value x DOTCLK unit In addition, set up more than "1".
	D_3 to D_0	VBPn	This bit sets vertical back porch period of RGB interface. Vertical back porch period = set value x HSYNC unit In addition, set up more than "2".
R27	D_8 to D_0	RGBSTn	These bits set the start line of the display area to be displayed by the RGB interface. (000H ≤ R27 ≤ 0EEH) Be sure to observe the relationship "Set value of R27 register < Set value of R28 register".
R28	D_8 to D_0	RGBEDn	These bits set the end line of the display area to be displayed by the RGB interface. (000H ≤ R28 ≤ 13FH) Be sure to observe the relationship "Set value of R27 register < Set value of R28 register".
R29	D_7 to D_0	CAPXMINn	Minimum of X address is set up at the time of window access at the time of selecting capture mode by the RGB interface.
R30	D_7 to D_0	CAPXMAXn	Maximum of X address is set up at the time of window access at the time of selecting capture mode by the RGB interface.
R31	D_8 to D_0	CAPYMINn	Minimum of Y address is set up at the time of window access at the time of selecting capture mode by the RGB interface.
R32	D_8 to D_0	CAPYMAXn	Maximum of Y address is set up at the time of window access at the time of selecting capture mode by the RGB interface.
R33	D_7 to D_0	E2An	The writing address to E^2PROM is specified.
R34	D_0	OC	This bit is used for calibration. The time from calibration start command execution until calibration stop command execution becomes the time for 1 line. 0: Calibration stop 1: Calibration start
R38	D_7 to D_0	PSD1n	The value set as PSD1n is outputted from the serial interface output for external IC control. For more details, refer to **5.1.8 Serial interface for power supply IC control**.
R39	D_7 to D_0	PSD2n	The value set as PSD2n is outputted from the serial interface output for external IC control. For more details, refer to **5.1.8 Serial interface for power supply IC control**.
R40	D_7 to D_0	PSD3n	The value set as PSD3n is outputted from the serial interface output for external IC control. For more details, refer to **5.1.8 Serial interface for power supply IC control**.
R41	D_7 to D_0	PSD4n	The value set as PSD4n is outputted from the serial interface output for external IC control. For more details, refer to **5.1.8 Serial interface for power supply IC control**.
R42	D_7 to D_0	PSD5n	The value set as PSD5n is outputted from the serial interface output for external IC control. For more details, refer to **5.1.8 Serial interface for power supply IC control**.
R43	D_4	GSEL	Sets the maximum/minimum output potential of the γ–correction register. If the internal γ-output adjustment circuit is selected, the maximum/minimum output potential of the γ-correction register is: 0: Sets power supply voltage (outputs V_S and V_{SS} potential). 1: Uses voltage of internal γ-output adjustment circuit (uses VPH, VNH, VPL, VNL output)
	D_0	GONSEL	About connection between γ-correction resistance and a power supply 0: Connect the both ends of positive-polarity γ-resistance with V_S and GND when in used γ-correction by positive-polarity. On the other hand, γ-resistance by negative-polarity does not connect with V_S and GND. Moreover, the both ends of negative-polarity γ-resistance are connected with V_S and GND when in used γ-correction by negative-polarity. In that case, γ-resistance by positive-polarity does not connect with V_S and GND. 1: Connect both V_S and GND on the side of positive and negative γ-correction regardless of output from positive- or negative-polarity.

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Register	Bit	Symbol	Function
R44	D_7 to D_0	GPHn	Sets the voltage value of γ-amplitude adjustment of positive polarity. For more detail, refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R45	D_7 to D_0	GNHn	Sets the voltage value of γ-amplitude adjustment of negative polarity. For more detail, refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R46	D_7 to D_0	GPLn	Sets the voltage value of γ-amplitude adjustment of positive polarity. For more detail, refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R47	D_7 to D_0	GNLn	Sets the voltage value of γ-amplitude adjustment of negative polarity. For more detail, refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R48	D_7 to D_4	VDRPn	Positive-polarity γ-amplitude adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_3 to D_0	VSRPn	Positive-polarity γ-amplitude adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R49	D_7 to D_4	VLRPn	Positive-polarity γ-inclination adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_3 to D_0	VHRPn	Positive-polarity γ-inclination adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R50	D_6 to D_4	VGR1Pn	Positive-polarity γ-fine tuning adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_2 to D_0	VGR0Pn	Positive-polarity γ-fine tuning adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R51	D_6 to D_4	VGR3Pn	Positive-polarity γ-fine tuning adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_2 to D_0	VGR2Pn	Positive-polarity γ-fine tuning adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R52	D_7 to D_4	VDRNn	Negative-polarity γ-amplitude adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_3 to D_0	VSRNn	Negative-polarity γ-amplitude adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R53	D_7 to D_4	VLRNn	Negative-polarity γ-inclination adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_3 to D_0	VHRNn	Negative-polarity γ-inclination adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R54	D_6 to D_4	VGR1Nn	Negative-polarity γ-fine tuning adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_2 to D_0	VGR0Nn	Negative-polarity γ-fine tuning adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R55	D_6 to D_4	VGR3Nn	Negative-polarity γ-fine tuning adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_2 to D_0	VGR2Nn	Negative-polarity γ-fine tuning adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R56	D_1, D_0	GV8S1	The voltage concerning a panel is set at the time of 8-color mode. 0 : Set power supply 1: Set amplifier output
R57	D_7 to D_0	E2IRn	The index which writes in to address to E^2PROM is specified. The index and data of the register specified to be this register are written in the address of E^2PROM specified by R33.
R58	D_7 to D_0	E2SAn	The reading start address of E^2PROM is specified.

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td rowspan="4">R59</td><td>D7</td><td>WHP</td><td>Sets the output mode of the reference voltage generator amplifier for setting the white level of the positive-polarity and negative-polarity sides (when VPL and VNL are normally white), as shown below.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
0: Normal mode
1: High-power mode (output circuit capacity: twice that of normal mode)</td></tr>
<tr><td>D6 to D4</td><td>WIn</td><td>Sets the output bias current of the reference voltage generator amplifier for setting the white level of the positive-polarity and negative-polarity sides (when VPL and VNL are normally white), as shown below.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
<table>
<tr><th>WI2</th><th>WI1</th><th>WI0</th><th>Amplifier Bias Current</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0.025 μA</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0.050 μA</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0.100 μA</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0.200 μA</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0.500 μA</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1.000 μA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1.500 μA</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>2.000 μA</td></tr>
</table></td></tr>
<tr><td>D3</td><td>BHP</td><td>Sets the output mode of the reference voltage generator amplifier for setting the black level of the positive-polarity and negative-polarity sides (when VPH and VNH are normally white), as shown below.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
0: Normal mode
1: High-power mode (output circuit capacity: twice that of normal mode)</td></tr>
<tr><td>D2 to D0</td><td>BIn</td><td>Sets the output bias current of the reference voltage generator amplifier for setting the black level of the positive-polarity and negative-polarity sides (when VPH and VNH are normally white), as shown below.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
<table>
<tr><th>BI2</th><th>BI1</th><th>BI0</th><th>Amplifier Bias Current</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0.025 μA</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0.050 μA</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0.100 μA</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0.200 μA</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0.500 μA</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1.000 μA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1.500 μA</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>2.000 μA</td></tr>
</table></td></tr>
</table>

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R60</td><td>D7 to D0</td><td>PSD6n</td><td>The value set as PSD6n is outputted from the serial interface output for external IC control. For more details, refer to 5.1.8 Serial interface for power supply IC control.</td></tr>
<tr><td>R61</td><td>D7 to D0</td><td>PSD7n</td><td>The value set as PSD7n is outputted from the serial interface output for external IC control. For more details, refer to 5.1.8 Serial interface for power supply IC control.</td></tr>
<tr><td>R62</td><td>D7 to D0</td><td>PSD8n</td><td>The value set as PSD8n is outputted from the serial interface output for external IC control. For more details, refer to 5.1.8 Serial interface for power supply IC control.</td></tr>
<tr><td>R63</td><td>D7 to D0</td><td>PSD9n</td><td>The value set as PSD9n is outputted from the serial interface output for external IC control. For more details, refer to 5.1.8 Serial interface for power supply IC control.</td></tr>
<tr><td>R64</td><td>D7 to D0</td><td>PSDAn</td><td>The value set as PSDAn is outputted from the serial interface output for external IC control. For more details, refer to 5.1.8 Serial interface for power supply IC control.</td></tr>
<tr><td>R65</td><td>D7 to D0</td><td>PSDBn</td><td>The value set as PSDBn is outputted from the serial interface output for external IC control. For more details, refer to 5.1.8 Serial interface for power supply IC control.</td></tr>
<tr><td rowspan="4">R66</td><td>D6</td><td>LACE3</td><td>3-line interlace display function is selected.
When select 3-line interlace display, blanking period setting register between frames (R75) should set four lines or more and a timing circuit selection register (R78:D7) as 0.
Refer to the 5.4.3 3-line interlace for operation of 3-line interlace.
In addition, this command is executed from the following frame after transmission.
0: Normal display (Non-Interlace display).
1: 3-line interlace display</td></tr>
<tr><td>D5</td><td>LACE2</td><td>The number of the dummy lines between the fields at the time of 3-line interlace display is selected.
In addition, this command is executed from the following frame after transmission.
0: Dummy 2-line 1: Dummy 1-line</td></tr>
<tr><td>D4
D3</td><td>LACE1
LACE0</td><td>The field selection signals EXT1 and EXT2 at the time of a 3-line interlace display change, and a position is selected.
<table>
<tr><th>LACE1</th><th>LACE0</th><th>Changing line</th><th>Changing timing</th></tr>
<tr><td>0</td><td>0</td><td>Just before GSTB output line</td><td>GCLK rising timing</td></tr>
<tr><td>0</td><td>1</td><td>Just before GSTB output line</td><td>GCLK falling timing</td></tr>
<tr><td>1</td><td>0</td><td>Line during GSTB output</td><td>GCLK rising timing</td></tr>
<tr><td>1</td><td>1</td><td>Line during GSTB output</td><td>GCLK falling timing</td></tr>
</table>
In addition, this command is executed from the following frame after transmission.</td></tr>
<tr><td>D2
D1</td><td>LMD2
LMD1</td><td>AMP drive ON/OFF of source output is selected.
<table>
<tr><th>LMD2</th><th>LMD1</th><th>Display Line</th><th>Blanking Period</th><th>8-color line (partial not displayed)</th></tr>
<tr><td>0</td><td>0</td><td>R/G/BSW period ON</td><td>Between the whole period OFF</td><td>Between the whole period OFF</td></tr>
<tr><td>0</td><td>1</td><td>Between the whole period ON</td><td>Between the whole period OFF</td><td>Between the whole period OFF</td></tr>
<tr><td>1</td><td>0</td><td>R/G/BSW period ON</td><td>The line period OFF set up by BSSPn (R18) from the Blanking period start. The line after it is R/G/BSW period ON.</td><td>Between the whole period OFF</td></tr>
<tr><td>1</td><td>1</td><td>Between the whole period ON</td><td>The line period OFF set up by BSSPn (R18) from the blanking period start. The line after it is between the whole period ON.</td><td>Between the whole period ON</td></tr>
</table></td></tr>
</table>

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R68</td><td>D_6 to D_4</td><td>REFMn</td><td>When partial display, the case where it is set as non-refreshing drive ([GSM = 0, PT1 = 1, PT0 = 1] and [GSM = 1, PT1 = 0, PT0 = 0]), non-refreshing frame (source output stop, gate scanning stop) and a refresh cycle (source white level output [the normally white panel], gate scan) are set up in the combination of the value set as this flag and the value set as the REFBn flag.
For more details, refer to 5.6.2 Partial display, non-display area and normal partial driving.
The number of non-refreshing frames = REFB [4:0] x REFM [3:0]

<table>
<tr><th>REFM2</th><th>REFM1</th><th>REFM0</th><th>Setting Value</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>8</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>16</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>32</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>64</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>128</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>256</td></tr>
</table>
</td></tr>
<tr><td></td><td>D_3 to D_0</td><td>REFBn</td><td>When partial display, the case where it is set as non-refreshing drive ([GSM = 0, PT1 = 1, PT0 = 1] and [GSM = 1, PT1 = 0, PT0 = 0]), non-refreshing frame (source output stop, gate scanning stop) and a refresh cycle (source white level output [the normally white panel], gate scan) are set up in the combination of the value set as this flag and the value set as the REFMn flag.
For more details, refer to 5.6.2 Partial display, non-display area and normal partial driving.
The number of non-refreshing frames = REFB [4:0] x REFM [3:0]

<table>
<tr><th>REFB3</th><th>REFB2</th><th>REFB1</th><th>REFB0</th><th>Setting Value</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Only non-refresh drive</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>14</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>15</td></tr>
</table>
</td></tr>
</table>

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R72</td><td>D7
D6
D5</td><td>DC4
DC3
DC2</td><td>The frequency of the clock outputted from the PCCLK pin used as clocks, such as a DC/DC converter circuit of a power supply IC, is set up. This clock is generated from oscillation frequency (fosc) or external clock DOTCLK, is cycle ratio by the number of setting of this flag, and is outputted.
<table>
<tr><th rowspan="2">DC4</th><th rowspan="2">DC3</th><th colspan="2">PCCLK Clock Frequency</th></tr>
<tr><th>DC2 = 0</th><th>DC2 = 1</th></tr>
<tr><td>0</td><td>0</td><td>fosc ÷ 4</td><td>DOUTCLK ÷ 32</td></tr>
<tr><td>0</td><td>1</td><td>fosc ÷ 8</td><td>DOUTCLK ÷ 64</td></tr>
<tr><td>1</td><td>0</td><td>fosc ÷ 16</td><td>DOUTCLK ÷ 128</td></tr>
<tr><td>1</td><td>1</td><td>fosc ÷ 32</td><td>DOUTCLK ÷ 256</td></tr>
</table>
Remark When outputs a clock signal from PCCLK pin, it is necessary to operate an oscillation circuit (OSC2OFF [R1] = 0).</td></tr>
<tr><td></td><td>D4 to D0</td><td>DSCGn</td><td>To compensate for a XDON output H output (it outputs from the next frame of RXDON = H), the output of ASW3, ASW2 and ASW1 are considered as the line period H output fixation set up with this flag. The output of ASW3, ASW2, ASW1, STV, CKV, FR and OEV are carried out to L output fixation after setting period.
When DSCGn = 000H setup, the output of ASW3, ASW2, ASW1, STV, CKV, FR and OEV are carried out to L output fixation to a XDON output H output (it outputs from the next frame of RXDON = H) and this timing.
For more details, refer to 5.8 Power Supply Sequence.
<table>
<tr><th>DSCG4</th><th>DSCG3</th><th>DSCG2</th><th>DSCG1</th><th>DSCG0</th><th>Setting Line Count</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>31</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>32</td></tr>
</table></td></tr>
<tr><td>R73</td><td>D3 to D0</td><td>BCONBn</td><td>The bias current for the liquid crystal drive AMP is set up.
<table>
<tr><th>BCONB3</th><th>BCONB2</th><th>BCONB1</th><th>BCONB0</th><th>Bias Current [μA]</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0.87</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1.67</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>2.43</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>3.18</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>3.98 (default)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>4.70</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>5.41</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>6.11</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>6.88</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>7.57</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>8.24</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>8.91</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>9.62</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>10.28</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>10.93</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>11.58</td></tr>
</table></td></tr>
</table>

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R75</td><td>D_7 to D_0</td><td>ADLNn</td><td>The number of lines set up by this register is set up as the number of lines of the FP [2 Line fixed] + BP period of a frame changing.
For more details, refer to 5.4.2 1-frame period timing.
ADLNn ≤ 2: Only BP period
ADLNn > 3: FP line count [2-line] + BP period line count = Setting line count = ADLNn setting value

<table>
<tr><th>ADLN7</th><th>ADLN6</th><th>ADLN5</th><th>ADLN4</th><th>ADLN3</th><th>ADLN2</th><th>ADLN1</th><th>ADLN0</th><th>Setting line count</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting prohibited</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>BP1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>BP2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>FP2 + BP1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>FP2 + BP2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>FP2 + BP3</td></tr>
<tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>FP2 + BP252</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>FP2 + BP253</td></tr>
</table>
</td></tr>
<tr><td>R76</td><td>D_4 to D_0</td><td>ADCKn</td><td>The number of clocks set up by this register is inserted as a dummy clock within 1-line drive period.
For more details, refer to 5.4.1 1-line period timing.

<table>
<tr><th>ADCK4</th><th>ADCK3</th><th>ADCK2</th><th>ADCK1</th><th>ADCK0</th><th>Setting Clock Count</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting prohibited</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>30</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>31</td></tr>
</table>
</td></tr>
</table>

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td rowspan="8">R77</td><td>D7
D6</td><td>RPCK1
RPCK0</td><td>ON/OFF control of the clock outputted from the PCCLK pin used as clocks, such as DC/DC converter circuit of power supply IC, is performed.

<table><tr><th>RPCK1</th><th>RPCK0</th><th>PCCLK clock output ON/OFF</th></tr><tr><td>0</td><td>0</td><td>The output ON during the whole period</td></tr><tr><td>0</td><td>1</td><td>The output OFF during the whole period</td></tr><tr><td>1</td><td>0</td><td>It output turns on the blanking period output OFF and except it.</td></tr><tr><td>1</td><td>1</td><td>The output OFF during the whole period</td></tr></table></td></tr>
<tr><td>D5</td><td>RSOUT</td><td>Operation of source output (Yn) is controlled.
0: OFF (VSS output fixed)
1: ON (Normal operation)
Setting by this flag becomes valid from the output timing of the following frame after inputted.
About the change timing of the frame, refer to 5.4.2 1-frame period timing.</td></tr>
<tr><td>D4</td><td>RGOE2</td><td>Operation of panel discharge is controlled.
0: GOE2 (H output), RSW, GSW and BSW (Normal operation)
1: GOE2 (L output), RSW, GSW and BSW (H fixed)
Setting by this flag becomes valid from the output timing of the following frame after inputted.
About the change timing of the frame, refer to 5.4.2 1-frame period timing.</td></tr>
<tr><td>D3</td><td>RGOE1</td><td>Operation of gate output enable signal is controlled.
0: OFF (VSS output fixed)
1: ON (Normal operation)
Setting by this flag becomes valid from the output timing of the following frame after inputted.
About the change timing of the frame, refer to 5.4.2 1-frame period timing.</td></tr>
<tr><td>D2</td><td>RXDON</td><td>Operation of panel discharge is controlled.
0: XDON (L output), ASW1, ASW2 and ASW3 (Normal operation)
1: XDON (H output), ASW1, ASW2 and ASW3 (H fixed)
Setting by this flag becomes valid from the output timing of the following frame after inputted.
About the change timing of the frame, refer to 5.4.2 1-frame period timing.</td></tr>
<tr><td>D1</td><td>ROEVE</td><td>OEVE output operation is controlled.
0: OEVE (L fixed)
1: OEVE (H fixed)
Setting by this flag becomes valid from the output timing of the following frame after inputted.
About the change timing of the frame, refer to 5.4.2 1-frame period timing.</td></tr>
<tr><td>D0</td><td>ROEV</td><td>Operation of output enable signal (OEV) is controlled.
0: OFF (L output fixed)
1: ON (Normal operation)
Setting by this flag becomes valid from the output timing of the following frame after inputted.
About the change timing of the frame, refer to 5.4.2 1-frame period timing.</td></tr>
</table>

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td rowspan="5">R78</td><td>D7</td><td>TCKSL</td><td>A liquid crystal control timing circuit is selected.
0: Timing Circuit 1 (GSTB, GCLK, GOE, GOE2, RSW, GSW, BSW, and GUD)
1: Timing Circuit 2 (STV, CKV, OEVE, OEV, ASW1, ASW2, ASW3, and XDON)
In addition, as for 3-line interlace display function, only the timing circuit 1 corresponds.</td></tr>
<tr><td>D6</td><td>RMMSK</td><td>The mask of the data of display RAM is carried out by "0" data.0: All "0" data mask
1: RAM data enable (Normal operation)</td></tr>
<tr><td>D5</td><td>RMST1</td><td rowspan="2">It sets up about operation of power supply supplied to RAM circuit.
<table><tr><th>RMST1</th><th>RMST0</th><th>Display RAM Power Supply</th><th>Display RAM State</th></tr><tr><td>0</td><td>0</td><td>Power OFF</td><td>RAM data is abandoned</td></tr><tr><td>0</td><td>1</td><td>Low Power</td><td>RAM data maintenance Note1</td></tr><tr><td>1</td><td>0</td><td>Power ON</td><td>RAM writing operation is possible Note2</td></tr><tr><td>1</td><td>1</td><td colspan="2">Setting prohibited</td></tr></table>Notes 1. Sleep mode etc. can be used when low power consumption and RAM data need to be held. When normal operation, do not set up (Display ON, writing of display data).
2. When normal operation, use it in this mode (Display ON, writing of display data).</td></tr>
<tr><td>D4</td><td>RMST0</td></tr>
<tr><td>D3</td><td>PT1</td><td rowspan="2">When partial display, the drive of non-display area can be selected by setup of PT1, PT0 and GSM [R0] as shown in below.
For more details, refer to 5.6.1 Partial display, non-display area driving.
<table><tr><th>GSM [R0]</th><th>PT1</th><th>PT0</th><th>Partial Display Operation</th></tr><tr><td rowspan="4">0</td><td>0</td><td>0</td><td rowspan="3">Normal partial drive</td></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>Non-refresh drive 1</td></tr><tr><td rowspan="2">1</td><td>0</td><td>0</td><td>Non-refresh drive 2</td></tr><tr><td colspan="2">Other than above</td><td>Setting prohibited</td></tr></table></td></tr>
<tr><td>D2</td><td>PT0</td></tr>
<tr><td>D1</td><td>REV</td><td>The gray-scale level of source output is inverted.
0: Normal operation
1: Gray-scale inversion output</td></tr>
<tr><td>R79</td><td>D5 to D0</td><td>GOSTn</td><td>The start timing of the signal outputted from GOE1 (/GOE1) and OEV (/OEV) pin is set up.
Set up in the range 001H ≤ R79 ≤ 026H.
In addition, prohibited for setting up the same value as R79 and R80.</td></tr>
<tr><td>R80</td><td>D5 to D0</td><td>GOEDn</td><td>The end timing of the signal outputted from GOE1 (/GOE1) and OEV (/OEV) pin is set up.
Set up in the range 001H ≤ R80 ≤ 026H.
In addition, prohibited for setting up the same value as R79 and R80.</td></tr>
<tr><td>R83</td><td>D5 to D0</td><td>RSTn</td><td>The start timing of the signal outputted from RSW (/RSW) and ASW1 (/ASW1) pin is set up.
Set up in the range 002H ≤ R83 ≤ 025H.
In addition, prohibited for setting up the same value as R83 and R84.</td></tr>
</table>

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Register	Bit	Symbol	Function
R84	D_5 to D_0	REDn	The end timing of the signal outputted from RSW (/RSW) and ASW1 (/ASW1) pin is set up. Set up in the range 002H ≤ R84 ≤ 025H. In addition, prohibited for setting up the same value as R83 and R84.
R85	D_5 to D_0	GSTn	The start timing of the signal outputted from GSW (/GSW) and ASW2 (/ASW2) pin is set up. Set up in the range 002H ≤ R85 ≤ 025H. In addition, prohibited for setting up the same value as R85 and R86.
R86	D_5 to D_0	GEDn	The end timing of the signal outputted from GSW (/GSW) and ASW2 (/ASW2) pin is set up. Set up in the range 002H ≤ R86 ≤ 025H. In addition, prohibited for setting up the same value as R85 and R86.
R87	D_5 to D_0	BSTn	The start timing of the signal outputted from BSW (/BSW) and ASW3 (/ASW3) pin is set up. Set up in the range 002H ≤ R87 ≤ 025H. In addition, prohibited for setting up the same value as R87 and R88.
R88	D_5 to D_0	BEDn	The end timing of the signal outputted from BSW (/BSW) and ASW3 (/ASW3) pin is set up. Set up in the range 002H ≤ R88 ≤ 025H. In addition, prohibited for setting up the same value as R87 and R88.
R89	D_5 to D_0	E1STn	The start timing of the signal outputted from EXT1 (/EXT1) pin is set up. Set up in the range 001H ≤ R89 ≤ 026H. In addition, when unused output signal from these pins, set up the same value as R89 and R90. In default, these bits are fixed to EXT1 = L, /EXT1 = H. By liquid crystal control timing circuit selection register (R78:D_7) = 1, this setup becomes valid, only when the timing circuit 2 is selected.
R90	D_5 to D_0	E1EDn	The end timing of the signal outputted from EXT1 (/EXT1) pin is set up. Set up in the range 001H ≤ R90 ≤ 026H. In addition, when unused output signal from these pins, set up the same value as R89 and R90. By liquid crystal control timing circuit selection register (R78:D_7) = 1, this setup becomes valid, only when the timing circuit 2 is selected.
R91	D_5 to D_0	E2STn	The start timing of the signal outputted from EXT2 (/EXT2) pin is set up. Set up in the range 001H ≤ R91 ≤ 026H. In addition, when unused output signal from these pins, set up the same value as R91 and R92. In default, these bits are fixed to EXT2 = L, /EXT2 = H. By liquid crystal control timing circuit selection register (R78:D_7) = 1, this setup becomes valid, only when the timing circuit 2 is selected.
R92	D_5 to D_0	E2EDn	The end timing of the signal outputted from EXT2 (/EXT2) pin is set up. Set up in the range 001H ≤ R92 ≤ 026H. In addition, when unused output signal from these pins, set up the same value as R91 and R92. By liquid crystal control timing circuit selection register (R78:D_7) = 1, this setup becomes valid, only when the timing circuit 2 is selected.

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Register	Bit	Symbol	Function
R93	D_6	RVCOT	Operation of common timing signal (VCOUT) is controlled. 0: VCOUT signal and FR signal OFF (L output fixed) 1: VCOUT signal and FR signal ON (Normal operation) Setting by this flag becomes valid from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_5	RGBSW	Operation of panel multi-plexus signal (RSW, GSW, BSW) is controlled. 0: OFF (L output fixed) 1: ON (Normal operation) Setting by this flag becomes valid from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_4	RGSTB	Operation of the strobe signal for gate control (GSTB) is controlled. 0: OFF (H output fixed) 1: ON (Normal operation) Setting by this flag becomes valid from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_3	RGCLK	Operation of the clock signal for gate control (GCLK) is controlled. 0: OFF (L output fixed) 1: ON (Normal operation) Setting by this flag becomes valid from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_2	RASW	Operation of panel multi-plexus signal (ASW1, ASW2, ASW3) is controlled. 0: OFF (L output fixed) 1: ON (Normal operation) Setting by this flag becomes valid from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_1	RSTV	Operation of the start signal for gate control (STV) is controlled. 0: OFF (L output fixed) 1: ON (Normal operation) Setting by this flag becomes valid from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_0	RCKV	Operation of the clock signal for gate control (CKV) is controlled. 0: OFF (L output fixed) 1: ON (Normal operation) Setting by this flag becomes valid from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.

9. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_S	–0.5 to +6.0	V
Power supply voltage	V_{DD1}	–0.5 to +2.2	V
Power supply voltage	V_{DD2}	–0.5 to +2.2	V
Power supply voltage	V_{DDIO}	–0.5 to +4.6	V
Power supply voltage	V_{CC1}	–0.5 to +4.6	V
γ-correction power supply	V_1 to V_5	–0.5 to V_S + 0.5	V
Input voltage	V_{I1}	–0.5 to V_{DDIO} + 0.5	V
Input voltage	V_{I2}	–0.5 to V_{CC1} + 0.5	V
Input current	I_I	±10	mA
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_S	4.0	5.0	5.5	V
Power supply voltage	V_{DD1}	1.6		2.0	V
Power supply voltage	V_{DD2}	1.6		2.0	V
Power supply voltage	V_{DDIO}	1.8		3.3	V
Power supply voltage	V_{CC1}	2.5		3.3	V
Input voltage	V_{I1} Note1	0		V_{DDIO}	V
Input voltage	V_{I2} Note2	0		V_{CC1}	V

Notes 1. About pins of V_{DDIO} power supply system: /CS, /RD (E), /WR (R,/W), D_0 to D_{17}, RS, /RESET, etc.

2. About pins of V_{CC1} power supply system: PSX, C86, TOUT0 to TOUT19, GOE1, GOE2, GSTB, GCLK, TSTRTST, TSTVIHL, etc.

Electrical Specifications (Unless Otherwise Specified, T_A = –40 to +85°C, V_{DD1} = V_{DD2} = 1.6 to 2.0 V, V_{CC1} = 2.5 to 3.3 V, V_{DDIO} = 1.8 to 3.3 V, V_S = 4.0 to 5.5 V)

Parameter	Symbol	Condition	MIN.	TYP.[Note1]	MAX.	Unit
High level input voltage	V_{IH1}	V_{DDIO}	0.8 V_{DDIO}			V
	V_{IH2}	V_{CC1}	0.8 V_{CC1}			V
Low level input voltage	V_{IL1}	V_{DDIO}			0.2 V_{DDIO}	V
	V_{IL2}	V_{CC1}			0.2 V_{CC1}	V
High level output voltage	V_{OH1}	V_{DDIO}, I_{OUT} = –1 mA	0.8 V_{DDIO}			V
	V_{OH2}	V_{CC1}, I_{OUT} = –1 mA	0.8 V_{CC1}			V
Low level output voltage	V_{OL1}	V_{DDIO}, I_{OUT} = 1 mA			0.2 V_{DDIO}	V
	V_{OL2}	V_{CC1}, I_{OUT} = 1 mA			0.2 V_{CC1}	V
High level input current	I_{IH1}	V_{DDIO}			1	μA
	I_{IH2}	V_{CC1}			1	μA
Low level input current	I_{IL1}	V_{DDIO}			–1	μA
	I_{IL2}	V_{CC1}			–1	μA
High level leakage current	I_{LIH}	D_0 to D_{17}			1	μA
Low level leakage current	I_{LIL}	D_0 to D_{17}			–1	μA
High level driver output current	I_{VOH}	V_X = 3.5 V, V_{OUT} = 3.0 V, V_S = 5.0 V			–25	μA
Low level driver output current	I_{VOL}	V_X = 1.5 V, V_{OUT} = 2.0 V, V_S = 5.0 V	25			μA
Current consumption	I_{DDIO}	V_{DDIO} (when non-access CPU)			5	μA
	I_{CC1}	V_{CC1} (when non-access CPU)			400	μA
	I_{STBY}	V_{DDIO}			1	μA
		V_{CC1} (STBY mode)			50	μA
		V_{CC1} (DEEP SLEEP)			200	μA
		V_{CC1} (SLEEP mode)			300	μA
	I_S	260,000-color mode[Note2]			1.5	μA
		8-color mode[Note2]			50	μA
		Stand-by mode			5	μA
Output voltage deviation	ΔV_O	V_S = 5.0 V, V_{OUT} = 1.65 V[Note3]			10	mV
		V_S = 5.0 V, V_{OUT} = 2.50 V[Note3]			10	mV

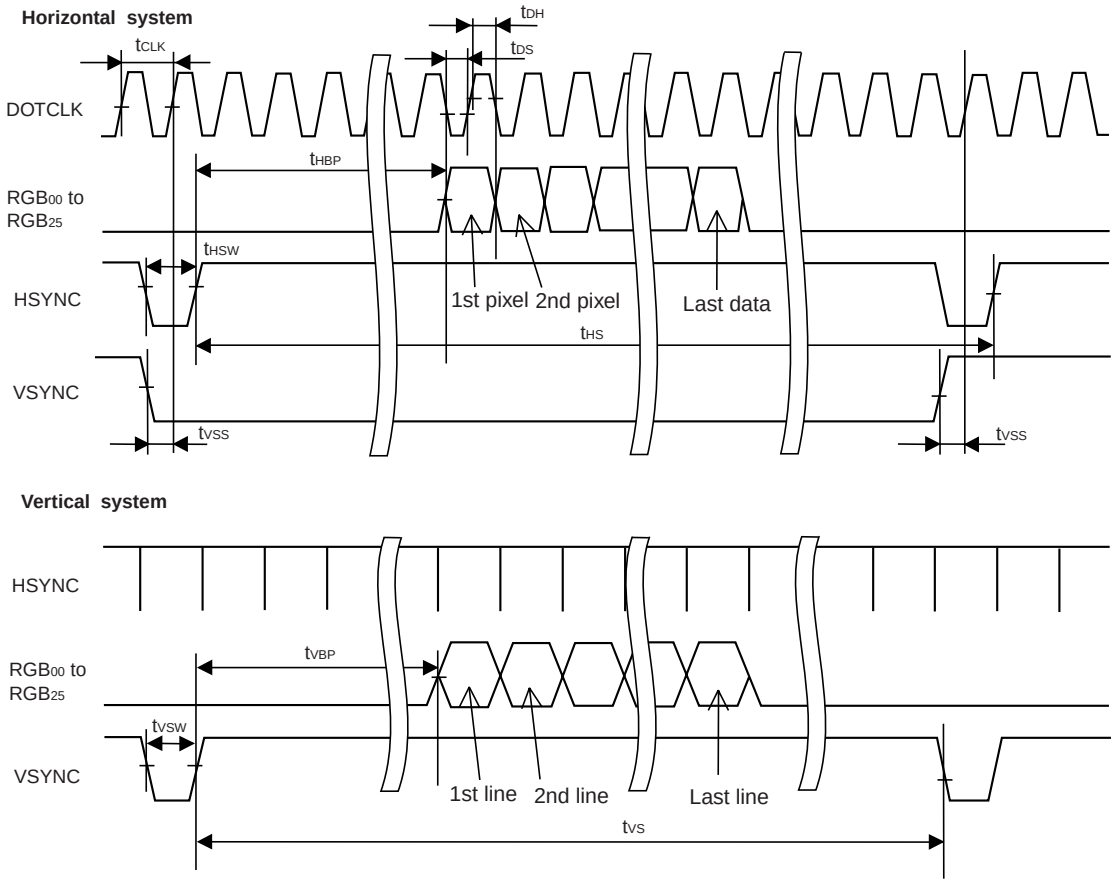
Notes 1. TYP. values are reference values when T_A = 25°C

2. Frame frequency: 60 Hz, line inversion mode selection, dot checkerboard input pattern, and no load.

3. V_X: The output voltage of analog output pins Y_1 to Y_{240}, V_{OUT}: The application voltage of analog output pins Y_1 to Y_{240}.

AC Characteristics (Unless Otherwise Specified, T_A = –40 to +85°C, V_{DD1} = V_{DD2} = 1.6 to 2.0 V, V_{CC1} = 2.5 to 3.3 V, V_S = 4.0 to 5.5 V)

(a) RGB interface



Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Dot clock cycle time	t_{CLK}		150			ns
Dot clock high level pulse width	t_{CLKH}		75			ns
Dot clock low level pulse width	t_{CLKL}		75			ns
Data setup time	t_{DS}		60			ns
Data hold time	t_{DH}		60			ns
HSYNC pulse width	t_{HSW}		1			DOTCLK
Horizon period back porch time	t_{HBP}		1			DOTCLK
VSYNC pulse width	t_{VSW}		1			HS
VSYNC setup time	t_{VSS}		60			ns
Vertical period back porch time	t_{VBP}		2			HS

Note TYP. values are reference values when T_A = 25°C.

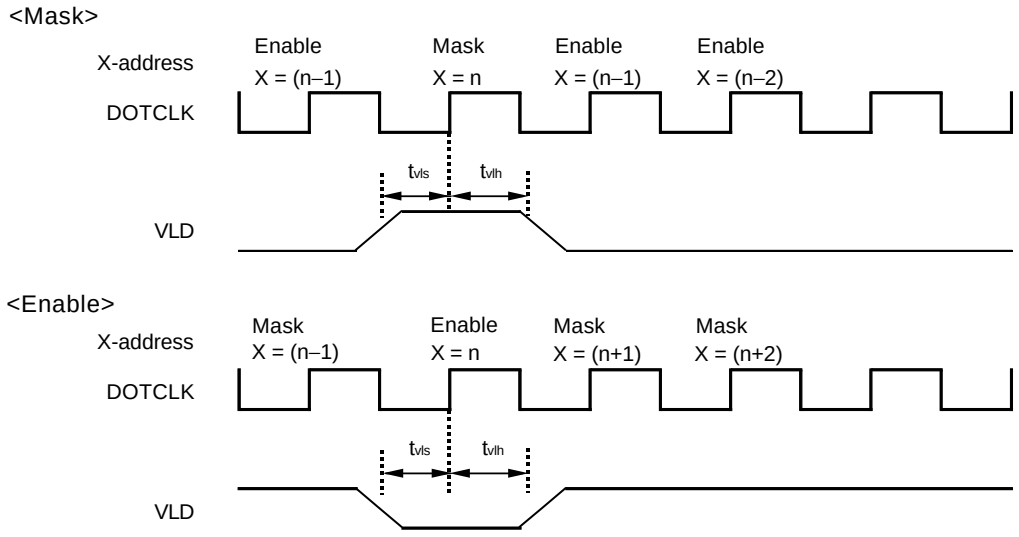
Remarks 1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC1}.

3. One frame period ≥ VSYNC active period (1 HS) + VBP value (2 HS) + display line count (320 HS) = 323-line period (HS)

4. 1 line period HSYNC active period (1 DOTCLK) + HBP value (1 DOTCLK) + display pixel count (240 DOTCLK) = 242 clock period (DOTCLK)

(b) RGB interface capture mode VLD function



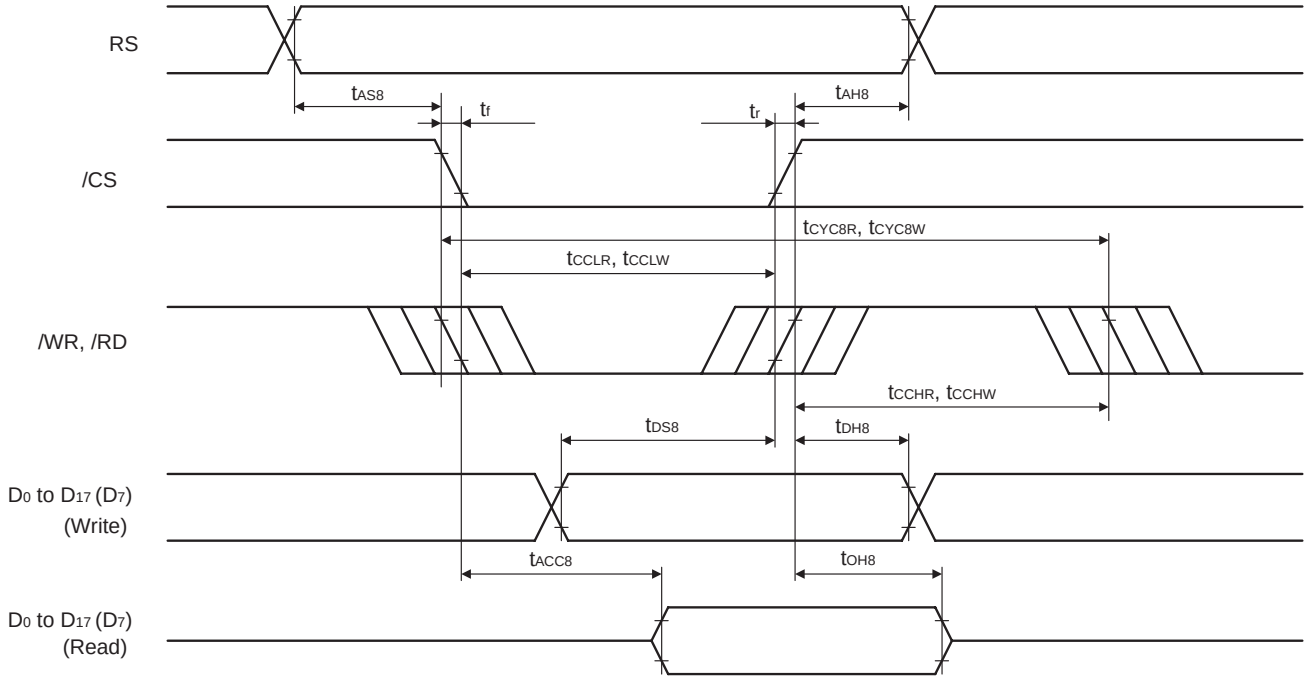
Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
VLD setup time	t_{VLS}		60			ns
VLD hold time	t_{VLH}		60			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC1}.

(c) i80 series CPU interface



When V_{DD1} = V_{DD2} = 1.6 to 2.0 V, V_{CC1} = 2.5 to 3.3 V (normal write mode)

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	10			ns
Address setup time	t_{AS8}	RS	10			ns
System cycle time (when write)	t_{CYC8W}	VSTBY = Low R98 = 005H	100			ns
		VSTBY = High V_{DD1} = V_{DD2} = 1.7 MIN. R98 = 005H	100			ns
System cycle time (when read)	t_{CYC8R}		250			ns
Control low-level pulse width (/WR)	t_{CCLW}	/WR	25			ns
Control low-level pulse width (/RD)	t_{CCLR}	/RD	140			ns
Control high-level pulse width (/WR)	t_{CCHW}	/WR	20			ns
Control high-level pulse width (/RD)	t_{CCHR}	/RD	80			ns
Data setup time	t_{DS8}	D_0 to D_{17}	25			ns
Data hold time	t_{DH8}	D_0 to D_{17}	10			ns
/RD access time	t_{ACC8}	D_0 to D_{17}, C_L = 100 pF			140	ns
Output disable time	t_{OH8}	D_0 to D_{17}, C_L = 100 pF	5		140	ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC1}.

When V_{DD1} = V_{DD2} = 1.6 to 2.0 V, V_{CC1} = 2.5 to 3.3 V (high-speed RAM write mode, valid only for writing data)

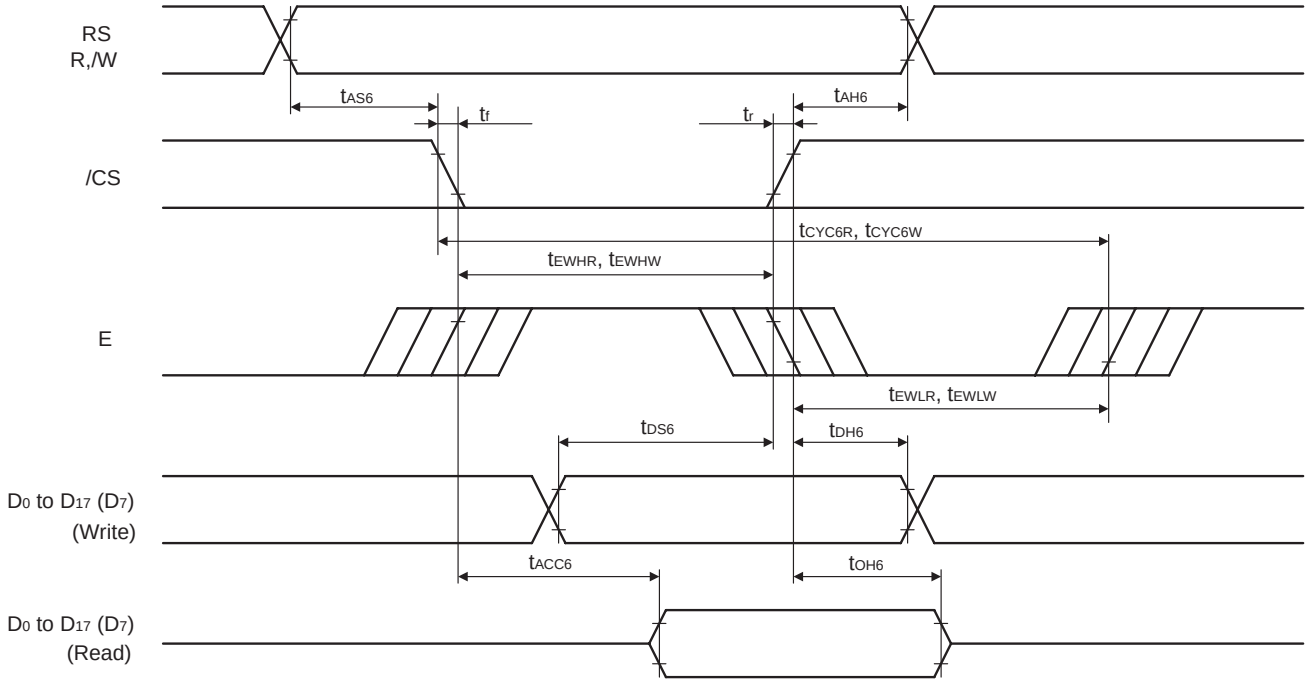
Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	10			ns
Address setup time	t_{AS8}	RS	10			ns
System cycle time (when write)	t_{CYC8W}		65			ns
Control low-level pulse width (/WR)	t_{CCLW}	/WR	25			ns
Control high-level pulse width (/WR)	t_{CCHW}	/WR	20			ns
Data setup time	t_{DS8}	D_0 to D_{17}	25			ns
Data hold time	t_{DH8}	D_0 to D_{17}	10			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC1}.

(d) M68 series CPU interface



When V_{DD1} = V_{DD2} = 1.6 to 2.0 V, V_{CC1} = 2.5 to 3.3 V (normal write mode)

Parameter		Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time		t_{AH6}	RS	10			ns
Address setup time		t_{AS6}	RS	10			ns
System cycle time (when write)		t_{CYC6W}	VSTBY = Low R98 = 005H	100			ns
			VSTBY = High V_{DD1} = V_{DD2} = 1.7 MIN. R98 = 005H	100			ns
System cycle time (when read)		t_{CYC6R}		250			ns
Data setup time		t_{DS6}	D_0 to D_{17}	25			ns
Data hold time		t_{DH6}	D_0 to D_{17}	10			ns
Access time		t_{ACC6}	D_0 to D_{17}, C_L = 100 pF			140	ns
Output disable time		t_{OH6}	D_0 to D_{17}, C_L = 100 pF	5		140	ns
Enable high level pulse width	Read	t_{EWHR}	E	140			ns
	Write	t_{EWHW}	E	35			ns
Enable low level pulse width	Read	t_{EWLR}	E	80			ns
	Write	t_{EWLW}	E	30			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less. When using a high-speed system cycle time, the rated value range is either ($t_r + t_f$) < ($t_{CYC6} - t_{EWLR} - t_{EWHR}$) or ($t_r + t_f$) < ($t_{CYC6} - t_{EWLW} - t_{EWHW}$).

2. All timing is rated based on 20 to 80% of V_{CC1}.

When V_{DD1} = V_{DD2} = 1.6 to 2.0 V, V_{CC1} = 2.5 to 3.3 V (high-speed RAM write mode, valid only for writing data)

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH6}	RS	10			ns
Address setup time	t_{AS6}	RS	10			ns
System cycle time	t_{CYC6W}		80			ns
Data setup time	t_{DS6}	D_0 to D_{17}	25			ns
Data hold time	t_{DH6}	D_0 to D_{17}	10			ns
Enable high level pulse width	t_{EWHW}	E	35			ns
Enable low level pulse width	t_{EWLW}	E	30			ns

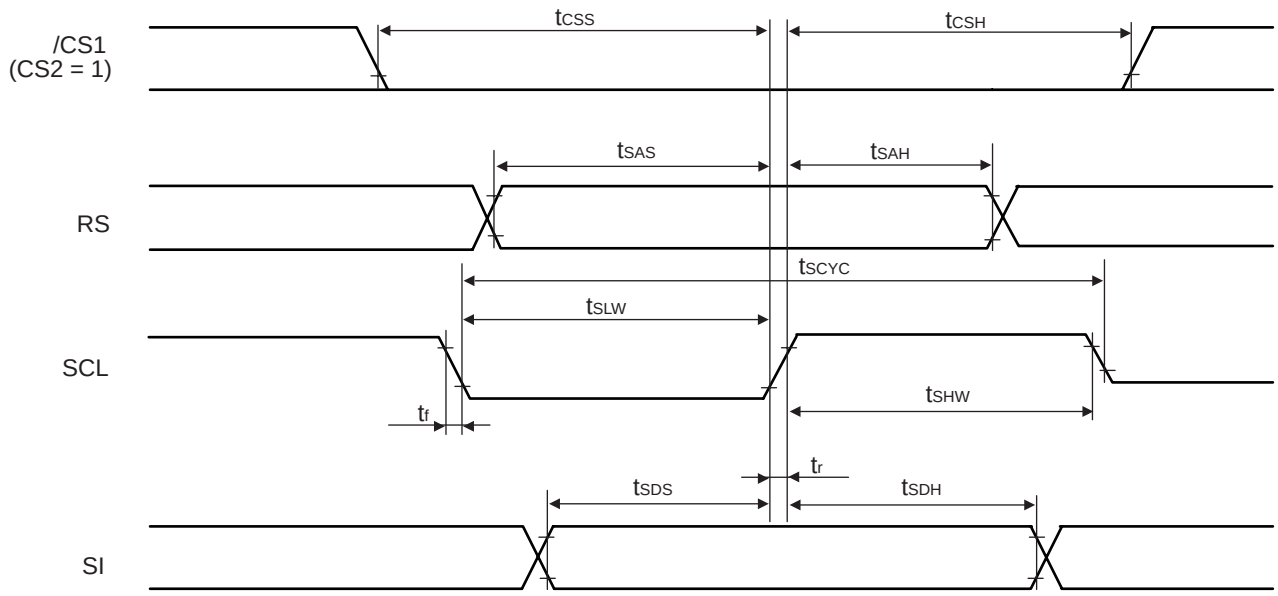
Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less. When using a high-speed system cycle time, the rated value range is either ($t_r + t_f$) < ($t_{CYC6} - t_{EWLR} - t_{EWHR}$) or ($t_r + t_f$) < ($t_{CYC6} - t_{EWLW} - t_{EWHW}$).

2. All timing is rated based on 20 to 80% of V_{CC1}.

(e) Serial interface

<1> Serial interface between CPU and the μPD161802



When V_{DD1} = V_{DD2} = 1.6 to 2.0 V, V_{CC1} = 2.5 to 3.3 V

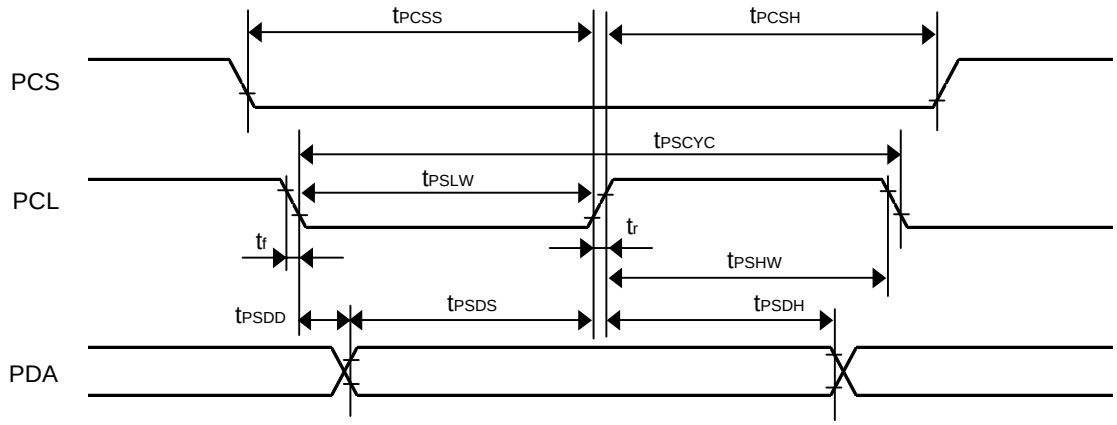
Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Serial clock cycle	t_{SCYC}	SCL	150			ns
SCL high level pulse width	t_{SHW}	SCL	60			ns
SCL low level pulse width	t_{SLW}	SCL	60			ns
Address hold time	t_{SAH}	RS	90			ns
Address set up time	t_{SAS}	RS	90			ns
Data set up time	t_{SDS}	SI	60			ns
Data hold time	t_{SDH}	SI	60			ns
CS - SCL time	t_{CSS}	/CS	90			ns
	t_{CSH}	/CS	90			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC1}.

<2> Serial interface between the μPD161802and the μPD161862



When $V_{DD1} = V_{DD2}$ = 1.6 to 2.0 V, V_{CC1} = 2.5 to 3.3 V

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Serial clock cycle	t_{PSCYC}		2			1/f_{OSC}
PCL high level pulse width	t_{PSHW}		1			1/f_{OSC}
PCL low level pulse width	t_{PSLW}		1			1/f_{OSC}
Data set up time	t_{PSDS}		1			1/f_{OSC}
Data hold time	t_{PSDH}		1			1/f_{OSC}
PCL↓ → PDA output delay time	t_{PSDD}		30			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC1}.

3. f_{OSC} is the internal oscillator's oscillation frequency.

(f) Common

Parameter	Symbol	Condition	MIN.	TYP.[Note1]	MAX.	Unit
Calibration setting time (frame frequency)	t_{cal} (f_{FRAME0})	**Note2**		51.9 (60)		μs (Hz)
Frame frequency	f_{FRAME2}	Calibrated [Note3]		60		Hz
	f_{FRAME3}	Calibrated [Note4]		60		Hz
Reset pulse width	t_{RW}		100			ns
Reset time	t_R	/RESET↑ to interface operation	100			ns

Notes 1. TYP. values are reference values when T_A = 25°C.

2. The relationship between the frame frequency and the calibration setting time is as follows.

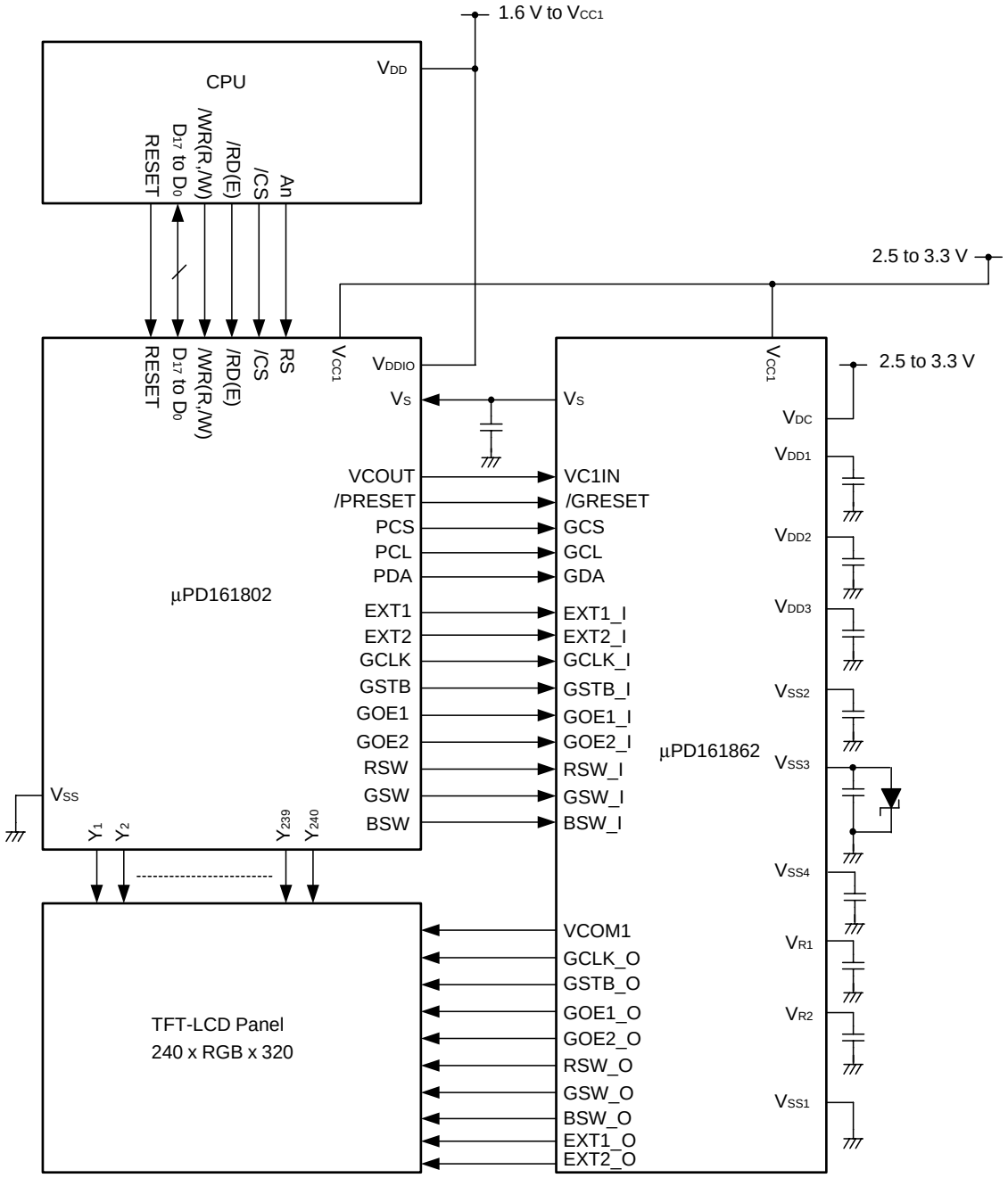
$f_{FRAME0} = 1/t_{cal} \times 321$

3. Measured at T_A = –40 to +85°C, after calibration at frame frequency = 60 Hz, T_A = 25°C exactly.

4. Measured at ±5°C, after calibration at frame frequency = 60 Hz exactly.

10. THE μPD161802 AND THE μPD161862 CONNECTION

Connection diagram examples for the μPD161802 and the μPD161862 are show below.

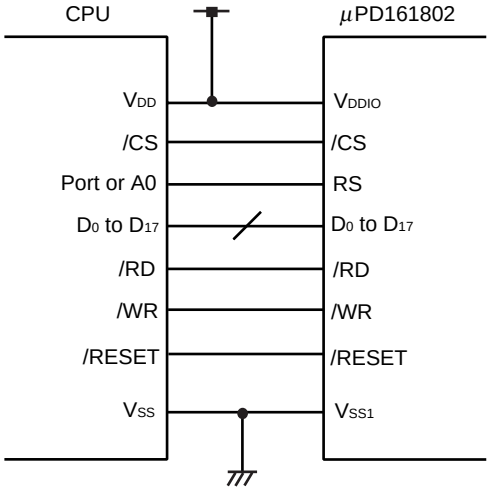


11. EXAMPLE OF THE μPD161802 AND CPU CONNECTION

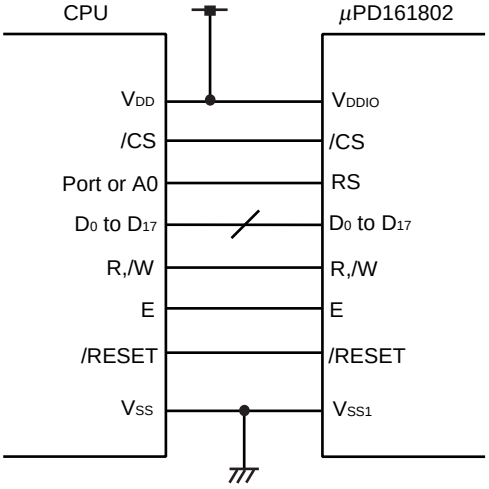
Examples of the μPD161802 and CPU connection are shown below.

In the example below, RS pin control in parallel interface mode is described for the case when the least significant bit of the address bus is being used.

(1) i80 series format



(2) M68 series format



HITACHI MODE

5. DESCRIPTION OF FUNCTIONS

5.1 CPU Interface

5.1.1 Selection of interface type

The μPD161802 is able to transfer data via an RGB interface (18-/16-/9-/6-bit) or via either of two CPU interfaces: the i80 parallel interface (18-/16-/8-bit). The following modes can be selected for these CPU interfaces, as set via the BSW0 to BSW3 pins. Also, the RGB interface becomes valid when at which time the bus width is selected according to the RIM1 and RIM0 [R00CH: D_1, D_0] settings.

Although the i80 parallel interface and the serial interface allow writing to both the display data RAM and the registers, the RGB interface can be used only to overwrite the display data RAM.

Moreover, the display operation mode at the time of each interface use can be set up by setup of DM1 and DM0 [R00CH:D_5, D_4]. Internal clock operation and external display interface operation can be changed by this setup.

Table 5–1. CPU Interface Bus Width Selection

BWS3	BWS2	BWS1	BWS0	Mode	/CS	RS	/RD	/WR	D_{17} to D_{10}	D_9	D_8 to D_1	D_0
L	L	L	X	Setting prohibited								
		H	L	16bit parallel	/CS	RS	/RD	/WR	D_{17} to D_{10}	Hi-Z Note	D_8 to D_1	Hi-Z Note
			H	8bit parallel	/CS	RS	/RD	/WR	D_{17} to D_{10}	Hi-Z Note		
	H	X	X	Setting prohibited								
H	L	L	X	Setting prohibited								
		H	L	18bit parallel	/CS	RS	/RD	/WR	D_{17} to D_{10}	D_9	D_8 to D_1	D_0
			H	9bit parallel	/CS	RS	X	Hi-Z Note	D_{17} to D_{10}	D_9	Hi-Z Note	
	H	X	X	Setting prohibited								

Remark X: Don't care

Note Hi-Z: High impedance

Table 5–2. Interface Selection

RM	RAM Access Interface
0	CPU system interface Set it as DM [1:0] = 1, 0 (VSYNIC interface) or at the time DM [1:0] = 0, 0 (internal clock).
1	RGB interface Set it as at the time DM [1:0] = 0, 1 (RGB interface).

Table 5–3. RGB Interface Bus Width Selection

RIM1	RIM0	Mode	RGB_{05} to RGB_{01}	RGB_{00}	RGB_{15} to RGB_{10}	RGB_{25} to RGB_{21}	RGB_{20}
L	L	18-bit parallel	RGB_{05} to RGB_{01}	RGB_{00}	RGB_{15} to RGB_{10}	RGB_{25} to RGB_{21}	RGB_{20}
L	H	16-bit parallel	RGB_{05} to RGB_{01}	Hi-Z Note	RGB_{15} to RGB_{10}	RGB_{25} to RGB_{21}	Hi-Z Note
H	L	6-bit parallel	Hi-Z Note	Hi-Z Note	Hi-Z Note	RGB_{25} to RGB_{21}	RGB_{20}
H	H	Setting prohibited					

Note Hi-Z: High impedance

Table 5–4. Display Interface Selection

DM1	DM0	The interface which performs display operation (reference clock)
0	0	Internal clock operation
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting prohibited

5.1.2 Selection of data transfer mode

When data bus width selection, it is fixed to 1 pixel = 18-bit at the time of 18-bit parallel interface selection, it is fixed to 1 pixel = 16-bit at the time of 16-bit parallel interface selection, and it is fixed to 1 pixel = 18-bit (9-bit x 2) at the time of 9-bit parallel interface selection.

1 pixel can be selected from 18-bit (TMI = 1 [R003H: D_{15}]) or 16-bit (TMI = 0 [R003H: D_{15}]) in 8-bit parallel interface. At moreover, the time of 1 pixel/18-bit selection (a data transmission format can be selected by setup of TMI = 1 [] and DFM [R003H: D_{14}].)

[18-bit Parallel Interface]

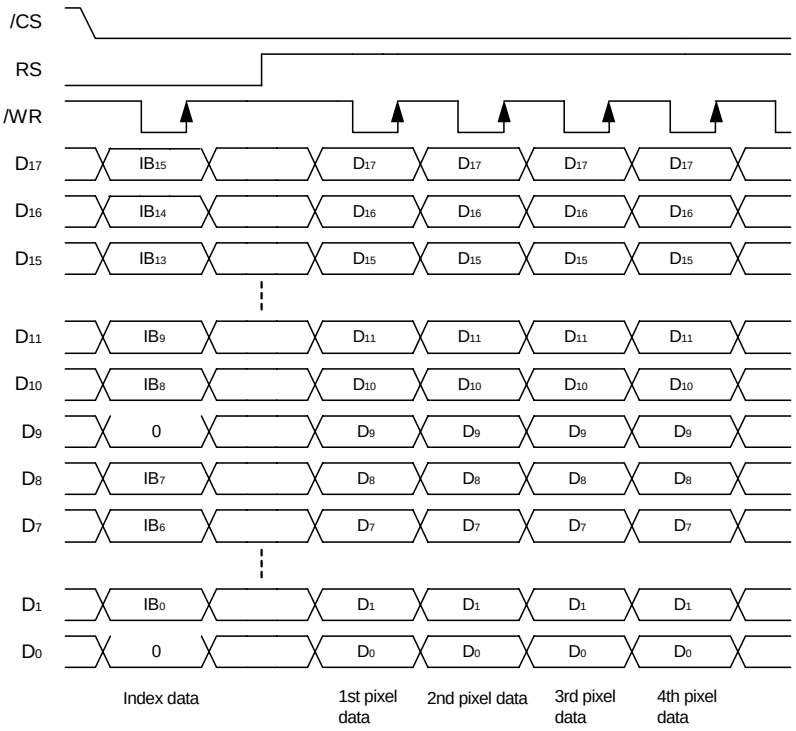
Figure 5–1. Relationship Between 18-bit Parallel Interface and Display RAM Data

Data bus side

18-bit data																	
D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R_5	R_4	R_3	R_2	R_1	R_0	G_5	G_4	G_3	G_2	G_1	G_0	B_5	B_4	B_3	B_2	B_1	B_0
R data						G data						B data					
1 pixel																	

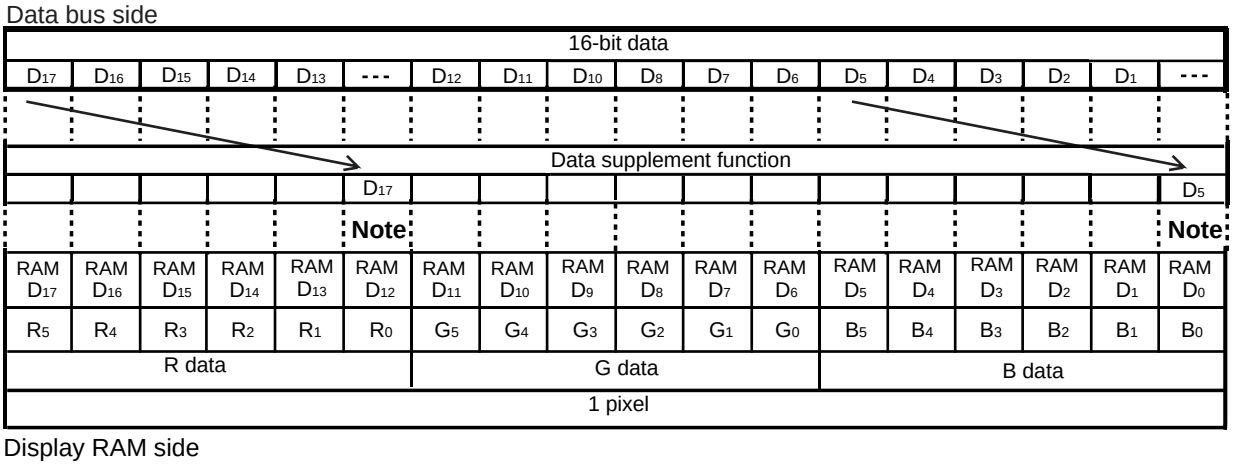
Display RAM side

Figure 5–2. 18-bit Parallel Interface Data Transfer



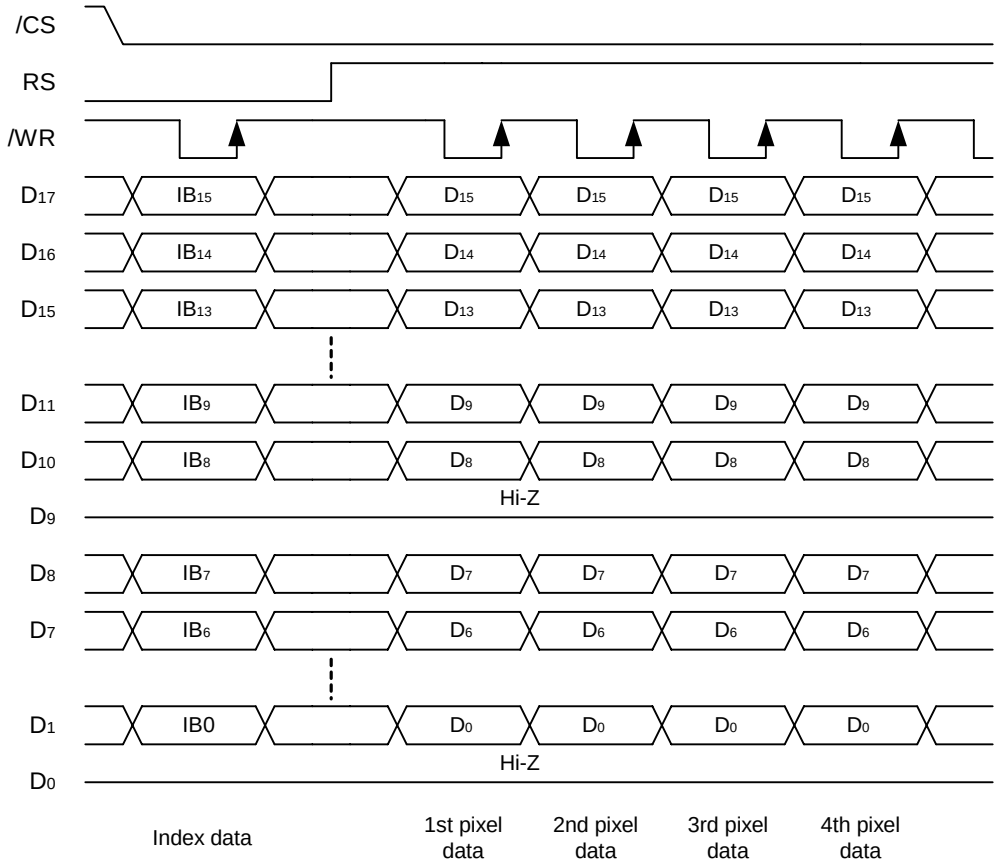
[16-bit Parallel Interface]

Figure 5–3. Relationship Between 16-bit Parallel Interface and Display RAM Data



Note When In used 16-bit parallel interface, display RAM data D_{12} and D_0 are supplemented by D_{17} and D_5 of bus data respectively, and written to the display RAM as 18-bit data.

Figure 5–4. 18-bit Parallel Interface Data Transfer



[9-bit Parallel Interface]

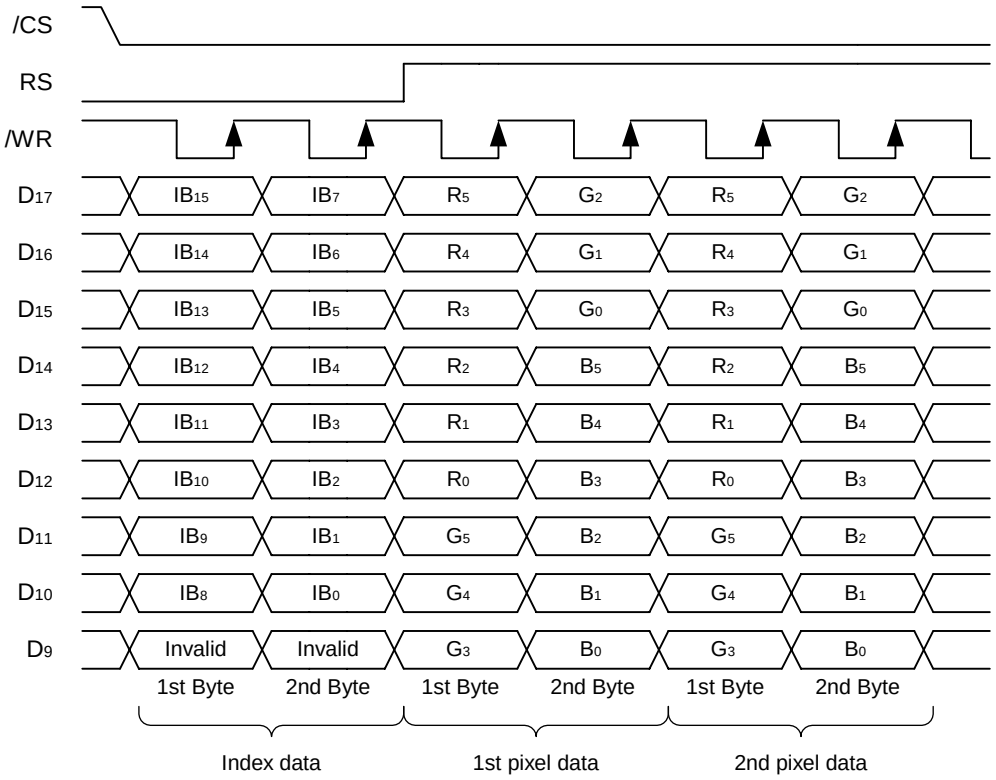
Figure 5–5. Relationship Between 9-bit Parallel Interface and Display RAM Data

Data bus side

9-bit (First transfer)									9-bit (Second transfer)								
D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R_5	R_4	R_3	R_2	R_1	R_0	G_5	G_4	G_3	G_2	G_1	G_0	B_5	B_4	B_3	B_2	B_1	B_0
R data						G data						B data					
1 pixel																	

Display RAM side

Figure 5–6. 9-bit Parallel Interface Data Transfer



[8-bit Parallel Interface]

Figure 5–7. Relationship Between 8-bit Parallel Interface and Display RAM Data 1

(1) TRI = 0: 2-time transfer mode

Data bus side

8-bit (First transfer)									8-bit (Second transfer)								
D_{17}	D_{16}	D_{15}	D_{14}	D_{13}		D_{12}	D_{11}	D_{10}	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R_5	R_4	R_3	R_2	R_1	R_0	G_5	G_4	G_3	G_2	G_1	G_0	B_5	B_4	B_3	B_2	B_1	B_0
R data						G data						B data					
1 pixel																	

Display RAM side

Figure 5–8. 8-bit Parallel Interface Data Transfer 1

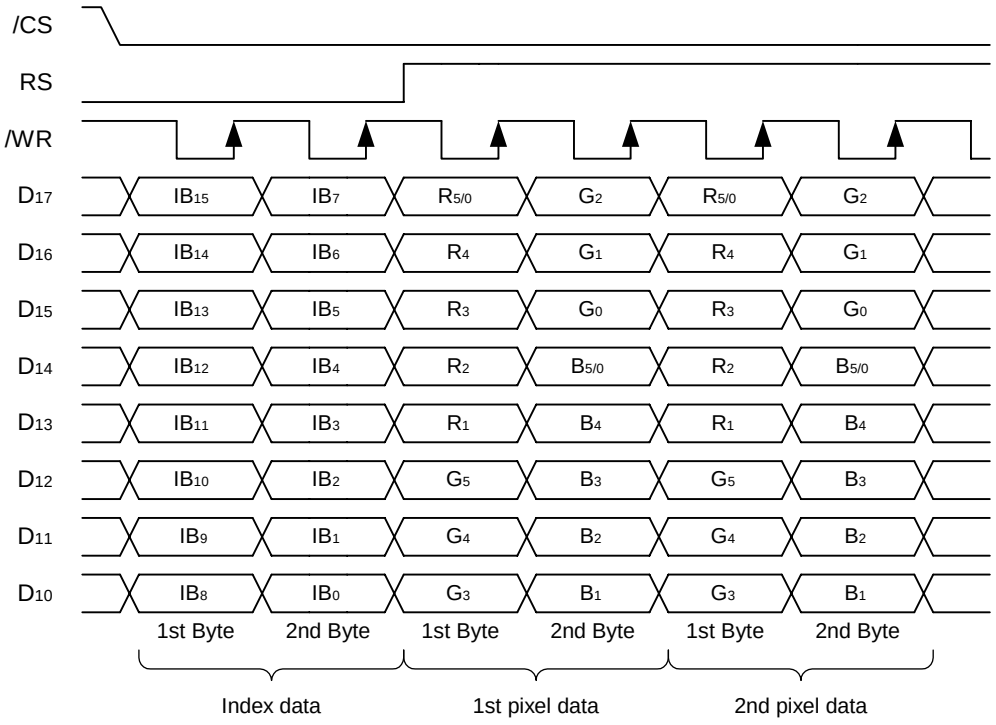


Figure 5–9. Relationship Between 8-bit Parallel Interface and Display RAM Data 2

(2) TRI = 1, DFM =0: 3-time transfer mode, Data transfer mode 1 (2 bit + 8 bit + 8 bit)

Data bus side

8-bit (First transfer)		8-bit (Second transfer)								8-bit (Third transfer)							
D_{11}	D_{10}	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R_5	R_4	R_3	R_2	R_1	R_0	G_5	G_4	G_3	G_2	G_1	G_0	B_5	B_4	B_3	B_2	B_1	B_0
R data						G data						B data					
1 pixel																	

Display RAM side

Figure 5–10. 8-bit Parallel Interface Data Transfer 2

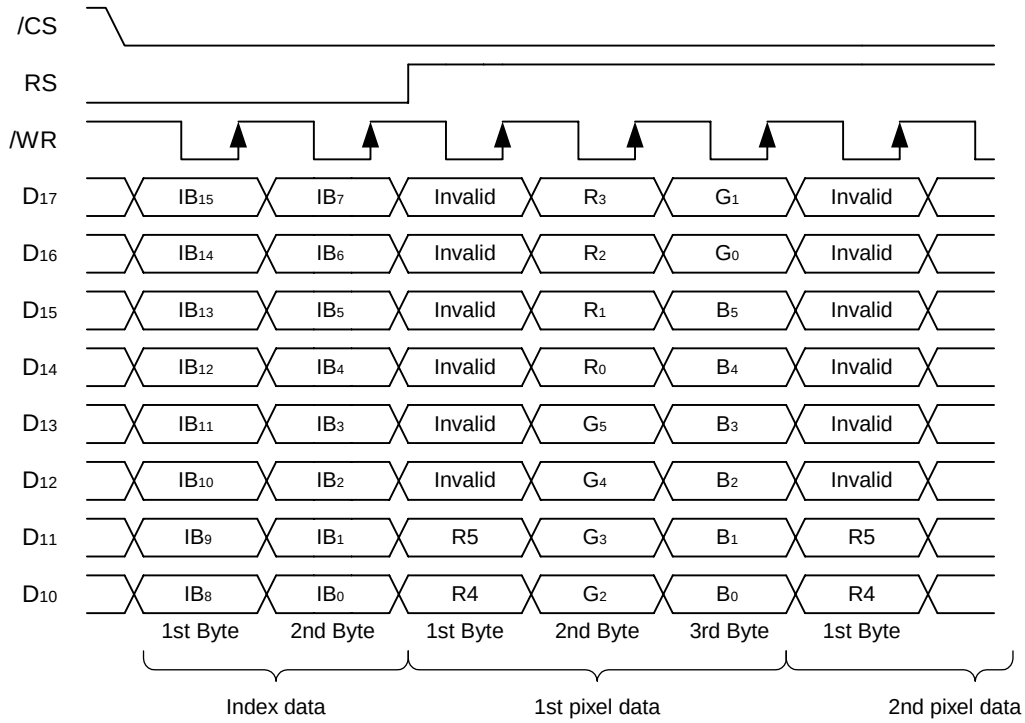


Figure 5–11. Relationship Between 8-bit Parallel Interface and Display RAM Data 2

(3) TRI = 1, DFM =1: 3-time transfer mode, Data transfer mode 2 (6 bit + 6 bit + 6 bit)

Data bus side

8-bit (First transfer)						8-bit (Second transfer)						8-bit (Third transfer)					
D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R_5	R_4	R_3	R_2	R_1	R_0	G_5	G_4	G_3	G_2	G_1	G_0	B_5	B_4	B_3	B_2	B_1	B_0
R data						G data						B data					
1 pixel																	

Display RAM side

Figure 5–12. 8-bit Parallel Interface Data Transfer 3

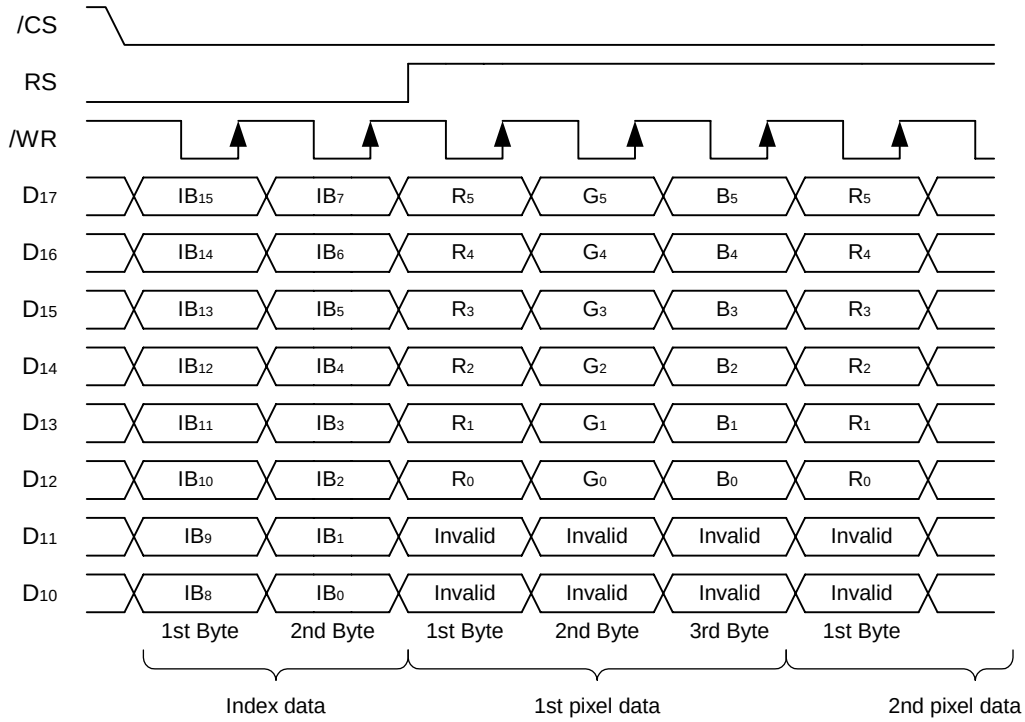


Figure 5–13. Relationship between Bus Data and Display RAM Data (18-bit RGB interface)

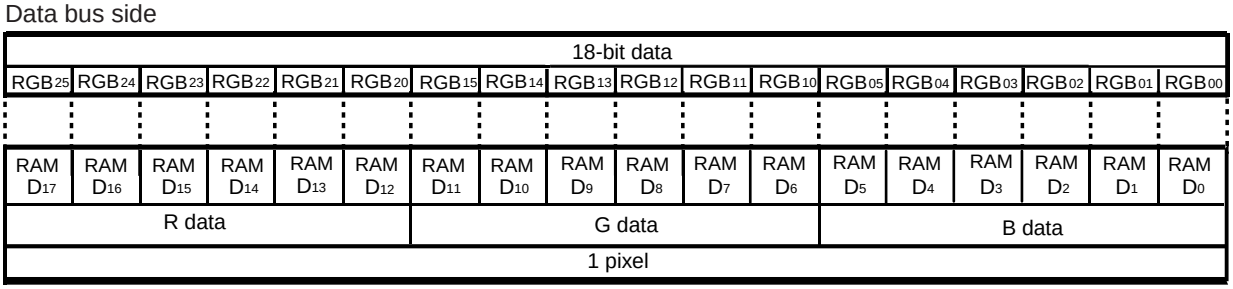
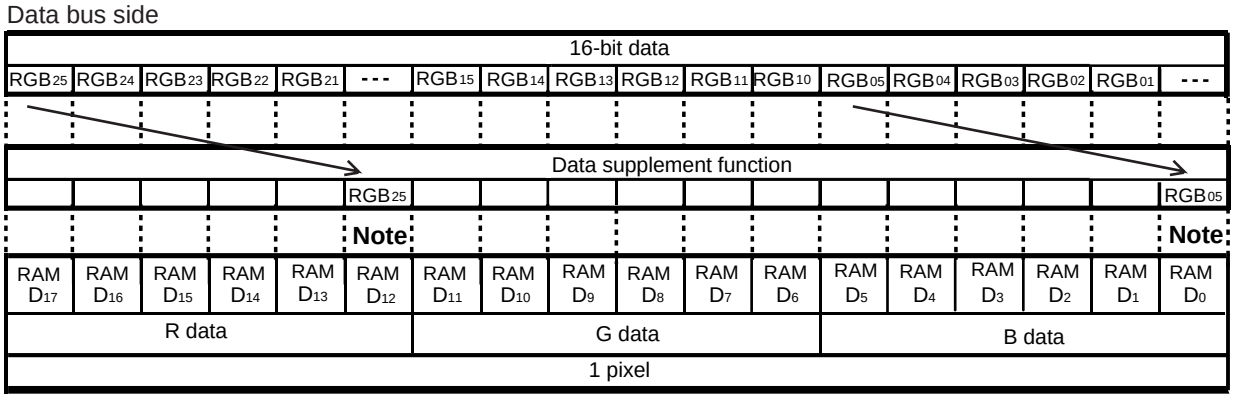
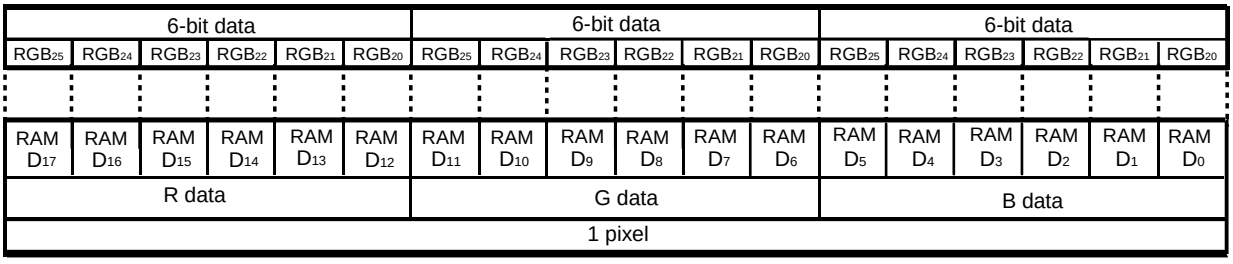


Figure 5–14. Relationship between Bus Data and Display RAM Data (16-bit RGB interface)



Note When In used 16-bit parallel interface, display RAM data D_{12} and D_0 are supplemented by RGB_{25} and RGB_{05} of bus data respectively, and written to the display RAM as 18-bit data.

Figure 5–15. Relationship between Bus Data and Display RAM Data (6-bit RGB interface)



5.1.3 RGB interface

The μPD161802 can be directly connected to the RGB interface when bit D_2 of the RGB interface control register (R00CH of RM (D_8 bit) = ”1”, DM1 (D_5 bit) = ”0” and DM0 (D_4 bit) = ”1”) is set.

The HSYNC and VSYNC signals establish synchronization in the horizontal and vertical direction, respectively, and data input to the data bus (RGB_{00} to RBG_{05}, RGB_{10} to RGB_{15}, and RGB_{20} to RGB_{25}) is latched in synchronization with DOTCLK. For the electrical specifications, refer to **9. ELECTRICAL SPECIFICATIONS**.

In addition, when it is set as a RGB interface in the case of the HITACHI mode, display output timing surely performs the writing to RAM while being <HSYNC/VSYNC/DOTCLK> fixation.

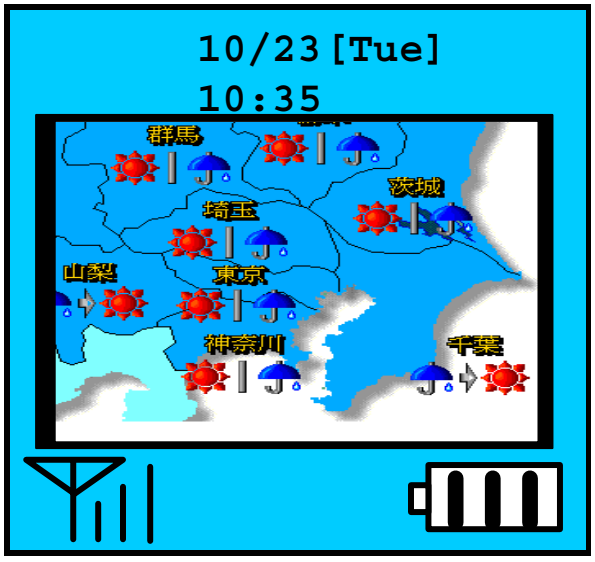
When capture mode is selected, DOTCLK is used as a write-in signal to a display data RAM. In addition, X addresses of an address pointer are reset by the HSYNC signal, and an increment is carried out by DOTCLK. Y address is reset by the VSYNC signal and an increment is carried out by the level synchronized signal.

The blanking period can be set by the horizontal back porch register and vertical back porch register. The active levels of HSYNC and VSYNC can be set. In addition, the active level of DOTCLK can also be set.

[Example of using RGB interface]

The area set in the window access mode is written by the RGB interface (R01BH to R01EH), and a domain which became active with the VLD pin (However, a register setup is confirmed when a register setup (R01BH to R01EH) and a VLD pin set both up.).

Even in this mode, the i80 parallel interface which are shared with the RGB interface, can be used. Note, however, that data can be written to a register while the RGB interface is accessed, but that the RAM cannot be accessed. Make sure that only one of these accesses is made (shift to the RGB data invalid mode so that video data is not input).



The RGB interface performs the writing to the RAM area specified to be a window area for the RGB interface.

I80/M68 parallel interface and the serial interface rewrite display data RAM to the RAM area specified by window access mode.

<Notes on using RGB interface>

<1> Be sure to input data from the RGB interface every frame.

<2> When changing the mode, issue defined mode of selection command after once always setting.

<3> Data (back porch period is included) of one line should be set within the period of HSYNC to HSYNC.

<4> Data (back porch period is included) of one frame should be set within the period of VSYNC to VSYNC.

<5> Do not set access to R00DH register and DM0/DM1/RM bit into standby mode.

<6> High-speed RAM write mode cannot be used.

<7> A setup of R200H, R201H, and R406H to R409H is invalid at the time of RGB interface mode (since these are set up of CPU interface).

<8> The period from "the DOTCLK rising after falling of HSYNC" to "the rising of DOTCLK after a HSYNC rising" should not start VSYNC. For more details, refer to the next **Figure 5–16**, **5–17.**

Figure 5–16. Example of HSYNC, VSYNC, DOTCLK Input Timing (both HSYNC and VSYNC are low active)

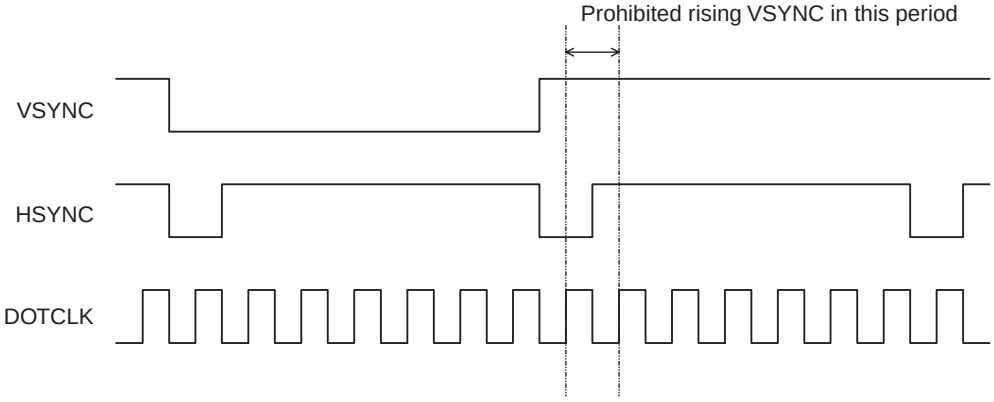
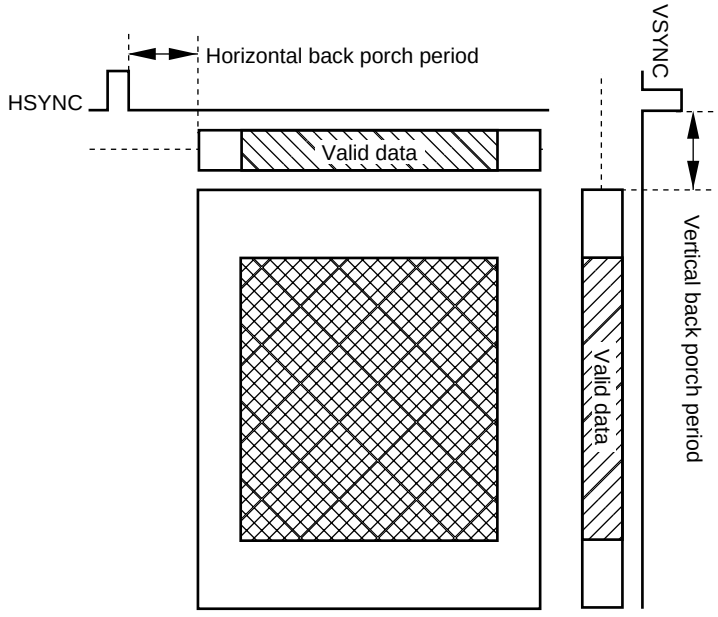


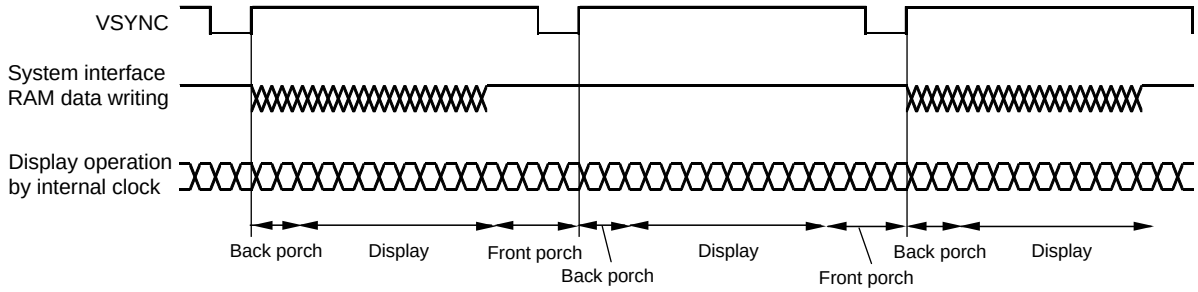
Figure 5–17. HSYNC and VSYNC Input Image Figure (when both HSYNC and VSYNC are high active)



5.1.4 VSYNIC Interface

The VSYNC interface in which video display is possible is built in only by a conventional system interface and a conventional frame synchronized signal (VSYNC).

The VSYNC interface becomes usable by setting up with R00CH and DM1 = 1, DM0 = 0, and RM = 0. In the VSYNC interface, internal display operation is synchronized by the frame synchronized signal (VSYNC). From a system interface, it abolishes that the data before rewriting and the data after rewriting are intermingled in 1 frame by writing display data in RAM at a writing speed more than fixed speed from internal display operation.



In addition, if VSYNC becomes active, being simultaneous (the above figure rising of VSYNC), when the writing from a system interface to RAM begins to be performed, it is necessary to write in data above the speed computed by the following expression of relations.

[The clock frequency for a display]

Built-in VCO frequency (f_{OSC}) [Hz] = frame frequency x (display line (320) + front porch + back porch) x the number of horizontal period clocks x variation

[RAM write in speed]

RAM write in speed (MIN.) [Hz] > 240 x display line/ {(back porch + display line (320)-margin) x the number of horizontal period clocks/fosc}

Caution The margin asks for a setup more than one.

[Example 1 of calculation] When writing in data of 240 RGB x 320 pixel

Display size	: 240 RGB x 320
The number of rewriting pixels	: 240 pixel
The number of rewriting lines	: 320 line
Back/Front porch	: 14 line/12 line
Frame frequency	: 60 Hz
The number of display line clocks	: 41 clock
Margin	: 2 line

Built-in VCO frequency (f_{OSC}) [Hz] = 60Hz x (320 + 2 + 14) line x 41 clock x 1.1/0.9 = 827 kHz ± 10%

RAM write in speed (MIN.) [Hz] = 240 x 320/ {(14 + 320 − 2) line x 41 clock/827 kHz} = 4.67 MHz (with no variation)

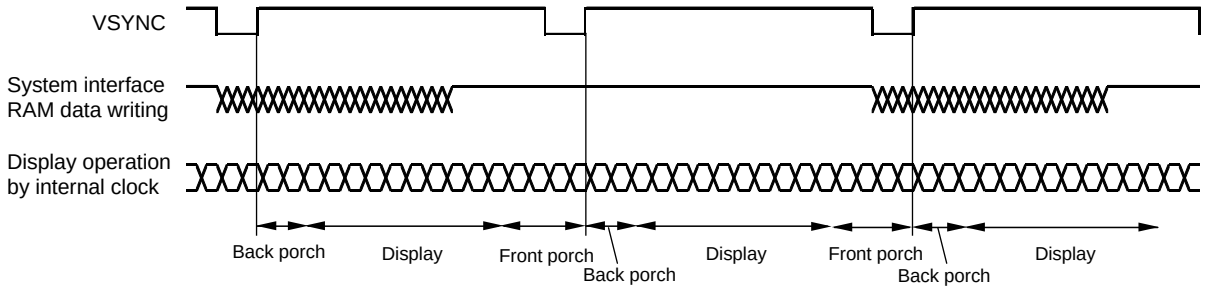
[Example 2 of calculation] When writing in data of 200 RGB x 300 pixel

Display size	: 240 RGB x 320
The number of rewriting pixels	: 200 pixel
The number of rewriting lines	: 300 line
Back/Front porch	: 14 line/12 line
Frame frequency	: 60 Hz
The number of display line clocks	: 41 clock
Margin	: 2 line

Built-in VCO frequency (f_{OSC}) [Hz] = 60Hz x (320 + 2 + 14) line x 41 clock x 1.1/0.9 = 827 kHz ± 10%

RAM write in speed (MIN.) [Hz] = 200 x 300/ {(14 + 320 – 2) line x 41 clock/827 kHz} = 3.65 MHz (with no variation)

Like the above and the example 2 of calculation, when rewriting size is made small, it is possible to make writing speed late. Moreover, as shown in the following figure, it is possible also by writing in data from falling of VSYNC to reduce the minimum of a writing speed.

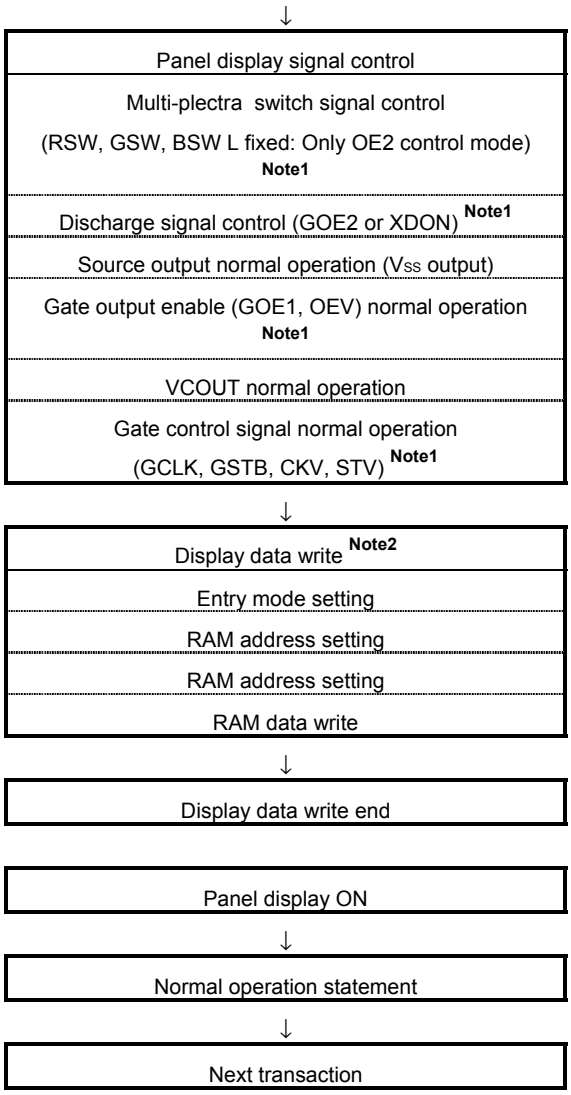


5.8 Power Supply Sequence

The power ON supply sequence of the μPD161802 recommends the sequence shown below.

Power ON	
↓	
WAIT	Power supply voltage stable time
↓	
Hard reset (/RESET ”L” pulse input)	
↓	
RAM address offset	RMOFS (R005H) = “1”
	By hard reset, the initial value is "0". When using it by "0" setup, it is not necessary to perform this processing.
↓	
Command reset	R003H AARESB = “1”
	All register setup to a default state.
↓	
Panel display OFF	R007H DISP1 = “1”, DISP0 = “0” (white display)
Stand-by mode	
↓	
SRAM power ON	R018H RMST [1:0] =1, 0
↓	
WAIT time (10 ms)	SRAM power supply rising wait time
	It is SRAM power supply circuit rising wait time with built-in IC.
↓	
Display RAM data output "0" data mask release	R018H RMMSK = ”1”
↓	
Sleep mode state	Display OFF, oscillation stop, logic power supply ON, SRAM power supply ON
↓	
Oscillator circuit operation start	R000H OSC2OFF = ”0”
↓	
Power supply IC control (power supply ON)	R110H (R38) to R114H (R42), R115H (R60) to R11AH (R65)
	Sequence changes with use power supply IC. Refer to the specifications of the power supply IC currently used. The inside of () is a register at the time of the NEC command.
↓	
WAIT time **Note**	Power supply rising wait time
↓	It is the power supply rising wait time of the power supply IC to "Display ON".

Note Set up the control system register flag of the signal actually used on a panel.



Notes1. Set up the control system register flag of the signal actually used on a panel.

2. The setup is possible at the same sequence as the driver by HITACHI company.

5.9 Stand-by Power Supply OFF Sequence

5.9.1 Stand-by by command input control

By state setup by the command input, μPD161802 can usually change free in each mode state of sleep, deep sleep, and stand-by from a state of operation, as shown in Figure 5–18. In addition, each mode specifies it that it is the following table, and is planning low power consumption.

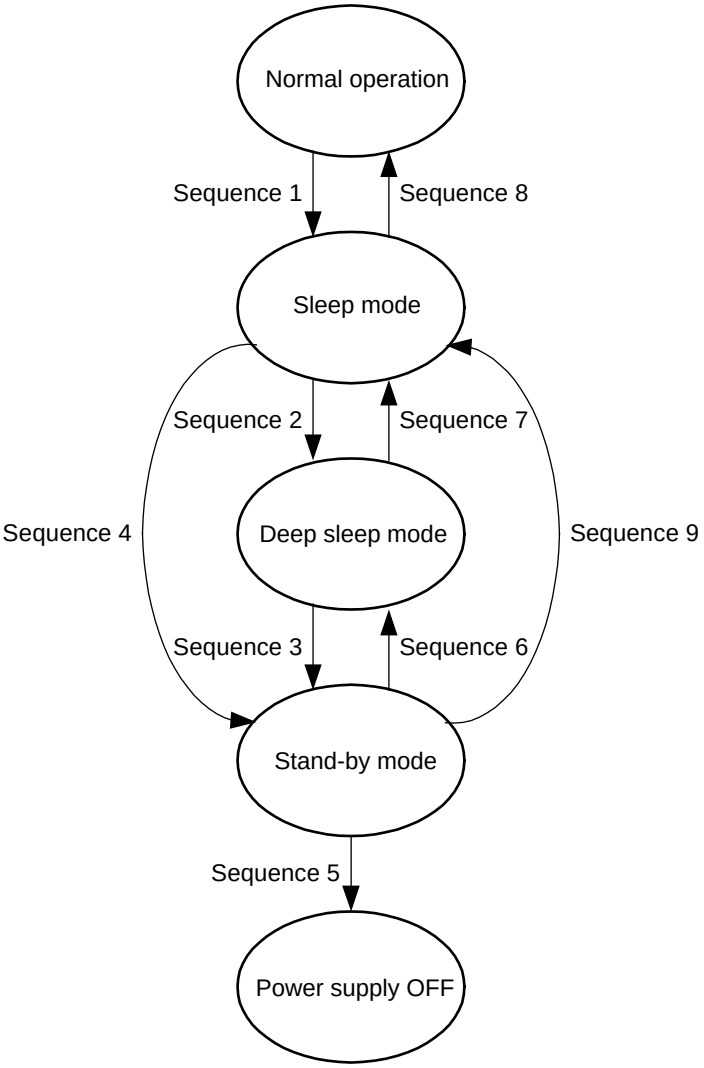
	μPD161802 Internal Operation State				
	Logic power supply	Command reception	SRAM power supply	SRAM state	Oscillation circuit
Normal operation	O	Possibility	O	Normal operation	Operation
Sleep mode	O	Possibility	O	Normal operation	Stop
Deep sleep mode	O	Possibility	Δ	Data hold	Stop
Standby mode	O	Possibility	X	Data abandonment	Stop

Remark O: Supply, Δ: Low power supply, X: Supply stop

Current: Normal operation > Sleep mode > Deep sleep mode > Standby mode

In addition, low power consumption as a module can plan further by setting up sequences, such as a power supply circuit stop of a power supply IC.

Figure 5–18. IC State Changes



<Sequence 1>

Normal operation statement	Display ON	
↓		
Panel display OFF	R007H	DISP1 = ”1”
↓		
WAIT time	Over 1-frame cycle time	
↓		
Panel display signal control 1		
Source output stop (V_{SS} output)	R017H	RSOUT = ”0”
Gate output stop (GOE1, OEV) signal stop Note1	R017H	RGOE1 = ”0” or ROEV = ”0”
VCOUT stop	R017H	RVCOT = ”0”
Gate control signal stop (GCLK, GSTB, CKV, STV) Note1	R017H	RGCLK = ”0”, RGSTB = ”0” or RCKV = ”0”, RSTV = ”0”
↓		
WAIT time	Over 1-frame cycle time Note2	
↓		
Panel discharge control 1		
Discharge control signal (GOE2 or XDON) Note1	R017H	RGOE2 = ”1” or RXDON = ”1”
↓		
WAIT time	**Note2**	
↓		
Panel discharge control 2		
Multi-plectra switch signal control (RSW, GSW, BSW L fixed: Only OE2 control) Note1	R017H	RGBW = ”0”
↓		
Power supply IC control (power supply OFF)	R110H (R38) to R114H (R42), R115H (R60) to R11AH (R65) sequence changes with use power supplies IC. Refer to the specifications of the power supply IC currently used. The inside of () is a register at the time of the NEC command.	
↓		
Oscillator stop	R000H	OSC2OFF = ”0”
↓		
Sleep mode statement	Display OFF, oscillator stop, logic power supply ON, SRAM power supply ON	
↓		
Next transaction		

This sequence is shown in illustration and changes with use panels. It is after checking the specification of the panel used about a sequence enough evaluation. It recommends as following condition after considering.

Notes 1. Set up the control system register flag of the signal actually used on a panel.

2. WAIT time is after checking the characteristic of a use panel, and specification enough evaluation.

<Sequence 2>

Sleep mode		Display OFF, oscillator stop, logic power supply ON, SRAM power supply ON
↓		
Display RAM data output ”0” data mask Note1	R018H	RMMSK = ”0”
↓		
SRAM power supply low power mode	R018H	RMST [1:0] = 0, 1
↓		
Deep sleep mode Note2		Display OFF, oscillator stop, logic power supply ON, SRAM power supply low power

Notes 1. When it set as a deep sleep mode state, be sure to input the following command. When this processing is not performed but it shifts to a deep sleep mode (RMST [1:0] = 0, 1), problems, such as an increase in penetration current, may occur.

2. Deep sleep mode state is operating the SRAM power supply for display data in the low power mode, and attains low power consumption. Although the data written to display RAM at this time is held, operation of write/read of display data cannot be performed. Note that no-guarantee about operation of IC at the time of accessing display RAM at the time of a deep sleep mode.

<Sequence 3>

Deep sleep mode		Display OFF, oscillator stop, logic power supply ON, SRAM power supply low power
↓		
SRAM power supply OFF	R018H	RMST [1:0] = 0, 0
↓		
Stand-by mode Note		Display OFF, oscillator stop, logic power supply ON, SRAM power supply OFF

Note Stand-by mode state is stopping supply of the SRAM power supply for display data, and is attaining further low power consumption. The data written to display RAM at this time is canceled. After stand-by mode setup, when usually changing in operation again, it is necessary to write in display data again.

<Sequence 4>

Sleep mode		Display OFF, oscillator stop, logic power supply ON, SRAM power supply ON
↓		
Display RAM data output ”0” data mask Note1	R018H	RMMSK = ”0”
↓		
SRAM power supply OFF	R018H	RMST [1:0] = 0, 0
↓		
Stand-by mode Note2		Display OFF, oscillator stop, logic power supply ON, SRAM power supply OFF

Notes 1. When it set as a deep sleep mode state, be sure to input the following command. When this processing is not performed but it shifts to a deep sleep mode (RMST [1:0] = 0, 1), problems, such as an increase in penetration current, may occur.

2. Stand-by mode state is stopping supply of the SRAM power supply for display data, and is attaining further low power consumption. The data written to display RAM at this time is canceled. After stand-by mode setup, when usually changing in operation again, it is necessary to write in display data again.

<Sequence 5>

Stand-by mode	Display OFF, oscillator stop, logic power supply ON, SRAM power supply OFF
↓	
<System power supply OFF>	

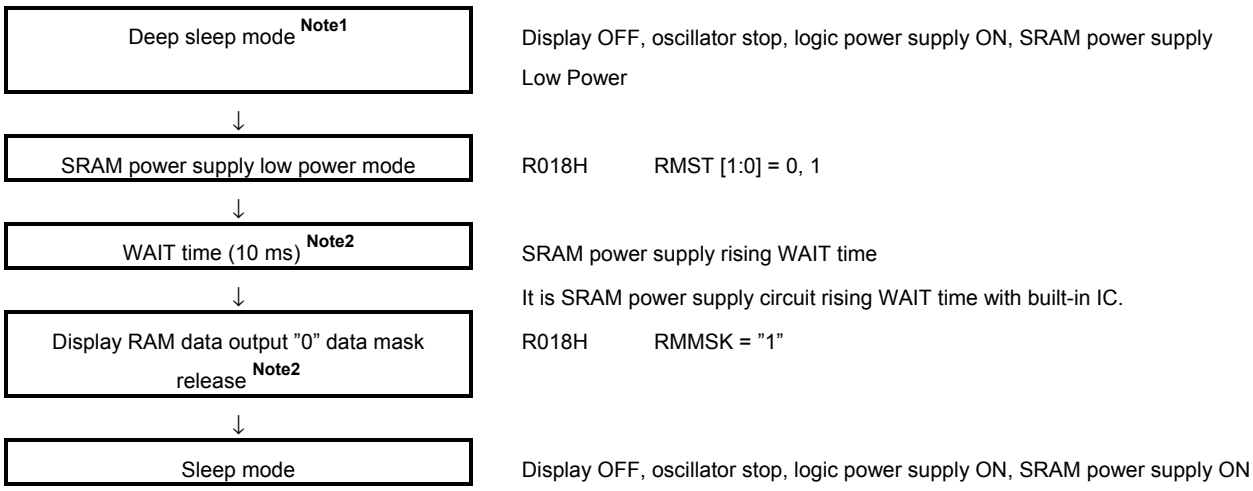
Safely, since system power supply is turned off, after setting it as stand-by mode, it recommends turning OFF system power supply.

<Sequence 6>

Stand-by mode Note		Display OFF, oscillator stop, logic power supply ON, SRAM power supply OFF
↓		
SRAM power supply low power mode	R018H	RMST [1:0] = 0, 1
↓		
Deep sleep mode		Display OFF, oscillator stop, logic power supply ON, SRAM power supply low power

Note Stand-by mode state is stopping supply of the SRAM power supply for display data, and is attaining further low power consumption. The data written to display RAM at this time is canceled. After stand-by mode setup, when usually changing in operation again, it is necessary to write in display data again.

<Sequence 7>



Notes 1. Deep sleep mode state is operating the SRAM power supply for display data in the low power mode, and attains low power consumption. Although the data written to display RAM at this time is held, operation of write/read of display data cannot be performed. Note that no-guarantee about operation of IC at the time of accessing display RAM at the time of a deep sleep mode.

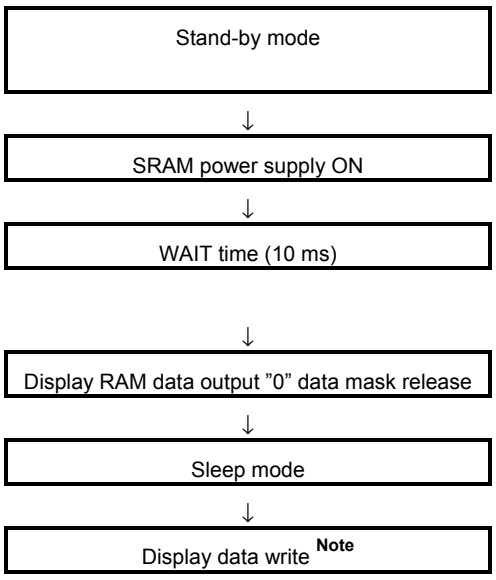
2. From deep sleep mode, sleep mode or when it usually returns to operation, input the following command. When display ON is carried out, all LCD displays will be "0" data outputs, without canceling a setup of this command.

<Sequence 8>

Sleep mode statement	Display OFF, oscillator stop, logic power supply ON, SRAM power supply ON	
↓		
Oscillator circuit operation start	R000H	OSC2OFF = ”1”
↓		
Power supply IC control (power supply ON)	R272H (R38) to R276H (R42), R277 (R60) to R282 (R65) Sequence changes with use power supplies IC. Refer to the specifications of the power supply IC currently used. The inside of () is a register at the time of the NEC command.	
↓		
WAIT time Note	Power supply rising WAIT time It is the power supply rising WAIT time of the power supply IC to "Display ON."	
↓		
Panel display signal control		
Multi-plectra switch signal control (RSW, GSW, BSW L fixed: Only OE2 control) Note	R017H	RGBW= ” 1”
Discharge control signal (GOE2 or XDON) Note	R017H	RGOE2 = ”0” or RXDON=”0”
Source output normal operation (V_{SS} output)	R017H	RSOUT = ”1”
Gate output stop (GOE1, OEV) normal operation Note	R017H	RGOE1 = ”1” or ROEV = ”1”
VCOUT stop	R017H	RVCOT = ”1”
Gate control signal stop (GCLK, GSTB, CKV, STV) Note	R017H	RGCLK = ”1”, RGSTB = ”1” or RCKV = ”1”, RSTV = ”1”
↓		
Panel display ON	R007H	DISP1 = ”0”, DISP0 = ”0”
↓		
Normal operation statement	Display ON	
↓		
Next transaction		

Note Set up the control system register flag of the signal actually used on a panel.

<Sequence 9>



Display OFF, oscillator stop, logic power supply ON, SRAM power supply OFF

R017H RMST [1:0] = 1, 0

SRAM power supply rising WAIT time

It is SRAM power supply circuit rising WAIT time with built-in IC.

R018H RMMSK = ”1”

Display OFF, oscillator stop, logic power supply ON, SRAM power supply ON

Note Stand-by mode state is stopping supply of the SRAM power supply for display data, and is attaining further low power consumption. The data written to display RAM at this time is canceled. After stand-by mode setup, when usually changing in operation again, it is necessary to write in display data again.

7. RESET

If the /RESET input becomes L or the reset command is input, the internal timing generator is initialized. The reset command will also initialize each register to its default value. These default values are listed in the table below.

(1/2)

Register		/RESET pin Note	Reset Command	Default Value
Oscillator control register	R000H	X	O	0000H
Driver output control register	R001H	X	O	0000H
Liquid crystal alternation current control register	R002H	X	O	0000H
Entry mode register	R003H	X	O	0030H
Reset register	R004H	X	O	0000H
RAM address offset	R005H	O	X	0000H
Display control (1)	R007H	X	O	0000H
Display control (2)	R008H	X	O	0101H
Gate interface control register	R00AH	X	O	0000H
External display interface control register (1)	R00CH	X	O	0000H
Frame frequency control register (1)	R00DH	X	O	0010H
External display interface control register (3)	R00FH	X	O	0000H
LTPS interface control register (1)	R010H	X	O	0425H
LTPS interface control register (2)	R011H	X	O	0505H
LTPS interface control register (3)	R012H	X	O	0D14H
LTPS interface control register (4)	R013H	X	O	151CH
LTPS interface control register (5)	R014H	X	O	1D24H
LTPS interface control register (6)	R015H	X	O	0909H
LTPS interface control register (7)	R016H	X	O	0909h
LTPS interface control register (8)	R017H	X	O	0000H
LTPS interface control register (9)	R018H	X	O	0000H
LTPS interface control register (10)	R019H	X	O	0000H
Blanking period bias control register	R021H	X	O	0000H
3 line interlace setting register	R022H	X	O	0000H
LTPS interface control register (11)	R01AH	X	O	0001H
LTPS interface control register (12)	R01BH	X	O	0000H
LTPS interface control register (13)	R01CH	X	O	00EFH
LTPS interface control register (14)	R01DH	X	O	0000H
LTPS interface control register (15)	R01EF	X	O	013FH
Power control register	R101H	X	O	0000H
External power supply IC control register (1) to (11)	R110H to R11AH	X	O	0000H
E^2PROM interface control register	R120H	O	O	0000H

(2/2)

Register		/RESET pin [Note]	Reset Command	Default Value
E^2PROM writing address specification register	R121H	X	O	0000H
E^2PROM writing index specification register	R122H	X	O	0000H
E^2PROM reading start address specification register	R123H	X	O	0000H
RAM address set register (1) [X address]	R200H	X	O	0000H
RAM address set register (2) [Y address]	R201H	X	O	0000H
RAM data write register	R202H	X	X	
RAM write data mask (1)	R203H	X	O	0000H
RAM write data mask (2)	R204H	X	O	0000H
γ– control register (1)	R300H	X	O	0000H
γ– control register (2)	R301H	X	O	0000H
γ– control register (3)	R302H	X	O	0000H
γ– control register (4)	R303H	X	O	8888H
γ– control register (5)	R304H	X	O	2772H
γ– control register (6)	R305H	X	O	4444H
γ– control register (7)	R306H	X	O	4444H
γ– control register (8)	R307H	X	O	0000H
γ– control register (9)	R308H	X	O	0033H
Vertical scroll control register (1)	R400H	X	O	0000H
Vertical scroll control register (2)	R401H	X	O	0000H
First panel drive position register (1)	R402H	X	O	0000H
First panel drive position register (2)	R403H	X	O	013FH
Second panel drive position register (1)	R404H	X	O	0000H
Second panel drive position register (2)	R405H	X	O	013FH
Horizontal RAM address position register (1)	R406H	X	O	0000H or 0010H
Horizontal RAM address position register (2)	R407H	X	O	00EFH or 00FFH
Vertical RAM address position register (1)	R408H	X	O	0000H
Vertical RAM address position register (2)	R409H	X	O	013FH
Liquid crystal drive amplifire bias current setting register	R554H	X	O	0000H

Remark O: Default value set, X: Default value not set

Note The internal counters are initialized only by a reset from the /RESET pin. Be sure to perform reset via the /RESET pin at power application.

Cautions 1. With setting value of RAM address offset register (R005H), a default value change as show in the below table.

R005H Setting Value	Default Value	
	R406H	R407H
000H	0000H	00EFH
001H	0010H	00FFH

2. The following value is set as the calibration setting time, t_{cal}, in a reset by reset command.
t_{cal} = 1/f_{OSC2} x 40 (f_{OSC2} returns to initial frequency)

3. The contents of RAM are saved in the case of both reset by /RESET pin and reset by reset command. Note that the RAM contents are unfixed immediately after the power is turned on.

The setting table at the time of /RESET = Low

Control Signal		All ON (default)	All OFF
Source Output		GND	Hi-Z
Gate Output Control Signal	GOE1	Normal	Low Fixation
	GOE2	Low Fixation	Normal [Note]
R/G/BSW Output		All High	All Low

Note The output of GOE2 changes with setup of RGON2 bit (R017H: D_4).

RGON2 = 0: GOE2 = High RGON2 = 1: GOE2 = Low (R/G/BSW = High fixation)

Cautions 1. The timing circuit 1 is set up and only a case is valid.

2. The source output, the gate output control signal, and R/G/BSW output can be set up individually.

8. COMMAND

8.1 Command List

(Register number is an estimate. Understand that there is a case where it changes later).

18-bit parallel interface mode, IB17, IB16 = 0 (1/5)

Rn	Register	RS	R,/W	Data bit							
				IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8
				IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R000H	Oscillator control register	1	0								
									OC	**OSC1OFF**	**OSC2OFF**
R001H	Driver output control register	1	0								SS
R002H	Liquid crystal alternation current drive control register	1	0							B/C	
R003H	Entry mode register	1	0	TRI	DFM					HWM1	HWM0
						ID1	ID0	AM			
R004H	Reset register	1	0								
										0	ARESB
R005H	RAM address offset	1	0								
											RMOFS
R007H	Display control register (1)	1	0	COLOR	**DISP1**	**DISP0**	**GSM**		VLE2	VLE1	SPT
				PT1	PT0				REV		
R008H	Display control register (2)	1	0				ADCK4	ADCK3	ADCK2	ADCK1	ADCK0
				ADLN7	ADLN6	ADLN5	ADLN4	ADLN3	ADLN2	ADLN1	ADLN0
R00AH	Gate interface control register	1	1								TE
R00CH	External display interface control register (1)	1	0		DCK2	DCK1	DCK0				RM
						DM1	DM0			RIM1	RIM0
R00DH	Frame frequency control register (1)	1	0							DIV1	DIV0
R00FH	External display interface control register (3)	1	0						RESSO	RESGA	RESSW
							VSPL	HSPL	VPL	0	DPL
R010H (R79, R80)	LTPS interface control register (1)	1	0			GOST5	GOST4	GOST3	GOST2	GOST1	GOST0
						GOED5	GOED4	GOED3	GOED2	GOED1	GOED0
R011H (R81, R82)	LTPS interface control register (2)	1	0			PCST5	PCST4	PCST3	PCST2	PCST1	PCST0
						PCED5	PCED4	PCED3	PCED2	PCED1	PCED0
R012H (R83, R84)	LTPS interface control register (3)	1	0			RST5	RST4	RST3	RST2	RST1	RST0
						RED5	RED4	RED3	RED2	RED1	RED0
R013H (R85, R86)	LTPS interface control register (4)	1	0			GST5	GST4	GST3	GST2	GST1	GST0
						GED5	GED4	GED3	GED2	GED1	GED0
R014H (R87, R88)	LTPS interface control register (5)	1	0			BST5	BST4	BST3	BST2	BST1	BST0
						BED5	BED4	BED3	BED2	BED1	BED0

18-bit parallel interface mode, IB17, IB16 = 0 (2/5)

Rn	Register	RS	R,/W	Data bit							
				IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8
				IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R015H	LTPS interface control register	1	0			E1ST5	E1ST4	E1ST3	E1ST2	E1ST1	E1ST0
(R89, R90)	(6)					E1ED5	E1ED4	E1ED3	E1ED2	E1ED1	E1ED0
R016H	LTPS interface control register	1	0			E2ST5	E2ST4	E2ST3	E2ST2	E2ST1	E2ST0
(R91, R92)	(7)					E2ED5	E2ED4	E2ED3	E2ED2	E2ED1	E2ED0
R017H	LTPS interface control register	1	0	TCKSL		GUD	RVCOT	RGBSW	RGSTB	RGCLK	RASW
(R77, R93)	(8)			RSTV	RCKV	RSOUT	RGOE2	RGOE1	RXDON	ROEVE	ROEV
R018H	LTPS interface control register	1	0							RPCK1	RPCK0
	(9)				RMMSK	RMST1	RMST0		LMD2	LMD1	0
R019H	LTPS interface control register	1	0				DSCG4	DSCG3	DSCG2	DSCG1	DSCG0
(R68, R72)	(10)				REFM2	REFM1	REFM0	REFB3	REFB2	REFB1	REFB0
R01AH	LTPS interface control register	1	0								
(R26)	(11)			VBP3	VBP2	VBP1	VBP0	HBP3	HBP2	HBP1	HBP0
R01BH	LTPS interface control register	1	0								
(R29)	(12)			CPXMIN7	CPXMIN6	CPXMIN5	CPXMIN4	CPXMIN3	CPXMIN2	CPXMIN1	CPXMIN0
R01CH	LTPS interface control register	1	0								
(R30)	(13)			CPXMAX7	CPXMAX6	CPXMAX5	CPXMAX4	CPXMAX3	CPXMAX2	CPXMAX1	CPXMAX0
R01DH	LTPS interface control register	1	0								CPYMIN8
(R31)	(14)			CPYMIN7	CPYMIN6	CPYMIN5	CPYMIN4	CPYMIN3	CPYMIN2	CPYMIN1	CPYMIN0
R01EH	LTPS interface control register	1	0								CPYMAX8
(R32)	(15)			CPYMAX7	CPYMAX6	CPYMAX5	CPYMAX4	CPYMAX3	CPYMAX2	CPYMAX1	CPYMAX0
R021H	Blanking period bias control	1	0								
(R18)	register			BSSP7	BSSP6	BSSP5	BSSP4	BSSP3	BSSP2	BSSP1	BSSP0
R022H	3 line interlace setting register	1	0								
(R66)								LACE3	LACE2	LACE1	LACE0
R101H	Power control register	1	0	DC4	DC3	DC2					
R110H	External power supply IC	1	0								
(R38)	control register (1)			PSD17	PSD16	PSD15	PSD14	PSD13	PSD12	PSD11	PSD10
R111H	External power supply IC	1	0								
(R39)	control register (2)			PSD27	PSD26	PSD25	PSD24	PSD23	PSD22	PSD21	PSD20
R112H	External power supply IC	1	0								
(R40)	control register (3)			PSD37	PSD36	PSD35	PSD34	PSD33	PSD32	PSD31	PSD30
R113H	External power supply IC	1	0								
(R41)	control register (4)			PSD47	PSD46	PSD45	PSD44	PSD43	PSD42	PSD41	PSD40
R114	External power supply IC	1	0								
(R42)	control register (5)			PSD57	PSD56	PSD55	PSD54	PSD53	PSD52	PSD51	PSD50

18-bit parallel interface mode, IB17, IB16 = 0 (3/5)

Rn	Register	RS	R,/W	Data bit							
				IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8
				IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R115H (R60)	External power supply IC control register (6)	1	0	PSD67	PSD66	PSD65	PSD64	PSD63	PSD62	PSD61	PSD60
R116H (R61)	External power supply IC control register (7)	1	0	PSD77	PSD76	PSD75	PSD74	PSD73	PSD72	PSD71	PSD70
R117H (R62)	External power supply IC control register (8)	1	0	PSD87	PSD86	PSD85	PSD84	PSD83	PSD82	PSD81	PSD80
R118H (R63)	External power supply IC control register (9)	1	0	PSD97	PSD96	PSD95	PSD94	PSD93	PSD92	PSD91	PSD90
R119H (R64)	External power supply IC control register (10)	1	0	PSDA7	PSDA6	PSDA5	PSDA4	PSDA3	PSDA2	PSDA1	PSDA0
R11AH (R65)	External power supply IC control register (11)	1	0	0	1	0	0	0	0	0	1
				PSDB7	PSDB6	PSDB5	PSDB4	PSDB3	PSDB2	PSDB1	PSDB0
R120H (R24)	E^2PROM interface control register	1	0								
									E2OPC2	E2OPC1	E2OPC0
R121H (R33)	E^2PROM writing address specification register	1	0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
R122H (R57)	E^2PROM writing index specification register	1	0	E2IR7	E2IR6	E2IR5	E2IR4	E2IR3	E2IR2	E2IR1	E2IR0
R123H (R58)	E^2PROM reading start address specification register	1	0	E2SA7	E2SA6	E2SA5	E2SA4	E2SA3	E2SA2	E2SA1	E2SA0

18-bit parallel interface mode, IB17, IB16 = 0 (4/5)

Rn	Register	RS	R,/W	Data bit							
				IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8
				IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R200H (R6)	RAM address set register (1) [X address register]	1	0	AD7 (XA7)	AD6 (XA6)	AD5 (XA5)	AD4 (XA4)	AD3 (XA3)	AD2 (XA2)	AD1 (XA1)	AD0 (XA0)
R201H (R7)	RAM address set register (2) [Y address register]	1	0	AD15 (YA7)	AD14 (YA6)	AD13 (YA5)	AD12 (YA4)	AD11 (YA3)	AD10 (YA2)	AD9 (YA1)	AD16 (YA8) AD8 (YA0)
R202H	RAM data write register	1	0								
R203H	RAM write data mask register (1)	1	0			WM11	WM10	WM9	WM8	WM7	WM6
						WM5	WM4	WM3	WM2	WM1	WM0
R204H	RAM write data mask register (2)	1	0			WM17	WM16	WM15	WM14	WM13	WM12
R300H (R43)	γ – control register (1)	1	0				GSEL				GONSEL
R301H (R46, R44)	γ – control register (2)	1	0	GPL7	GPL6	GPL5	GPL4	GPL3	GPL2	GPL1	GPL0
				GPH7	GPH6	GPH5	GPH4	GPH3	GPH2	GPH1	GPH0
R302H (R47, R45)	γ– control register (3)	1	0	GNL7	GNL6	GNL5	GNL4	GNL3	GNL2	GNL1	GNL0
				GNH7	GNH6	GNH5	GNH4	GNH3	GNH2	GNH1	GNH0
R303H (R52, R48)	γ– control register (4)	1	0	VDRN3	VDRN2	VDRN1	VDRN0	VSRN3	VSRN2	VSRN1	VSRN0
				VDRP3	VDRP2	VDRP1	VDRP0	VSRP3	VSRP2	VSRP1	VSRP0
R304H (R53, R49)	γ– control register (5)	1	0	VLRN3	VLRN2	VLRN1	VLRN0	VHRN3	VHRN2	VHRN1	VHRN0
				VLRP3	VLRP2	VLRP1	VLRP0	VHRP3	VHRP2	VHRP1	VHRP0
R305H (R51, R50)	γ– control register (6)	1	0		VGR3P2	VGR3P1	VGR3P0		VGR2P2	VGR2P1	VGR2P0
					VGR1P2	VGR1P1	VGR1P0		VGR0P2	VGR0P1	VGR0P0

18-bit parallel interface mode, IB17, IB16 = 0 (5/5)

Rn	Register	RS	R,/W	Data bit							
				IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8
				IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R306H (R55, R54)	γ– control register (6)	1	0		VGR3N2	VGR3N1	VGR3N0		VGR2N2	VGR2N1	VGR2N0
					VGR1N2	VGR1N1	VGR1N0		VGR0N2	VGR0N1	VGR0N0
R307H (R56)	γ– control register (7)	1	0								
										GV8S1	GV8S0
R308H (R59)	γ– control register (8)	1	0								
				WHP	WI2	WI1	WI0	BHP	BI2	BI1	BI0
R400H	Vertical scroll control register (1)	1	0								VL18
				VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10
R401H	Vertical scroll control register (2)	1	0								VL28
				VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20
R402H	First panel drive position register (1)	1	0								SS18
				SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
R403H	First panel drive position register (2)	1	0								SE18
				SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
R404H	Second panel drive position register (1)	1	0								SS28
				SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
R405H	Second panel drive position register (2)	1	0								SE28
				SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20
R406H	Horizontal RAM address position register (1)	1	0								
				HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
R407H	Horizontal RAM address position register (2)	1	0								
				HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
R408H	Vertical RAM address position register (1)	1	0								VSA8
				VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
R409H	Vertical RAM address position register (2)	1	0								VEA8
				VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
R554H (R73)	Liquid crystal amplifier bias current setting register	1	0								
								BCONB3	BCONB2	BCONB1	BCONB0

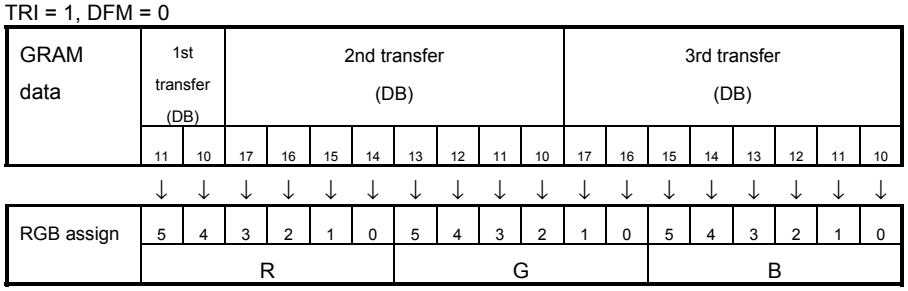
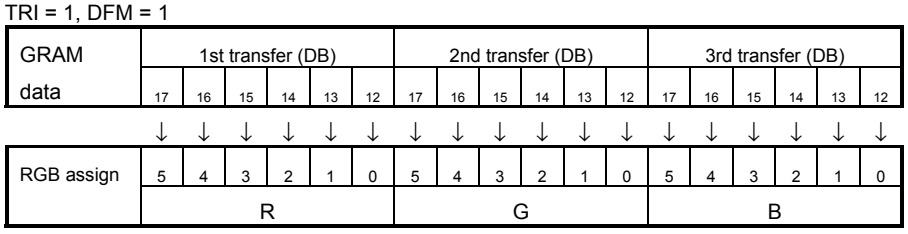
Cautions 1. Be sure to input 0 in blank area.

2. Access is prohibited about the register is not in the above register.

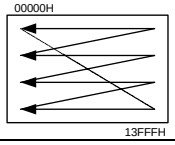
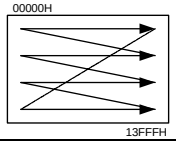
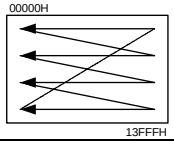
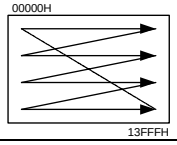
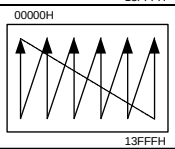
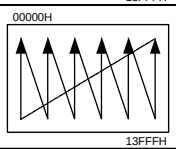
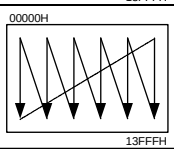
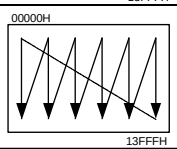
8.2 Command Explanation

(Register number is an estimate. Understand that there is a case where it changes later).

(1/22)

Register	Bit	Symbol	Function
R000H	D_2	OC	This bit is used for calibration. The time from calibration start command execution until calibration stop command execution becomes the time for 1 line. 0: Calibration stop 1: Calibration start
	D_1	OSC1OFF	This is oscillator circuit stop bit for calibration. This command is stop when in stand-by mode. 0: Oscillator operation 1: Oscillator stop
	D_0	OSC2OFF	This is oscillator circuit stop bit for LCD display. This command is stop when in stand-by mode. 0: Oscillator operation 1: Oscillator stop
R001H	D_8	SS	The output shift direction of a source driver can be selected. 0: it is outputted to S240 from S1 1: it is outputted to S1 from S240
R002H	D_9	B/C	The liquid crystal alternating current drive method is selected. 0: select a frame alternating current waveform. 1 Perform alternating current for every panel and perform a liquid crystal drive. 1: select a line alternating current waveform. 1 Perform alternating current for every line and perform a liquid crystal drive.
R003H	D_{15}	TRI	8 Set up the RAM data transmission system at the time of a bit bus interface. 0: 2 time transmission mode 1 (16 bit length: 65 K color mode) 1: 3 time transmission mode (18 bit length: 260 K color mode)
	D_{14}	DFM	By the 8 bit bus interface, the data format at the time of TRI = 1 is set up. TRI = 1, DFM = 0  TRI = 1, DFM = 1 

(2/22)

<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R003H</td><td>D_9, D_8</td><td>HWM1,
HWM0</td><td>High-speed writing can be performed to GRAM at the time of HWM1, HWM0 = 11. After writing in the data for 2 pixels in the mode with enzyme, data is collectively written in GRAM. It is necessary to transmit data access from CPU every 2 pixels. Since it is not written in display RAM about the data with which a part for 2 pixels is not filled when the data with which 2 pixels are not filled is transmitted at the time of high-speed RAM writing mode use, it is not reflected in a liquid crystal display even if it transmits CPU data. The data which is not reflected at this time becomes data writing from a continuation of a register, when having become being stored in a register with as, and transmitting data next. However, the data stored is canceled when RS signal is changed in the middle of writing of data (RS = L). When using high-speed RAM writing mode, it recommends transmitting display data every 2 pixels.</td></tr>
<tr><td></td><td>D_5, D_4</td><td>I/D1,
I/D0</td><td>At the time of I/D1, I/D0 = 1, after data writing in to GRAM, it is an address counter (AC). +1 increment is carried out automatically. Moreover, at the time of I/D1, I/D0 = 0, after writing in to GRAM, −1 decrement of the address counter (AC) is carried out. A setup performs independently the increment/decrement setup of the address counter by I/D1 and I/D0 in an address higher rank (AD16 to AD8) and a low rank (AD7 to AD0). The address advance direction at the time of GRAM writing is setup in AM bit.
<table>
<tr><th>I/D1</th><th>I/D0</th><th>Address height direction</th><th>Address length direction</th></tr>
<tr><td>0</td><td>0</td><td>Decrement</td><td>Decrement</td></tr>
<tr><td>0</td><td>1</td><td>Decrement</td><td>Increment</td></tr>
<tr><td>1</td><td>0</td><td>Increment</td><td>Decrement</td></tr>
<tr><td>1</td><td>1</td><td>Increment</td><td>Increment</td></tr>
</table></td></tr>
<tr><td></td><td>D_3</td><td>AM</td><td>After writing in to GRAM, it is an address counter (AC). The renewal method of automatic is set up. At the time of AM = 0, it writes in continuously horizontally, and writes in continuously perpendicularly at the time of AM = 1. At the time of window address specification, the writing to GRAM in a window address can be performed according to a setup of I/D1, I/D0 and AM.
<table>
<tr><td></td><td>I/D1-0 = 00
Length direction : decrement
Height direction : decrement</td><td>I/D1-0 = 01
Length direction : increment
Height direction : decrement</td><td>I/D1-0 = 10
Length direction : decrement
Height direction : increment</td><td>I/D1-0 = 01
Length direction : increment
Height direction : increment</td></tr>
<tr><td>AM = 0
Horizontal direction</td><td> 
</td><td> 
</td><td> 
</td><td> 
</td></tr>
<tr><td>AM = 1
Vertical direction</td><td> 
</td><td> 
</td><td> 
</td><td> 
</td></tr>
</table>
Remark It can write only in GRAM in a window address at the time of a window address setup.</td></tr>
</table>

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Register	Bit	Symbol	Function
R004H	D_0	ARESB	Command reset function. Be sure to execute this bit after power ON. Command reset automatically clears this bit following execution (RES = 1H). Therefore, it is not necessary to set 0 (select normal operation) again by software. Moreover, since the time required for the value of this bit to change (1 → 0) following command reset execution is extremely short, it is not necessary to secure time until the next command is set following command reset setting. 0: Normal operation 1: Command reset
R005H	D_0	RMOFS	Offset is applied to the address value of X addresses of the display RAM. The relation between X addresses and an output is setup as follows. 0: Offset OFF, 000H (0) to 0EFH (239) 1: Offset ON, 020H (0) to 0FFH (239)
R007H	D_{15}	COLOR (R0)	This pin switches the 260,000-color mode and the 8-color mode. When the 8-color mode is selected, low power supply can be selected in order to stop the amplifier at each output circuit. In the 8-color mode, the value of the MSB of the internal RAM data is used as the color data. This command is executed following transfer from the next frame. 0: 260,000-color mode (18-bit/pixels) 1: 8-color mode (3-bit/pixels) **Caution In 8-color mode, it does not become low power consumption at the time of built-in γ -output adjustment circuit use by GSEL(R43:D_4) =1 setup.**
	D_{14}	DISP1 (R0)	This command performs the same output as when 8-color mode white, independently of the internal RAM data (case of normally white). This command is executed, after it has been transferred, when the next line is output. 0: Normal operation 1: Ignores data of RAM and outputs all display line 8-color mode whites. DISP1 takes precedence over DISP0. When DISP1 = 1, DISP0 = 1 is ignored.
	D_{13}	DISP0 (R0)	This command performs the same output as when 8-color mode black, independently of the internal RAM data (case of normally white). This command is executed, after it has been transferred, when the next line is output. 0: Normal operation 1: Ignores data of RAM and outputs all display line 8-color mode black.
	D_{12}	GSM (R0)	Sets output of the gate scanning signal during partial display. If this bit is set to 1, the gate scan of the lines set in the partial non-display area is stopped. This command is executed following transfer from the next frame. 0: Normal mode 1: Stops gate scanning in partial non-display area

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R007H</td><td>D_{10}, D_9</td><td>VLEn</td><td>The scroll panel of a panel scroll function is set up.
Vertical scrolling is performed on the 1st panel at the time of VLE1 = 1. Vertical scrolling is performed on the 2nd panel at the time of VLE2 = 1.

<table>
<tr><th>VLE2</th><th>VLE1</th><th>Second Panel</th><th>First Panel</th></tr>
<tr><td>0</td><td>0</td><td>Fixed display</td><td>Fixed display</td></tr>
<tr><td>0</td><td>1</td><td>Fixed display</td><td>Scroll display</td></tr>
<tr><td>1</td><td>0</td><td>Scroll display</td><td>Fixed display</td></tr>
<tr><td>1</td><td>1</td><td>Scroll display</td><td>Scroll display</td></tr>
</table>

Remark This function cannot use it at the time of an external display interface. At the time of external display interface use, it is surely give as VLE [2:1] = "0, 0"</td></tr>
<tr><td></td><td>D_8</td><td>SPT</td><td>The panel division drive is controlled.
0: Normal mode
1: 2 division liquid crystal drive
This function cannot use it at the time of an external display interface. At the time of external display interface use, it is surely give as STEP = "0"</td></tr>
<tr><td></td><td>D_7, D_6</td><td>PTn</td><td>The source output at the time of the non-displaying area drive at the time of a partial display is specified.

<table>
<tr><th rowspan="2">PT1</th><th rowspan="2">PT0</th><th colspan="2">Source output of non-display area</th></tr>
<tr><th>Positive polarity</th><th>Negative polarity</th></tr>
<tr><td>0</td><td>0</td><td>V63</td><td>V0</td></tr>
<tr><td>0</td><td>1</td><td>V63</td><td>V0</td></tr>
<tr><td>1</td><td>0</td><td>GND</td><td>GND</td></tr>
<tr><td>1</td><td>1</td><td>Hi-Z (REFBn = 0)
Refresh/Non-refresh drive
(REFBn ≠ 0)</td><td>Hi-Z (REFBn = 0)
Refresh/Non-refresh drive
(REFBn ≠ 0)</td></tr>
</table></td></tr>
<tr><td></td><td>D_2</td><td>REV</td><td>The panel of display area is indicated by inversion. Since a gradation level can be reversed, this gradation panel can be expressed as the same data on the panel of normally white and a normally black. However, the source output during a front/back porch, and the blanking period at the time of 2 panel division displays follows a setup of PT [1:0].

<table>
<tr><th rowspan="2">REV</th><th rowspan="2">GRAM data</th><th colspan="2">Source Output</th></tr>
<tr><th>Positive polarity</th><th>Negative polarity</th></tr>
<tr><td>0</td><td>18’h00000
:
18’h3FFFF</td><td>V63
:
V0</td><td>V0
:
V63</td></tr>
<tr><td>1</td><td>18’h00000
:
18’h3FFFF</td><td>V0
:
V63</td><td>V63
:
V0</td></tr>
</table></td></tr>
</table>

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R008H</td><td>D_{12} to D_8</td><td>ADCKn</td><td>The number of clocks set up by this register is inserted as a dummy clock within 1-line drive period.
For more details, refer to 5.4.1 1-line period timing.

<table>
<tr><th>ADCK4</th><th>ADCK3</th><th>ADCK2</th><th>ADCK1</th><th>ADCK0</th><th>Setting Clock Count</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting prohibited</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>30</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>31</td></tr>
</table></td></tr>
<tr><td></td><td>D_7 to D_0</td><td>ADLNn</td><td>The number of lines set up by this register is set up as the number of lines of the FP [2 Line fixed] + BP period of a frame changing.
For more details, refer to 5.4.2 1-frame period timing.
ADLNn ≤ 2: Only BP period
ADLNn > 3: FP line count [2-line] + BP period line count = Setting line count = ADLNn setting value

<table>
<tr><th>ADLN7</th><th>ADLN6</th><th>ADLN5</th><th>ADLN4</th><th>ADLN3</th><th>ADLN2</th><th>ADLN1</th><th>ADLN0</th><th>Setting line count</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting prohibited</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>BP 1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>BP 2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>FP 2 + BP 1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>FP 2 + BP 2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>FP 2 + BP 3</td></tr>
<tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>FP 2 + BP 252</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>FP 2 + BP 253</td></tr>
</table></td></tr>
<tr><td>R00AH</td><td>D_8</td><td>TE</td><td>It is serial transmission enable to the external power supply IC. When this register is read, it can be transmitted serial at the time of TE = 0. If data is written in a power control register (R110H-R11A), register data will be outputted from the serial interface for power supply IC control. Since it starts 16 clocks (internal oscillation frequency ÷ 2), be careful of data transmission. Write in a power control register continuously, and set more than wait time T.B.D.μs and transmit data, or a case should transmit the following data, after supervising TE flag and checking TE = 0.</td></tr>
</table>

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R00CH</td><td>D14
D13
D12</td><td>DCK2
DCK1
DCK0</td><td>The divider ratio of the external input DOTCLK and a display clock is set up.
<table>
<tr><th>DCK2</th><th>DCK1</th><th>DCK0</th><th>Divide ratio</th><th>1 line output DOTCLK number</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>6 divide</td><td>[240] + [HBP] + [HSYNC ACT] over</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>7 divide</td><td>[280] + [HBP] + [HSYNC ACT] over</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>8 divide</td><td>[320] + [HBP] + [HSYNC ACT] over</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>9 divide</td><td>[360] + [HBP] + [HSYNC ACT] over</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>10 divide</td><td>[400] + [HBP] + [HSYNC ACT] over</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>11 divide</td><td>[440] + [HBP] + [HSYNC ACT] over</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>12 divide</td><td>[480] + [HBP] + [HSYNC ACT] over</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td colspan="2">Setting prohibited</td></tr>
</table></td></tr>
<tr><td></td><td>D8</td><td>RM</td><td>The interface which accesses RAM is set up. The interface set up in RM bit to RAM access is attained. When write in display data from a RGB interface, give as RM = 1. Since it can set up independently with display operation mode, display data can be changed from a system interface by considering as RM = 0 also in the organization which is displaying by the RGB interface.
<table>
<tr><th>RM</th><th>Interface performs RAM access</th></tr>
<tr><td>0</td><td>System interface
Set up at the time of DM [1:0] = 1, 0 (VSYNC interface) or DM [1:0] = 0, 0 (internal clock operation)</td></tr>
<tr><td>1</td><td>RGB interface
Set up at the time (RGB interface) of DM [1:0] = 0 and 1.</td></tr>
</table></td></tr>
<tr><td></td><td>D5, D4</td><td>DM1,
DM0</td><td>Display operation mode is set up. The interface which performs display operation can be set up with DM [1:0]. It is possible to change internal clock operation and an external display interface by this setup. However, do not make a change in the time of external display interface use (RGB I/F and VSYNC I/F).
<table>
<tr><th>DM1</th><th>DM0</th><th>Interface performs display operation</th></tr>
<tr><td>0</td><td>0</td><td>Internal clock operation</td></tr>
<tr><td>0</td><td>1</td><td>RGB interface</td></tr>
<tr><td>1</td><td>0</td><td>VSYNC interface</td></tr>
<tr><td>1</td><td>1</td><td>Setting prohibited</td></tr>
</table></td></tr>
</table>

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R00CH</td><td>D1, D0</td><td>RIM1,
RIM0</td><td>The RGB interface mode at the time of RGB interface selection is set up. When a RGB interface is selected in DM bit and RM bit, this setup becomes valid and selects the mode to be used. Set up this setup before displaying in an external display interface. Moreover, do not change this setup while on display.

<table>
<tr><th>RIM1</th><th>RIM0</th><th>RGB interface mode</th></tr>
<tr><td>0</td><td>0</td><td>18-bit RGB interface (once transfer/pixel)</td></tr>
<tr><td>0</td><td>1</td><td>16-bit RGB interface (once transfer/pixel)</td></tr>
<tr><td>1</td><td>0</td><td>6-bit RGB interface (three times transfer/pixel)</td></tr>
<tr><td>1</td><td>1</td><td>Setting prohibited</td></tr>
</table></td></tr>
<tr><td>R00DH</td><td>D9, D8</td><td>DIV1,
DIV0</td><td>The divider ratio of a clock at the time of internal clock operation is set up. The divide clock set up by DIV [1:0] performs internal operation. Adjustment of frame frequency can be performed by this setup.

<table>
<tr><th>DIV1</th><th>DIV0</th><th>Divide cycle ratio</th><th>Internal operation clock frequency</th></tr>
<tr><td>0</td><td>0</td><td>1 divide cycle</td><td>fosc ÷ 1</td></tr>
<tr><td>0</td><td>1</td><td>2 divide cycle</td><td>fosc ÷ 2</td></tr>
<tr><td>1</td><td>0</td><td>4 divide cycle</td><td>fosc ÷ 4</td></tr>
<tr><td>1</td><td>1</td><td>8 divide cycle</td><td>fosc ÷ 8</td></tr>
</table></td></tr>
<tr><td rowspan="8">R0FH</td><td>D10</td><td>RESSO</td><td>The source output at the time of /RESET is set up.
0: Source output is VSS at the time of /RESET.
1: Source output is Hi-Z at the time of /RESET</td></tr>
<tr><td>D9</td><td>RESGA</td><td>The GOE1 and GOE2 output at the time of /RESET are set up.
0: At the time of /RESET, GOE1 = normal output and GOE2 = L level output
1: At the time of /RESET, GOE1 = L level output and GOE2 = normal output</td></tr>
<tr><td>D8</td><td>RESSW</td><td>The RSW, GSW and BSW output at the time of /RESET are set up.
0: At the time of /RESET, RSW/GSW/BSW = ALL and H level output
1: At the time of /RESET, RSW/GSW/BSW = ALL and L level output</td></tr>
<tr><td>D4</td><td>VSPL</td><td>The signal polarity of VSYNC signal is set up.
0: It becomes low active
1: It becomes high active</td></tr>
<tr><td>D3</td><td>HSPL</td><td>The signal polarity of HSYNC signal is set up.
0: It becomes low active
1: It becomes high active</td></tr>
<tr><td>D2</td><td>VPL</td><td>The signal polarity of VLD signal is set up.
0: RAM writing becomes valid by VLD = L. It writes in RAM at the time of VLD = H, and becomes invalid
1: RAM writing becomes valid by VLD = H. It writes in RAM at the time of VLD = L, and becomes invalid</td></tr>
<tr><td>D0</td><td>DPL</td><td>The signal polarity of DOTCLK signal is set up.
0 : take in data by the rising edge of DOTCLK
1: take in data by the falling edge of DOTCLK</td></tr>
</table>

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Register	Bit	Symbol	Function
R010H (R79, R80)	D_{13} to D_8	GOSTn	The start timing of the signal outputted from GOE1 (/GOE1) and OEV (/OEV) pin is set up. Set up in the range 001H ≤ GOSTn ≤ 026H. In addition, prohibited for setting up the same value as GOSTn and GOEDn.
	D_5 to D_0	GOEDn	The end timing of the signal outputted from GOE1 (/GOE1) and OEV (/OEV) pin is set up. Set up in the range 001H ≤ GOEDn ≤ 026H. In addition, prohibited for setting up the same value as GOSTn and GOEDn.
R012H (R83, R84)	D_{13} to D_8	RSTn	The start timing of the signal outputted from RSW (/RSW) and ASW1 (/ASW1) pin is set up. Set up in the range 002H ≤ RSTn ≤ 025H. In addition, prohibited for setting up the same value as RSTn and REDn.
	D_5 to D_0	REDn	The end timing of the signal outputted from RSW (/RSW) and ASW1 (/ASW1) pin is set up. Set up in the range 002H ≤ REDn ≤ 025H. In addition, prohibited for setting up the same value as RSTn and REDn.
R013H (R85, R86)	D_{13} to D_8	GSTn	The start timing of the signal outputted from GSW (/GSW) and ASW2 (/ASW2) pin is set up. Set up in the range 002H ≤ GSTn ≤ 025H. In addition, prohibited for setting up the same value as GSTn and GEDn.
	D_5 to D_0	GEDn	The end timing of the signal outputted from GSW (/GSW) and ASW2 (/ASW2) pin is set up. Set up in the range 002H ≤ GEDn ≤ 025H. In addition, prohibited for setting up the same value as GSTn and GEDn.
R014H (R87, R88)	D_{13} to D_8	BSTn	The start timing of the signal outputted from BSW (/BSW) and ASW3 (/ASW3) pin is set up. Set up in the range 002H ≤ BSTn ≤ 025H. In addition, prohibited for setting up the same value as BSTn and BEDn.
	D_5 to D_0	BEDn	The end timing of the signal outputted from BSW (/BSW) and ASW3 (/ASW3) pin is set up. Set up in the range 002H ≤ BEDn ≤ 025H. In addition, prohibited for setting up the same value as BSTn and BEDn.
R015H (R89, R90)	D_{13} to D_8	E1STn	The start timing of the signal outputted from EXT1 (/EXT1) pin is set up. Set up in the range 001H ≤ E1STn ≤ 026H. In addition, when unused output signal from these pins, set up the same value as E1STn and E1EDn. In default, these bits are fixed to EXT1 = L, /EXT1 = H.
	D_5 to D_0	E1EDn	The end timing of the signal outputted from EXT1 (/EXT1) pin is set up. Set up in the range 001H ≤ E1EDn ≤ 026H. In addition, when unused output signal from these pins, set up the same value as E1STn and E1EDn.

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Register	Bit	Symbol	Function
R016H (R91, R92)	D_{13} to D_8	E2STn	The start timing of the signal outputted from EXT2 (/EXT2) pin is set up. Set up in the range 001H ≤ E2STn ≤ 026H. In addition, when unused output signal from these pins, set up the same value as E2STn and E2EDn. In default, these bits are fixed to EXT2 = L, /EXT2 = H.
	D_5 to D_0	E2EDn	The end timing of the signal outputted from EXT2 (/EXT2) pin is set up. Set up in the range 001H ≤ E2EDn ≤ 026H. In addition, when unused output signal from these pins, set up the same value as E2STn and E2EDn.
R017H	D_{15}	TCKSL (R78)	A liquid crystal control timing circuit is selected. 0: Timing Circuit 1 (GSTB, GCLK, GOE, GOE2, RSW, GSW, BSW, and GUD) 1: Timing Circuit 2 (STV, CKV, OEVE, OEV, ASW1, ASW2, ASW3, and XDON) In addition, as for 3-line interlace display function, only the timing circuit 1 corresponds.
	D_{14}	(R93)	γ- resistance is changed. By change of this bit, the resistance between V_S-V_0 which changes with setup of R303H, and the resistance between V63 to V_{SS1} change. For details, refer to **5.5.3 Amplitude adjustment by built-in resistance**.
	D_{13}	GUD (R1)	This pin can be used when changing the direction of gate scan of a panel. A display is possible for a vertical contrary by changing the direction of gate scan of a panel also in the time of the through mode of RGB interface using the output signal from this pin. This command is executed following transfer from the next frame. 0: GUD pin L output (at the time of 3-line interlace opposite direction) 1: GUD pin H output (at the time of 3-line interlace the direction of order) The signal change timing is the same as frame change timing. About frame change timing, refer to **5.4.2 1-frame period timing**.
	D_{12}	RVCOT (R93)	Operation of common timing signal (VCOUT) is controlled. 0: VCOUT signal and FR signal OFF (L output fixed) 1: VCOUT signal and FR signal ON (Normal operation) Setting by this flag becomes valid from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_{11}	RGBSW (R93)	Operation of panel multi-plexus signal (RSW, GSW, BSW) is controlled. 0: OFF (L output fixed) 1: ON (Normal operation) Setting by this flag becomes valid from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_{10}	RGSTB (R93)	Operation of the strobe signal for gate control (GSTB) is controlled. 0: OFF (H output fixed) 1: ON (Normal operation) Setting by this flag becomes valid from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_9	RGCLK (R93)	Operation of the clock signal for gate control (GCLK) is controlled. 0: OFF (L output fixed) 1: ON (Normal operation) Setting by this flag becomes valid from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_8	RASW (R93)	Operation of panel multi-plexus signal (ASW1, ASW2, ASW3) is controlled. 0: OFF (L output fixed) 1: ON (Normal operation) Setting by this flag becomes valid from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.

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Register	Bit	Symbol	Function
R017H	D_7	RSTV (R93)	Operation of the start signal for gate control (STV) is controlled. 0: OFF (L output fixed) 1: ON (Normal operation) Setting by this flag becomes valid from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_6	RCKV (R93)	Operation of the clock signal for gate control (CKV) is controlled. 0: OFF (L output fixed) 1: ON (Normal operation) Setting by this flag becomes valid from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_5	RSOUT (R77)	Operation of source output (Yn) is controlled. 0: OFF (V_{SS} output fixed) 1: ON (Normal operation) Setting by this flag becomes valid from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_4	RGOE2 (R77)	Operation of panel discharge is controlled. 0: GOE2 (H output), RSW, GSW and BSW (Normal operation) 1: GOE2 (L output), RSW, GSW and BSW (H fixed) Setting by this flag becomes valid from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_3	RGOE1 (R77)	Operation of gate output enable signal is controlled. 0: OFF (V_{SS} output fixed) 1: ON (Normal operation) Setting by this flag becomes valid from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_2	RXDON (R77)	Operation of panel discharge is controlled. 0: XDON (L output), ASW1, ASW2 and ASW3 (Normal operation) 1: XDON (H output), ASW1, ASW2 and ASW3 (H fixed) Setting by this flag becomes valid from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_1	ROEVE (R77)	OEVE output operation is controlled. 0: OEVE (L fixed) 1: OEVE (H fixed) Setting by this flag becomes valid from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_0	ROEV (R77)	Operation of output enable signal (OEV) is controlled. 0: OFF (L output fixed) 1: ON (Normal operation) Setting by this flag becomes valid from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td rowspan="4">R018H</td><td>D9
D8</td><td>RPCK1
RPCK0</td><td>ON/OFF control of the clock outputted from the PCCLK pin used as clocks, such as DC/DC converter circuit of power supply IC, is performed.

<table>
<tr><th>RPCK1</th><th>RPCK0</th><th>PCCLK clock output ON/OFF</th></tr>
<tr><td>0</td><td>0</td><td>The output ON during the whole period</td></tr>
<tr><td>0</td><td>1</td><td>The output OFF during the whole period</td></tr>
<tr><td>1</td><td>0</td><td>It output turns on the blanking period output OFF and except it.</td></tr>
<tr><td>1</td><td>1</td><td>The output OFF during the whole period</td></tr>
</table></td></tr>
<tr><td>D6</td><td>RMMSK
(R78)</td><td>The mask of the data of display RAM is carried out by "0" data.
0: All "0" data mask
1: RAM data enable (Normal operation)</td></tr>
<tr><td>D5, D4</td><td>RMST1,
RMST0
(R78)</td><td>It sets up about operation of power supply supplied to RAM circuit.

<table>
<tr><th>RMST1</th><th>RMST0</th><th>Display RAM Power Supply</th><th>Display RAM State</th></tr>
<tr><td>0</td><td>0</td><td>Power OFF</td><td>RAM data is abandoned</td></tr>
<tr><td>0</td><td>1</td><td>Low Power</td><td>RAM data maintenance Note1</td></tr>
<tr><td>1</td><td>0</td><td>Power ON</td><td>RAM writing operation is possible Note2</td></tr>
<tr><td>1</td><td>1</td><td colspan="2">Setting prohibited</td></tr>
</table>

Notes 1. Sleep mode etc. can be used when low power consumption and RAM data need to be held. When normal operation, do not set up (Display ON, writing of display data).
2. When normal operation, use it in this mode (Display ON, writing of display data).</td></tr>
<tr><td>D2
D1</td><td>LMD2
LMD1
(R66)</td><td>AMP drive ON/OFF of source output is selected.

<table>
<tr><th>LMD2</th><th>LMD1</th><th>Display Line</th><th>Blanking Period</th><th>8-color line (partial not displayed)</th></tr>
<tr><td>0</td><td>0</td><td>R/G/BSW period ON</td><td>Between the whole period OFF</td><td>Between the whole period OFF</td></tr>
<tr><td>0</td><td>1</td><td>Between the whole period ON</td><td>Between the whole period OFF</td><td>Between the whole period OFF</td></tr>
<tr><td>1</td><td>0</td><td>R/G/BSW period ON</td><td>The line period OFF set up by BSSPn (R18) from the Blanking period start. The line after it is R/G/BSW period ON.</td><td>Between the whole period OFF</td></tr>
<tr><td>1</td><td>1</td><td>Between the whole period ON</td><td>The line period OFF set up by BSSPn (R18) from the blanking period start. The line after it is between the whole period ON.</td><td>Between the whole period ON</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R019H</td><td>D_{12} to D_8</td><td>DSCGn (R72)</td><td>To compensate for a XDON output H output (it outputs from the next frame of RXDON = H), the output of ASW3, ASW2 and ASW1 are considered as the line period H output fixation set up with this flag. The output of ASW3, ASW2, ASW1, STV, CKV, FR and OEV are carried out to L output fixation after setting period.
When DSCGn = 000H setup, the output of ASW3, ASW2, ASW1, STV, CKV, FR and OEV are carried out to L output fixation to a XDON output H output (it outputs from the next frame of RXDON = H) and this timing.
For more details, refer to 5.8 Power Supply Sequence.

<table>
<tr><th>DSCG4</th><th>DSCG3</th><th>DSCG2</th><th>DSCG1</th><th>DSCG0</th><th>Setting Line Count</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>30</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>31</td></tr>
</table>
</td></tr>
<tr><td></td><td>D_6 to D_4</td><td>REFMn (R68)</td><td>When partial display, the case where it is set as non-refreshing drive ([GSM = 0, PT1 = 1, PT0 = 1] and [GSM = 1, PT1 = 0, PT0 = 0]), non-refreshing frame (source output stop, gate scanning stop) and a refresh cycle (source white level output [the normally white panel], gate scan) are set up in the combination of the value set as this flag and the value set as the REFBn flag.
For more details, refer to 5.6.2 Partial display, non-display area and normal partial driving.
The number of non-refreshing frames = REFB [4:0] x REFM [3:0]

<table>
<tr><th>REFM2</th><th>REFM1</th><th>REFM0</th><th>Setting Value</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>8</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>16</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>32</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>64</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>128</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>256</td></tr>
</table>
</td></tr>
</table>

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R019H</td><td>D3 to D0</td><td>REFBn (R68)</td><td>When partial display, the case where it is set as non-refreshing drive ([GSM = 0, PT1 = 1, PT0 = 1] and [GSM = 1, PT1 = 0, PT0 = 0]), non-refreshing frame (source output stop, gate scanning stop) and a refresh cycle (source white level output [the normally white panel], gate scan) are set up in the combination of the value set as this flag and the value set as the REFMn flag.
For more details, refer to 5.6.2 Partial display, non-display area and normal partial driving.
The number of non-refreshing frames = REFB [4:0] x REFM [3:0]
<table>
<tr><th>REFB3</th><th>REFB2</th><th>REFB1</th><th>REFB0</th><th>Setting Value</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Only non-refresh drive</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>14</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>15</td></tr>
</table>
</td></tr>
<tr><td>R01AH (R26)</td><td>D7 to D4</td><td>VBP</td><td>This bit sets vertical back porch period of RGB interface.
Vertical back porch period = set value x HSYNC unit
In addition, set up more than “2”.</td></tr>
<tr><td></td><td>D3 to D0</td><td>HBP</td><td>This bit sets horizontal back porch period of RGB interface.
Horizontal back porch period = set value x DOTCLK unit
In addition, set up more than “1”.</td></tr>
<tr><td>R01BH (R29)</td><td>D7 to D0</td><td>CAPXMINn</td><td>Minimum of X address is set up at the time of window access at the time of selecting capture mode by the RGB interface.</td></tr>
<tr><td>R01CH (R30)</td><td>D7 to D0</td><td>CAPXMAXn</td><td>Maximum of X address is set up at the time of window access at the time of selecting capture mode by the RGB interface.</td></tr>
<tr><td>R01DH (R31)</td><td>D7 to D0</td><td>CAPYMINn</td><td>Minimum of Y address is set up at the time of window access at the time of selecting capture mode by the RGB interface.</td></tr>
<tr><td>R01EH (R32)</td><td>D7 to D0</td><td>CAPYMAXn</td><td>Maximum of Y address is set up at the time of window access at the time of selecting capture mode by the RGB interface.</td></tr>
</table>

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R021H
(R18)</td><td>D_7 to
D_0</td><td>BSSPn</td><td>The number of bias-off lines from the blanking period start is set up at the time of source output amplifier bias control register LMD = 1 setup.
<table>
<tr><th>Display Mode</th><th>BSSP = 0 Setting</th><th>It is more than BSSP = 1 at the setting time</th></tr>
<tr><td>Internal OSC display</td><td rowspan="2">It is all the blanking period bias ON.</td><td>The bias OFF between several lines of a setting value and henceforth are bias-turned ON from the blanking period start.</td></tr>
<tr><td>VSYNC/HSYNC/ DOTCLK display</td><td>VFP line number + VSYNV Bias is turned off from several lines which applied the BSSP value −1 to the number of ACT lines, and the blanking period start line, and it bias turns on henceforth.
At the time of through mode, it takes −1 from the above-mentioned calculation.
At the time of three-line interlace mode, several dummy line minutes are subtracted from the above-mentioned formula.
Dummy setup of 1 line: −2 line
Dummy setup of 2 line: −4 line</td></tr>
</table></td></tr>
</table>

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R022H
(R34)</td><td>D_3</td><td>LACE3</td><td>3-line interlace display function is selected.
When select 3-line interlace display, blanking period setting register between frames (R75) should set four lines or more and a timing circuit selection register (R78:D_7) as 0.
Refer to the 5.4.3 3-line interlace for operation of 3 line interlace.
In addition, this command is executed from the following frame after transmission.
0: Normal display (Non-Interlace display).
1: 3-line interlace display</td></tr>
<tr><td></td><td>D_2</td><td>LACE2</td><td>The number of the dummy lines between the fields at the time of 3-line interlace display is selected.
In addition, this command is executed from the following frame after transmission.
0: Dummy 2-line 1: Dummy 1-line</td></tr>
<tr><td></td><td>D_1
D_0</td><td>LACE1
LACE0</td><td>The field selection signals EXT1 and EXT2 at the time of a 3-line interlace display change, and a position is selected.

<table>
<tr><th>LACE1</th><th>LACE0</th><th>Changing line</th><th>Changing timing</th></tr>
<tr><td>0</td><td>0</td><td>Just before GSTB output line</td><td>GCLK rising timing</td></tr>
<tr><td>0</td><td>1</td><td>Just before GSTB output line</td><td>GCLK falling timing</td></tr>
<tr><td>1</td><td>0</td><td>Line during GSTB output</td><td>GCLK rising timing</td></tr>
<tr><td>1</td><td>1</td><td>Line during GSTB output</td><td>GCLK falling timing</td></tr>
</table>

In addition, this command is executed from the following frame after transmission.</td></tr>
<tr><td>R101H
(R72)</td><td>D_{15}
D_{14}
D_{13}</td><td>DC4,
DC3
DC2</td><td>The frequency of the clock outputted from the PCCLK pin used as clocks, such as a DC/DC converter circuit of a power supply IC, is set up. This clock is generated from oscillation frequency (f_{OSC}) or external clock DOTCLK, is cycle ratio by the number of setting of this flag, and is outputted.

<table>
<tr><th rowspan="2">DC4</th><th rowspan="2">DC3</th><th colspan="2">PCCLK Clock Frequency</th></tr>
<tr><th>DC2 = 0</th><th>DC2 = 1</th></tr>
<tr><td>0</td><td>0</td><td>f_{OSC} ÷ 4</td><td>DOTCLK ÷ 32</td></tr>
<tr><td>0</td><td>1</td><td>f_{OSC} ÷ 8</td><td>DOTCLK ÷ 64</td></tr>
<tr><td>1</td><td>0</td><td>f_{OSC} ÷ 16</td><td>DOTCLK ÷ 128</td></tr>
<tr><td>1</td><td>1</td><td>f_{OSC} ÷ 32</td><td>DOTCLK ÷ 256</td></tr>
</table>

Remark When outputs a clock signal from PCCLK pin, it is necessary to operate an oscillation circuit (OSC2OFF [R1] = 0).</td></tr>
<tr><td>R110H
(R38)</td><td>D_7 to
D_0</td><td>PSD1n</td><td>The value set as PSD1n is outputted from the serial interface output for external IC control. For more details, refer to 5.1.8 Serial interface for power supply IC control.</td></tr>
<tr><td>R111H
(R39)</td><td>D_7 to
D_0</td><td>PSD2n</td><td>The value set as PSD2n is outputted from the serial interface output for external IC control. For more details, refer to 5.1.8 Serial interface for power supply IC control.</td></tr>
</table>

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R112H
(R40)</td><td>D_7 to
D_0</td><td>PSD3n</td><td>The value set as PSD3n is outputted from the serial interface output for external IC control. For more details, refer to 5.1.8 Serial interface for power supply IC control.</td></tr>
<tr><td>R113H
(R41)</td><td>D_7 to
D_0</td><td>PSD4n</td><td>The value set as PSD4n is outputted from the serial interface output for external IC control. For more details, refer to 5.1.8 Serial interface for power supply IC control.</td></tr>
<tr><td>R114H
(R42)</td><td>D_7 to
D_0</td><td>PSD5n</td><td>The value set as PSD5n is outputted from the serial interface output for external IC control. For more details, refer to 5.1.8 Serial interface for power supply IC control.</td></tr>
<tr><td>R115H
(R60)</td><td>D_7 to
D_0</td><td>PSD6n</td><td>The value set as PSD6n is outputted from the serial interface output for external IC control. For more details, refer to 5.1.8 Serial interface for power supply IC control.</td></tr>
<tr><td>R116H
(R61)</td><td>D_7 to
D_0</td><td>PSD7n</td><td>The value set as PSD7n is outputted from the serial interface output for external IC control. For more details, refer to 5.1.8 Serial interface for power supply IC control.</td></tr>
<tr><td>R117H
(R62)</td><td>D_7 to
D_0</td><td>PSD8n</td><td>The value set as PSD8n is outputted from the serial interface output for external IC control. For more details, refer to 5.1.8 Serial interface for power supply IC control.</td></tr>
<tr><td>R118H
(R63)</td><td>D_7 to
D_0</td><td>PSD9n</td><td>The value set as PSD9n is outputted from the serial interface output for external IC control. For more details, refer to 5.1.8 Serial interface for power supply IC control.</td></tr>
<tr><td>R119H
(R64)</td><td>D_7 to
D_0</td><td>PSDAn</td><td>The value set as PSDAn is outputted from the serial interface output for external IC control. For more details, refer to 5.1.8 Serial interface for power supply IC control.</td></tr>
<tr><td>R11AH
(R65)</td><td>D_7 to
D_0</td><td>PSDBn</td><td>The value set as PSDBn is outputted from the serial interface output for external IC control. For more details, refer to 5.1.8 Serial interface for power supply IC control.</td></tr>
<tr><td>R120H
(R24)</td><td>D_2
D_1
D_0</td><td>E2OPC2
E2OPC1
E2OPC0</td><td>E^2PROM interface is controlled.
<table>
<tr><th>E2OPC2</th><th>E2OPC1</th><th>E2OPC0</th><th>E^2PROM Control</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Setting prohibited</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>EPSAVE: Write in execution to E^2PROM</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>MASKON: Writing / elimination permission to E^2PROM</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>MASKOGF: Writing / elimination permission to E^2PROM</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>EPCLK: All area elimination of E^2PROM</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>EPWALL: It is the writing of FFH to all the area of E^2PROM.</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>EPREAD: Reading execution of E^2PROM</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Setting prohibited</td></tr>
</table></td></tr>
<tr><td>R121H
(R33)</td><td>D_7 to
D_0</td><td>E2An</td><td>The writing address to E^2PROM is specified.</td></tr>
<tr><td>R122H
(R57)</td><td>D_{10} to
D_0</td><td>E2IRn</td><td>The index which writes in to address to E^2PROM is specified.
The index and data of the register specified to be this register are written in the address of E^2PROM specified by R33.</td></tr>
<tr><td>R123H
(R58)</td><td>D_7 to
D_0</td><td>E2SAn</td><td>The reading start address of E^2PROM is specified.</td></tr>
</table>

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Register	Bit	Symbol	Function
R200H (R6)	D_7 to D_0	AD_7 to AD_0	This register sets the X address of the display RAM. Set 000H to 0EFH.
R201H (R7)	D_8 to D_0	AD_{16} to AD_8	This register sets the Y address of the display RAM. Set 000H to 13FH.
R202H			
R203H	D_{13} to D_8	WM_{11} to WD_6	At the time of the writing to GRAM, a write mask is carried out per bit. At the time of WM17 = 1, the mask of the most upper bit of GRAM writing data is carried out, and the writing to GRAM is not performed. Moreover, the mask of the GRAM writing data is carried out similarly 0 bit of WM16 to WM0, respectively. Note to that write data mask is performed to GRAM writing data (18 bits).
	D_5 to D_0	WM_5 to WD_0	
R204H	D_5 to D_0	WM_{17} to WD_{12}	**Remark** This function cannot be used at the time of RGB interface use.

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Register	Bit	Symbol	Function
R300H (R43)	D_4	GSEL	Sets the maximum/minimum output potential of the γ–correction register. If the internal γ-output adjustment circuit is selected, the maximum/minimum output potential of the γ-correction register is: 0: Sets power supply voltage (outputs V_S and V_{SS} potential). 1: Uses voltage of internal γ-output adjustment circuit (uses VPH, VNH, VPL, VNL output)
	D_0	GONSEL	About connection between γ-correction resistance and a power supply 0: Connect the both ends of positive-polarity γ-resistance with V_S and GND when in used γ-correction by positive-polarity. On the other hand, γ-resistance by negative-polarity does not connect with V_S and GND. Moreover, the both ends of negative-polarity γ-resistance are connected with V_S and GND when in used γ-correction by negative-polarity. In that case, γ-resistance by positive-polarity does not connect with V_S and GND. 1: Connect both V_S and GND on the side of positive and negative γ-correction regardless of output from positive- or negative-polarity.
R301H	D_{15} to D_8	GPLn (R46)	Sets the voltage value of γ-amplitude adjustment of positive polarity. For more detail, refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_7 to D_0	GPHn (R44)	Sets the voltage value of γ-amplitude adjustment of positive polarity. For more detail, refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R302H	D_7 to D_0	GNLn (R47)	Sets the voltage value of γ-amplitude adjustment of negative polarity. For more detail, refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_7 to D_0	GNHn (R45)	Sets the voltage value of γ-amplitude adjustment of negative polarity. For more detail, refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R303H	D_{15} to D_{12}	VDRNn (R52)	Negative-polarity γ-amplitude adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_{11} to D_8	VSRNn (R52)	Negative-polarity γ-amplitude adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_7 to D_4	VDRPn (R48)	Positive-polarity γ-amplitude adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_3 to D_0	VSRPn (R48)	Positive-polarity γ-amplitude adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R304H	D_{15} to D_{12}	VLRNn (R53)	Negative-polarity γ-inclination adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_{11} to D_8	VHRNn (R53)	Negative-polarity γ-inclination adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_7 to D_4	VLRPn (R49)	Positive-polarity γ-inclination adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_3 to D_0	VHRPn (R49)	Positive-polarity γ-inclination adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R305H	D_{14} to D_{12}	VGR3Pn (R51)	Positive-polarity γ-fine tuning adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_{10} to D_8	VGR2Pn (R51)	Positive-polarity γ-fine tuning adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_6 to D_4	VGR1Pn (R50)	Positive-polarity γ-fine tuning adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_2 to D_0	VGR0Pn (R50)	Positive-polarity γ-fine tuning adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td rowspan="4">R306H</td><td>D_{14} to D_{12}</td><td>VGR3Nn (R55)</td><td>Negative-polarity γ-fine tuning adjustment register
Refer to 5.5 γ- Curve Correction Power Supply Circuit.</td></tr>
<tr><td>D_{10} to D_8</td><td>VGR2Nn (R55)</td><td>Negative-polarity γ-fine tuning adjustment register
Refer to 5.5 γ- Curve Correction Power Supply Circuit.</td></tr>
<tr><td>D_6 to D_4</td><td>VGR1Nn (R54)</td><td>Negative-polarity γ-fine tuning adjustment register
Refer to 5.5 γ- Curve Correction Power Supply Circuit.</td></tr>
<tr><td>D_2 to D_0</td><td>VGR0Nn (R54)</td><td>Negative-polarity γ-fine tuning adjustment register
Refer to 5.5 γ- Curve Correction Power Supply Circuit.</td></tr>
<tr><td>R307H (R56)</td><td>D_1, D_0</td><td>GV8S1</td><td>The voltage concerning a panel is set at the time of 8-color mode.
0 : Set power supply
1: Set amplifier output</td></tr>
<tr><td rowspan="2">R308H (R59)</td><td>D_7</td><td>WHP</td><td>Sets the output mode of the reference voltage generator amplifier for setting the white level of the positive-polarity and negative-polarity sides (when VPL and VNL are normally white), as shown below.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
0: Normal mode
1: High-power mode (output circuit capacity: twice that of normal mode)</td></tr>
<tr><td>D_6 to D_4</td><td>WIn</td><td>Sets the output bias current of the reference voltage generator amplifier for setting the white level of the positive-polarity and negative-polarity sides (when VPL and VNL are normally white), as shown below.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
<table>
<tr><th>WI2</th><th>WI1</th><th>WI0</th><th>Amplifier Bias Current</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0.025 μA</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0.050 μA</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0.100 μA</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0.200 μA</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0.500 μA</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1.000 μA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1.500 μA</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>2.000 μA</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td rowspan="2">R308H
(R59)</td><td>D_3</td><td>BHP</td><td>Sets the output mode of the reference voltage generator amplifier for setting the black level of the positive-polarity and negative-polarity sides (when VPL and VNL are normally white), as shown below.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
0: Normal mode
1: High-power mode (output circuit capacity: twice that of normal mode)</td></tr>
<tr><td>D_2 to D_0</td><td>BIn</td><td>Sets the output bias current of the reference voltage generator amplifier for setting the black level of the positive-polarity and negative-polarity sides (when VPL and VNL are normally white), as shown below.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
<table><tr><th>WI2</th><th>WI1</th><th>WI0</th><th>Amplifier Bias Current</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0.025 μA</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0.050 μA</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0.100 μA</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0.200 μA</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0.500 μA</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1.000 μA</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1.500 μA</td></tr><tr><td>1</td><td>1</td><td>1</td><td>2.000 μA</td></tr></table></td></tr>
</table>

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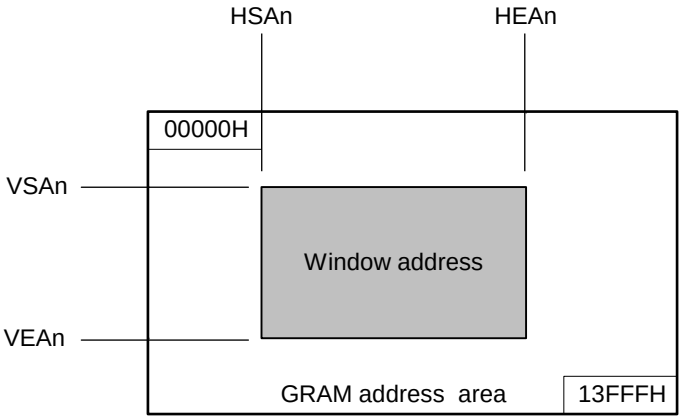
<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R400H</td><td>D8 to D0</td><td>VL18 to VL10</td><td>The amount of scroll of the 1st panel scroll display is specified, and a vertical smooth scroll display is performed. It can display of scroll arbitrary line from 0 to 319 lines. The display is again started after displaying the last 320 lines repeatedly from top 1 line. In addition, the amount of scroll (VL18 to VL10) becomes valid when 1st panel vertical scroll enable bit VLE1 = 1. When VLE1 = 0, it becomes the fixed line display.
Caution This function cannot be used at the time of external display interface use.

<table>
<tr><th>VL18</th><th>VL17</th><th>VL16</th><th>VL15</th><th>VL14</th><th>VL13</th><th>VL12</th><th>VL11</th><th>VL10</th><th>Amount of scroll</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0 line</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1 line</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2 line</td></tr>
<tr><td colspan="5"></td><td>:</td><td></td><td></td><td></td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>318 line</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>319 line</td></tr>
</table>
</td></tr>
<tr><td>R401H</td><td>D8 to D0</td><td>VL28 to VL20</td><td>The amount of scroll of the 2nd panel scroll display is specified, and a vertical smooth scroll display is performed. It can display of scroll arbitrary line from 0 to 319 lines. The display is again started after displaying the last 320 lines repeatedly from top 1 line. In addition, the amount of scroll (VL28 to VL20) becomes valid when 1st panel vertical scroll enable bit VLE2 = 1. When VLE2 = 0, it becomes the fixed line display.
Caution This function cannot be used at the time of external display interface use.

<table>
<tr><th>VL28</th><th>VL27</th><th>VL26</th><th>VL25</th><th>VL24</th><th>VL23</th><th>VL22</th><th>VL21</th><th>VL20</th><th>Amount of scroll</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0 line</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1 line</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2 line</td></tr>
<tr><td colspan="5"></td><td>:</td><td></td><td></td><td></td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>318 line</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>319 line</td></tr>
</table>
</td></tr>
<tr><td>R402H</td><td>D8 to D0</td><td>SS18 to SS10</td><td>The drive start position of the 1st panel is specified per line. The liquid crystal drive is started from the line of the setting value + 1.</td></tr>
<tr><td>R403H</td><td>D8 to D0</td><td>SE18 to SE10</td><td>The drive end position of the 1st panel is specified per line. The liquid crystal drive is performed to the line of the setting value +1. For example, when SS18 to SS10 = 07H, SE18 to SE10 = 10H are set up, the liquid crystal drive is performed to 8 to 17 line, and a drive non-switching on the light is performed after 1 to 7 line and 18 line. Be sure to set up the size relation of SS18 to SS10 ≤ SE18 to SE10 ≤ 13FH.</td></tr>
<tr><td>R404H</td><td>D8 to D0</td><td>SS28 to SS20</td><td>The drive start position of the 2nd panel is specified per line. The liquid crystal drive is started from the line of the setting value + 1. In addition, be sure to set up the size relation of SE18 to SE10 < SS28 to SS20.</td></tr>
<tr><td>R405H</td><td>D8 to D0</td><td>SE28 to SE20</td><td>The drive end position of the 2nd panel is specified per line. The liquid crystal drive is performed to the line of the setting value +1. For example, when SS28 to SS20 = 07H, SE28 to SE20 = 10H are set up, the liquid crystal drive is performed to 8 to 17 line, and a drive non-switching on the light is performed after 1 to 7 line and 18 line. Be sure to set up the size relation of SS28 to SS20 ≤ SE28 to SE20 ≤ 23FH.</td></tr>
</table>

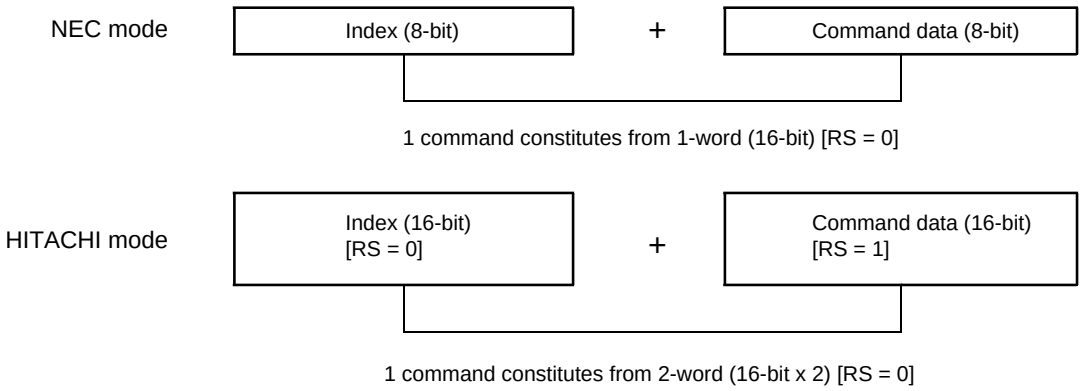
<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R406H</td><td>D7 to D0</td><td>HSA7 to HSA0</td><td rowspan="3">The horizon address start/end position of window address is specified per address. The data can be written in GRAM in the address specified to be VEA7 to VEA0 from the address set as VSA7 to VSA0. However, be sure to perform an address set before RAM writing. Be sure to set up the size relation of 000 H ≤ HSA7 to HSA0 ≤ HEA7 to HEA0 ≤ FFH.</td></tr>
<tr><td>R407H</td><td>D7 to D0</td><td>HEA7 to HEA0</td></tr>
<tr><td>R408H</td><td>D8 to D0</td><td>VSA7 to VSA0</td></tr>
<tr><td>R409H</td><td>D8 to D0</td><td>VEA7 to VEA0</td><td>The vertical address start/end position of window address is specified per address. The data can be written in GRAM in the address specified to be VEA7 to VEA0 from the address set as VSA7 to VSA0. However, be sure to perform an address set before RAM writing. Be sure to set up the size relation of 000 H ≤ HSA7 to HSA0 ≤ HEA7 to HEA0 ≤ 13FH.
 

Caution Be sure to set up the area of window address to enter in GRAM address space.</td></tr>
<tr><td>R554H
(R73)</td><td>D3 to D0</td><td>BCONBn</td><td>The bias current for liquid crystal drive AMP is set up.

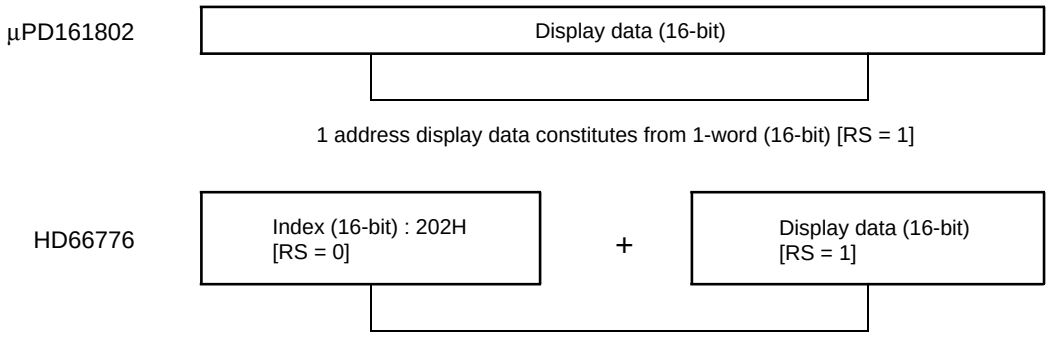
<table>
<tr><th>BCONB3</th><th>BCONB2</th><th>BCONB1</th><th>BCONB0</th><th>Bias Current [μA]</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0.87</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1.67</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>2.43</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>3.18</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>3.98 (default)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>4.70</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>5.41</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>6.11</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>6.88</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>7.57</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>8.24</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>8.91</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>9.62</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>10.28</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>10.93</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>11.58</td></tr>
</table>
</td></tr>
</table>

[NEC mode, HITACHI mode difference]

1. Command input system



2. Display data input system (example of 16-bit/pixel)



By the index (RS = 0), display data is inputted for [RAM data write/read : 202H] after selection (RS = 1).
Display data is also dealt with as a part of index register.

REVISION HISTORY

Edition/Data	Page		Description	
	Previous edition	This version	Type of revision	Location
September 2003 Ver 0.2	p.66	p.66	Correction	3-line interlace explanation correction
	p.190, p.208	p.190, p.208	Correction	E2IR [7:0] is corrected to E2IR [10:0]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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