

5 V, SILICON MMIC WIDEBAND AMPLIFIER

DESCRIPTION

The μPC3224TB is a silicon monolithic IC designed as IF amplifier for DBS tuners. This IC is manufactured using our 30 GHz f_{max} UHS0 (Ultra High Speed Process) silicon bipolar process.

FEATURES

- Wideband response : $f_u = 3.2$ GHz TYP. @ 3 dB bandwidth
- Low current : $I_{CC} = 9.0$ mA TYP.
- Power gain : $G_P = 21.5$ dB TYP. @ $f = 1.0$ GHz
: $G_P = 21.5$ dB TYP. @ $f = 2.2$ GHz
- Supply voltage : $V_{CC} = 4.5$ to 5.5 V
- Port impedance : input/output $50\ \Omega$

APPLICATION

- IF amplifiers in DBS converters etc.

ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
μPC3224TB-E3	6-pin super minimold	C3K	<ul style="list-style-type: none"> • Embossed tape 8 mm wide • 1, 2, 3 pins face the perforation side of tape • Qty 3 kpcs/reel

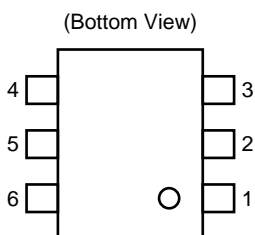
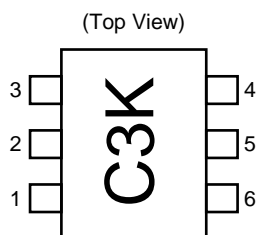
Remark To order evaluation samples, contact your nearby sales office.

Part number for sample order: μPC3224TB

Caution Observe precautions when handling because these devices are sensitive to electrostatic discharge.

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Not all devices/types available in every country. Please check with local NEC Compound Semiconductor Devices representative for availability and additional information.

PIN CONNECTIONS



Pin No.	Pin Name
1	INPUT
2	GND
3	GND
4	OUTPUT
5	GND
6	V _{CC}

PRODUCT LINE-UP OF 5 V-BIAS SILICON MMIC MEDIUM WIDEBAND AMPLIFIER

(T_A = +25°C, f = 1 GHz, V_{CC} = V_{out} = 5.0 V, Z_s = Z_L = 50 Ω)

Part No.	f _u (GHz)	P _{O(sat)} (dBm)	G _P (dB)	NF (dB)	I _{cc} (mA)	Package	Marking
μ PC2711TB	2.9	+1.0	13	5.0	12	6-pin super minimold	C1G
μ PC2712TB	2.6	+3.0	20	4.5	12		C1H
μ PC3215TB ^{Note}	2.9	+3.5	20.5	2.3	14		C3H
μ PC3224TB	3.2	+4.0	21.5	4.3	9.0		C3K

Note μ PC3215TB is f = 1.5 GHz

Remark Typical performance. Please refer to **ELECTRICAL CHARACTERISTICS** in detail.

PIN EXPLANATIONS

PIN No.	Pin Name	Applied Voltage (V)	Pin Voltage (V) <small>Note</small>	Function and Applications
1	INPUT	—	0.91	Signal input pin. A internal matching circuit, configured with resistors, enables 50 Ω connection over a wide band. A multi-feedback circuits is designed to cancel the deviations of h_{FE} and resistance. This pin must be coupled to signal source with capacitor for DC cut.
4	OUTPUT	—	4.42	Signal output pin. A internal matching circuit, configured with resistors, enables 50 Ω connection over a wide band. This pin must be coupled to next stage with capacitor for DC cut.
6	V _{CC}	4.5 to 5.5	—	Power supply pin. This pin should be externally equipped with bypass capacitor to minimize its impedance.
2 3 5	GND	0	—	Ground pin. This pin should be connected to system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. All the ground pins must be connected together with wide ground pattern to decrease impedance difference.

Note Pin Voltage is measured at V_{CC} = 5.0 V

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{CC}	$T_A = +25^{\circ}\text{C}$	6.0	V
Total Circuit Current	I_{CC}	$T_A = +25^{\circ}\text{C}$	25	mA
Power Dissipation	P_D	$T_A = +85^{\circ}\text{C}$ Note	270	mW
Operating Ambient Temperature	T_A		-40 to +85	$^{\circ}\text{C}$
Storage Temperature	T_{stg}		-55 to +150	$^{\circ}\text{C}$
Input Power	P_{in}	$T_A = +25^{\circ}\text{C}$	+10	dBm

Note Mounted on double-sided copper-clad 50 × 50 × 1.6 mm epoxy glass PWB

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Operating Ambient Temperature	T_A		-40	+25	+85	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = +25^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V}$, $Z_S = Z_L = 50\ \Omega$)

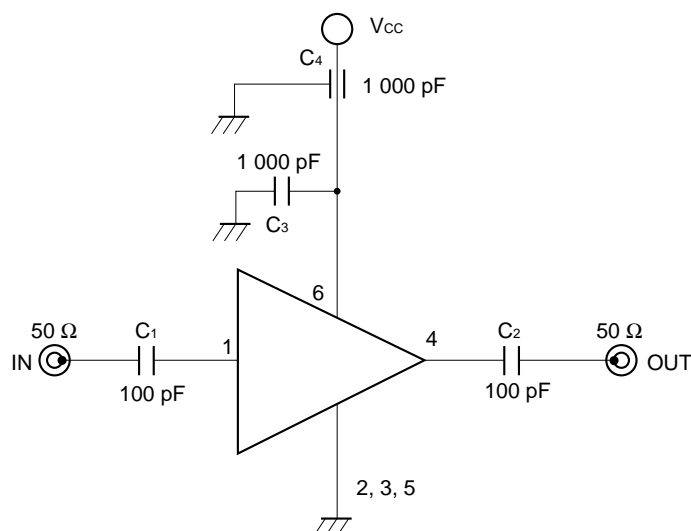
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	I_{CC}	No input signal	7.0	9.0	12.0	mA
Power Gain	G_P	$f = 1.0\text{ GHz}$, $P_{in} = -30\text{ dBm}$	19.0	21.5	24.0	dB
		$f = 2.2\text{ GHz}$, $P_{in} = -30\text{ dBm}$	18.5	21.5	24.5	
Saturated Output Power	$P_{O(sat)}$	$f = 1.0\text{ GHz}$, $P_{in} = -5\text{ dBm}$	+1.5	+4.0	—	dBm
		$f = 2.2\text{ GHz}$, $P_{in} = -5\text{ dBm}$	-1.5	+1.5	—	
Gain 1 dB Compression Output Power	$P_{O(1\text{ dB})}$	$f = 1.0\text{ GHz}$	-6.5	-3.5	—	dBm
		$f = 2.2\text{ GHz}$	-8.5	-5.5	—	
Noise Figure	NF	$f = 1.0\text{ GHz}$	—	4.3	5.8	dB
		$f = 2.2\text{ GHz}$	—	4.3	5.8	
Upper Limit Operating Frequency	f_u	3 dB down below flat gain at $f = 0.1\text{ GHz}$	2.8	3.2	—	GHz
Isolation	ISL	$f = 1.0\text{ GHz}$, $P_{in} = -30\text{ dBm}$	35.0	40.0	—	dB
		$f = 2.2\text{ GHz}$, $P_{in} = -30\text{ dBm}$	37.0	42.0	—	
Input Return Loss	RL_{in}	$f = 1.0\text{ GHz}$, $P_{in} = -30\text{ dBm}$	9.0	12.0	—	dB
		$f = 2.2\text{ GHz}$, $P_{in} = -30\text{ dBm}$	10.0	14.0	—	
Output Return Loss	RL_{out}	$f = 1.0\text{ GHz}$, $P_{in} = -30\text{ dBm}$	11.0	17.0	—	dB
		$f = 2.2\text{ GHz}$, $P_{in} = -30\text{ dBm}$	8.0	12.0	—	
Gain Flatness	ΔG_P	$f = 0.1\text{ to }2.2\text{ GHz}$	—	± 0.8	—	dB

OTHER CHARACTERISTICS, FOR REFERENCE PURPOSES ONLY

(T_A = +25°C, V_{CC} = 5.0 V, Z_S = Z_L = 50 Ω)

Parameter	Symbol	Test Conditions	Reference Value	Unit
Output Intercept Point	OIP ₃	f = 1.0 GHz	+7.0	dBm
		f = 2.2 GHz	+5.5	

TEST CIRCUIT



The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

COMPONENTS OF TEST CIRCUIT FOR MEASURING ELECTRICAL CHARACTERISTICS

	Type	Value
C ₁ , C ₂	Chip Capacitor	100 pF
C ₃	Chip Capacitor	1 000 pF
C ₄	Feed-through Capacitor	1 000 pF

CAPACITORS FOR THE V_{CC}, INPUT AND OUTPUT PINS

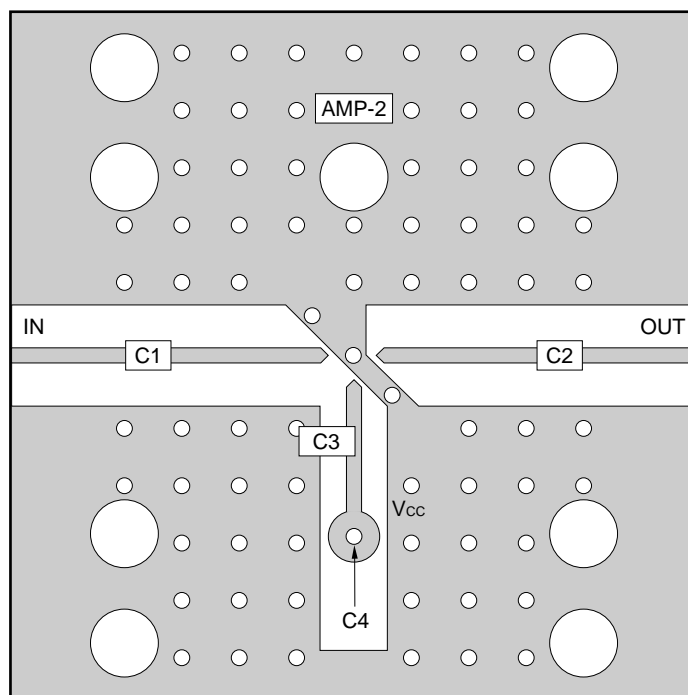
Capacitors of 1000 pF are recommendable as the bypass capacitor for the V_{CC} pin and the coupling capacitors for the input and output pins.

The bypass capacitor connected to the V_{CC} pin is used to minimize ground impedance of V_{CC} pin. So, stable bias can be supplied against V_{CC} fluctuation.

The coupling capacitors, connected to the input and output pins, are used to cut the DC and minimize RF serial impedance. Their capacitances are therefore selected as lower impedance against a 50 Ω load. The capacitors thus perform as high pass filters, suppressing low frequencies to DC.

To obtain a flat gain from 100 MHz upwards, 1 000 pF capacitors are used in the test circuit. In the case of under 10 MHz operation, increase the value of coupling capacitor such as 10 000 pF. Because the coupling capacitors are determined by equation, $C = 1/(2 \pi R f_c)$.

ILLUSTRATION OF THE TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD



COMPONENT LIST

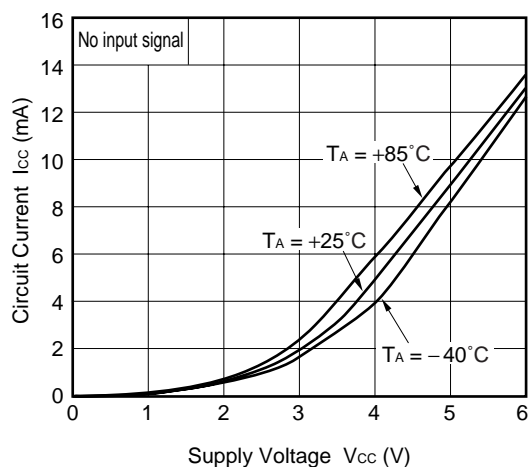
	Value
C ₁ , C ₂	100 pF
C ₃ , C ₄	1 000 pF

Notes

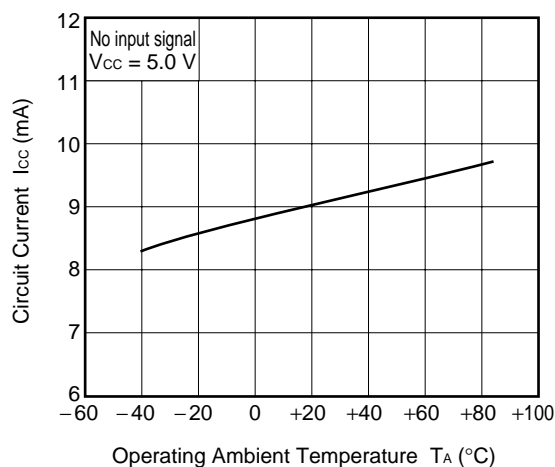
1. 30 × 30 × 0.4 mm double sided copper clad polyimide board.
2. Back side: GND pattern
3. Solder plated on pattern
4. ○○: Through holes

TYPICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$, unless otherwise specified)

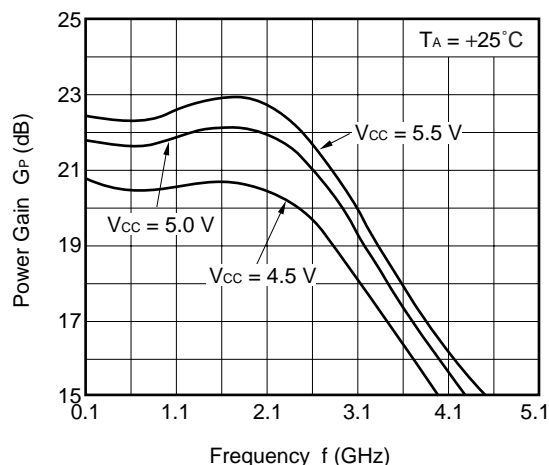
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



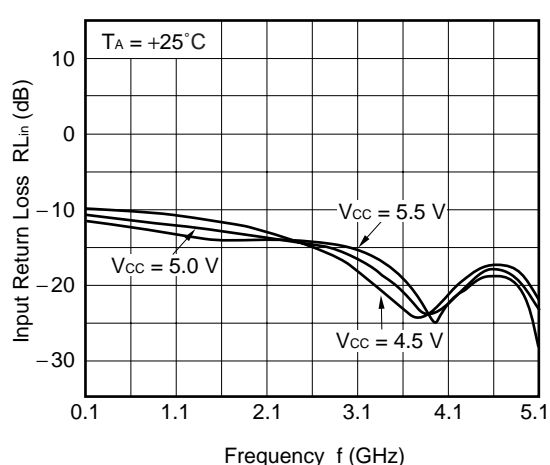
CIRCUIT CURRENT vs. OPERATING AMBIENT TEMPERATURE



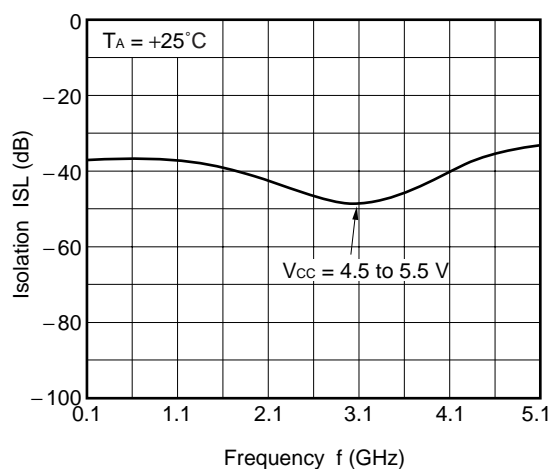
POWER GAIN vs. FREQUENCY



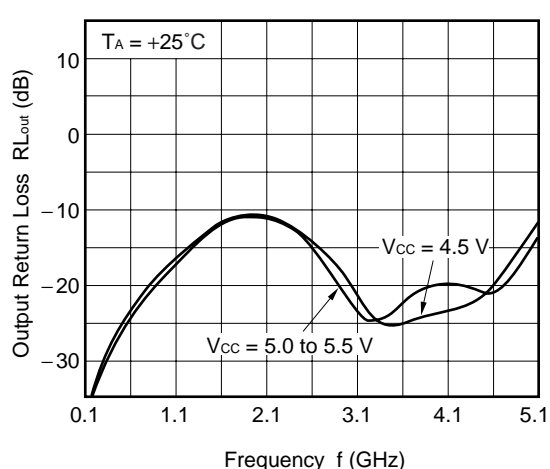
INPUT RETURN LOSS vs. FREQUENCY



ISOLATION vs. FREQUENCY

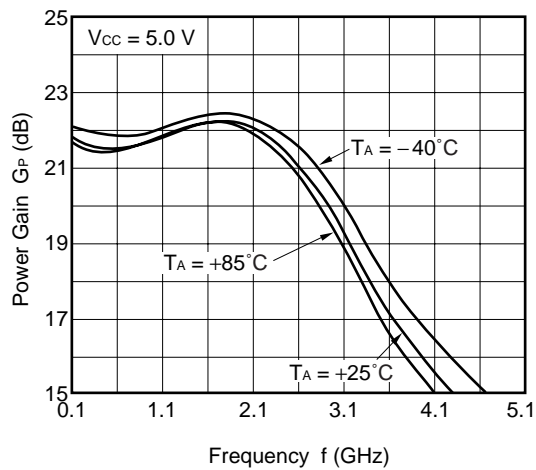


OUTPUT RETURN LOSS vs. FREQUENCY

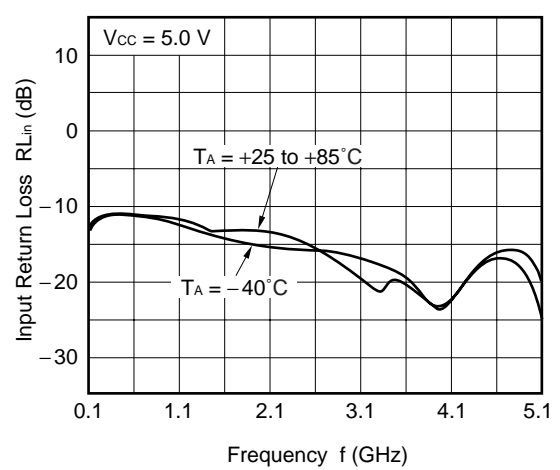


Remark The graphs indicate nominal characteristics.

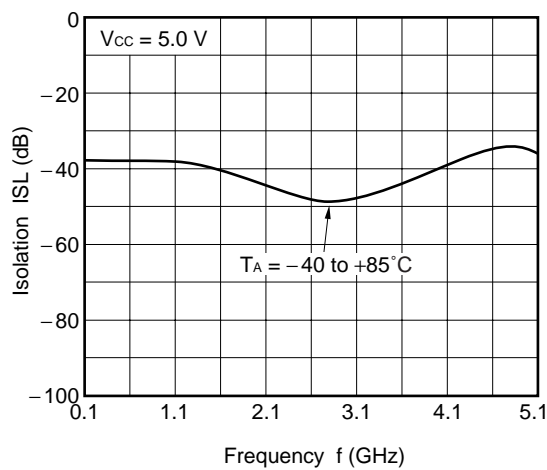
POWER GAIN vs. FREQUENCY



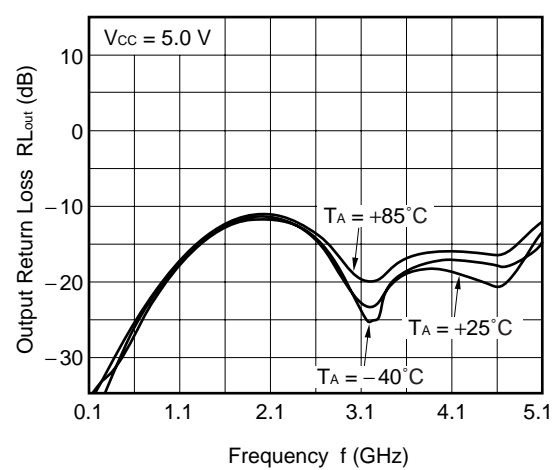
INPUT RETURN LOSS vs. FREQUENCY



ISOLATION vs. FREQUENCY

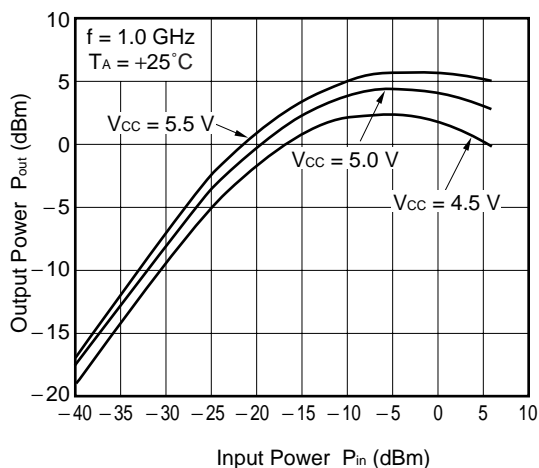


OUTPUT RETURN LOSS vs. FREQUENCY

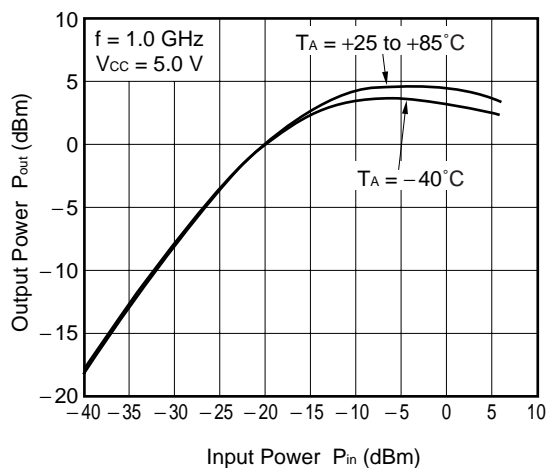


Remark The graphs indicate nominal characteristics.

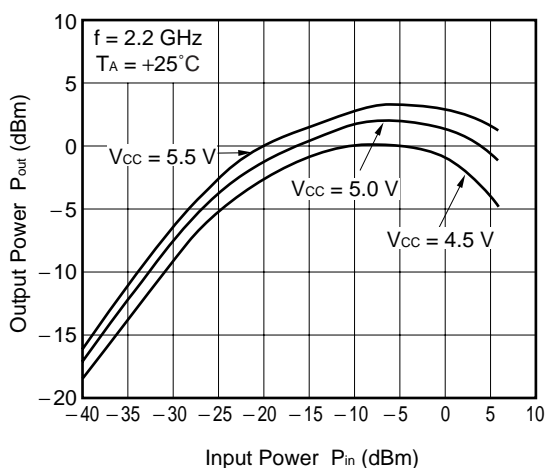
OUTPUT POWER vs. INPUT POWER



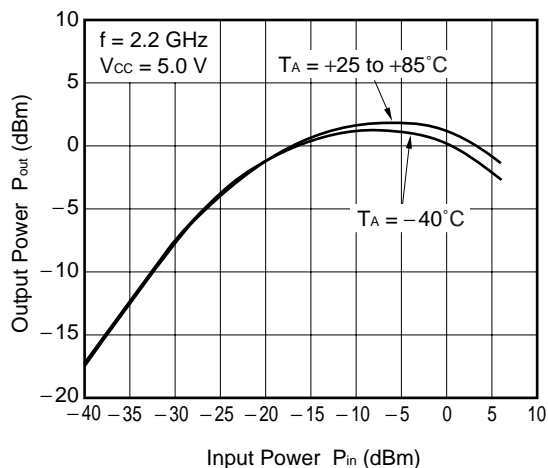
OUTPUT POWER vs. INPUT POWER



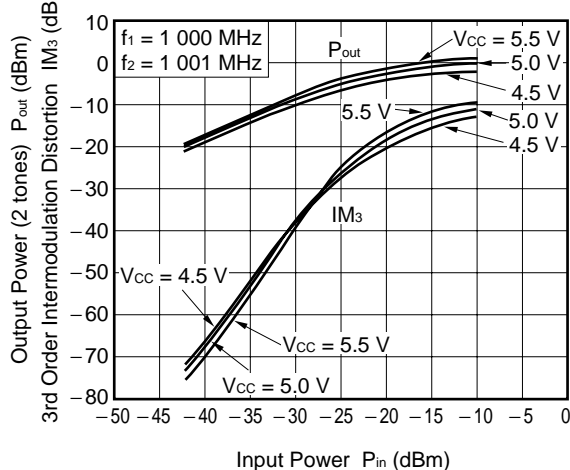
OUTPUT POWER vs. INPUT POWER



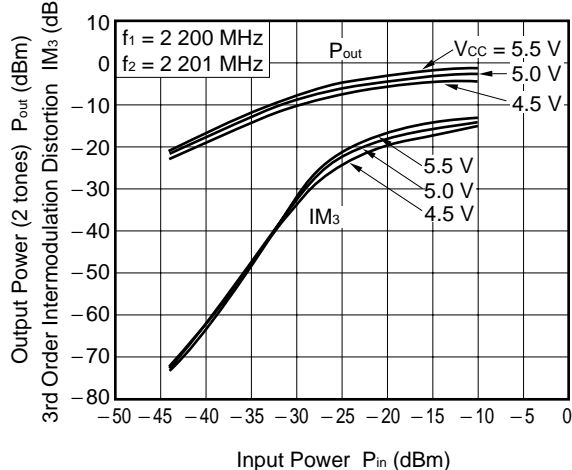
OUTPUT POWER vs. INPUT POWER



OUTPUT POWER (2 tones), IM_3 vs. INPUT POWER



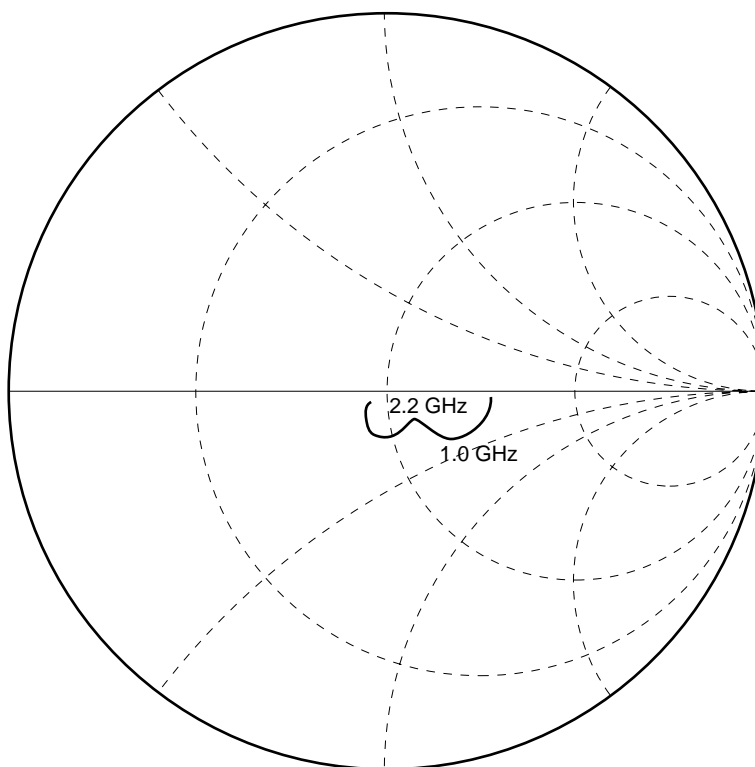
OUTPUT POWER (2 tones), IM_3 vs. INPUT POWER



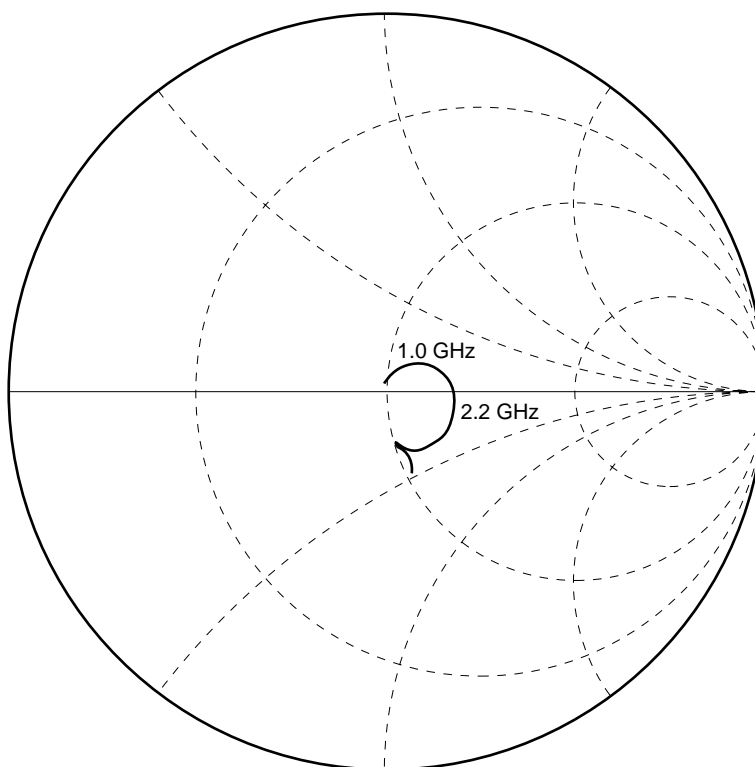
Remark The graphs indicate nominal characteristics.

S-PARAMETERS ($T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

S_{11} -FREQUENCY

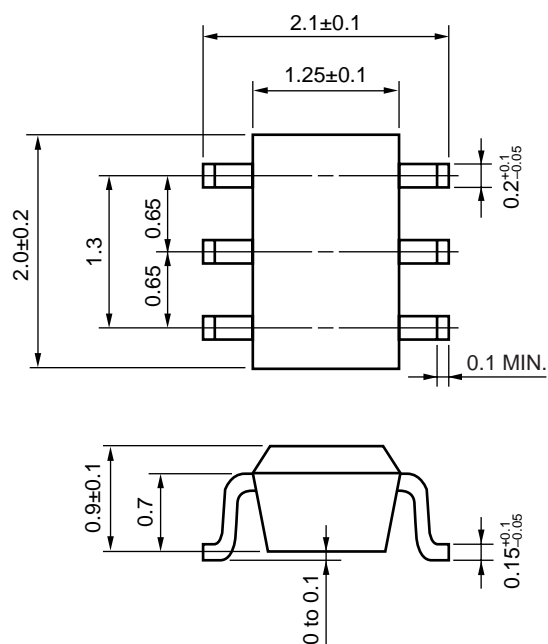


S_{22} -FREQUENCY



PACKAGE DIMENSIONS

6-PIN SUPER MINIMOLD (UNIT: mm)



NOTES ON CORRECT USE

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired oscillation).
All the ground pins must be connected together with wide ground pattern to decrease impedance difference.
- (3) The bypass capacitor should be attached to Vcc line.
- (4) The DC cut capacitor must be each attached to input and output pin.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions	Condition Symbol
Infrared Reflow	Peak temperature (package surface temperature) : 260°C or below Time at peak temperature : 10 seconds or less Time at temperature of 220°C or higher : 60 seconds or less Preheating time at 120 to 180°C : 120±30 seconds Maximum number of reflow processes : 3 times Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	IR260
Wave Soldering	Peak temperature (molten solder temperature) : 260°C or below Time at peak temperature : 10 seconds or less Preheating temperature (package surface temperature) : 120°C or below Maximum number of flow processes : 1 time Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	WS260
Partial Heating	Peak temperature (pin temperature) : 350°C or below Soldering time (per side of device) : 3 seconds or less Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	HS350

Caution Do not use different soldering methods together (except for partial heating).

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