# uP9531P

## Dual Output 2+1 Phase PWM Controller with 3 Embedded 5V Drivers for AMD® SVI2 Mobile CPU Core Power

## General Description

The uP9531P is an AMD® SVI2 compliant mobile CPU voltage regulator controller that integrates a 2-phase PWM controller for VDD and a 1-phase PWM controller for VDDA. The VDD controller can be configured as 2/1-phase, and the VDDA controller can be configured as1/0-phase (0 denotes VDDA controller is disabled) for platform power design flexibility. The controller provides further flexible operating phase configuration to support 3+0 application.

This device has 3 embedded 5V MOSFET drivers with integrated bootstrap diodes. This device combines true differential output voltage sense, inductor DCR current sense, input voltage sense and adaptive voltage positioning to provide accurately regulated voltage for mobile CPU. It adopts uPI's proprietary RCOT+™ (Robust Constant On-Time) control topology to have fast transient response. The uP9531P supports diode emulation mode operation to enhance the light load efficiency.

The uP9531P provides power good indicator and thermal hot indicator. It also provides complete fault protection functions, including over voltage, under voltage, over current, thermal shutdown and under voltage lockout. The uP9531P is available in WQFN5x5 - 40L package.

## Features

- AMD® SVI2 Compliant
- RCOT+™ Control Topology
  - Easy Setting
  - Fast Transient Response
- 3-Embedded MOSFET Drivers with Bootstrap Diode
- Flexible Operation Phase Configuration
  - 2/1-Phase for VDD
  - 1/0-Phase for VDDA
  - Support 3+0 Phase Application
- SVI2 Voltage Regulator Address Selection
- Diode Emulation Mode at Light Load Condition
- Function Setting Pin for Regulator Parameter Setting
- Inductor DCR Current Sense for Droop/Per Phase OCP/Total Output OCP
- Differential Remote Output Voltage Sense
- Power Good Indicator
- Temperature Sense and Thermal Hot Indicator
- OCP/UVP/OVP/UVLO/Thermal Shutdown
- RoHS Compliant and Halogen Free

## Applications

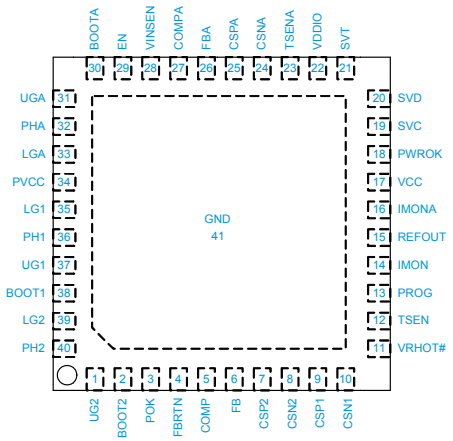
- AMD® SVI2 Mobile CPU Voltage Regulator
- Laptop Computer

## Ordering Information

| Order Number | Package Type | Top Marking |
|---|---|---|
| uP9531PQKJ | WQFN5x5-40L | uP9531P |

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

## Pin Configuration





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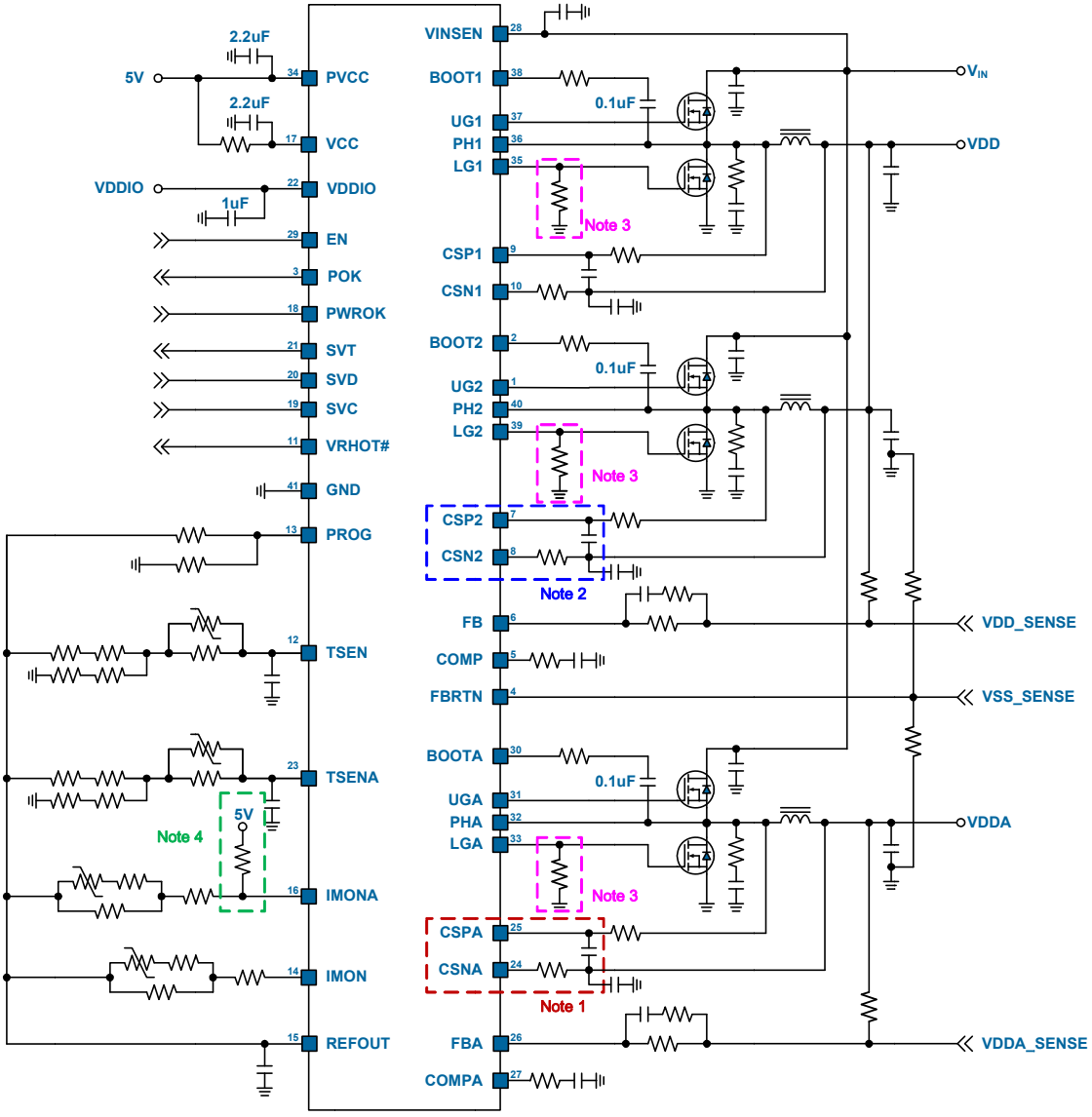
# uP9531P

## Typical Application Circuit




Note 1:
To disable VDDA for 2+0 phase application,
CSNA should be pulled up to 5V with R=1kΩ, and CSPA should be connected to GND.

Note 2:
To disable phase 2 of VDD for 1+1 phase application,
CSN2 should be pulled up to 5V with R=1kΩ, and CSP2 should be connected to GND.

Note 3:
The program setting resistor of LG1,LG2 and LGA must be required within 15kΩ to 65kΩ.

Note 4:
For 3+0 phase application, IMONA should be pulled up to 5V with R=1kΩ.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## Functional Pin Description

| Pin No. | Name | Pin Function |
|---|---|---|
| 1 | UG2 | **Upper Gate Driver Output for VDD Phase 2.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when to turn on/off upper MOSFET. |
| 2 | BOOT2 | **Bootstrap Supply of Upper Gate Driver for VDD Phase 2.** This pin is the supply input for the upper MOSFET gate driver. Connect the bootstrap capacitor $C_{BOOT}$ between BOOT2 pin and PH2 pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Use at least 0.1uF MLCC as $C_{BOOT}$, and make sure it is placed close to the controller. |
| 3 | POK | **Power Good Indicator.** This pin is an open-drain structure and it is active high. Pull up this pin through a proper resistor to a voltage source. The controller asserts POK (goes high) at the end of both VDD and VDDA output ramping up to their Vboot voltage if no fault occurs. |
| 4 | FBRTN | **Output Voltage Feedback Return for VDD and VDDA.** This pin is the inverting input to the differential voltage sense amplifier. Connect this pin directly to the processor output voltage feedback return sense point, namely VSS_SENSE. For AMD processors, both the VDD and VDDA outputs share the same output voltage feedback return input. |
| 5 | COMP | **Output of Control Loop Error Amplifier for VDD.** Connect a resistor in series with a capacitor from this pin to GND for voltage control loop compensation. |
| 6 | FB | **Inverting Input of the Error Amplifier for VDD.** |
| 7 | CSP2 | **Positive Differential Current Sense Input for VDD Phase 2.** When VDD phase 2 is not used, short this pin to GND to let VDD voltage regulator operate in single phase configuration. |
| 8 | CSN2 | **Negative Differential Current Sense Input for VDD Phase 2.** When VDD phase 2 is not used, pull high this pin to 5V through a 1kΩ resistor to let VDD voltage regulator operate in single phase configuration. |
| 9 | CSP1 | **Positive Differential Current Sense Input for VDD Phase 1.** |
| 10 | CSN1 | **Negative Differential Current Sense Input for VDD Phase 1.** |
| 11 | VRHOT# | **Thermal Hot Indicator.** This pin is an open drain structure and it is active low. Pull up this pin through a proper resistor to a voltage source. The controller asserts VRHOT#(goes low) when the voltage of TSEN or TSENA is lower than 2.2V. |
| 12 | TSEN | **Thermal Sense Input for VDD.** This pin is a multi-functional pin, and it provides three functions as below.<br>1. Temperature sense input of VRHOT# indicator for VDD regulator. Connect a resistor voltage divider with a specified negative temperature coefficient (NTC) thermistor network from REFOUT pin to GND for VDD voltage regulator temperature sense.<br>2. VDD output voltage offset setting. Connect a resistor divider network to set the VDD output voltage offset. The VDD output voltage is the sum of VID value and the voltage offset. Refer to Output Voltage Offset section for detail.<br>3. Provide switching frequency compensation with load with TSENA pin for VDD and VDDA. Refer to Switching Frequency Compensation section for detail. |
| 13 | PROG | **Function Setting Pin.** Connect a resistor voltage divider from REFOUT to GND to set the regulator parameters, including initial start up voltage (Vboot) for VDDA, PWM on time, operation phase configuration and downward slew rate of dynamic VID transition for VDD and VDDA. Refer to related sections for detail. |



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## Functional Pin Description

| Pin No. | Name | Pin Function |
|---|---|---|
| 14 | IMON | **Output Current Monitor for VDD.** The output current of this pin is proportional to the VDD total load current. Connect a resistor network with NTC thermistor from this pin to REFOUT. The voltage across IMON and REFOUT is proportional to the total load current. This voltage is used for load line, total output over current protection and output current telemetry. Do not connect any capacitor to this pin. |
| 15 | REFOUT | **Reference Voltage Output.** This pin outputs 1.2V as the reference voltage for IMON and IMONA. Connect a capacitor from this pin to GND. Use a 0.1uF~0.47uF MLCC as $C_{REFOUT}$, and place it close to this pin. |
| 16 | IMONA | **Output Current Monitor for VDDA.** The output current of this pin is proportional to the VDDA total load current. Connect a resistor network with NTC thermistor from this pin to REFOUT. The voltage across IMONA and REFOUT is proportional to the total load current. This voltage is used for load line, total output over current protection and output current telemetry. Do not connect any capacitor to this pin. |
| 17 | VCC | **Supply Input for Logic Control Circuit.** Connect this pin to a 5V voltage source via an RC filter. VCC is the supply input for the logic control circuit. |
| 18 | PWROK | **System Power OK Input.** This pin receives the power good signal from system. Logic high input to this pin indicates that all voltage planes and free-running clocks are within specification. When PWROK deasserts (logic low) while EN=high, both VDD and VDDA ramps to their Vboot voltage. |
| 19 | SVC | **Serial VID Clock.** SVC is a push-pull output of the processor. |
| 20 | SVD | **Serial VID Data.** SVD is a push-pull with high-Z output of the processor. SVD can be driven by the voltage regulator during the acknowledgement phase. |
| 21 | SVT | **Serial VID Telemetry.** SVT is a push-pull output of the controller. |
| 22 | VDDIO | **Reference Voltage for Processor I/O Signal.** Connect a capacitor from this pin to GND. VDDIO serves as the reference for the miscellaneous processor I/O signals including PWROK, SVD, SVC, and SVT. VDDIO is used to power and reference the SVI2 related pins. |
| 23 | TSENA | **Thermal Sense Input for VDDA.** This pin is a multi-functional pin, and it provides three functions as below.<br>1. Temperature sense input of VRHOT# indicator for VDDA regulator. Connect a resistor voltage divider with a specified negative temperature coefficient (NTC) thermistor network from REFOUT pin to GND for VDDA voltage regulator temperature sense.<br>2. VDDA output voltage offset setting. Connect a resistor divider network to set the VDDA output voltage offset. The VDDA output voltage is the sum of VID value and the voltage offset. Refer to Output Voltage Offset section for detail.<br>3. Provide switching frequency compensation with load with TSEN pin for VDD and VDDA. Refer to Switching Frequency Compensation section for detail. |
| 24 | CSNA | **Negative Differential Current Sense Input for VDDA.** When VDDA regulator is not used, pull high this pin to 5V through a 1kΩ resistor to disable the VDDA regulator. |
| 25 | CSPA | **Positive Differential Current Sense Input for VDDA.** When VDDA regulator is not used, short this pin to GND to disable the VDDA regulator. |
| 26 | FBA | **Inverting Input of the Error Amplifier for VDDA.** |



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## Functional Pin Description

| Pin No. | Name | Pin Function |
|---|---|---|
| 27 | COMPA | **Output of Control Loop Error Amplifier for VDDA.** Connect a resistor in series with a capacitor from this pin to GND for voltage control loop compensation. |
| 28 | VINSEN | **Power Stage Input Voltage Sense.** Directly connect this pin to the power stage input VIN. The controller senses the voltage on this pin for power stage input voltage VIN detection. The VINSEN voltage is also used for PWM on-time calculation. |
| 29 | EN | **Chip Enable Control Input.** Pull this pin above 2V to enable the chip. Pull this pin below 0.8V to disable the chip. There is an internal 200kΩ pull-down resistor connected to the EN pin to prevent inadvertently enable event. |
| 30 | BOOTA | **Bootstrap Supply of Upper Gate Driver for VDDA.** This pin is the supply input for the upper MOSFET gate driver. Connect the bootstrap capacitor $C_{BOOT}$ between BOOTA pin and PHA pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Use at least 0.1uF MLCC as $C_{BOOT}$ , and make sure it is placed close to the controller. |
| 31 | UGA | **Upper Gate Driver Output for VDDA.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when to turn on/off upper MOSFET. |
| 32 | PHA | **Switch Node for VDDA.** Connect this pin to the joint of upper MOSFET source, inductor and lower MOSFET drain. This pin is used as the return ground for upper MOSFET floating drive. Voltage on this pin is monitored by the shoot-through protection circuitry to determine when to turn on the lower MOSFET. |
| 33 | LGA | This pin is a multi-functional pin. It is the lower gate driver output for VDDA and also used to set the VDDA droop (load line) function.<br>**Lower Gate Driver Output for VDDA.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when to turn on the upper MOSFET.<br>**VDDA Droop (Load Line) Setting.** Connect a resistor from this pin to GND to set the droop (load line) function for VDDA regulator. The resistor value should be within 15kΩ to 65kΩ. To keep function work normally, it is recommended that the total capacitance from LGA to GND be lower than 6nF. |
| 34 | PVCC | **Supply Input for Embedded MOSFET Driver.** Connect this pin to 5V voltage source, and bypass this pin to GND with at least 1.0uF MLCC placed very close to PVCC pin. PVCC must share the same 5V power source with VCC. |
| 35 | LG1 | This pin is a multi-functional pin. It is the lower gate driver output for VDD phase 1 and also used to set the VDD droop (load line) function.<br>**Lower Gate Driver Output for VDD Phase 1.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when to turn on the upper MOSFET.<br>**VDD Droop (Load Line) Setting.** Connect a resistor from this pin to GND to set the droop (load line) function for VDD regulator. The resistor value should be within 15kΩ to 65kΩ. To keep function working normally, it is recommended that the total capacitance from LG1 to GND be lower than 6nF. |



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## Functional Pin Description

| Pin No. | Name | Pin Function |
|---|---|---|
| 36 | PH1 | **Switch Node for VDD Phase 1.** Connect this pin to the joint of upper MOSFET source, inductor and lower MOSFET drain. This pin is used as the return ground for upper MOSFET floating drive. Voltage on this pin is monitored by the shoot-through protection circuitry to determine when to turn on the lower MOSFET. |
| 37 | UG1 | **Upper Gate Driver Output for Phase 1.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when to turn on/off upper MOSFET. |
| 38 | BOOT1 | **Bootstrap Supply of Upper Gate Driver for Phase 1.** This pin is the supply input for the upper MOSFET gate driver. Connect the bootstrap capacitor $C_{BOOT}$ between BOOT1 pin and PH1 pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Use at least 0.1uF MLCC as $C_{BOOT}$, and make sure it is placed close to the controller. |
| 39 | LG2 | This pin is a multi-functional pin. It is lower gate driver for VDD phase 2 and also used to set the VDD and VDDA DVID boost function.<br>**Lower Gate Driver Output for VDD Phase 2.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when to turn on the upper MOSFET.<br>**VDD and VDDA DVID Boost Function.** Connect a resistor from this pin to GND to set the VDD and VDDA DVID boost function.The resistor value should be within 15kΩ to 65kΩ. To keep function work normally, it is recommended that the total capacitance from LG2 to GND be lower than 6nF. |
| 40 | PH2 | **Switch Node for VDD Phase 2.** Connect this pin to the joint of upper MOSFET source, inductor and lower MOSFET drain. This pin is used as the return ground for upper MOSFET floating drive. Voltage on this pin is monitored by the shoot-through protection circuitry to determine when to turn on the lower MOSFET. |
| Exposed Pad | | **Ground.** The exposed pad is the ground of embedded MOSFET drivers and logic control circuits, and it must be soldered to a large PCB and connected to GND. |



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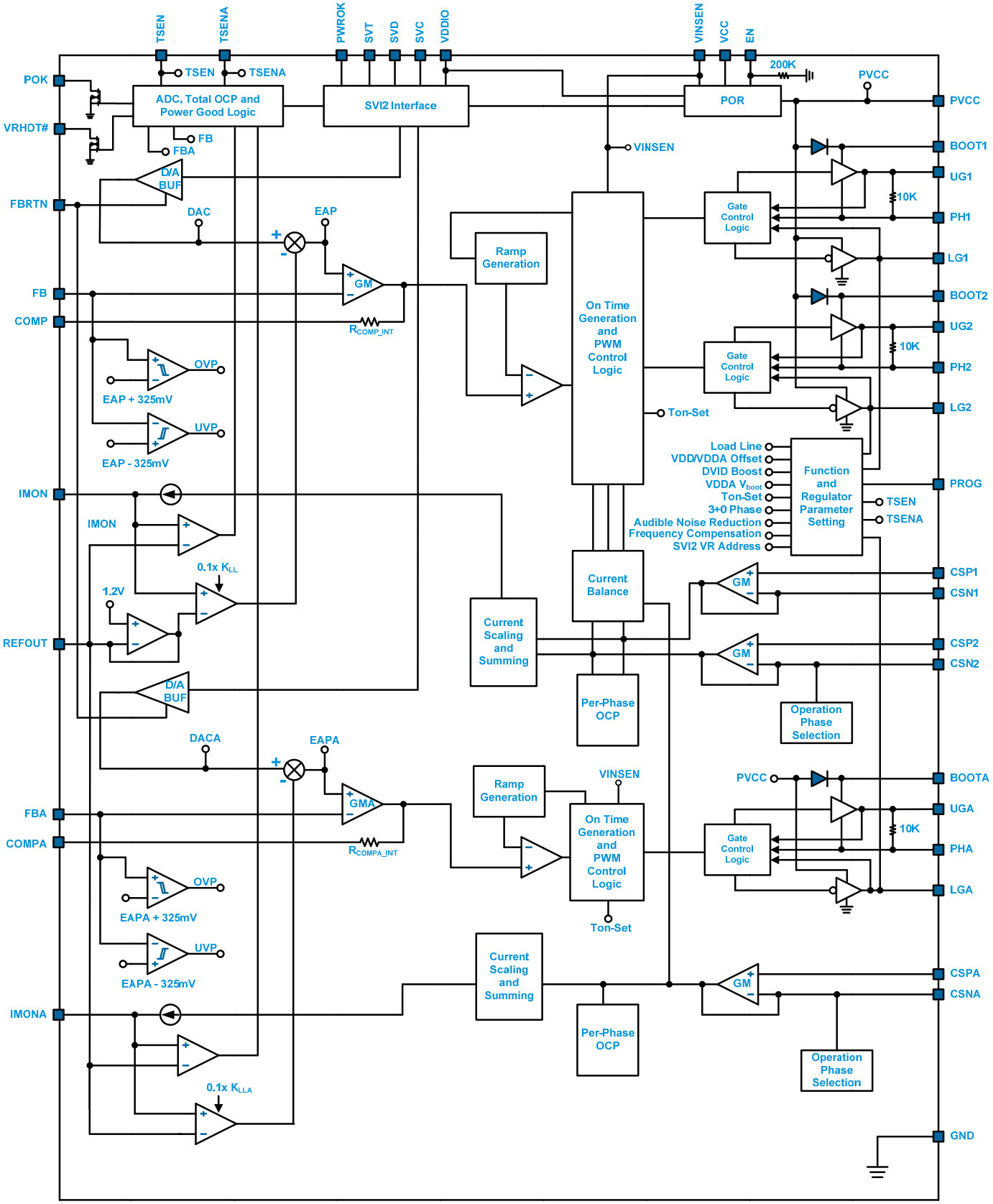
# uP9531P

## Functional Block Diagram



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## Functional Description

**Power Input and Power On Reset**

The uP9531P has two power inputs, VCC and PVCC. VCC pin is the 5V supply input for control logic circuit of the controller. RC filter to VCC is required for locally bypassing this supply input. PVCC pin is the 5V supply power of three integrated MOSFET gate drivers, RC filter to PVCC pin is not required. In addition, VINSEN pin is the power stage input voltage sense input. The controller monitors the VINSEN input voltage for PWM on-time calculation and VIN detection. VDDIO pin serves as the reference for PWROK, SVD, SVC, and SVT pins. VDDIO input voltage is monitored for power on reset. EN pin is the chip enable input. Logic high input to this pin enables the controller, and logic low input to this pin disables the controller. The five inputs above (VCC, PVCC, VINSEN, VDDIO and EN) are monitored to determine whether the controller is ready for operation.

Figure 1 shows the power ready detection circuit. The VCC voltage is monitored for power on reset with typically 4.3V threshold at its rising edge. The VINSEN voltage is monitored for power on reset with typically 5.3V threshold at its rising edge. VDDIO input voltage is monitored for power on reset with typically 0.8V threshold at its rising edge. When VCC, PVCC, VINSEN and VDDIO are all ready, the controller waits for EN to start up. When EN pin is driven above 2V, the controller begins its start up sequence. When EN pin is driven below 0.8V, the controller is turned off, and it clears all fault states to prepare to next start up once the controller is re-enabled. Anytime any one of the five inputs falls below their power on reset level will shutdown the controller. However, VINSEN and VDDIO POR does not clear any fault state. Note that **only VCC or EN toggle clears all fault states.** For example, if the controller shuts down due to the over current protection tripping of VDD regulator, it is not expected to re-start up by toggling PVCC, VINSEN or VDDIO.

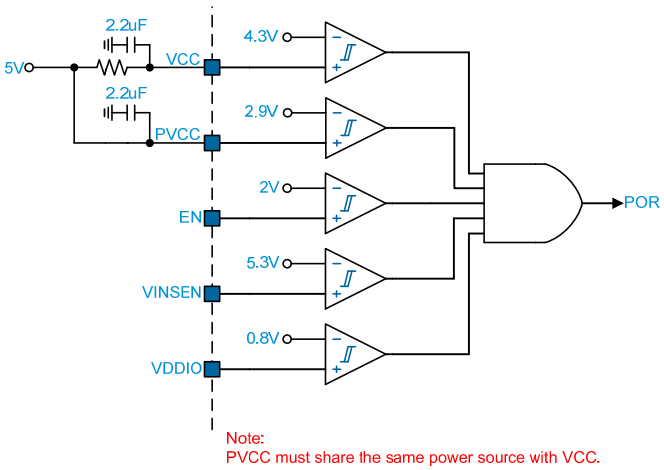


Figure 1. Circuit of Power Ready Detection

**Power Up Sequence**

Figure 2 shows a typical power-up sequence of uP9531P. When VCC, PVCC, VINSEN and VDDIO inputs are all ready, the controller waits for the EN signal to initiate the power on sequence. After EN goes high ( > 2.0V), the controller waits for a delay time $T_A$ ( about 2.4ms), then the VDD and VDDA output voltage starts to ramp up to their Vboot. The time interval $T_B$ is determined by the VID upward slew rate. For example, if VID ramps from 0V to 1.2V, with slew rate 12mV/us, then $T_B$ =100us. The controller asserts POK when both VDD and VDDA rails are in regulation of the Vboot voltage at the end of ramp up operation.



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## Functional Description

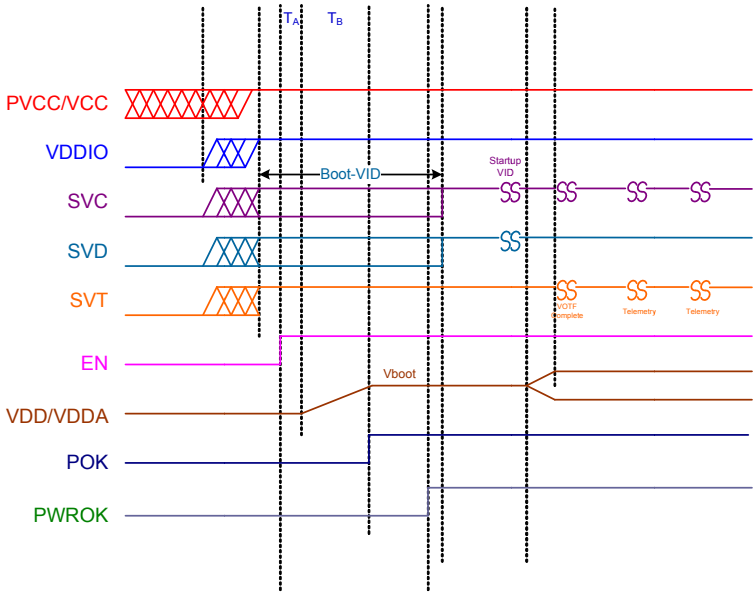


Figure 2. Power-Up Sequence Timing

**Operation Phase Number Setting**

The uP9531P supports operation phase disable function to increase the design flexibility of application. Platform power designer can choose to disable some phases by hardware pin strap setting to meet their design requirement. The VDD regulator supports 2/1-phase configuration, and the VDDA regulator supports 1/0-phase configuration. The minimum operation phase number of VDD and VDDA is 1 and 0, respectively. Therefore the minimum operation phase configuration is 1+0 phase, where 0 denotes the VDDA regulator is disabled. In general, to disable a specific phase, pull up CSNx to VCC through a 1kΩ resistor and tie CSPx to ground for that phase. The controller detects all the CSNx and CSPx input voltage at VCC and EN power on reset to determine the operation phase number. Table 1 shows the operation phase number setting.

Table 1. Operation Phase Number Setting

| Configuration | Supported Operation Phase Number | Pin Connection, Pull High / Pull Low to Target | | | | | |
|---|---|---|---|---|---|---|---|
| | | CSP1 | CSN1 | CSP2 | CSN2 | CSPA | CSNA |
| 2+1 Phase | 2+1 | -- | -- | -- | -- | -- | -- |
| | 2+0 | -- | -- | -- | -- | GND | VCC |
| | 1+1 | -- | -- | GND | VCC | -- | -- |
| | 1+0 | -- | -- | GND | VCC | GND | VCC |
| 3+0 Phase | 3+0 | -- | -- | -- | -- | -- | -- |
| | 2+0 | -- | -- | -- | -- | GND | VCC |
| | 1+0 | -- | -- | GND | VCC | GND | VCC |

Note 1. " -- " denotes normal connection.
Note 2. Use 1kΩ pull up resistor when pull up to VCC.
Note 3. Strictly follow the table for phase disable. Incorrect pin pull-up/down connection will cause catastrophic fault.
Note 4. For 3+0 phase application, IMONA should be connected to R=1kΩ to pull up to 5V.



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## Functional Description

**Operating Phase Number**

On the basis of the maximum operation number determined by hardware pin strap setting described in the above section, the operating phase number is further governed by the SVI2 command from processor. The SVI2 command and operating phase number are shown in Table 2, in which CCM denotes continuous conduction mode, and PSM denotes pulse skipping mode or diode emulation mode.

Table 2. SVI2 Command and Regulator Operating Phase Number

| PSI0_L bit | PSI1_L bit | VDD Regulator Operating Phase Number and Mode | VDDA Regulator Operating Phase Number and Mode |
|---|---|---|---|
| 1 | 1 | Full Phase CCM | 1-Phase CCM |
| 1 | 0 | Full Phase CCM | 1-Phase CCM |
| 0 | 1 | 1-Phase CCM | 1-Phase CCM |
| 0 | 0 | 1 Phase PSM | 1-Phase PSM |

**Voltage Regulator Parameter Setting**

The controller has dual outputs. They are VDD regulator and VDDA regulator. For each regulator, the controller provides several parameters or function settings, such as initial boot up voltage (Vboot), dynamic VID transition boost, DC load line, output voltage offset, PWM on time, SVI2 voltage regulator address selection, 3+0 phase application support and audible noise reduction. These parameters and function settings are determined by different pins, and they are detailed in the following sections.

**Standard Initial Boot Up Voltage (Vboot)**

The initial boot up voltage (Vboot) is determined upon the logic input to SVC and SVD pins during VCC and EN POR. Table 3 shows the standard Vboot voltage for VDD and VDDA output. Upon receiving EN=high (after about 2.4ms delay time), the VDD and VDDA output starts to ramp up to their Vboot voltage.

Table 3. Standard Vboot Voltage for Both VDD and VDDA

| SVC | SVD | Vboot |
|---|---|---|
| 0 | 0 | 1.1V |
| 0 | 1 | 1.0V |
| 1 | 0 | 0.9V |
| 1 | 1 | 0.8V |

**Extended VDDA Initial Boot Up Voltage (Set by PROG Pin)**

In addition to the standard Vboot voltage, the uP9531P features selectable initial start up voltage specifically for the VDDA output. This function is set by the PROG pin. Figure 3 shows the connection of this pin. As shown in Table 4, user can select 1.5V, 1.35V, 1.2V, or follow the SVI2 standard setting. This feature is utilized to extend the application range of the VDDA regulator, such as for DDR memory power, which requires Vboot higher than the SVI2 standard setting. Note that this feature is applicable only for VDDA regulator, the VDD regulator always follows the standard Vboot setting. When the Vboot of VDDA regulator is different from that of VDD regulator, the controller waits for both VDD and VDDA regulator output voltage settling to their target voltage then asserts POK. For example, VDD Vboot=0.9V, VDDA Vboot=1.35V, after enable, the VDD output voltage reaches 0.9V earlier than VDDA reaches 1.35V, the controller asserts POK when VDDA reaches 1.35V since there is only single POK output.



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## Functional Description

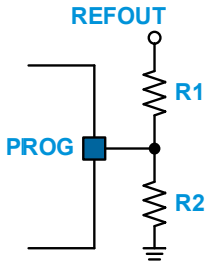


Figure 3 PROG Connection

Table 4. PROG Function and Resistor Setting

| R1 and R2 Resistor Value (kΩ) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **VDDA Regulator VBoot Voltage** | **PWM On Time (VDD and VDDA)** | For 400kHz | | For 300kHz | | For 300kHz | | For 300kHz | | For 400kHz | |
| | Configuration SVI2 VR Address | 2+1 VDD=0, VDDA=1 | | 2+1 VDD=0, VDDA=1 | | 1+2 VDD=1,VDDA=0 (SVI2 VR Address Swap) | | 3+0 VDD=0 VDDA=1 | | 3+0 VDD=0 VDDA=1 | |
| | Audible Noise Reduction | R1 | R2 | R1 | R2 | R1 | R2 | R1 | R2 | R1 | R2 |
| 1.50V | Disable | 4.92 | 3.37 | 24.61 | 16.84 | 44.3 | 30.32 | 73.84 | 50.53 | 147.67 | 101.06 |
| 1.35V | | 4.27 | 3.77 | 21.33 | 18.83 | 38.4 | 33.89 | 63.99 | 56.48 | 127.99 | 112.95 |
| 1.20V | | 3.76 | 4.27 | 18.82 | 21.34 | 33.88 | 38.4 | 56.47 | 64.01 | 112.93 | 128.01 |
| Follow SVI2 Standard Setting | | 3.37 | 4.92 | 16.84 | 24.62 | 30.31 | 44.31 | 50.52 | 73.86 | 101.04 | 147.71 |
| 1.50V | Enable | 3.05 | 5.82 | 15.24 | 29.1 | 27.43 | 52.37 | 45.71 | 87.29 | 91.42 | 174.57 |
| 1.35V | | 2.78 | 7.11 | 13.91 | 35.56 | 25.04 | 64.01 | 41.74 | 106.69 | 83.47 | 213.37 |
| 1.20V | | 2.56 | 9.14 | 12.8 | 45.72 | 23.04 | 82.3 | 38.4 | 137.17 | 76.8 | 274.35 |
| Follow SVI2 Standard Setting | | 2.37 | 12.8 | 11.85 | 64.02 | 21.33 | 115.24 | 35.55 | 192.06 | 71.11 | 384.12 |

Note 1: The tolerance of the resistance listed in this table is ±3%. It is recommended to choose the resistor with ±1%. tolerance for setting. For example, choose 3.32k for R1 (error=(3.32-3.37)/3.37= -1.48%, within ±3%.), and choose 4.99k for R2 (error=(4.99-4.92)/4.92=1.42%, within ±3%.)

Note 2: For 3+0 phase application, IMONA should be connected to R=1kΩ pull up to 5V.



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## Functional Description

**PWM On Time (Set by PROG Pin)**

The PWM on time of VDD regulator and VDDA regulator is determined by the PROG pin setting. Refer to Table 4, the controller provides two PWM on time (for 300kHz or for 400kHz) settings to choose from. Note that both the VDD regulator and VDDA regulator share the same PWM on time setting.

**SVI2 VR Address Selection (Set by PROG Pin)**

The standard SVI2 voltage regulator address for VDD regulator and VDDA regulator is 0 and 1, respectively. Therefore the configuration is 2+1 phase. To further extend the application flexibility, the uP9531P features SVI2 voltage regulator address selection, which is set by the PROG pin. Refer to Table 4, user can choose to swap the regulator address to let the controller operate in 1+2 phase configuration, namely the address for VDD regulator and VDDA regulator is 1 and 0, respectively. This feature is utilized to further extend the application range, specifically for the case that the current demand for regulator address=1 is greater than that of regulator address=0.

**3+0 Phase Application (Set by PROG Pin)**

The standard configuration of the controller is 2+1 phase application. To widen the application range, the controller supports 3+0 phase application, in which only single output is required and the output current demand requires 3-phase operation to fulfill. In this scenario, the only working regulator is VDD, which has three phases and its SVI2 VR address=0. VDDA regulator is disabled, and any SVI2 command sent to regulator address 1 is not acknowledged since the VDDA regulator is disabled. Refer to Table 4 for 3+0 phase application setting. For 3+0 phase application, IMONA should be connected to R=1kΩ pull up to 5V.

**Dynamic VID Change and Slew Rate**

The controller receives VID command via the SVI2 interface to change the regulator output voltage dynamically while the regulator is running and supplying current to the load. This is commonly referred to as the VID on-the-fly (VID OTF). A VID OTF event may occur under either light or heavy load condition. Depends on the VID command, the voltage change direction can be upward or downward. The value of VID upward transition slew rate is 12mV/us in CCM, and the value of VID downward transition slew rate is by default 1/3 of VID upward slew rate in CCM.

**Audible Noise Reduction (Set by PROG Pin)**

For the purpose of energy saving, microprocessor tends to let the supply voltage decrease to several hundreds of mV or 0V if the workload is low, and increase the supply voltage to normally above 1V at high workload. In other words, the processor frequently enters/exits different sleeping states with large step supply voltage change. The frequently large step increase/decrease in regulator output voltage denotes the output capacitor of the regulator is frequently charged/discharged. This operation sometimes causes audible noise. One of the solutions to reduce the audible noise caused by the dynamic VID transition is to reduce the voltage change step. The controller provides an effective way to implement the audible noise reduction function, which is to decrease the slew rate only for downward dynamic VID transition. Refer to Table 4 for setting to enable this function.

The standard slew rate of downward VID transition of the controller is 4mV/us (1/3 of 12mV/us). When the audible noise reduction function is enabled, the slew rate is reduced to typical 0.18mV/us. Although this function helps reduce the audible noise, the price to be paid is the power dissipation of processor. It is usually a trade-off for the platform power designer.



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## Functional Description

**Dynamic VID Transition Boost (Set by LG2 Pin)**

The voltage regulator to supply power for micro processor usually requires droop (namely load line, or active voltage positioning) function. In a positive VID transition event, the output current increases during the transition to charge the output capacitor such that the output voltage ramps up to a target level. Due to the nature of load line, the output voltage is expected to be lower than the required level at the end of transition. The controller provides a function to help boost the ramping up of output voltage to meet the requirement in a positive dynamic VID transition event. This dynamic VID boost function is set by resistor strap to the LG2 pin. Table 5 shows the setting and the recommended resistance value. Both the VDD regulator and VDDA regulator share the same boost setting. To ensure correct setting, the resistance value should be within 15kΩ to 65kΩ, and it is recommended that the total capacitance from LG2 to GND be lower than 6nF. Given the total output capacitance and the upward VID transition slew rate and load line, the boost level can be calculated as a start point. Then fine tune the level per actual measurement. For example, total output capacitance is 990uF, slew rate SR is 12mV/us, load line LL=0.7mΩ, the droop voltage caused by the inrush current during upward dynamic VID transition can be expressed as: Vdroop = (Cout*SR*LL) = 8.3mV, then choose $R_{LG2}$ = 16.5kΩ (as shown in Table 5) as the baseline. Because VDD and VDDA share the same setting, it is recommended to select the regulator whose droop voltage is greater for setting. Fine-tuning is required per actual measurement to ensure that both regulators meet the requirements.

Table 5. Dynamic VID Transition Boost Setting

| DVID Boost (mV), shared by VDD and VDDA | LG2 Resistor Strap (kΩ) | DVID Boost (mV), shared by VDD and VDDA | LG2 Resistor Strap (kΩ) |
|---|---|---|---|
| 0 | 15 | 60 | 23.7 |
| 7.5 | 16.5 | 67.5 | 24.9 |
| 15 | 17.4 | 75 | 26.1 |
| 22.5 | 18.7 | 82.5 | 27 |
| 30 | 19.6 | 90 | 28 |
| 37.5 | 20.5 | 97.5 | 29.4 |
| 45 | 21.5 | 105 | 30.1 |
| 52.5 | 22.6 | 112.5 | 31.6 |

**Load Line Factor $K_{LL}$ and Load Line Setting (Set by LG1,LGA Pins)**

As shown in Figure 4, the current $I_{CSNx}$ denotes the sensed current in each phase. These currents are scaled and summed as $I_{IMON}$, which denotes the total output current, and it is fed to the IMON pin. The voltage difference between IMON and REFOUT is internally converted to generate a scaled voltage, which is subtracted from the reference voltage for load line. As total load current increases, the scaled voltage increases. This makes the output voltage decreases linearly as the total output current linearly increases, which is also known as active voltage positioning (AVP). The slope of output voltage decrease to total load current increase is referred to as load line. The load line is defined as follows.

$V_{EAP} = V_{DAC} - R_{LL} \times I_{LOAD}$

$V_{EAP}$ and $V_{DAC}$ are internal signals

Load Line = $R_{LL} = \frac{\Delta V_{DRP}}{\Delta I_{OUT}} = \frac{1}{5} \times \frac{R_{DC}}{R_{CSN}} \times R_{IMON} \times K_{LL}$



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## Functional Description

Where $R_{LL}$ is the load line, $R_{DC}$ is the DC resistance of inductor, and they are given parameters. $K_{LL}$ is the load line factor to be determined. $R_{CSN}$ is obtained by giving the per phase OCP level. The $R_{IMON}$ value is obtained through total OCP calculation, then load line factor $K_{LL}$ can be obtained as follows.

$$K_{LL} = \frac{R_{CSN}}{R_{DC}} \times 5 \times \frac{R_{LL}}{R_{IMON}}$$

For VDD regulator, the LG1 is a multi-functional pin, and a resistor $R_{LG1}$ connected from this pin to GND is used to set the $K_{LL}$ value for load line setting. During the initial setting period, a 10uA current source is turned on for a period of time to flow out of LG1 pin through $R_{LG1}$ to create voltage drop on this pin. This voltage is used to determine the $K_{LL}$ value, which is defined as below equation. Note that the resistance of $R_{LG1}$ = 65 kΩ is for $R_{LL}$ = 0. To ensure correct setting, the resistor value should be within 15kΩ to 65kΩ.

$$R_{LG}(k\Omega) = 65 \times \left(1 - \frac{128 \times K_{LL}}{248}\right)$$

Similarly, the above load line factor and load line setting calculations also apply to the VDDA regulator, where a resistor ($R_{LGA}$) strap to the LGA pin is used to set the load line for VDDA regulator.

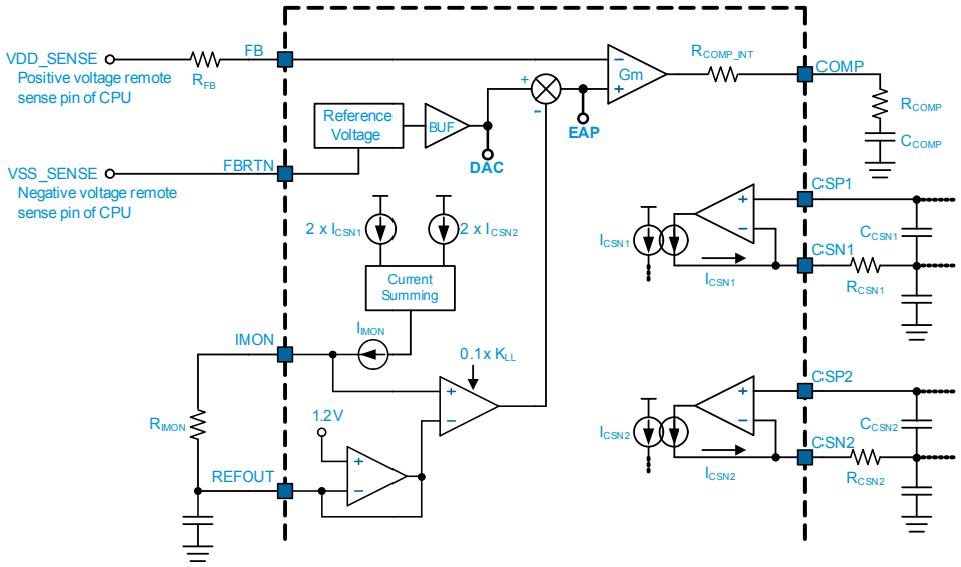


Figure 4. Load Line and Output Voltage Differential Sense

### Output Voltage Differential Sense

For VDD regulator, the controller uses differential sense by a high-gain low offset error amplifier for output voltage differential sense as shown in Figure 4. The CPU voltage is sensed by the FB and FBRTN pins for VDD regulator. FB pin is connected to the positive remote sense pin VDD_SENSE of the CPU via the resistor $R_{FB}$. FBRTN pin is connected to the negative remote sense pin VSS_SENSE of CPU directly. For VDDA regulator, the output voltage is sensed by the FBA and FBRTN pins. Because of the single VSS_SENSE pin of CPU, the VDD and VDDA regulator shares the FBRTN pin for remote output voltage sense.



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## Functional Description

**Thermal Sense, Output Voltage Offset and Switching Frequency Compensation**

The TSEN and TSENA pins are multi-functional pins, and they provide three functions for VDD regulator and VDDA regulator, respectively.

The first function is temperature sense input of VRHOT# thermal indicator for voltage regulator. Refer to Figure 5, a resistor voltage divider network with a specified negative temperature coefficient (NTC) thermistor is connected between TSEN/TSENA pin, REFOUT pin and GND. A current $I_{TSEN}$ flows out of the TSEN/TSENA pin, and the voltage at the TSEN/TSENA pin decreases as the NTC thermistor temperature increases, thus to achieve voltage regulator temperature sense.

The second function is regulator output voltage offset setting. This function is used to provide positive offset to the output voltage when needed. Connect a resistor divider network to set the regulator output voltage offset as shown in Figure 5. The regulator output voltage is the sum of VID voltage and the voltage offset.

The third function is to adjust the PWM on time to compensate the switching frequency to decrease the deviation of switching frequency over load current to improve the efficiency at heavy load. Connect a resistor divider network to set the frequency compensation factor M as shown in Figure 5 and Table 6. Both the VDD regulator and VDDA regulator share the same frequency compensation setting.

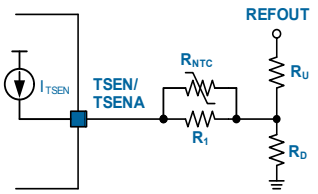


Figure 5. Resistor Network for Thermal Monitor

**Regulator Thermal Sense**

The NTC thermistor is placed close to the hottest point of the regulator, normally close to the inductor and low-side MOSFET of phase 1. The controller asserts VRHOT#, which is an open drain architecture pin and active low when the sensed temperature is higher than the threshold value. Either VDD or VDDA regulator can trigger VRHOT# as long as the temperature of any of the two regulators exceeds the maximum temperature threshold. VRHOT# is triggered when voltage at TSEN/TSENA pin reduces to 2.2V(typical). VRHOT# is an indicator to the platform for the purpose of thermal warning, and it does not impact the regulator operation. The regulator is still running when VRHOT# is triggered.

Take VDD regulator as an example, the recommended NTC thermistor is 100kΩ with β = 4485 from Murata (NCP03WL104J05RL), and thermistor network resistors $R_1$, $R_U$ and $R_D$ are determined by the equation (1) as below.

$$I_{TSEN} \times \left(\frac{R_1 \times R_{Trig}}{R_1 + R_{Trig}}\right) + I_{TSEN} \times \left(\frac{R_U \times R_D}{R_U + R_D}\right) + V_{REFOUT} \times \frac{R_D}{R_U + R_D} = 2.2 \qquad (1)$$

Where $I_{TSEN}$ = 100uA(typical), which is an internal precision current source of the the controller. $V_{REFOUT}$ = 1.2V, which is output voltage of REFOUT. $R_{Trig}$ is the NTC thermistor resistance value at the required temperature threshold. The above thermal sense mechanism and calculation equation also apply to the VDDA regulator.



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## Functional Description

**Output Voltage Offset (Set by TSEN, TSENA Pins)**

The controller provides a function to add positive voltage to the regulator output voltage. The regulator output voltage is the sum of VID voltage and the offset voltage. The offset voltage for VDD and VDDA regulator is set by TSEN and TSENA pin, respectively. The setting level is calculated according to equation (1) in previous section, and the corresponding voltage offset is shown in Table 6.

**Switching Frequency Compensation with Load (Set by TSEN and TSENA pin)**

uP9531P is a constant on time based PWM controller, the switching frequency usually increases as load current increases in order to compensate the power loss of the regulator. The increase in switching frequency at heavy load usually results in the decrease of conversion efficiency. The uP9531P provides a function to adjust the PWM on time to compensate the switching frequency to decrease the deviation of switching frequency over load current to improve the efficiency at heavy load. The frequency compensation factor is denoted by M, and this parameter has two values (M=[00], [01]=[TSEN TSENA]) to choose from, and it is determined by the two bit setting from selecting $R_U$ and $R_D$ for TSEN and TSENA pin, respectively. Refer to Table 6 for setting to select frequency compensation factor M value. Note that both the VDD regulator and VDDA regulator share the same frequency compensation setting. The reference setting value can be obtained from uPI.

Table 6. VDD/VDDA Output Voltage Offset and Frequency Compensation Factor Setting

| $V_{TSEN/TSENA}$ = % of REFOUT | VDD/VDDA Output Voltage Offset (mV) | Frequency Compensation Factor: M [TSEN:TSENA]=[1:0] | |
|---|---|---|---|
| | | TSEN | TSENA |
| 40.625 | 0 | 0 | 0 |
| 46.875 | 6.25 | | |
| 53.125 | 12.5 | | |
| 59.375 | 18.75 | | |
| 65.625 | 0 | -- | 1 |
| 71.875 | 6.25 | | |
| 78.125 | 12.5 | | |
| 84.375 | 18.75 | | |

Note:
1. M=00, 01 by selecting $R_U$ and $R_D$
2. The output voltage offset is set by selecting $R_U$ and $R_D$.

**DCR Current Sense and Per-Phase Over Current Protection**

The controller provides per-phase over current protection (OCP) function to protect the voltage regulator. The controller uses DCR current sense technique to sense the inductor current in each phase for per-phase OCP and current balance as shown in Figure 6. In this inductor current sense circuit, the time constant is expressed as follows.

$$k \times \frac{L}{R_{DC}} = R_{CSPx} \times C_{CSNx}$$

where L is the output inductor, $R_{DC}$ is its DC resistance and k is a constant.



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## Functional Description

Theoretically, if k = 1, the sensed current signal $I_{CSNx}$ is expressed as follows.

$$I_{CSNx} = \frac{I_{LX} \times R_{DC}}{R_{CSNx}}$$

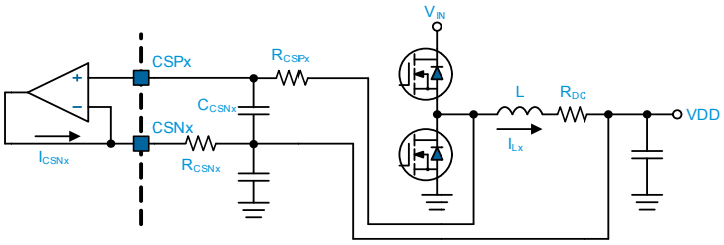


Figure 6. Inductor DCR Current Sense

Note that the resistance value of $R_{CSNx}$ must be less than 2kΩ to ensure the current sensing circuit in normal operation. The sensed current $I_{CSNx}$ represents the current in each phase, and it is compared to a 50uA current source internally for per-phase OCP. If any inductor current of the active operating phase exceeds the threshold for a specific delay time, the regulator shuts down and POK is pulled low immediately, then both UGx and LGx is held low to turn off all MOSFETs to shutdown the regulator. The per-phase OCP is a latch-off type protection, and it can only be reset by VCC or EN toggling.

When one regulator triggers per-phase OCP, after about 5us, the other unaffected regulator also shuts down with both UGx and LGx are held low. The resistance of $R_{CSNx}$ and the per-phase OCP level can be obtained using equation as follows.

$$R_{CSNx} = \frac{I_{OCP\_perphase} \times R_{DC}}{50uA}$$

The above per-phase OCP mechanism and setting calculations also apply to the VDDA regulator.

**Total Output Over Current Protection**

In addition to the per-phase OCP, the controller provides total output over current protection (TOCP). As shown in Figure 7, the current $I_{CSNx}$ denotes the sensed per-phase current, and the summed current is further internally mirrored to IMON pin as $I_{IMON}$ for total output over current protection. A resistor $R_{IMON}$ is connected from IMON pin to REFOUT pin. This $I_{IMON}$ current flows through the resistor $R_{IMON}$, creating voltage drop across it. As the total load current increases, the voltage on IMON pin ($V_{IMON}$) increases proportionally. When the IMON voltage is greater than $V_{REFOUT}$ +1.5V for a specific delay time, the total output over current protection is triggered. POK is pulled low immediately, and both UGx and LGx are held low to turn off all MOSFETs to shutdown the regulator. When one regulator triggers total output OCP, after about 5us, the other unaffected regulator also shuts down with both UGx and LGx held low. The total output OCP is a latch-off type protection, and it can only be reset by VCC or EN toggling.

Avoid adding any capacitor to the IMON pin since it brings extra delay. The output current level of triggering total output OCP is calculated as follows.

$$I_{OUT\_OCP} = \frac{1.5}{R_{IMON}} \times \frac{R_{CSNx}}{R_{DC}} \times \frac{1}{2}$$

The above total output OCP mechanism and setting calculations also apply to the VDDA regulator.



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## Functional Description

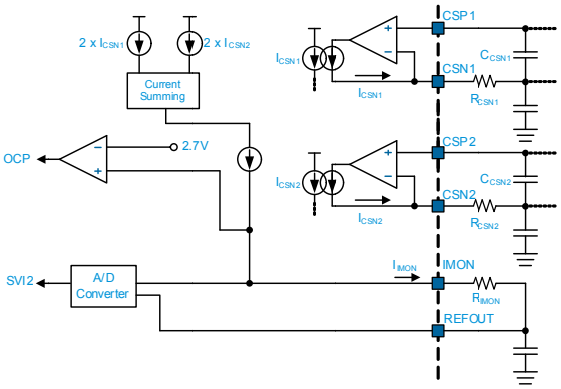


Figure 7. Phase Current Summing and Total Output OCP

**Total Output OCP Ratio and Operating Phase Number**

The total output OCP level is usually designed for the voltage regulator that is operated in full phase condition by hardware setting. The actual operating phase number is further controlled by the SVI2 command. When the operating phase number is decreased, the total output OCP level is decreased as well. The total output OCP level is changed per actual operating phase number. Table 7 shows the total output OCP ratio per actual operating phase number and the hardware configuration.

Table 7. Total Output OCP Ratio and Operating Phase Number

| Hardware Configuration | Total Ouput OCP Ratio | |
|---|---|---|
| | Full Phase | 1-Phase |
| 3-Phase* | 1 | 5/12 |
| 2-Phase | 1 | 7/12 |
| 1-Phase | 1 | 1 |
| *Note: Applicable only for 3+0 phase configuration | | |

**Output Current Telemetry**

Refer to Figure 7, the summed current is internally mirrored and fed to IMON pin as $I_{IMON}$. A resistor $R_{IMON}$ is connected between IMON and REFOUT. The current $I_{IMON}$ flows through the resistor $R_{IMON}$, creating voltage drop across it. As the total load current increases, the voltage on IMON pin ($V_{IMON}$) increases proportionally. An internal analog-to-digital converter (ADC) converts the voltage difference between IMON and REFOUT to a digital content for output current telemetry through SVI2 interface. As $V_{IMON}$ voltage increases, the output current telemetry data increases. REFOUT is used as the reference of IMON, therefore $V_{IMON}$ =1.2V means that output current telemetry data=00h. The ADC input range is typically 1.5V, which means the current telemetry data=FFh when $V_{IMON}$ = 2.7V. Further increment $V_{IMON}$ ( > 2.7V) is allowed, but the ADC results will remain at FFh. The above output current mechanism also applies to the VDDA regulator.



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## Functional Description

**Output Voltage Telemetry**

In addition to the output current telemetry, the output voltage telemetry is also transmitted via the SVI2 interface. The voltage on FB and FBA pin is converted to digital content via the ADC for output voltage telemetry of VDD and VDDA, respectively.

**Over Voltage Protection**

The controller monitors the voltage on FB pin for over voltage protection (OVP). After output voltage ramps up to Vboot, the controller initiates OVP function. Once $V_{FB}$ exceeds the OVP threshold (VID+325mV - Vdroop) for a specific delay time, OVP is triggered and POK is pulled low immediately, then UGx is held low, LGx is held high to turn off high side MOSFET and turn on low side MOSFET to protect CPU. Since the low side MOSFET is turned on, the regulator output capacitor is discharged and output voltage decreases as well. When FB pin voltage decreases to lower than typical 0.5V, LGx is held low to turn off the low side MOSFET to avoid negative output voltage. The OVP is a latch-off type protection, and it can only be reset by VCC or EN toggling. The OVP detection circuit has a fixed delay time to prevent false trigger. When one regulator triggers OVP, after about 5us, the other unaffected regulator also shuts down but with both UGx and LGx held low. Similarly, the above OVP mechanism also applies to the VDDA regulator, in which the output voltage is monitored by the FBA pin.

**Absolute Over Voltage Protection**

In addition to OVP, which threshold is the target voltage (subtracts droop voltage from VID voltage) plus the OVP threshold voltage, the controller further provides absolute over voltage protection (AOVP). The controller monitors the voltage on FB pin for AOVP, which is referred to GND. After output voltage ramps up to Vboot, the controller initiates AOVP function. Once $V_{FB}$ exceeds the AOVP threshold (1.85V) for a specific delay time, AOVP is triggered. POK is pulled low immediately. UGx is held low, LGx is held high to turn off high side MOSFET and turn on low side MOSFET to protect CPU. Since the low side MOSFET is turned on, the regulator output capacitor is discharged and output voltage decreases as well. When FB pin voltage decreases to lower than typical 0.5V, LGx is held low to turn off the low side MOSFET to avoid negative output voltage. The AOVP is a latch-off type protection, and it can only be reset by VCC or EN toggling. The AOVP detection circuit has a fixed delay time to prevent false trigger. When one regulator triggers AOVP, after about 5us , the other unaffected regulator also shuts down but with both UGx and LGx held low. Similarly, the above AOVP mechanism also applies to the VDDA regulator, in which the output voltage is monitored by the FBA pin.

**Under Voltage Protection**

The controller monitors the voltage on FB pin for under voltage protection(UVP). After output voltage ramps up to Vboot, the controller initiates UVP function. Once $V_{FB}$ is lower than the UVP threshold (VID-325mV-Vdroop) for a specific delay time, UVP is triggered and POK is pulled low immediately, then both UGx and LGx are held low to turn off all MOSFETs to shutdown the regulator. The UVP is a latch-off type protection, and it can only be reset by VCC or EN toggling. The UVP detection circuit has a fixed delay time to prevent false trigger. When one regulator triggers UVP, after about 5us, the other unaffected regulator also shuts down with both UGx and LGx held low. In a similar way, the above UVP mechanism also applies to the VDDA regulator, in which the output voltage is monitored by the FBA pin.

**Thermal Shutdown**

The uP9531P provides thermal shutdown function by monitoring the temperature of the chip. If the temperature exceeds typical 160℃, the controller shuts down. All the UGx and LGx of VDD and VDDA regulator are held low. The thermal shutdown function is a latch-off type protection, and it can only be reset by VCC or EN toggling.



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## Functional Description

Table 8. VID Table

| SVID[7:0] | Voltage(V) | SVID[7:0] | Voltage(V) | SVID[7:0] | Voltage(V) | SVID[7:0] | Voltage(V) |
|---|---|---|---|---|---|---|---|
| 0000_0000 | 1.55000 | 0010_0000 | 1.35000 | 0100_0000 | 1.15000 | 0110_0000 | 0.95000 |
| 0000_0001 | 1.54375 | 0010_0001 | 1.34375 | 0100_0001 | 1.14375 | 0110_0001 | 0.94375 |
| 0000_0010 | 1.53750 | 0010_0010 | 1.33750 | 0100_0010 | 1.13750 | 0110_0010 | 0.93750 |
| 0000_0011 | 1.53125 | 0010_0011 | 1.33125 | 0100_0011 | 1.13125 | 0110_0011 | 0.93125 |
| 0000_0100 | 1.52500 | 0010_0100 | 1.32500 | 0100_0100 | 1.12500 | 0110_0100 | 0.92500 |
| 0000_0101 | 1.51875 | 0010_0101 | 1.31875 | 0100_0101 | 1.11875 | 0110_0101 | 0.91875 |
| 0000_0110 | 1.51250 | 0010_0110 | 1.31250 | 0100_0110 | 1.11250 | 0110_0110 | 0.91250 |
| 0000_0111 | 1.50625 | 0010_0111 | 1.30625 | 0100_0111 | 1.10625 | 0110_0111 | 0.90625 |
| 0000_1000 | 1.50000 | 0010_1000 | 1.30000 | 0100_1000 | 1.10000 | 0110_1000 | 0.90000 |
| 0000_1001 | 1.49375 | 0010_1001 | 1.29375 | 0100_1001 | 1.09375 | 0110_1001 | 0.89375 |
| 0000_1010 | 1.48750 | 0010_1010 | 1.28750 | 0100_1010 | 1.08750 | 0110_1010 | 0.88750 |
| 0000_1011 | 1.48125 | 0010_1011 | 1.28125 | 0100_1011 | 1.08125 | 0110_1011 | 0.88125 |
| 0000_1100 | 1.47500 | 0010_1100 | 1.27500 | 0100_1100 | 1.07500 | 0110_1100 | 0.87500 |
| 0000_1101 | 1.46875 | 0010_1101 | 1.26875 | 0100_1101 | 1.06875 | 0110_1101 | 0.86875 |
| 0000_1110 | 1.46250 | 0010_1110 | 1.26250 | 0100_1110 | 1.06250 | 0110_1110 | 0.86250 |
| 0000_1111 | 1.45625 | 0010_1111 | 1.25625 | 0100_1111 | 1.05625 | 0110_1111 | 0.85625 |
| 0001_0000 | 1.45000 | 0011_0000 | 1.25000 | 0101_0000 | 1.05000 | 0111_0000 | 0.85000 |
| 0001_0001 | 1.44375 | 0011_0001 | 1.24375 | 0101_0001 | 1.04375 | 0111_0001 | 0.84375 |
| 0001_0010 | 1.43750 | 0011_0010 | 1.23750 | 0101_0010 | 1.03750 | 0111_0010 | 0.83750 |
| 0001_0011 | 1.43125 | 0011_0011 | 1.23125 | 0101_0011 | 1.03125 | 0111_0011 | 0.83125 |
| 0001_0100 | 1.42500 | 0011_0100 | 1.22500 | 0101_0100 | 1.02500 | 0111_0100 | 0.82500 |
| 0001_0101 | 1.41875 | 0011_0101 | 1.21875 | 0101_0101 | 1.01875 | 0111_0101 | 0.81875 |
| 0001_0110 | 1.41250 | 0011_0110 | 1.21250 | 0101_0110 | 1.01250 | 0111_0110 | 0.81250 |
| 0001_0111 | 1.40625 | 0011_0111 | 1.20625 | 0101_0111 | 1.00625 | 0111_0111 | 0.80625 |
| 0001_1000 | 1.40000 | 0011_1000 | 1.20000 | 0101_1000 | 1.00000 | 0111_1000 | 0.80000 |
| 0001_1001 | 1.39375 | 0011_1001 | 1.19375 | 0101_1001 | 0.99375 | 0111_1001 | 0.79375 |
| 0001_1010 | 1.38750 | 0011_1010 | 1.18750 | 0101_1010 | 0.98750 | 0111_1010 | 0.78750 |
| 0001_1011 | 1.38125 | 0011_1011 | 1.18125 | 0101_1011 | 0.98125 | 0111_1011 | 0.78125 |
| 0001_1100 | 1.37500 | 0011_1100 | 1.17500 | 0101_1100 | 0.97500 | 0111_1100 | 0.77500 |
| 0001_1101 | 1.36875 | 0011_1101 | 1.16875 | 0101_1101 | 0.96875 | 0111_1101 | 0.76875 |
| 0001_1110 | 1.36250 | 0011_1110 | 1.16250 | 0101_1110 | 0.96250 | 0111_1110 | 0.76250 |
| 0001_1111 | 1.35625 | 0011_1111 | 1.15625 | 0101_1111 | 0.95625 | 0111_1111 | 0.75625 |



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## Functional Description

Table 8. VID Table (Cont.)

| SVID[7:0] | Voltage(V) | SVID[7:0] | Voltage(V) | SVID[7:0] | Voltage(V) | SVID[7:0] | Voltage(V) |
|---|---|---|---|---|---|---|---|
| 1000_0000 | 0.75000 | 1010_0000 | 0.55000 | 1100_0000 | 0.35000 | 1110_0000 | 0.15000 |
| 1000_0001 | 0.74375 | 1010_0001 | 0.54375 | 1100_0001 | 0.34375 | 1110_0001 | 0.14375 |
| 1000_0010 | 0.73750 | 1010_0010 | 0.53750 | 1100_0010 | 0.33750 | 1110_0010 | 0.13750 |
| 1000_0011 | 0.73125 | 1010_0011 | 0.53125 | 1100_0011 | 0.33125 | 1110_0011 | 0.13125 |
| 1000_0100 | 0.72500 | 1010_0100 | 0.52500 | 1100_0100 | 0.32500 | 1110_0100 | 0.12500 |
| 1000_0101 | 0.71875 | 1010_0101 | 0.51875 | 1100_0101 | 0.31875 | 1110_0101 | 0.11875 |
| 1000_0110 | 0.71250 | 1010_0110 | 0.51250 | 1100_0110 | 0.31250 | 1110_0110 | 0.11250 |
| 1000_0111 | 0.70625 | 1010_0111 | 0.50625 | 1100_0111 | 0.30625 | 1110_0111 | 0.10625 |
| 1000_1000 | 0.70000 | 1010_1000 | 0.50000 | 1100_1000 | 0.30000 | 1110_1000 | 0.10000 |
| 1000_1001 | 0.69375 | 1010_1001 | 0.49375 | 1100_1001 | 0.29375 | 1110_1001 | 0.09375 |
| 1000_1010 | 0.68750 | 1010_1010 | 0.48750 | 1100_1010 | 0.28750 | 1110_1010 | 0.08750 |
| 1000_1011 | 0.68125 | 1010_1011 | 0.48125 | 1100_1011 | 0.28125 | 1110_1011 | 0.08125 |
| 1000_1100 | 0.67500 | 1010_1100 | 0.47500 | 1100_1100 | 0.27500 | 1110_1100 | 0.07500 |
| 1000_1101 | 0.66875 | 1010_1101 | 0.46875 | 1100_1101 | 0.26875 | 1110_1101 | 0.06875 |
| 1000_1110 | 0.66250 | 1010_1110 | 0.46250 | 1100_1110 | 0.26250 | 1110_1110 | 0.06250 |
| 1000_1111 | 0.65625 | 1010_1111 | 0.45625 | 1100_1111 | 0.25625 | 1110_1111 | 0.05625 |
| 1001_0000 | 0.65000 | 1011_0000 | 0.45000 | 1101_0000 | 0.25000 | 1111_0000 | 0.05000 |
| 1001_0001 | 0.64375 | 1011_0001 | 0.44375 | 1101_0001 | 0.24375 | 1111_0001 | 0.04375 |
| 1001_0010 | 0.63750 | 1011_0010 | 0.43750 | 1101_0010 | 0.23750 | 1111_0010 | 0.03750 |
| 1001_0011 | 0.63125 | 1011_0011 | 0.43125 | 1101_0011 | 0.23125 | 1111_0011 | 0.03125 |
| 1001_0100 | 0.62500 | 1011_0100 | 0.42500 | 1101_0100 | 0.22500 | 1111_0100 | 0.02500 |
| 1001_0101 | 0.61875 | 1011_0101 | 0.41875 | 1101_0101 | 0.21875 | 1111_0101 | 0.01875 |
| 1001_0110 | 0.61250 | 1011_0110 | 0.41250 | 1101_0110 | 0.21250 | 1111_0110 | 0.01250 |
| 1001_0111 | 0.60625 | 1011_0111 | 0.40625 | 1101_0111 | 0.20625 | 1111_0111 | 0.00625 |
| 1001_1000 | 0.60000 | 1011_1000 | 0.40000 | 1101_1000 | 0.20000 | 1111_1000 | OFF |
| 1001_1001 | 0.59375 | 1011_1001 | 0.39375 | 1101_1001 | 0.19375 | 1111_1001 | OFF |
| 1001_1010 | 0.58750 | 1011_1010 | 0.38750 | 1101_1010 | 0.18750 | 1111_1010 | OFF |
| 1001_1011 | 0.58125 | 1011_1011 | 0.38125 | 1101_1011 | 0.18125 | 1111_1011 | OFF |
| 1001_1100 | 0.57500 | 1011_1100 | 0.37500 | 1101_1100 | 0.17500 | 1111_1100 | OFF |
| 1001_1101 | 0.56875 | 1011_1101 | 0.36875 | 1101_1101 | 0.16875 | 1111_1101 | OFF |
| 1001_1110 | 0.56250 | 1011_1110 | 0.36250 | 1101_1110 | 0.16250 | 1111_1110 | OFF |
| 1001_1111 | 0.55625 | 1011_1111 | 0.35625 | 1101_1111 | 0.15625 | 1111_1111 | OFF |



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## Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VCC and PVCC ---------- -0.3V to +6V
VINSEN ---------- -0.3V to +30V
BOOTx to PHx
DC ---------- -0.3V to +6V
PHx to GND
DC ---------- -0.7V to +28V
< 100ns ---------- -8V to +36V
BOOTx to GND
DC ---------- -0.3V to +34V
< 100ns ---------- -5V to +42V
UGx to PHx
DC ---------- -0.3V to +6V
< 100ns ---------- -5V to +7V
LGx to GND
DC ---------- -0.3V to +6V
< 100ns ---------- -5V to +7V
Other Pins ---------- -0.3V to +6V
Storage Temperature Range ---------- -65℃ to +150℃
Junction Temperature ---------- 150℃
Lead Temperature (Soldering, 10 sec) ---------- 260℃
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV

## Thermal Information

Package Thermal Resistance (Note 3)
WQFN5x5-40L $\theta_{JA}$ ---------- 36℃/W
WQFN5x5-40L $\theta_{JC}$ ---------- 3℃/W
Power Dissipation, $P_D$ @ $T_A$ = 25℃
WQFN5x5-40L ---------- 2.78W

## Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40℃ to +125℃
Operating Ambient Temperature Range ---------- -40℃ to +85℃
Supply Input Voltage, VCC and PVCC ---------- 4.5V to 5.5V
Power Stage Input Voltage, $V_{IN}$ ---------- 6V to 26V

**Note 1.** Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

**Note 2.** Devices are ESD sensitive. Handling precaution recommended.

**Note 3.** $\theta_{JA}$ is measured in the natural convection at $T_A$ = 25℃ on a high effective thermal conductivity test board of *JEDEC 51-7* thermal measurement standard.

**Note 4.** The device is not guaranteed to function outside its operating conditions.



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## Electrical Characteristics

(VCC = PVCC = 5V, $T_A$ = 25℃, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Supply Input** | | | | | | |
| VCC POR High Threshold | $PORH_{VCC}$ | VCC rising | 4.1 | 4.3 | 4.5 | V |
| VCC POR Hysteresis | $HYS_{VCC}$ | | -- | 0.3 | -- | V |
| VCC Supply Current | $I_{VCC}$ | EN = 5V, VDD and VDDA, no switching | -- | 7 | -- | mA |
| VCC Shutdown Current | $I_{VCC\_SHDN}$ | EN = 0V | -- | 5 | -- | uA |
| PVCC POR High Threshold | $PORH_{PVCC}$ | VCC rising | 2.7 | 2.9 | 3.1 | V |
| PVCC POR Hysteresis | $HYS_{PVCC}$ | | -- | 0.2 | -- | V |
| PVCC Supply Current | $I_{PVCC}$ | EN = 5V, VDD and VDDA, no switching | -- | 40 | -- | uA |
| PVCC Shutdown Current | $I_{PCCC\_SHDN}$ | EN = 0V | -- | 5 | -- | uA |
| **VIN Sense** | | | | | | |
| VINSEN POR High Threshold | $PORH_{VINSEN}$ | VINSEN rising | -- | 5.25 | -- | V |
| VINSEN POR Hysteresis | $HYS_{VINSEN}$ | | -- | 0.75 | -- | V |
| VINSEN Input Current | $I_{VINSEN}$ | VINSEN = 12V | -- | 30 | -- | uA |
| **EN Input** | | | | | | |
| Input Low | $V_{IL}$ | | -- | -- | 0.8 | V |
| Input High | $V_{IH}$ | | 2 | -- | -- | V |
| Pull-Low Resistance | $R_{EN\_PL}$ | | -- | 200 | -- | kΩ |
| **VDDIO Input** | | | | | | |
| VDDIO POR High Threshold | $PORH_{VDDIO\_r}$ | VDDIO rising | -- | 0.8 | -- | V |
| VDDIO POR Low Threshold | $PORL_{VDDIO\_f}$ | VDDIO falling | -- | 0.45 | -- | V |
| Input Current | $I_{VDDIO}$ | VDDIO = 1.5V | -- | 100 | -- | uA |
| **Reference Output** | | | | | | |
| REFOUT Output Voltage | $V_{REFOUT}$ | $-1mA \leq I_{REFOUT} \leq 1mA$ | -- | 1.2 | -- | V |
| **SVI2 Bus Timing Parameters (Guaranteed by Design)** | | | | | | |
| SVC Period | $T_{PERIOD}$ | | 47.6 | -- | -- | ns |
| SVC Frequency | $F_{SVC}$ | | 0.1 | -- | 21 | MHz |
| SVC High Time | $T_{HIGH}$ | | 20 | -- | -- | ns |
| SVC Low Time | $T_{LOW}$ | | 30 | -- | -- | ns |
| SVD,SVT Setup Time to SVC Rising Edge | $T_{SETUP}$ | | 5 | -- | -- | ns |
| SVD,SVT Hold Time from SVC Falling Edge | $T_{HOLD}$ | | 5 | -- | -- | ns |
| SVD,SVT Start Time to SVC Falling Edge | $T_{START}$ | | 15 | -- | -- | ns |
| SVD,SVT Stop Time from SVC Rising Edge | $T_{STOP}$ | | 5 | -- | -- | ns |



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## Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **SVI2 Bus Timing Parameters (Guaranteed by Design) cont.** | | | | | | |
| SVC,SVD,SVT Fall Time | $T_{FALL}$ | $V_{OH\_DC}$ to $V_{OL\_DC}$ | -- | -- | 1 | ns |
| SVC,SVD,SVT Rise Time | $T_{RISE}$ | $V_{OL\_DC}$ to $V_{OH\_DC}$ | -- | -- | 1 | ns |
| **SVI2** | | | | | | |
| SVC,SVD,SVT and PWROK Input Low Voltage | $V_{IL\_DC}$ | | 0 | -- | 0.35 *VDDIO | V |
| SVC,SVD,SVT and PWROK Input High Voltage | $V_{IH\_DC}$ | | 0.7 *VDDIO | -- | VDDIO | V |
| SVC,SVD,SVT and PWROK Hysteresis Voltage | $V_{HYST}$ | | 0.1 *VDDIO | -- | -- | V |
| SVC,SVD,SVT and PWROK Input Leakage Current | $I_L$ | | -100 | -- | 100 | uA |
| SVC,SVD,SVT and PWROK Input Capacitances | $C_{IN}$ | Guaranteed by design | -- | -- | 5 | pF |
| SVC,SVD,SVT Output Low Voltage | $V_{OL}$ | | 0 | -- | 0.2 | V |
| SVC,SVD,SVT Output High Voltage | $V_{OH}$ | | VDDIO -0.2 | -- | VDDIO | V |
| SVC,SVD,SVT Output Current | $I_{OH}$ | when driving $V_{OH}$ | 4 | -- | -- | mA |
| SVD,High Z Output Leakage Current | $I_{OZ}$ | | -100 | -- | 100 | uA |
| **Telemetry and ADC** | | | | | | |
| ADC Accuracy | | FB/FBA = 0.8V to 1.2V | -1 | -- | 1 | LSB |
| ADC Accuracy | | FB/FBA > 1.2V or < 0.8V | -2 | -- | 2 | LSB |
| **VID Voltage Accuracy** | | | | | | |
| VID Voltage Accuracy | VID | 0.5V < VID ≤ 0.8V | -15 | -- | 15 | mV |
| | | 0.8V < VID ≤ 1.0V | -10 | -- | 10 | mV |
| | | 1.0V < VID ≤ 1.55V | -1 | -- | 1 | % |
| **Slew Rate** | | | | | | |
| DVID Up Slew Rate | SR_UP | | 7.5 | 12 | -- | mV/us |
| DVID Down Slew Rate | SR_DOWN | Set audible noise reduction = disable | -- | 4 | -- | mV/us |
| DVID Down Slew Rate Slow | SR_DOWN_SLOW | Set audible noise reduction = enable | -- | 0.18 | -- | mV/us |
| **Error Amplifier** | | | | | | |
| Trans-Conductance | GM | | -- | 2020 | -- | uA/V |
| Gain Bandwidth Product | GBW(EA) | Guaranteed by design | -- | 10 | -- | MHz |
| **PWM On-Time Setting** | | | | | | |
| PWM On-Time | $T_{ON}$ | VINSEN = 12V, VID = 1.2V, Fsw=400kHz | -- | 250 | -- | ns |
| Minimum Off-Time | $T_{MIN\_OFF}$ | | -- | 150 | -- | ns |



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## Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Current Sense Amplifier** | | | | | | |
| Offset Voltage | $V_{OS(CSA)}$ | | -1 | -- | 1 | mV |
| CSP Input Bias Current | $I_{BC(CSA)}$ | $V_{CSPx}$ = 1.1V, guaranteed by design | -10 | -- | 10 | nA |
| Maximum Sourcing Current | $I_{MAXSRC}$ | | 100 | -- | -- | uA |
| Gain Bandwidth Product | $G_{BW(CSA)}$ | Guaranteed by design | -- | 10 | -- | MHz |
| **Output Current Monitoring IMON** | | | | | | |
| Current Mirror Accuracy | $I_{ACCU\_IMON}$ | $I_{IMON}$ to $I_{CSNx}$ ratio | 190 | 200 | 210 | % |
| Output Voltage | $V_{IMON\_00h}$ | telemetry = 00h | -- | 1.2 | -- | V |
| | $V_{IMON\_FFh}$ | telemetry = FFh | -- | 2.7 | -- | |
| **Current Monitoring for Droop** | | | | | | |
| Current Mirror Accuracy | $I_{ACCU\_DROOP}$ | Set $K_{LL}$ =1, $\Delta$Vdroop to $\Delta V_{IMON}$ ratio | 9 | 10 | 11 | % |
| **Source Current for LG Setting** | | | | | | |
| Source Current | | EN = 2V, during function setting period (LG1,LG2, LGA) | -- | 10 | -- | uA |
| **MOSFET Gate Driver** | | | | | | |
| Upper Gate Source | $R_{UG\_SRC}$ | $V_{BOOT}$ - $V_{PH}$ = 5V, source current = 80mA | -- | 0.7 | 1.3 | Ω |
| Upper Gate Sink | $R_{UG\_SNK}$ | $V_{BOOT}$ - $V_{PH}$ = 5V, sink current = 80mA | -- | 0.4 | 0.7 | Ω |
| Lower Gate Source | $R_{LG\_SRC}$ | source current = 80mA | -- | 0.7 | 1.3 | Ω |
| Lower Gate Sink | $R_{LG\_SNK}$ | sink current = 80mA | -- | 0.4 | 0.7 | Ω |
| Dead Time | $T_{DT\_UG-LG}$ | from UG < 1V to LG > 1V | -- | 20 | -- | ns |
| | $T_{DT\_LG-UG}$ | from LG < 1V to UG > 1V | -- | 20 | -- | ns |
| **Bootstrap Diode** | | | | | | |
| Forward Voltage | | Forward bias current = 3.5mA | -- | 0.33 | -- | V |
| **VRHOT#, POK** | | | | | | |
| Output Low Voltage | $V_{OL}$ | $I_{SINK}$ = 4mA | 0 | -- | 0.2 | V |
| Output Leakage Current | $I_L$ | pull up to 5V | 0 | -- | 1 | uA |



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## Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Over Current Protection** | | | | | | |
| Total Current OCP Threshold | $V_{OCP}$ | $V_{IMON}$ - $V_{REFOUT}$, full phase operation | -- | 1.5 | -- | V |
| Total Current OCP Delay | $T_{OCP}$ | | -- | 2.5 | -- | us |
| Per-Phase OCP Threshold | $I_{PEROCP}$ | Measure $I_{CSNx}$ current | -- | 50 | -- | uA |
| Per-Phase OCP Delay | $T_{PEROCP}$ | | -- | 6 | -- | us |
| **Under Voltage Protection** | | | | | | |
| UVP Threshold | $V_{UVP}$ | Load = 0A, VID - $V_{FB}$ | -- | 325 | -- | mV |
| UVP Delay Time | $T_{UVP\_DELAY}$ | | -- | 7.5 | -- | us |
| **Over Voltage Protection** | | | | | | |
| Absolute OVP Threshold | $V_{A\_OVP}$ | $V_{FB}$ to GND, $V_{FBA}$ to GND | -- | 1.85 | -- | V |
| Absolute OVP Delay Time | $T_{H\_OVP\_DELAY}$ | | -- | 1 | -- | us |
| OVP Threshold | $V_{OVP}$ | Load = 0A, $V_{FB}$ - VID | -- | 325 | -- | mV |
| OVP Delay Time | $T_{OVP\_DELAY}$ | | -- | 5 | -- | us |
| **Thermal Sense** | | | | | | |
| TSEN/TSENA Source Current | | EN = 5V | 95 | 100 | 105 | uA |
| VRHOT# Assert Threshold | | | -- | 2.2 | -- | V |
| VRHOT# De-Assert Threshold | | | -- | 2.3 | -- | V |
| **Thermal Shutdown Protection** | | | | | | |
| Thermal Shutdown Threshold | $T_{OTP}$ | Guaranteed by design | -- | 160 | -- | ℃ |



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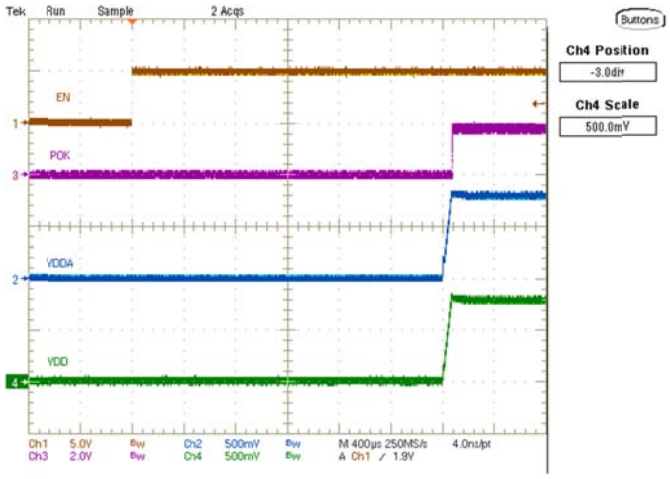
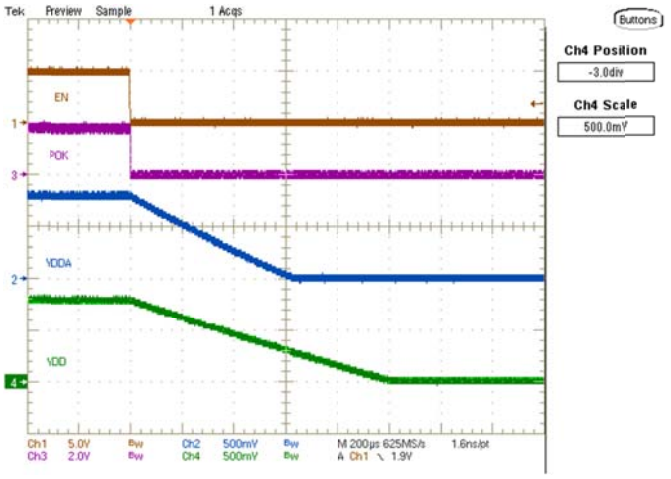
## Typical Operation Characteristics

**VDD Power On from EN**



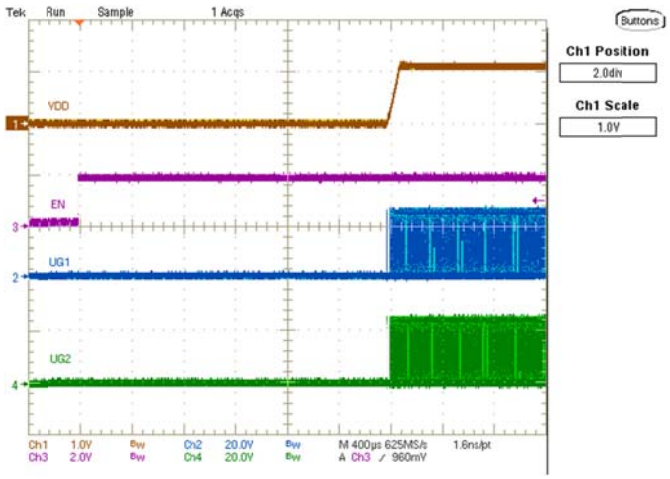

$V_{IN}$ = 19V, Full phase, $I_{OUT}$=0A

**VDD Power Off from EN**



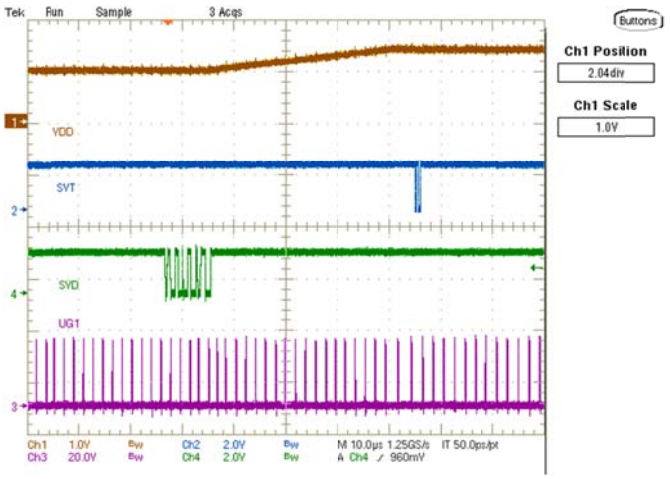

$V_{IN}$ = 19V, Full phase, $I_{OUT}$ =1A

**VDD Power On from EN**



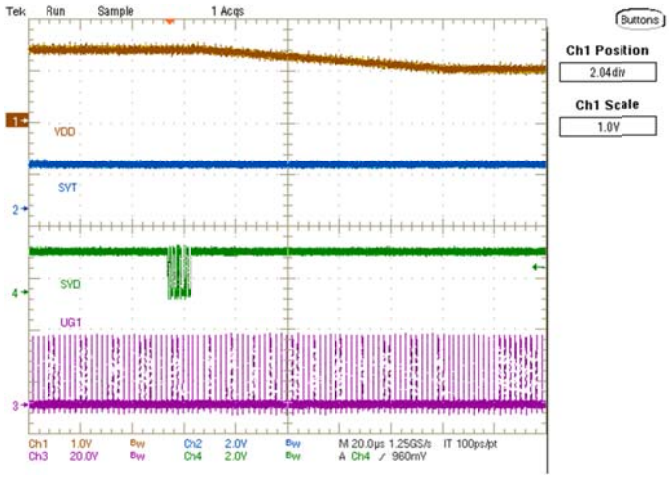

$V_{IN}$ = 19V, Full phase, $I_{OUT}$=0A

**VDD VR Dynamic VID Up**



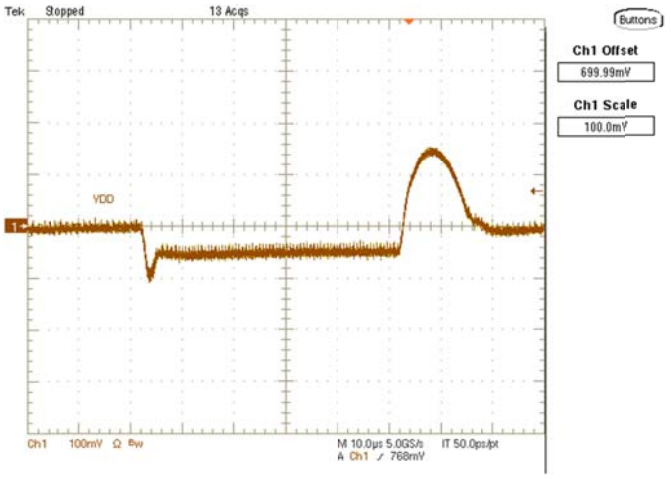

$V_{IN}$ = 19V, Full phase, VID = 1V to 1.4V, $I_{OUT}$ = 16.5A

**VDD VR Dynamic VID Down**




$V_{IN}$ = 19V, Full phase, VID = 1.4V to 1V, $I_{OUT}$ = 16.5A

**VDD VR Load Transient**




$V_{IN}$ = 19V, Full phase, VDD = 0.7V, $I_{OUT}$ = 5A ~ 70A



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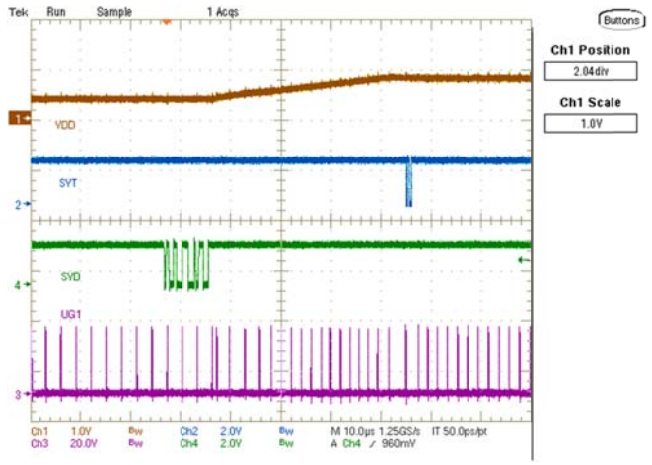
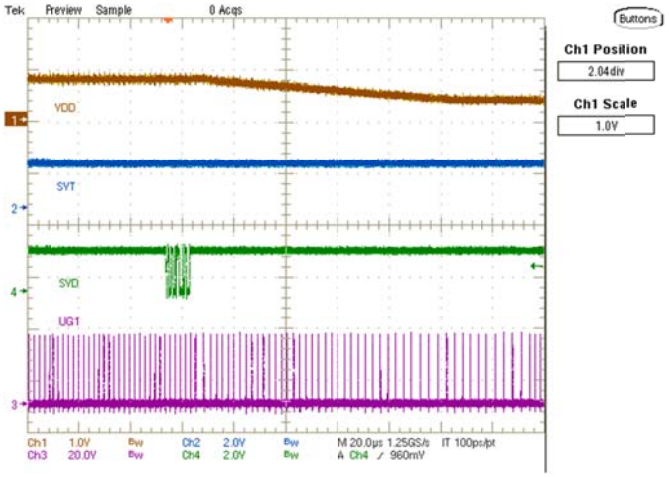
## Typical Operation Characteristics

**VDD VR Dynamic VID Up**



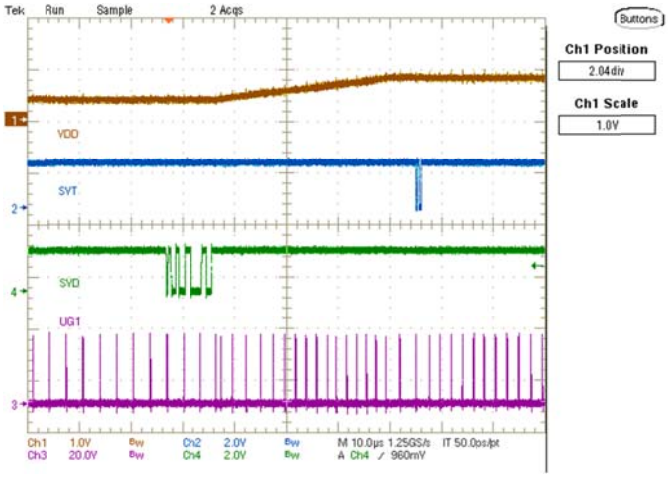

$V_{IN}$ = 19V, 1-phase CCM,VID = 0.4V to 0.8V, $I_{OUT}$ = 0A

**VDD VR Dynamic VID Down**



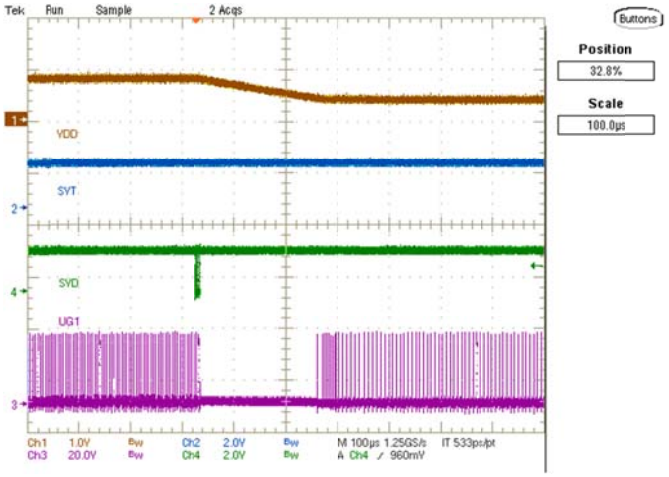

$V_{IN}$ = 19V, 1-phase CCM, VID = 0.8V to 0.4V, $I_{OUT}$ = 9A

**VDD VR Dynamic VID Up**



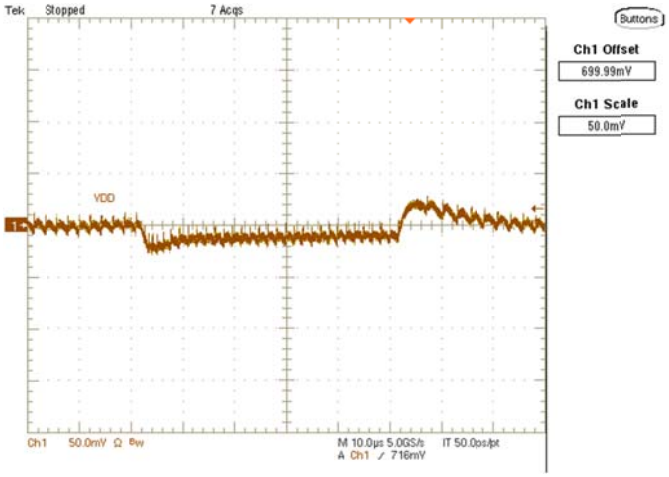

$V_{IN}$ = 19V, 1-phase DCM, VID = 0.4V to 0.8V, $I_{OUT}$ = 5A

**VDD VR Dynamic VID Down**



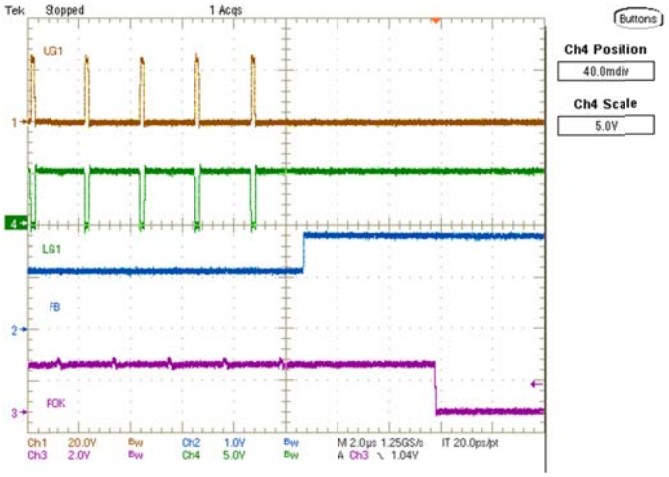

$V_{IN}$ = 19V, 1-phase DCM, VID = 0.8V to 0.4V, $I_{OUT}$ = 2A

**VDD VR Load Transient**




$V_{IN}$ = 19V, 1-phase DCM,VDD = 0.7V, $I_{OUT}$ = 4A ~ 18A

**VDD VR OVP**




$V_{IN}$ = 19V, VDD=1.1V, $I_{OUT}$=0A



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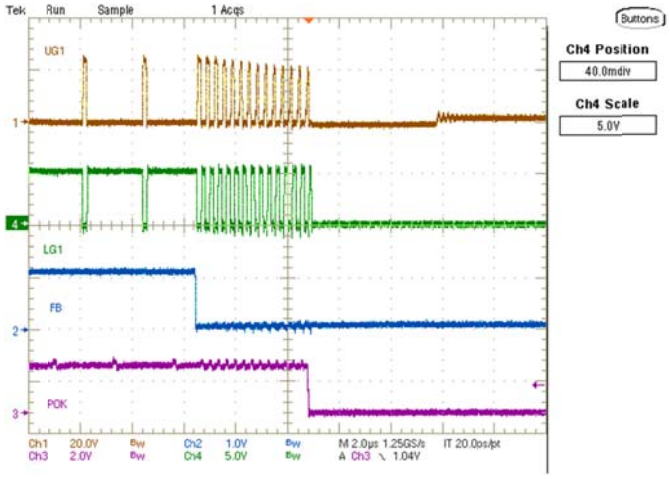
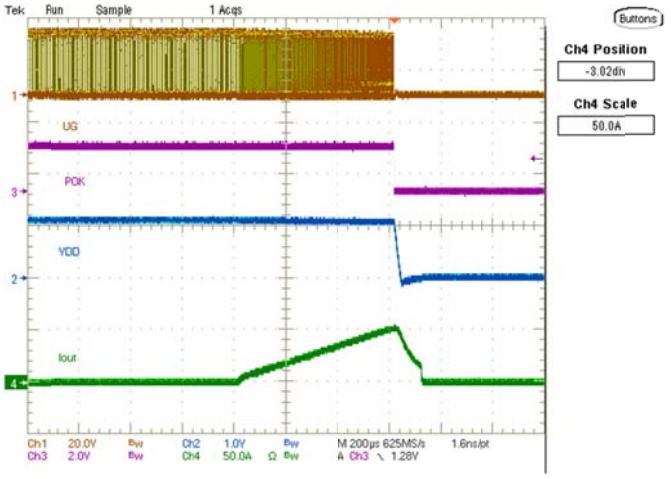
## Typical Operation Characteristics

**VDD VR UVP**



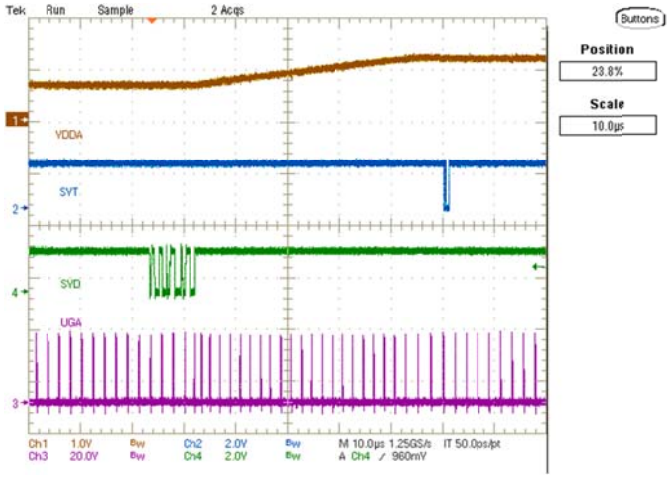

$V_{IN}$ = 19V, VDD=1.1V, $I_{OUT}$=0A

**VDD VR OCP**



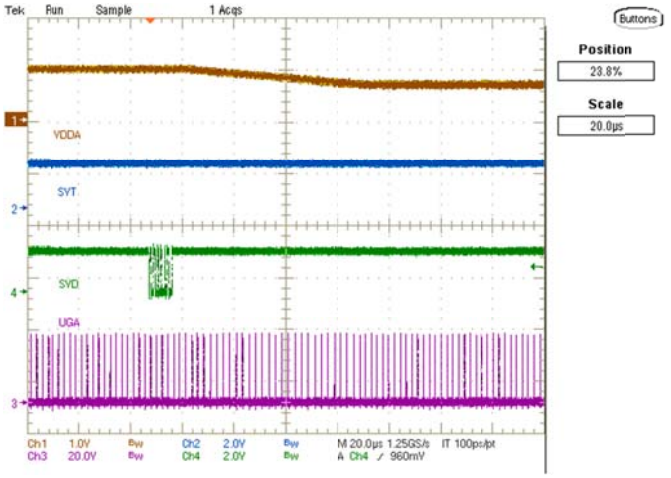

$V_{IN}$ = 19V, VDD=1.1V

**VDDA VR Dynamic VID Up**



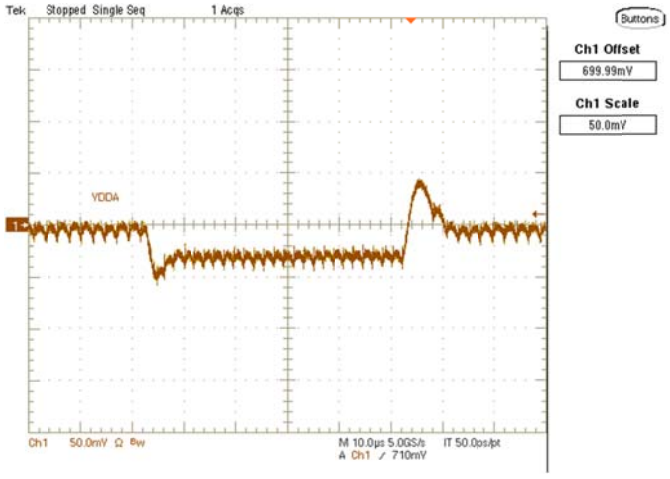

$V_{IN}$ = 19V, Full phase, VID = 0.7V to 1.2V, $I_{OUT}$ = 6.5A

**VDDA VR Dynamic VID Down**



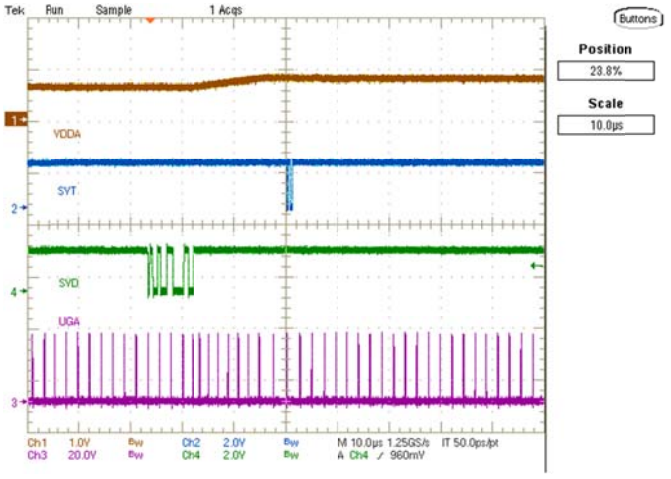

$V_{IN}$ = 19V, Full phase, VID = 1V to 0.7V, $I_{OUT}$ =5A

**VDDA VR Load Transient**




$V_{IN}$ = 19V, Full phase, VDDA = 0.7V, $I_{OUT}$ = 4A ~ 17A

**VDDA VR Dynamic VID Up**




$V_{IN}$ = 19V, 1-phase DCM, VID = 0.65V to 0.8V, $I_{OUT}$ = 5A



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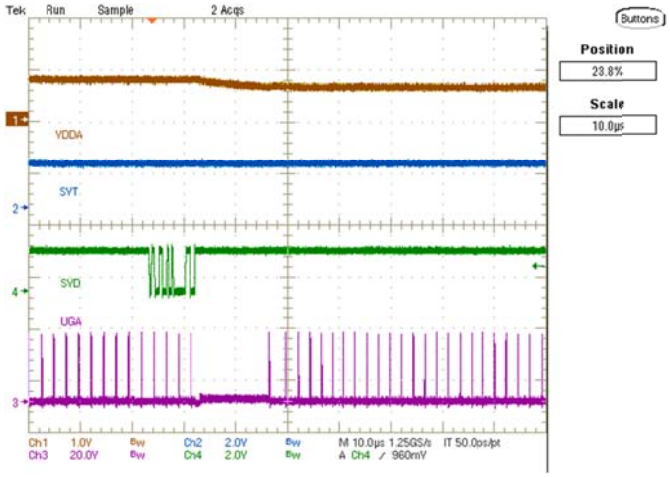
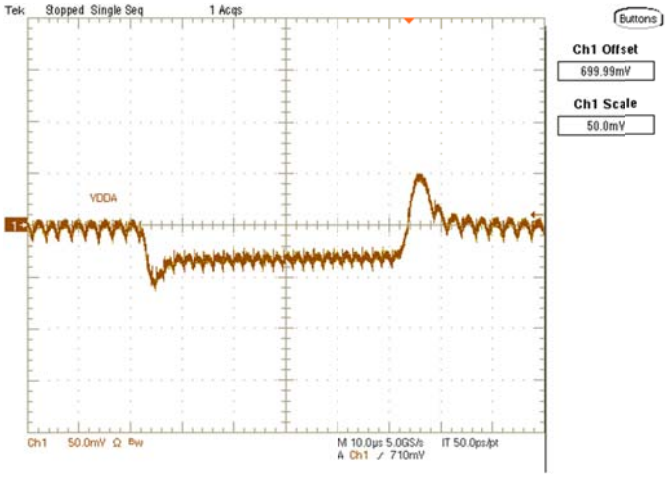
## Typical Operation Characteristics

**VDDA VR Dynamic VID Down**



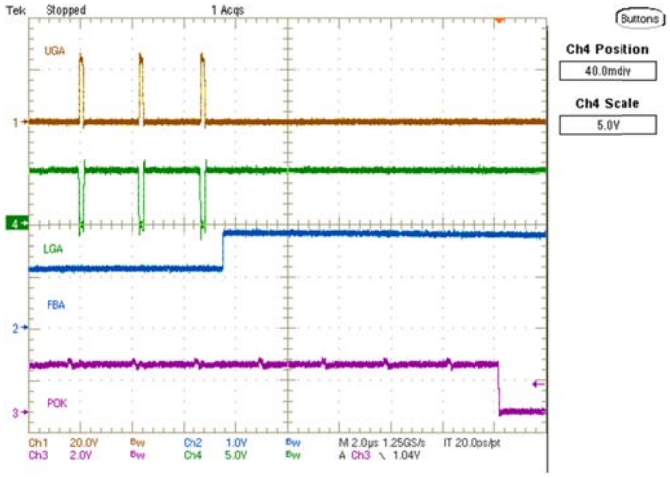

$V_{IN}$ = 19V, 1-phase DCM, VID = 0.8V to 0.65V, $I_{OUT}$ = 5A

**VDDA VR Load Transient**



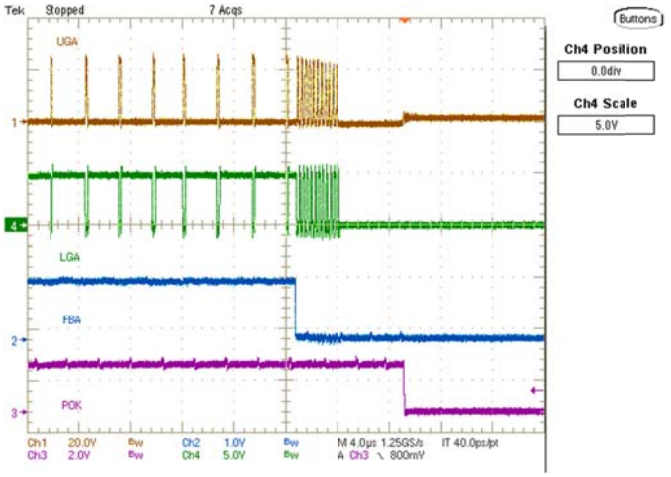

$V_{IN}$ = 19V, 1-phase DCM,VID = 0.7V, $I_{OUT}$ = 4A ~ 17A

**VDDA VR OVP**



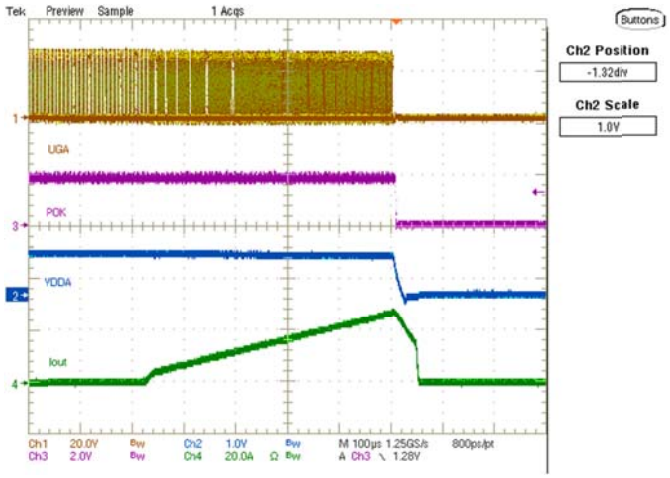

$V_{IN}$ = 19V, VDDA=1.1V

**VDDA VR UVP**




$V_{IN}$ = 19V, VDDA=1.1V

**VDDA VR OCP**




$V_{IN}$ = 19V, VDDA=1.1V



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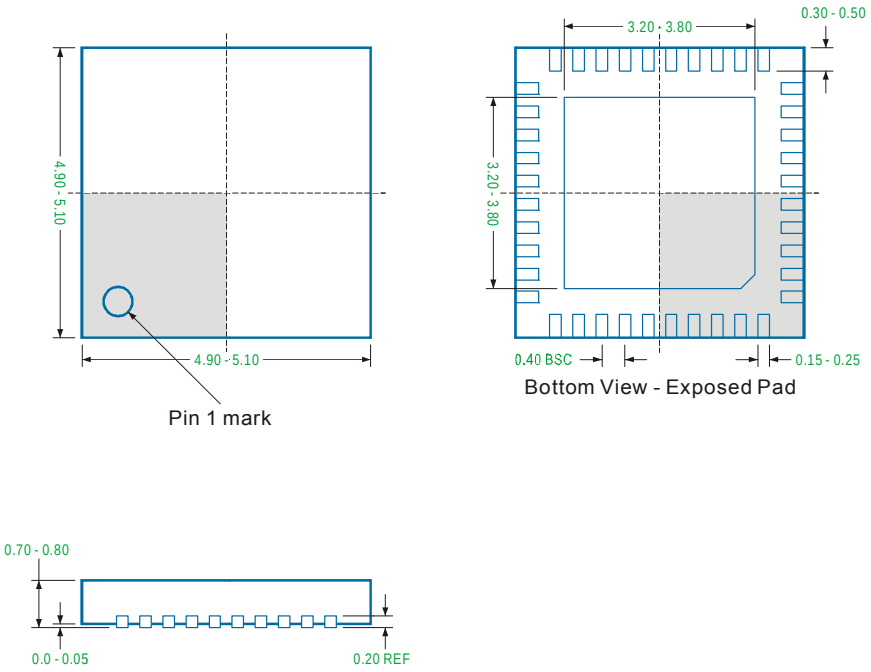
# uP9531P

## Package Information

WQFN5x5-40L




Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.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