uP9523R

2-Phase PWM Controller for IMVP9 Voltage Regulator

General Description

The uP9523R is an Intel® IMVP9 compatible 2-phase PWM voltage regulator controller for mobile/desktop platform application. This device has two embedded 5V MOSFET drivers with integrated bootstrap diodes. The controller supports 2/1-phase configuration to provide flexibility in platform power design. This device combines true differential output voltage sense, inductor DCR current sense, input voltage sense and adaptive voltage positioning to provide accurately regulated power for mobile/desktop CPU. It adopts uPI's proprietary RCOT+™ (Robust Constant On-Time) control topology to have fast transient response and smooth mode transition.

The uP9523R supports selectable voltage regulator parameters, such as Vboot voltage, switching frequency and dynamic VID transition slew rate. It also provides complete fault protection functions, including over voltage protection, under voltage protection, over current protection, over current limit, over temperature protection and under voltage lockout. The uP9523R is available in WQFN4x4 - 32L package.

Features

- Intel® IMVP9 Compatible
  - Support Mobile CPU
  - Support Desktop CPU
- RCOT+™ Control Topology
  - Easy Setting
  - Smooth Mode Transition
  - Fast Transient Response
- 2-Embedded 5V MOSFET Drivers
  - With Integrated Bootstrap Diodes
- Support Operation Phase Disable Function
  - 2/1-Phase Configuration
- Selectable Voltage Regulator Parameter
  - Vboot Voltage
  - Switching Frequency
  - Dynamic VID Transtion Slew Rate
- System Input Power Monitor Psys
- Enable Control and VR_RDY Indicator
- Thermal Sense Input and VRHOT# Indicator
- Differential Output Voltage Remote Sense
- Inductor DCR Current Sense
- OVP/UVP/OCP/OCL/UVLO/Thermal Shutdown
- RoHS Compliant and Halogen Free

Applications

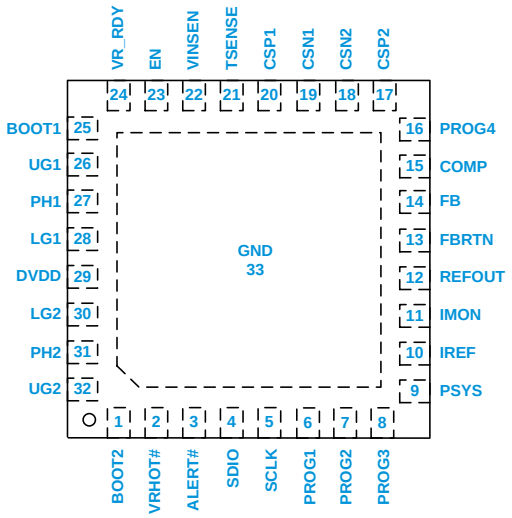
- Mobile CPU Power Supplies
- Desktop PC CPU Power Supplies

Ordering Information

Order Number	Package Type	Top Marking
uP9523RQKI	WQFN4x4-32L	uP9523R

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

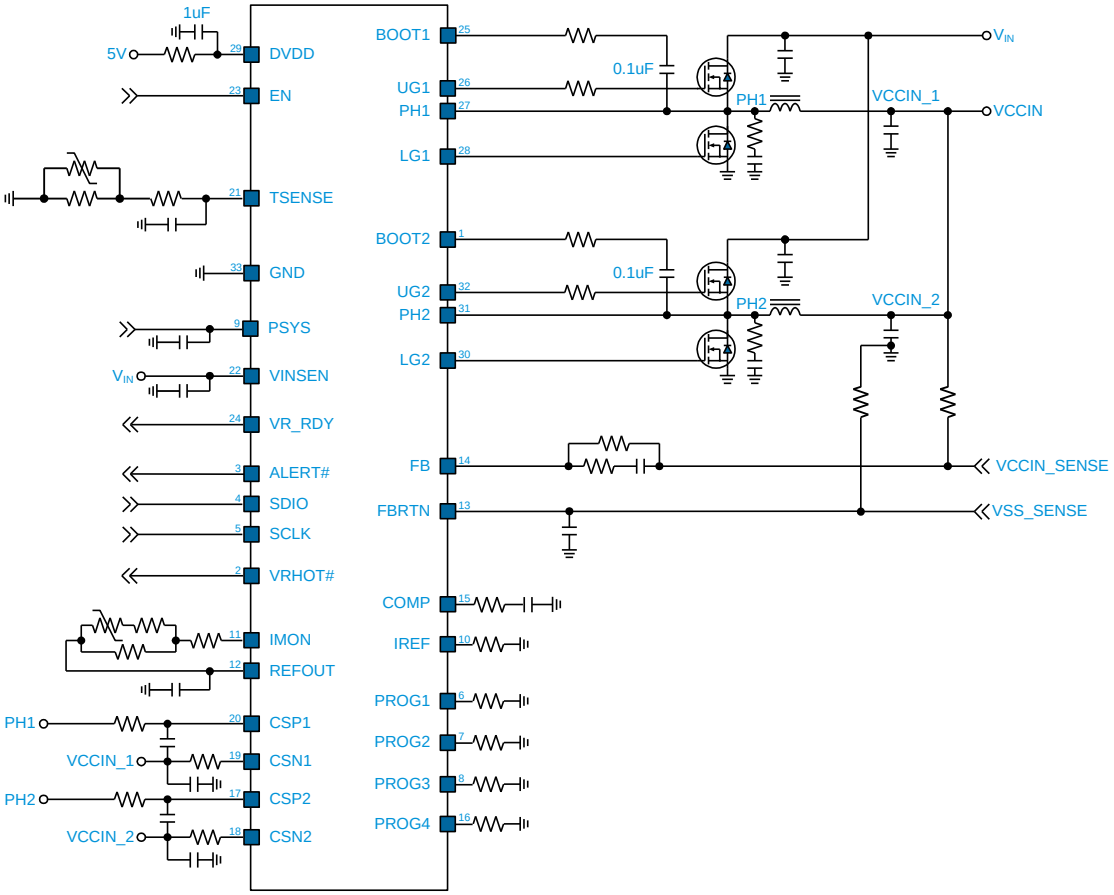
Pin Configuration



uP9523R

Typical Application Circuit

2-Phase Application



Functional Pin Description

Pin No.	Name	Pin Function
1	BOOT2	**Bootstrap Supply of Upper Gate Driver for Phase 2.** This pin is the supply input for the upper MOSFET gate driver. Connect the bootstrap capacitor C_{BOOT} between BOOT2 pin and PH2 pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Use at least 0.1uF MLCC as C_{BOOT}, and make sure it is placed close to the controller.
2	VRHOT#	**Thermal Indicator.** This pin is an open drain structure and it is active low. The controller asserts VRHOT# to indicate the platform that the VR temperature is higher than 106℃.
3	ALERT#	**SVID Alert# Line.**
4	SDIO	**SVID Data I/O.**
5	SCLK	**SVID Clock Input.**
6	PROG1	**Dynamic VID Boost Setting.** Connect a resistor from this pin to GND to set the dynamic VID boost function. The resistor value should be greater than 10kΩ.
7	PROG2	**Iccmax Setting Input.** Connect a resistor from this pin to GND to set the SVID Iccmax register (0x21h) value. The resistor value should be greater than 10kΩ
8	PROG3	**DC Load Line Setting.** Connect a resistor from this pin to GND to set the value of load line. The resistor value should be greater than 15kΩ.
9	PSYS	**Input of System Input Power Monitor.** This pin is for total platform system power monitor. The built-in analog-to-digital converter (ADC) converts the PSYS pin voltage to digital content for total platform system power monitor (0x1Bh) via SVID interface. The ADC input and output range is from 0V (=00h) to 2.56V (=FFh) with 10mV resolution. Connect this pin to a voltage source from platform, or connect this pin to a current source from platform along with a resistor from this pin to GND to implement this function. A capacitor can be added to this pin to adjust the response time. If this function is not used, please short this pin to GND.
10	IREF	**Dynamic VID Transition Slew Rate Setting.** Connect a resistor from this pin to GND to set the value of dynamic VID transition slew rate. Use 10kΩ for mobile platform application, and use 20kΩ for desktop platform application.
11	IMON	**Output Current Monitor.** The output current of this pin is proportional to the total load current. Connect a resistor network with NTC thermistor from this pin to REFOUT. The voltage across IMON and REFOUT is then proportional to the total load current. This voltage is used for load line, total output current protection and output current reporting. A built-in analog-to-digital converter (ADC) converts the voltage across IMON and REFOUT to digital content for output current reporting via SVID interface. Do not connect any capacitor to this pin.
12	REFOUT	**Reference Voltage Output.** This pin outputs a 1.2V as the reference voltage for IMON. Connect a capacitor from this pin to GND. Use a 0.1uF to 0.22uF MLCC as C_{REFOUT}, and place it close to this pin.

Functional Pin Description

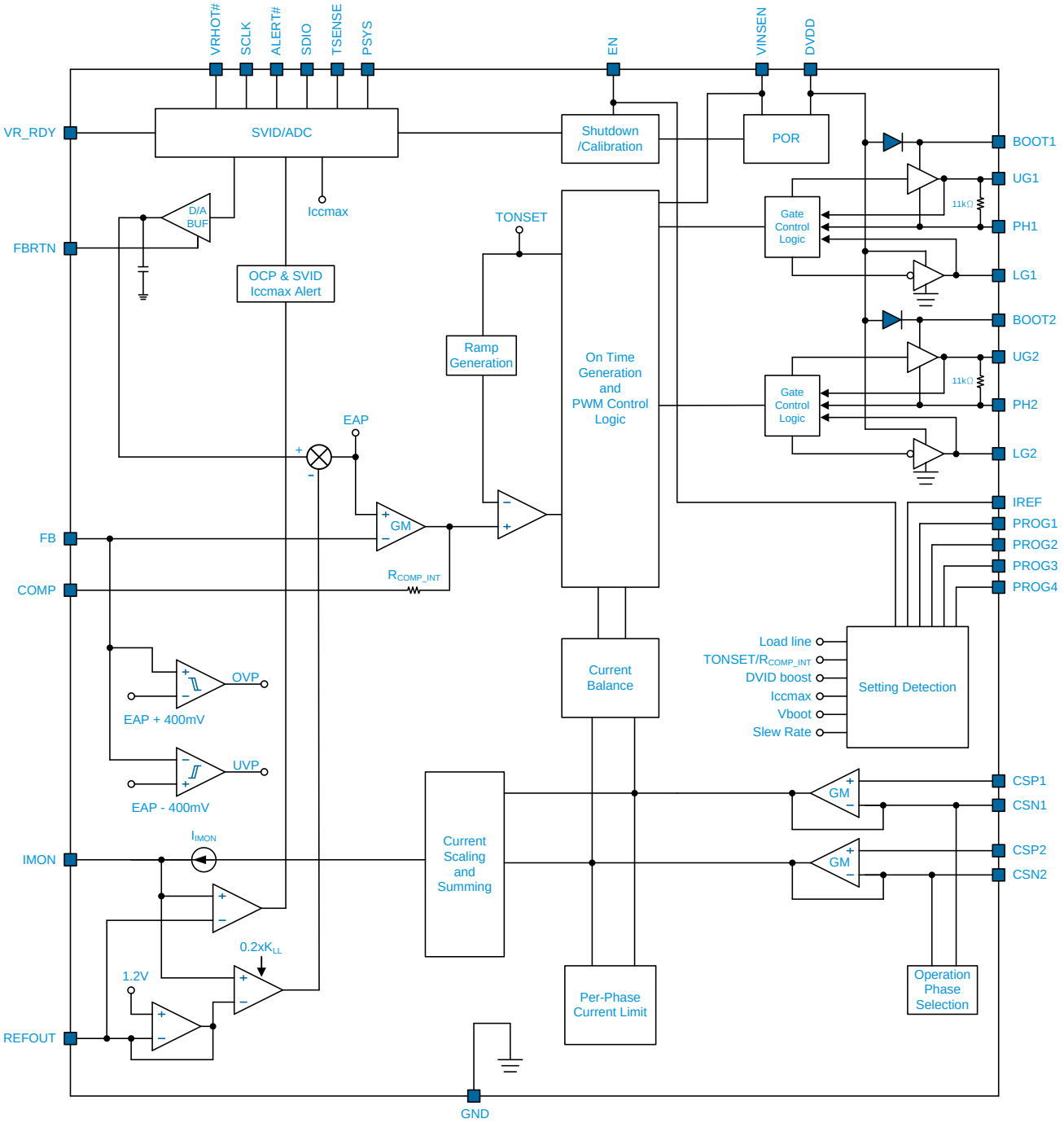
Pin No.	Name	Pin Function
13	FBRTN	**Output Voltage Feedback Return.** Inverting input to the differential voltage sense amplifier. Connect this pin directly to the processor output voltage feedback return sense point, namely VSS_SENSE.
14	FB	**Inverting Input of the Error Amplifier.**
15	COMP	**Output of Control Loop Error Amplifier.** Connect a resistor in series with a capacitor from this pin to GND for voltage control loop compensation.
16	PROG4	**PWM On-Time Setting and Internal Compensation Resistor R_{COMP_INT}.** Connect a resistor from this pin to GND to set the PWM on-time and internal compensation resistor R_{COMP_INT}. The resistor value should be greater than 15kΩ.
17	CSP2	**Positive Differential Current Sense Input for Phase 2.** When phase 2 is not used, short this pin to GND to let the controller operate in 1-phase configuration.
18	CSN2	**Negative Differential Current Sense Input for Phase 2.** When phase 2 is not used, pull high this pin to DVDD through a 1kΩ resistor to let the controller operate in 1-phase configuration.
19	CSN1	**Negative Differential Current Sense Input for Phase 1.**
20	CSP1	**Positive Differential Current Sense Input for Phase 1.**
21	TSENSE	**Thermal Monitoring Input.** Connect a specified negative temperature coefficient (NTC) thermistor network from this pin to GND for the voltage regulator temperature sensing Recommend to use 100kΩ/β=4250 NTC thermistor by Murata (NCP15WF104F03RC). See the related section in Application Information for detail.
22	VINSEN	**Power Stage Input Voltage Sense.** Directly connect this pin to the power stage input V_{IN}. The controller senses the voltage on this pin for power stage input voltage V_{IN} detection. The VINSEN voltage is also used for PWM on-time calculation.
23	EN	This pin is a multi-functional pin. It is chip enable control input and also used to set initial start up voltage Vboot. **Chip Enable Control Input.** Pull this pin above 0.8V enables the chip. Pull this pin below 0.3V to disable the chip. Pull up EN to 3.3V for 1.8V Vboot application. Follow the recommended power sequence and make sure DVDD is ready before EN goes high.
24	VR_RDY	**VR Ready Indicator.** This pin is an open drain structure and it is active high. Pull up this pin through a proper resistor to a voltage source. The controller asserts VR_RDY (goes high) at the end of Vboot ramp to indicate that the controller is ready to accept SVID command.
25	BOOT1	**Bootstrap Supply of Upper Gate Driver for Phase 1.** This pin is the supply input for the upper MOSFET gate driver. Connect the bootstrap capacitor C_{BOOT} between BOOT1 pin and PH1 pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Use at least 0.1uF MLCC as C_{BOOT}, and make sure it is placed close to the controller.

Functional Pin Description

Pin No.	Name	Pin Function
26	UG1	**Upper Gate Driver Output for Phase 1.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when to turn on/off upper MOSFET.
27	PH1	**Switch Node for Phase 1.** Connect this pin to the joint of upper MOSFET source, inductor and lower MOSFET drain. This pin is used as the return ground for upper MOSFET floating drive. Voltage on this pin is monitored by the shoot-through protection circuitry to determine when to turn on the lower MOSFET.
28	LG1	**Lower Gate Driver Output for Phase 1.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when to turn on the upper MOSFET.
29	DVDD	**Supply Input for the IC.** Connect this pin to a 5V voltage source via an RC filter, and bypass this pin to GND with at least 1uF MLCC and placed very close to this pin. DVDD is the supply input for both the logic control circuit and embedded MOSFET drivers.
30	LG2	**Lower Gate Driver Output for Phase 2.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when to turn on the upper MOSFET.
31	PH2	**Switch Node for Phase 2.** Connect this pin to the joint of upper MOSFET source, inductor and lower MOSFET drain. This pin is used as the return ground for upper MOSFET floating drive. Voltage on this pin is monitored by the shoot-through protection circuitry to determine when to turn on the lower MOSFET.
32	UG2	**Upper Gate Driver Output for Phase 2.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when to turn on/off upper MOSFET.
Exposed Pad		**Ground.** The exposed pad is the ground of embedded MOSFET drivers and logic control circuits, and it must be soldered to a large PCB and connected to GND.

uP9523R

Functional Block Diagram



Functional Description

Power Input and Power On Reset

The uP9523R has single power input DVDD. DVDD is the 5V supply input for control logic circuit of the controller and the embedded MOSFET drivers. RC filter to DVDD is required for locally bypassing this supply input. DVDD has power on reset (POR) function. VINSEN is the power stage input voltage sense pin, and it also has power on reset function. The controller monitors the VINSEN voltage for PWM on-time calculation. EN is the chip enable input pin. Logic high to this pin enables the controller, and logic low to this pin disables the controller. The above three inputs (DVDD, VINSEN and EN) are monitored to determine whether the controller is ready for operation.

Figure 1 shows the power ready detection circuit. The DVDD voltage is monitored for power on reset with typical 4.3V threshold at its rising edge. The VINSEN voltage is monitored for power on reset with typical 5.3V threshold at its rising edge. When DVDD and VINSEN are all ready, the controller waits for EN to start up. When EN pin is driven above 0.8V, the controller begins its start up sequence. When EN pin is driven below 0.3V, the controller will be turned off, and it will clear all fault states to prepare for next soft-start once the controller is re-enabled. Note that only DVDD or EN toggle will clear all fault state. VINSEN toggle is not used for clearing fault state. Anytime any one of the three inputs falls below their power on reset level will shutdown the controller.

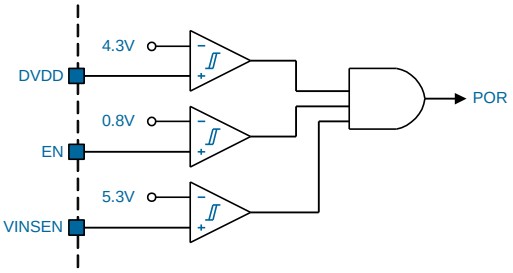


Figure 1. Circuit of Power Ready Detection

Controller Start up Sequence

When DVDD and VINSEN inputs are all ready, the controller waits for the EN signal to initiate the power on sequence. Figure 2 shows the typical start up sequence for non-zero Vboot case. After EN goes high (3.3V), the output voltage starts to ramp up to 1.8V. The controller asserts ALERT# when Vboot target is reached, and asserts VR_RDY at the end of Vboot ramp. The delay time from EN go high to VR_RDY assertion is T_A (< 2.5ms). Then the start up sequence is over. Figure 3 shows the typical start up sequence of zero Vboot case. After EN goes high (1.0V), the controller waits for a delay time T_B (< 2.5ms) then asserts VR_RDY to indicate that the PWM controller is ready for accepting SVID command. For the zero Vboot case, the output voltage slew rate is determined by the received SetVID command.

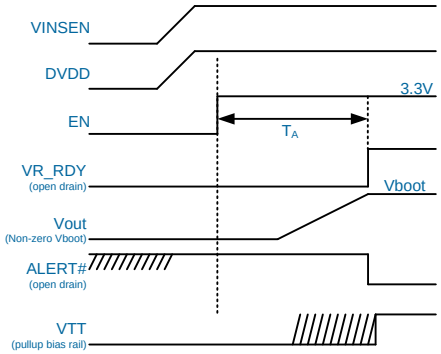


Figure 2. Start-Up Sequence and Enable Timing with Non-zero Vboot

Functional Description

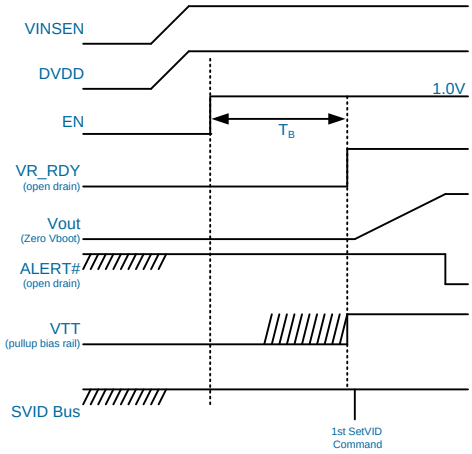


Figure 3. Start-Up Sequence and Enable Timing with Zero Vboot

Voltage Regulator Parameter Setting

There are four voltage regulator parameters that need to be determined, such as dynamic VID transition boost, SVID Iccmax register 0x21h value, load line, PWM on time setting. They are programmed by PROG1, PROG2, PROG3, PROG4, respectively as shown in Figure 4. Each parameter setting is detailed in the following sections.

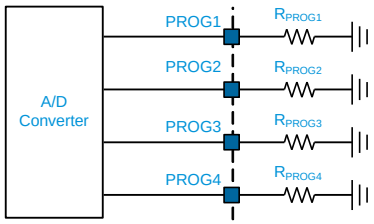


Figure 4. Initial Parameter Setting

Dynamic VID Transition Boost (PROG1)

The uP9523R provides dynamic VID (DVID) transition boost function to improve the DVID transition performance. The PROG1 pin is used to set the DVID boost function. Table 1 lists the PROG1 resistor setting for dynamic VID transition boost. Below is an example of choosing the PROG1 resistor. No matter what the DVID transition slew rate SR setting is, use 13mV/us as the slew rate in the DVID transition boost setting calculation. Given slew rate SR = 13mV/us, load line (LL) = 2mΩ, Cout = 1000uF, the droop voltage caused by the inrush current during upward dynamic VID transition can be calculated as Vdroop = (Cout*SR)*LL = 26mV. The DVID boost factor K is defined as K = Vdroop(mV)/K_SR, where K_SR =15. Then K = 26/15 = 1.73, choose K = 2 from Table 1, therefore the resistor R_{PROG1} = 18.7kΩ. Fine-tuning may be required per actual measurement to ensure that the dynamic VID transition performance meets the requirement.

Functional Description

Table 1. Dynamic VID Transition Boost Setting

DVID Boost Factor (K)	Recommended Resistor R_{PROG1} (kΩ)	DVID Boost Factor (K)	Recommended Resistor R_{PROG1} (kΩ)
0	16.2	8	24.9
1	17.8	9	26.1
2	18.7	10	26.7
3	19.6	11	28
4	20.5	12	28.7
5	21.5	13	30.1
6	22.6	14	30.9
7	23.7	15	32.4

SVID Register 0x21h (Iccmax) Value (PROG2)

The PROG2 pin is used to set the SVID register 0x21h value as shown in Figure 4. During the initial setting period, a 10uA current source is turned on for a period of time to flow out of PROG2 pin through R_{PROG2} to create voltage drop on this pin. This voltage is digitized by an internal 8-bit A/D converter and stored in SVID register 0x21h (Iccmax). The Iccmax register value is calculated as below equation.

$$\text{Iccmax(A)} = \frac{R_{PROG2}(k\Omega)}{65} \times 255$$

The recommended resistance range of R_{PROG2} is from 10kΩ to 65kΩ. The programmable range is from 27h to FFh (39A to 255A). If the pin voltage is greater than 0.65V, the SVID register 0x21h value is still FFh. Note that this setting is only for determining SVID register value, and is not used for over current protection or SVID Iccmax alert function.

Load Line Factor K_{LL} and Load Line Setting (PROG3)

As shown in Figure 5, the current I_{CSNx} denotes the sensed current in each phase. These currents are scaled and summed as I_{IMON}, which denotes the total output current, and it is fed to the IMON pin. The voltage difference between IMON and REFOUT is internally converted to generate a scaled voltage, which is subtracted from the reference voltage for load line. As total load current increases, the scaled voltage increases. This makes the output voltage decreases linearly as the total output current increases, which is also known as active voltage positioning (AVP). The slope of output voltage decrease to total load current increase is referred to as load line. The load line is defined as follows.

$$\text{Load Line} = R_{LL} = \frac{2}{5} \times \frac{R_{DC}}{R_{CSN}} \times R_{IMON} \times K_{LL}$$

Where R_{LL} is the load line, R_{DC} is the DC resistance of inductor, and they are given parameters. K_{LL} is the load line factor to be determined. R_{CSN} is obtained by giving the per phase current limit level. The R_{IMON} value is obtained through Iccmax trigger level calculation, then load line factor K_{LL} can be obtained as follows.

$$K_{LL} = \frac{R_{CSN}}{R_{DC}} \times \frac{5}{2} \times \frac{R_{LL}}{R_{IMON}}$$

Functional Description

The PROG3 pin is used to set the K_{LL} value for load line setting. During the initial setting period, a 10uA current source is turned on for a period of time to flow out of PROG3 pin through R_{PROG3} to create voltage drop on this pin. This voltage is used to determine the K_{LL} value, which is defined as below equation. Note that the resistance of R_{PROG3} = 255 kΩ or greater is for LL= 0 and R_{PROG3} = 15kΩ is also for LL = 0. Fine-tuning may be required per actual measurement to ensure that the DC load line meets the requirement.

$$K_{LL} = \frac{255 - R_{PROG3}(k\Omega)}{128}$$

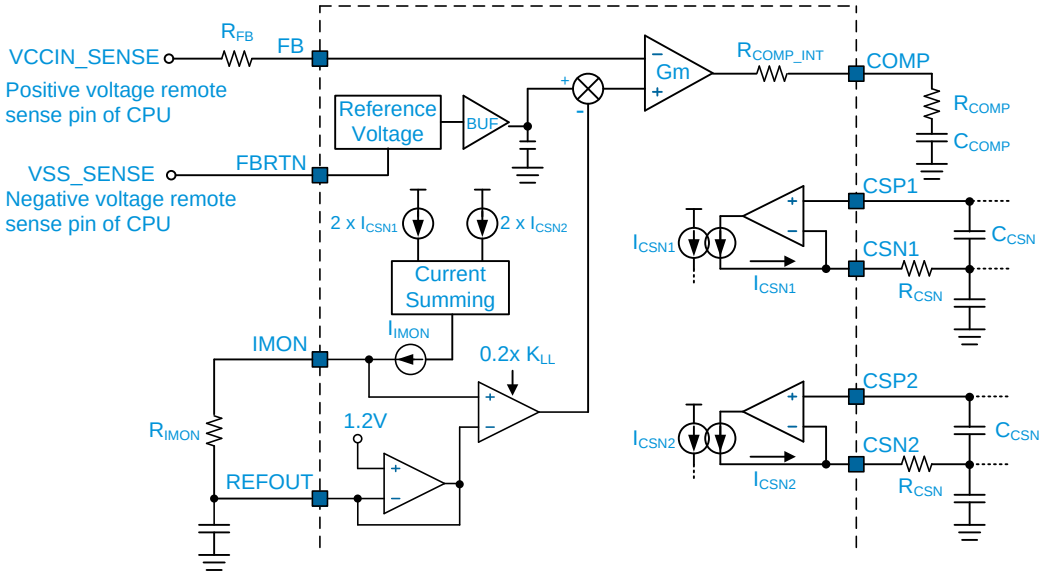


Figure 5. Load Line and Output Voltage Differential Sense

PWM On Time (Switching Frequency) and Internal R_{COMP_INT} (PROG4)

Refer to Figure 4, a resistor R_{PROG4} connected from PROG4 pin to GND is used to set two parameters: PWM on time and internal compensation resistor R_{COMP_INT}. The PWM on time determines the switching frequency. Table 2 shows the recommended resistance value for R_{COMP_INT} and the switching frequency (with the condition of V_{IN} = 12V, V_{OUT} = 1.8V). Select the resistor from Table 2 to set the switching frequency. The other parameter to be set is R_{COMP_INT}, which is a resistor internal to the COMP pin. There is an external resistor R_{COMP} connected to COMP pin for voltage loop compensation. The additional internal compensation resistor (R_{COMP_INT}) will be in series with the external R_{COMP} only when the voltage regulator is in single-phase operation to improve the load transient response. When the voltage regulator is in multi-phase operation, the R_{COMP_INT} is fixed at 2.5kΩ.

Functional Description

Table 2. R_{COMP_INT} and Switching Frequency

Recommended Resistor R_{PROG4} (kΩ)	R_{COMP_INT} in Single-Phase	Switching Frequency (kHz)
15.8	+7.5kΩ	300
21.5		400
30.1		500
40.2		600
54.9	+5kΩ	600
75.0		500
95.3		400
118		300
147	+2.5kΩ	300
182		400
226		500
open		600

Initial Start Up Voltage (Vboot)

The EN pin is used for chip enable control input and also used to set initial start up voltage Vboot. The uP9523R has selectable initial start up voltage (Vboot) for design flexibility. The Vboot can be set to 0V or 1.8V as below.

If V_{EN} < 2V, Vboot = 0V.

If V_{EN} > 2V, Vboot = 1.8V.

It is recommended to use 3.3V from system for 1.8V Vboot typical implementation.

Operation Phase Disable Function

uP9523R supports operation phase disable function to further increase the design flexibility. Platform designer can choose to disable a phase to meet their design requirement. The minimum operation phase number is 1 phase. In general, to disable phase 2, pull up CSN2 to DVDD through 1kΩ resistor and tie CSP2 to ground. The controller detects all the CSNx and CSPx voltage at DVDD power on reset to determine operation phase number.

Dynamic VID Transition Slew Rate

The IREF pin is used for the dynamic VID transition slew rate setting. The slew rate can be set to 52mV/us (for mobile platform application) or 13mV/us (for desktop platform application) by the R_{IREF} resistor as shown in Figure 6. Table 3 shows the recommended resistance value for slew rate selection. Make sure to connect a resistor from IREF pin to GND and place this resistor close to the controller. This resistor is used to generate the reference current for thermal sense by TSENSE.

Functional Description

Table 3. Dynamic VID Transition Slew Rate Setting

Recommended Resistor R_{IREF} (kΩ)	10	20
Fast Slew Rate (mV/us)	52	13
Slow Slew Rate (mV/us)	13	3
Slew Rate During Soft Start Operation (mV/us)	52	13

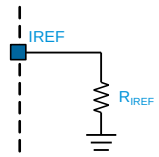


Figure 6.IREF Connection

Dynamic VID Transition

The controller accepts SetVID command via SVID bus for output voltage change during normal operation. This allows the output voltage to change while the voltage regulator is running and supplying current to the load. This is commonly referred to as VID on-the-fly (VID OTF). A VID OTF event may occur under either light or heavy load condition. This voltage change direction can be upward or downward. Per SetVID command, the slew rate can be fast or slow. The default value of slow slew rate is 1/4 of fast slew rate. The slow slew rate is determined by the processor in SVID register 2Ah, which can only be programmed by the processor.

Soft Start

The slew rate of output voltage during soft start operation and dynamic VID voltage change is determined internally. The slew rate during soft start operation for non-zero Vboot case (refer to Figure 2) is shown in Table 3.

Output Voltage Differential Sense

The uP9523R uses differential sense by a high-gain low offset error amplifier for output voltage differential sense as shown in Figure 5. The CPU voltage is sensed by the FB and FBRTN pins. FB pin is connected to the positive remote sense pin VCCIN_SENSE of the CPU via the resistor R_{FB}. FBRTN pin is connected to the negative remote sense pin VSS_SENSE of CPU directly.

Iccmax Alert and Total Output Over Current Protection (OCP)

As shown in Figure 7, the current I_{CSNx} denotes the sensed per-phase load current, and the summed current is further internally mirrored to IMON pin as I_{IMON} for SVID Iccmax alert function and total output over current protection (OCP). A resistor R_{IMON} is connected from IMON pin to REFOUT. This I_{IMON} current flows through the resistor R_{IMON}, creating voltage drop across it. As the total load current increases, the voltage on IMON pin (V_{IMON}) increases proportionally.

When the IMON voltage is greater than V_{REFOUT}+1.5V, the SVID Iccmax alert is triggered, and then the ALERT# is pulled low to indicate the processor that the voltage regulator is in Iccmax condition.

Functional Description

The output current level of triggering SVID Iccmax alert is calculated as follows.

$$I_{OUT\_Iccmax} = \frac{1.5}{R_{IMON}} \times \frac{R_{CSN}}{R_{DC}} \times \frac{1}{2}$$

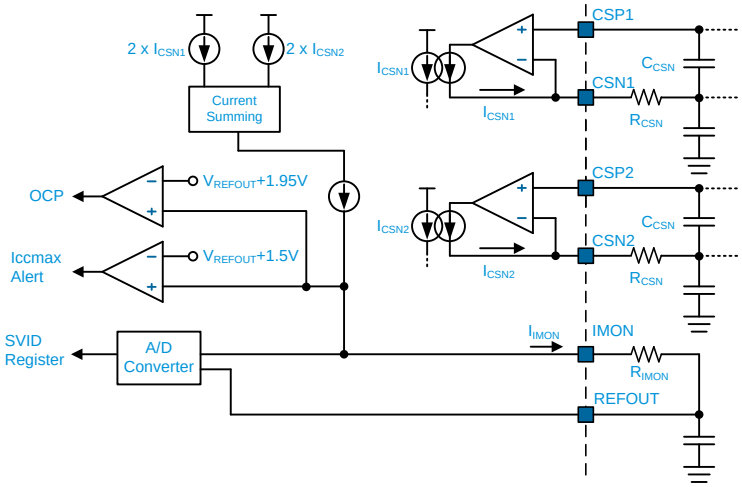


Figure 7. Iccmax Alert and Total Output OCP

When the IMON voltage further increases to greater than the OCP threshold (it is typically 130% of SVID Iccmax alert threshold) for a specific delay time, the total output current protection will be triggered. VR_RDY will be pulled low immediately; both UGx and LGx will be held low, to turn off all MOSFETs to shutdown the regulator. The total output OCP is a latch-off type protection, and it can only be reset by DVDD or EN toggling. Avoid connecting any capacitor to the IMON pin since it brings extra delay. The output current level of triggering total output OCP is calculated as follows.

$$I_{OUT\_OCP} = \frac{1.5 \times 1.3}{R_{IMON}} \times \frac{R_{CSN}}{R_{DC}} \times \frac{1}{2}$$

Total Output OCP and Operating Phase Number

The total output OCP level is usually designed for the voltage regulator that is operated in full phase condition by hardware setting. The actual operating phase number is controlled by the SVID SetPS command. When the operating phase number is decreased, the total output OCP level is decreased as well. The total output OCP level is changed per actual operating phase number. Table 4 shows the total output OCP ratio per actual operating phase number and the hardware configuration.

Table 4. Total Output OCP and Operation Phase Number

Total Output OCP Ratio		Operation Condition	
		2-Phase	1-Phase
Hardware Configuration	2-Phase	1	7/12
	1-Phase	--	1

Functional Description

Output Current Reporting

Refer to Figure 7, the summed current is internally mirrored and fed to IMON pin as I_{IMON} for SVID output current reporting function. A resistor R_{IMON} is connected between IMON and REFOUT. The current I_{IMON} flows through the resistor R_{IMON}, creating voltage drop across it. As the total load current increases, the voltage on IMON pin (V_{IMON}) increases proportionally. An internal analog-to-digital converter (ADC) converts the voltage difference between IMON and REFOUT to a digital content for output current reporting through SVID interface. As V_{IMON} voltage increases, the SVID register 0x15h content increases. REFOUT is used as the reference of IMON, therefore V_{IMON} = 1.2V means SVID register 0x15h = 00h. The ADC input range is typically 1.5V, which means the SVID register 0x15h = FFh when V_{IMON} = 2.7V. Further increase of V_{IMON} (>2.7V) is allowed, but the ADC results will remain at FFh. The total output current level for SVID register 0x15h = FFh is calculated as follows.

$$I_{OUT\,SVID\,0x15h=\,FFh} = \frac{1.5}{R_{IMON}} \times \frac{R_{CSN}}{R_{DC}} \times \frac{1}{2}$$

Over Voltage Protection (OVP)

The controller monitors the voltage on FB pin for over voltage protection. After output voltage ramps up to Vboot, the controller initiates OVP function. Once V_{FB} exceeds the OVP threshold for a specific delay time, OVP is triggered. VR_RDY is pulled low immediately, UGx is held low, LGx is held high, and turns on low side MOSFET and turns off high side MOSFET to protect CPU. Since the low side MOSFET is turned on, the regulator output capacitor is discharged and output voltage decreases as well. When FB pin voltage decreases to lower than typical 0.5V, LGx is held low to turn off the low side MOSFET to avoid negative output voltage. The OVP is a latch-off type protection, and it can only be reset by DVDD or EN toggling. The OVP detection circuit has a fixed delay time to prevent false trigger. Note that the OVP is blocked during VID OTF.

Under Voltage Protection (UVP)

The controller monitors the voltage on FB pin for under voltage protection. After output voltage ramps up to Vboot, the controller initiates UVP function. Once V_{FB} is lower than the UVP threshold for a specific delay time, UVP is triggered. VR_RDY is pulled low immediately, both UGx and LGx is held low, and then turns off all MOSFETs to shutdown the regulator. The UVP is a latch-off type protection, and it can only be reset by DVDD or EN toggling. The UVP detection circuit has a fixed delay time to prevent false trigger. Note that the UVP is blocked during VID OTF.

Per-Phase Over Current Limit

In addition to the total output current OCP, the controller provides per-phase peak current limit function to protect the voltage regulator. The controller uses DCR current sense technique to sense the inductor current in each phase for per-phase current peak limit and current balance as shown in Figure 8. In this inductor current sensing topology, the time constant is expressed as follows

$$k \times \frac{L}{R_{DC}} = R_{CSPx} \times C_{CSNx}$$

Functional Description

where L is the output inductor, R_{DC} is its DC resistance and k is a constant. Theoretically, if k = 1, the sensed current signal I_{CSNx} is expressed as follows.

$$I_{CSNx} = \frac{I_{LX} \times R_{DC}}{R_{CSNx}}$$

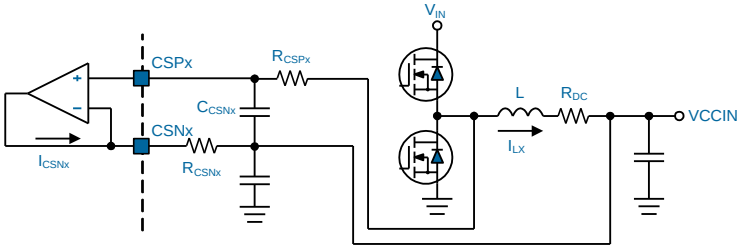


Figure 8. Inductor DCR Current Sense

The sensed current I_{CSNx} represents the current in each phase, and it is compared to a 60uA current source for per-phase peak current limit. If the inductor current of any of the active operating phase exceeds the threshold, the per-phase output inductor current is limited to an averaged current. A continuous over load event will cause the output voltage to drop and eventually trigger under voltage protection to shut down the voltage regulator.

Note that the resistance value of R_{CSNx} must be less than 1kΩ to ensure the current sensing circuit in normal operation. The resistance of R_{CSNx} and the per-phase current limit level can be obtained using equation as follows.

$$R_{CSNx} = \frac{I_{OCP\_perphase} \times R_{DC}}{60uA}$$

Thermal Monitoring and VRHOT#

The TSENSE pin is used for voltage regulator thermal monitoring. Connect a negative temperature coefficient (NTC) thermistor network from TSENSE pin to GND to implement this function as shown in Figure 9. The NTC thermistor is placed close to the hottest point of the regulator, normally close to the inductor and low-side MOSFET of phase 1. A precision current source flows out of the TSENSE pin through the temperature sense network to create a voltage drop V_{TSENSE} on this pin. As regulator temperature rises, the V_{TSENSE} decreases. Therefore the controller detects the V_{TSENSE} to obtain regulator thermal information for SVID thermal alert and VRHOT# function.

The controller asserts VRHOT# when the sensed temperature is higher than the value of SVID register 0x22h (Temp_Max), in which the value is 6Ah (106℃).

The temperature for SVID thermal alert and VRHOT# assertion is 103℃ and 106℃, respectively. The curve of TSENSE pin voltage and the sensed temperature is shown in Figure 10. The regulator can trigger the VRHOT# as long as the temperature exceeds the maximum temperature threshold. It is highly recommended to use 7.32kΩ as R_P, and 100kΩ/β= 4250 NTC thermistor by Murata (NCP15WF104F03RC). R_S is reserved for fine tune.

Functional Description

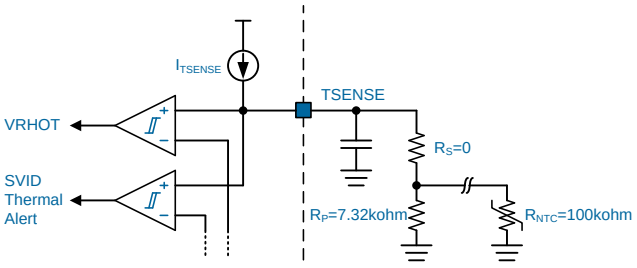


Figure 9. Regulator Temperature Sense

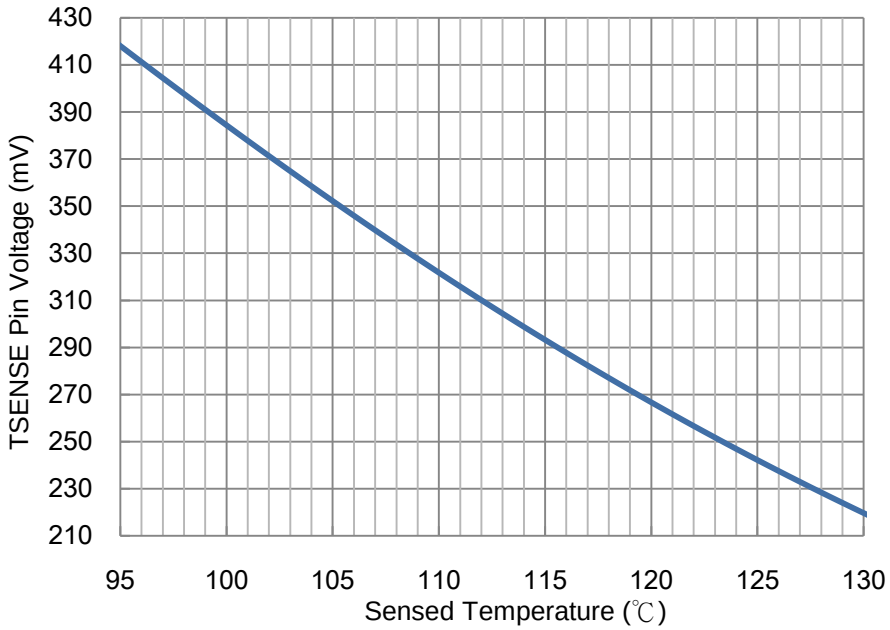


Figure 10. TSENSE Pin Voltage and Sensed Temperature

Control Loop

The uP9523R adopts the uPI's proprietary RCOT^{+TM} control technology. The RCOT uses the constant on-time modulator. The output voltage is sensed to compare with the internal high accurate reference voltage. The reference voltage is commanded by CPU through the SVID interface. The amplified error signal V_{COMP} is compared to the internal ramp to initiate a PWM on-time. The RCOT^{+TM} features easy design, fast transient response, smooth mode transition for powering the microprocessor.

Functional Description

Table 5. IMVP9 VID Table

SVID HEX	VID (V)	SVID HEX	VID (V)	SVID HEX	VID (V)	SVID HEX	VID (V)	SVID HEX	VID (V)	SVID HEX	VID (V)	SVID HEX	VID (V)
0x00	0.00	0x25	0.56	0x4A	0.93	0x6F	1.30	0x94	1.67	0xB8	2.03	0xDC	2.39
0x01	0.20	0x26	0.57	0x4B	0.94	0x70	1.31	0x95	1.68	0xB9	2.04	0xDD	2.40
0x02	0.21	0x27	0.58	0x4C	0.95	0x71	1.32	0x96	1.69	0xBA	2.05	0xDE	2.41
0x03	0.22	0x28	0.59	0x4D	0.96	0x72	1.33	0x97	1.70	0xBB	2.06	0xDF	2.42
0x04	0.23	0x29	0.60	0x4E	0.97	0x73	1.34	0x98	1.71	0xBC	2.07	0xE0	2.43
0x05	0.24	0x2A	0.61	0x4F	0.98	0x74	1.35	0x99	1.72	0xBD	2.08	0xE1	2.44
0x06	0.25	0x2B	0.62	0x50	0.99	0x75	1.36	0x9A	1.73	0xBE	2.09	0xE2	2.45
0x07	0.26	0x2C	0.63	0x51	1.00	0x76	1.37	0x9B	1.74	0xBF	2.10	0xE3	2.46
0x08	0.27	0x2D	0.64	0x52	1.01	0x77	1.38	0x9C	1.75	0xC0	2.11	0xE4	2.47
0x09	0.28	0x2E	0.65	0x53	1.02	0x78	1.39	0x9D	1.76	0xC1	2.12	0xE5	2.48
0x0A	0.29	0x2F	0.66	0x54	1.03	0x79	1.40	0x9E	1.77	0xC2	2.13	0xE6	2.49
0x0B	0.30	0x30	0.67	0x55	1.04	0x7A	1.41	0x9F	1.78	0xC3	2.14	0xE7	2.50
0x0C	0.31	0x31	0.68	0x56	1.05	0x7B	1.42	0xA0	1.79	0xC4	2.15	0xE8	2.51
0x0D	0.32	0x32	0.69	0x57	1.06	0x7C	1.43	0xA1	1.80	0xC5	2.16	0xE9	2.52
0x0E	0.33	0x33	0.70	0x58	1.07	0x7D	1.44	0xA2	1.81	0xC6	2.17	0xEA	2.53
0x0F	0.34	0x34	0.71	0x59	1.08	0x7E	1.45	0xA3	1.82	0xC7	2.18	0xEB	2.54
0x10	0.35	0x35	0.72	0x5A	1.09	0x7F	1.46	0xA4	1.83	0xC8	2.19	0xEC	2.55
0x11	0.36	0x36	0.73	0x5B	1.10	0x80	1.47	0xA5	1.84	0xC9	2.20	0xED	2.56
0x12	0.37	0x37	0.74	0x5C	1.11	0x81	1.48	0xA6	1.85	0xCA	2.21	0xEE	2.57
0x13	0.38	0x38	0.75	0x5D	1.12	0x82	1.49	0xA7	1.86	0xCB	2.22	0xEF	2.58
0x14	0.39	0x39	0.76	0x5E	1.13	0x83	1.50	0xA8	1.87	0xCC	2.23	0xF0	2.59
0x15	0.40	0x3A	0.77	0x5F	1.14	0x84	1.51	0xA9	1.88	0xCD	2.24	0xF1	2.60
0x16	0.41	0x3B	0.78	0x60	1.15	0x85	1.52	0xAA	1.89	0xCE	2.25	0xF2	2.61
0x17	0.42	0x3C	0.79	0x61	1.16	0x86	1.53	0xAB	1.90	0xCF	2.26	0xF3	2.62
0x18	0.43	0x3D	0.80	0x62	1.17	0x87	1.54	0xAC	1.91	0xD0	2.27	0xF4	2.63
0x19	0.44	0x3E	0.81	0x63	1.18	0x88	1.55	0xAD	1.92	0xD1	2.28	0xF5	2.64
0x1A	0.45	0x3F	0.82	0x64	1.19	0x89	1.56	0xAE	1.93	0xD2	2.29	0xF6	2.65
0x1B	0.46	0x40	0.83	0x65	1.20	0x8A	1.57	0xAF	1.94	0xD3	2.30	0xF7	2.66
0x1C	0.47	0x41	0.84	0x66	1.21	0x8B	1.58	0xB0	1.95	0xD4	2.31	0xF8	2.67
0x1D	0.48	0x42	0.85	0x67	1.22	0x8C	1.59	0xB1	1.96	0xD5	2.32	0xF9	2.68
0x1E	0.49	0x43	0.86	0x68	1.23	0x8D	1.60	0xB2	1.97	0xD6	2.33	0xFA	2.69
0x1F	0.50	0x44	0.87	0x69	1.24	0x8E	1.61	0xB3	1.98	0xD7	2.34	0xFB	2.70
0x20	0.51	0x45	0.88	0x6A	1.25	0x8F	1.62	0xB4	1.99	0xD8	2.35	0xFC	2.71
0x21	0.52	0x46	0.89	0x6B	1.26	0x90	1.63	0xB5	2.00	0xD9	2.36	0xFD	2.72
0x22	0.53	0x47	0.90	0x6C	1.27	0x91	1.64	0xB6	2.01	0xDA	2.37	0xFE	2.73
0x23	0.54	0x48	0.91	0x6D	1.28	0x92	1.65	0xB7	2.02	0xDB	2.38	0xFF	2.74
0x24	0.55	0x49	0.92	0x6E	1.29	0x93	1.66	--	--	--	--	--	--

Functional Description

Table 6. Supported SVID Data and Configuration Register for Address = 00h

Index	Register Name	Access	Default	Description
00h	Vendor ID	RO	27h	Vendor ID
01h	Product ID	RO	1Fh	Product ID
02h	Product Revision	RO	01h	Product Revision
05h	Protocol ID	RO	08h	Identifies what version of SVID protocol the controller supports. IMVP9 = 08h.
06h	Capability	RO	A1h	Bit mapped register, identifies the SVID VR capabilities and which of the optional telemetry are supported.
10h	Status_1	RO	00h (Zero Vboot) 01h (Non-zeroVboot)	Data register containing the status of VR.
11h	Status_2	RC	00h	Data Register containing the status of transmission.
15h	Output Current	RO	--	Averaged output current. This read-only field yields the conversion result for VR output current commonly referred to as IMON.
1Bh	Input Power (PSYS)	RO	--	Averaged input power or PSYS. This read-only field contains the telemetry's input power measurement data.
1Ch	Status2_LastRead	RO	00h	This register contains a copy of the status2 data that was last read with the GETREG (status2) command.
21h	ICC_Max	RO	--	Data register containing the ICC maximum the plastform supports.
22h	Temp_Max	RO	6Ah	Data register containing the temperature maximum the platform supports and the level VRHOT# asserts. Binary format in ℃, i.e. 6Ah = 106℃.
24h	SR_Fast	RO	34h (mobile) 0Dh (desktop)	Data register containing the capability of fast slew rate the platform can sustain. Binary format in mV/us, i.e. 0Dh = 13mV/us. 34h = 52mV/us. The register content depends on the resistor setting of IREF pin.
25h	SR_Slow	RO	0Dh (mobile) 03h (desktop)	Data register containing the capability of slow slew rate the platform can sustain. Binary format in mV/us, i.e. 03h = 3mV/us. 0Dh = 13mV/us. The register content depends on the resistor setting of IREF pin.

Functional Description

Table 6. Supported SVID Data and Configuration Register for Address = 00h (cont.)

Index	Register Name	Access	Default	Description
26h	Vboot	RO	--	Data register containing Vboot voltage in VID steps. The register content depends on the EN voltage level.
2Ah	Slow Slew Selector	RW	02h	Default 02h denotes slow slew rate is 1/4 of fast slew rate.
2Bh	PS4 Exit Latency	RO	7Bh	This register holds an encoded value that represents the VR PS4 exit latency. 7Bh represents 88us.
2Ch	PS3 Exit Latency	RO	45h	This register holds an encoded value that represents the VR PS3 exit latency. 45h represents 5us.
2Dh	ENABLE to SVID Ready	RO	C9h	This register holds an encoded value that represents the VR ENABLE to Ready. C9h represents 2304us.
30h	Vout_Max	RW	D3h	This register is programmed by the master and sets the maximum VID. D3h = 2.3V.
31h	VID_Setting	RO	--	Data register containing currently programmed VID.
32h	Power_State	RW	00h	Register containing the programmed power state.
33h	Voltage Offset	RW	00h	Set offset in VID steps.
34h	Multi_VR_Config	SW	01h	Bit mapped data register which configures multiple VRs behavior on the same bus.
35h	SetRegADR	RW	00h	Scratch pad register for temporary storage of the SetRegADR pointer register.

Functional Description

Table 7. Supported SVID Data and Configuration Register for Address = 0Dh

Index	Register Name	Access	Default	Description
00h	Vendor ID	RO	27h	Vendor ID
01h	Product ID	RO	1Fh	Product ID
02h	Product Revision	RO	01h	Product Revision
05h	Protocol ID	RO	08h	Identifies what version of SVID protocol the controller supports IMVP9 =08h.
10h	Status_1	RO	01h	Data register containing the status of VR.
11h	Status_2	RC	00h	Data register containing the status of transmission.
15h	Output Current	RO	--	Averaged output current. This read-only field yields the conversion result for VR output current commonly referred to as IMON.
1Bh	Input Power (PSYS)	RO	--	Averaged input power or PSYS. This read-only field contains the telemetry's input power measurement data.
1Ch	Status2_LastRead	RO	00h	This register contains a copy of the status2 data that was last read with the GETREG (status2) command.
32h	Power_State	RW	00h	Register containing the programmed power state.
34h	Multi_VR_Config	SW	01h	Bit mapped data register which configures multiple VRs behavior on the same bus.
49h	PSYSC_DBC_CLR	RW	00h	Thie register contains the minimum time for which the input system power (Psys input) must continually be below the CRITICAL threshold (PsysCrLvl) before VRHOT# is de-asserted (high).
4Ah	PSYS_CR_LVL_H	RW	00h	This register field sets the Psys Critical Power Detector comparator threshold level.
4Bh	PSYS_W2_LVL_H	RW	00h	This register field sets the threshold level of the WARNING2 comparator.
4Ch	PSYS_W1_LVL_H	RW	00h	This register field sets the threshold level of the WARNING1 comparator.
4Dh	PSYS_WARN2_CNT	RC	00h	This register contains the total time for which input Psys is above or below the WARNING2 threshold (PsysW2Lvl).
4Eh	PSYS_WARN1_CNT	RC	00h	This register contains the total time for which input Psys is above or below the WARNING1 threshold (PsysW1Lvl).
4Fh	PSYSC_DBC_SET	RW	00h	This register contains the minimum time for which the input system power (Psys input) must continually meet or exceed CRITICAL threshold (PsysCrLvl) before VRHOT# is asserted (low).

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, DVDD ---------- -0.3V to +6V
VINSEN ---------- -0.3V to +30V
BOOTx to PHx
DC ---------- -0.3V to +6V
PHx to GND
DC ---------- -0.7V to +28V
< 100ns ---------- -8V to +36V
BOOTx to GND
DC ---------- -0.3V to +34V
< 100ns ---------- -5V to +42V
UGx to PHx
DC ---------- -0.3V to +6V
< 100ns ---------- -5V to +7V
LGx to GND
DC ---------- -0.3V to +6V
< 100ns ---------- -5V to +7V
Other Pins ---------- -0.3V to +6V
Storage Temperature Range ---------- -65℃ to +150℃
Junction Temperature ---------- 150℃
Lead Temperature (Soldering,10 sec) ---------- 260℃
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV

Thermal Information

Package Thermal Resistance (Note 3)
WQFN4x4-32L θ_{JA} ---------- 37℃/W
WQFN4x4-32L θ_{JC} ---------- 2℃/W
Power Dissipation, P_D @ T_A = 25℃
WQFN4x4-32L ---------- 2.7W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40℃ to +125℃
Operating Ambient Temperature Range ---------- -40℃ to +85℃
Supply Input Voltage, DVDD ---------- 4.5V to 5.5V
Power Stage Input Voltage, V_{IN} ---------- 6V to 26V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25℃ on a low effective thermal conductivity test board of *JEDEC 51-3* thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(DVDD = 5V, T_A = 25℃, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
DVDD POR High Threshold	$PORH_{DVDD}$	DVDD rising	4	4.3	4.5	V
DVDD POR Hysteresis	HYS_{DVDD}		--	0.3	--	V
Supply Current	I_{DVDD}	EN = 5V, VID = 0V, PWM no switching	--	5	--	mA
Shutdown Current	I_{DVDD_SHDN}	EN = 0V	--	10	--	uA
Supply Current in PS4	I_{DVDD_PS4}	EN = 5V, PS4 state	--	--	100	uA
VIN Sense						
VINSEN POR High Threshold	$PORH_{VINSEN}$	VINSEN rising	--	5.25	--	V
VINSEN POR Low Threshold	$PORL_{VINSEN}$	VINSEN falling	--	4.5	--	V
VINSEN Input Current	I_{VINSEN}	EN = 5V, VINSEN = 12V	--	25	--	uA
EN Input						
Input Low	V_{IL}		--	--	0.3	V
Input High	V_{IH}		0.8	--	--	V
Pull-Low Resistance	R_{EN_PL}		--	200	--	kΩ
Slew Rate						
Slew Rate Fast	SR_Fast	SetVID_Fast, R_{IREF} = 10kΩ	--	52	--	mV/us
		SetVID_Fast, R_{IREF} = 20kΩ	--	13	--	
Slew Rate Slow	SR_Slow	SetVID_Slow, SVID register 0x2Ah = 02h, R_{IREF} = 10kΩ	--	13	--	mV/us
		SetVID_Slow, SVID register 0x2Ah = 02h, R_{IREF} = 20kΩ	--	3	--	
PWM On-Time Setting						
PWM On-Time	T_{ON}	VINSEN = 12V, VID = 1.8V, Fsw=300kHz	400	500	600	ns
Minimum Off-Time	T_{OFF_MIN}		--	150	--	ns
VR_RDY						
Output Low Voltage	V_{OL}	I_{SINK} = 4mA	--	--	0.2	V
Output Leakage Current	I_L	Pull up to 5V	--	--	1	uA
Error Amplifier						
Trans-Conductance	GM		--	2020	--	uA/V
Gain Bandwidth Product	$G_{BW(EA)}$	Guaranteed by design	--	10	--	MHz
Current Sense Amplifier						
Offset Voltage	$V_{OS(CSA)}$		-1	--	1	mV
Input Bias Current	$I_{BC(CSA)}$	V_{CSPx} = 1.8V, guaranteed by design	-10	--	10	nA
Maximum Sourcing Current	I_{MAXSRC}		100	--	--	uA
Gain Bandwidth Product	$G_{BW(CSA)}$	Guaranteed by design	--	10	--	MHz

Electrical Characteristics

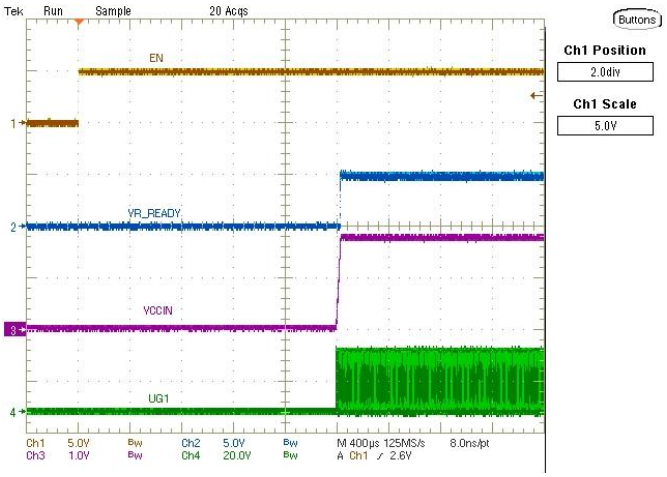
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Current Monitoring IMON						
Current Mirror Accuracy	I_{ACCU_IMON}	I_{IMON} to I_{CSNx} ratio	190	200	210	%
Output Voltage	V_{IMON_00}	SVID register 0x15h readout = 00h	--	1200	--	mV
	V_{IMON_FF}	SVID register 0x15h readout = FFh	--	2700	--	
Current Monitoring for Droop						
Current Mirror Accuracy	I_{ACCU_DROOP}	Set K_{LL} =1, ΔV_{DRP} to ΔV_{IMON} ratio	18	20	22	%
Thermal Monitoring						
TSENSE Source Current	I_{TSENSE}	EN = 5V, R_{IREF} = 10kΩ	114	120	126	uA
ALERT# Assert Threshold	$V_{TSENSE1}$	Temperature ADC result = 103℃	--	365	--	mV
ALERT# De-Assert Threshold	$V_{TSENSE2}$	Temperature ADC result = 100℃	--	384	--	mV
VRHOT# Assert Threshold	$V_{TSENSE3}$	Temperature ADC result = 106℃	--	346	--	mV
VRHOT# De-Assert Threshold	$V_{TSENSE4}$	Temperature ADC result = 103℃	--	365	--	mV
SCLK,SDIO, ALERT#, VRHOT#						
Input Low Voltage (SCLK, SDIO)	V_{IL_SVID}		--	--	0.45	V
Input High Voltage (SCLK, SDIO)	V_{IH_SVID}		0.65	--	--	V
Pull Down Resistance (SDIO, ALERT#, VRHOT#)	R_{ON_SVID}		4	--	13	Ω
Leakage Current (SDIO, ALERT#, VRHOT#)	I_{L_SVID}		-1	--	1	uA
VID Voltage Accuracy						
VID Voltage Accuracy	VID	0.0V < VID ≤ 0.495V	-10	--	10	mV
		0.5V ≤ VID ≤ 0.795V	-8	--	8	mV
		0.795V < VID	-0.5	--	0.5	%
Reference Output						
REFOUT Output Voltage	V_{REFOUT}	-1mA ≤ I_{REFOUT} ≤ 1mA	--	1.2	--	V
System Input Power Monitoring Psys						
A/D Accuracy		PSYS pin voltage = 1.28V, read SVID register 0x1Bh	124	128	132	DEC
SVID Iccmax Register Setting						
A/D Accuracy		PROG2 pin voltage = 0.39V, read SVID register 0x21h	149	153	157	DEC

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PROG						
Source Current	I_{SRC_PROG}	EN = 5V, during function setting period (PROG1,PROG2,PROG3)	--	10	--	uA
		EN = 5V, during function setting period (PROG4)	--	30	--	
MOSFET Gate Driver						
Upper Gate Source	R_{UG_SRC}	V_{BOOT} - V_{PH} = 5V, I_{UG} = -80mA	--	0.7	1.3	Ω
Upper Gate Sink	R_{UG_SNK}	V_{BOOT} - V_{PH} = 5V, I_{UG} = 80mA	--	0.4	0.7	Ω
Lower Gate Source	R_{LG_SRC}	I_{LG} = -80mA	--	0.7	1.3	Ω
Lower Gate Sink	R_{LG_SNK}	I_{LG} = 80mA	--	0.4	0.7	Ω
Dead Time	T_{DT_UG-LG}		--	30	--	ns
	T_{DT_LG-UG}		--	30	--	ns
Bootstrap Diode						
Forward Voltage		Forward bias current = 3.5mA	--	0.33	--	V
Over Voltage Protection						
OVP Threshold	V_{OVP}	Load = 0A, VID =1.8V, V_{FB} - VID	--	400	--	mV
OVP Delay Time	T_{OVP_DELAY}		--	5	--	us
Under Voltage Protection						
UVP Threshold	V_{UVP}	Load = 0A, VID =1.8V, VID - V_{FB}	--	400	--	mV
UVP Delay Time	T_{UVP_DELAY}		--	7.5	--	us
Over Current Protection						
ALERT# Assertion (SVID Iccmax ALERT) Threshold	V_{ALERT}	V_{IMON} - V_{REFOUT}	--	1.5	--	V
Total Current OCP Threshold	V_{OCP}	V_{IMON} - V_{REFOUT}, full phase operation	--	1.95	--	V
Total Current OCP Delay	T_{OCP}		--	2.5	--	us
Per-Phase OC Limit Threshold	$I_{OCLIMIT}$	Measure I_{CSNx} current	--	60	--	uA
Thermal Shutdown Protection						
Thermal Shutdown Threshold	T_{OTP}	Guaranteed by design	--	160	--	℃

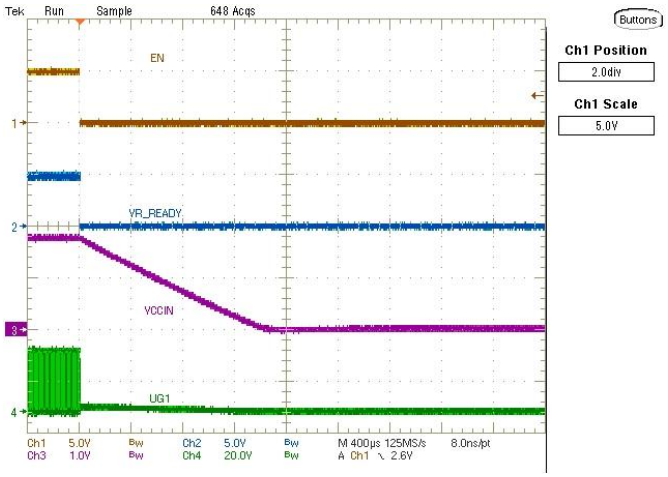
Typical Operation Characteristics

Power On from EN



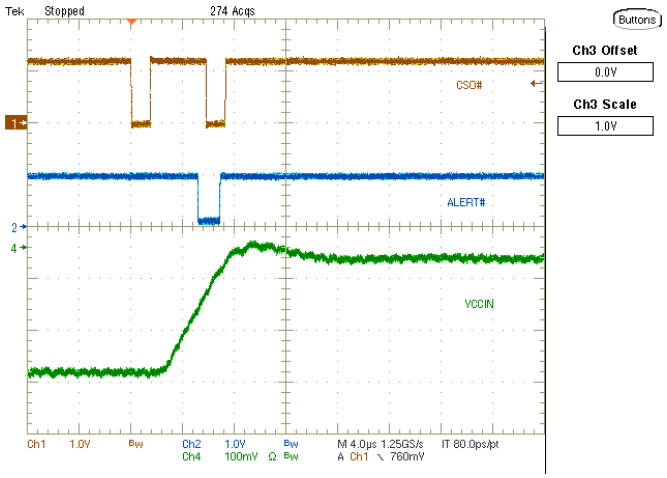
V_{IN}=19V VCCIN=1.8V I_{OUT}=0A

Power Off from EN



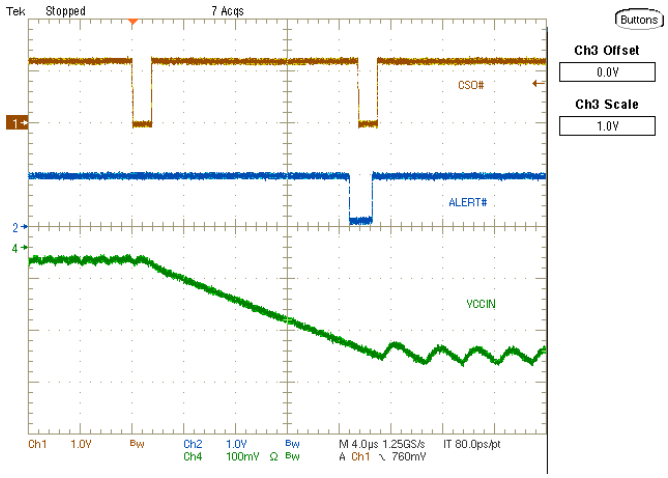
V_{IN}=19V VCCIN=1.8V I_{OUT}=0.75A

VR SetVID_Fast Upward



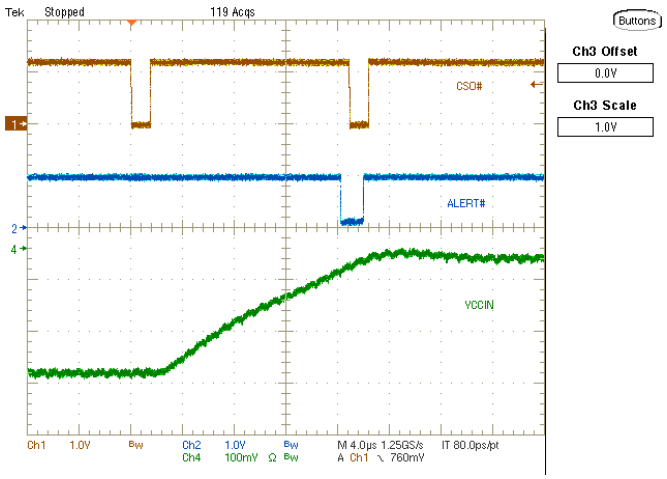
V_{IN}=19V VID=1.6V to 1.8V I_{OUT}=13A

VR SetVID_Decay



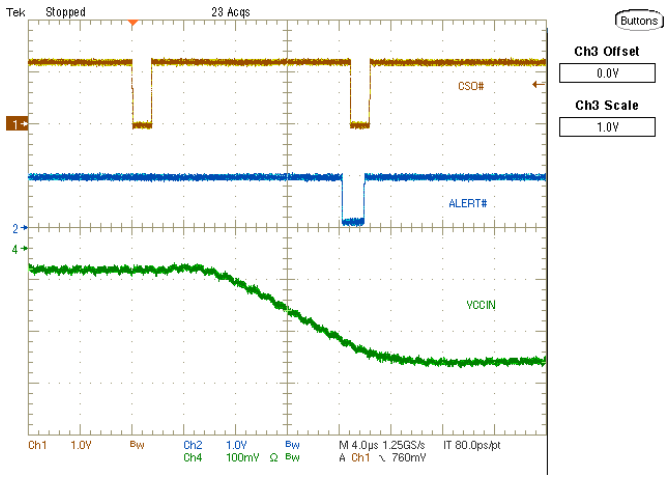
V_{IN}=19V VID=1.8V to 1.6V I_{OUT}=5A

VR SetVID_Slow Upward



V_{IN}=19V VID=1.6V to 1.8V I_{OUT}=13A

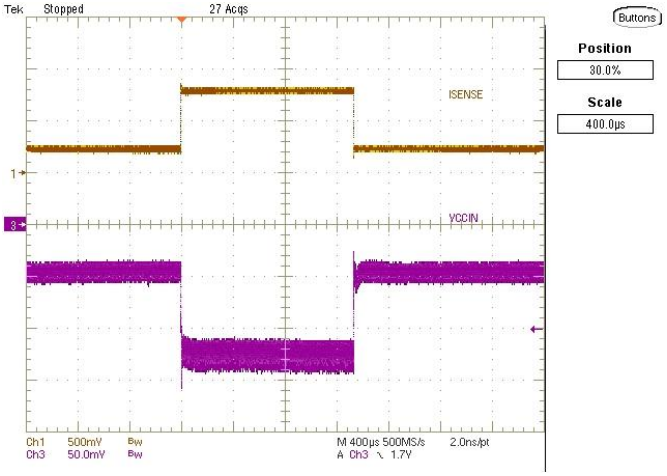
VR SetVID_Slow Downward



V_{IN}=19V VID=1.8V to 1.6V I_{OUT}=13A

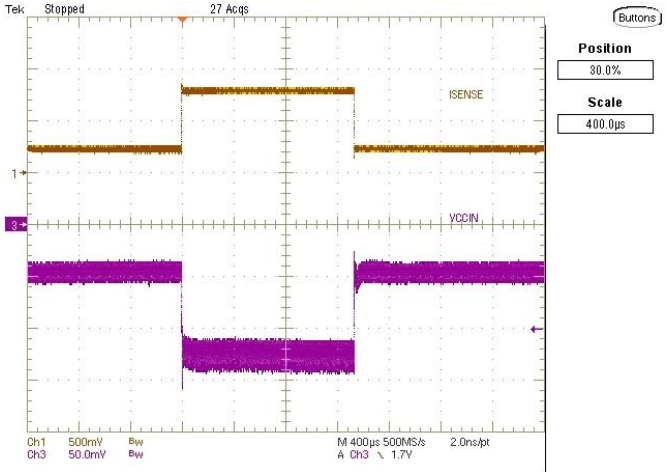
Typical Operation Characteristics

VR Load Transient Response



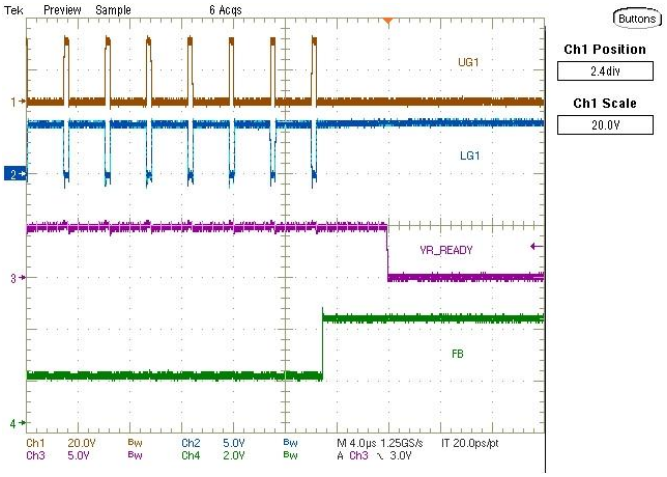
VCCIN=1.8V, I_{OUT}=16A~55A

VR Load Transient Response



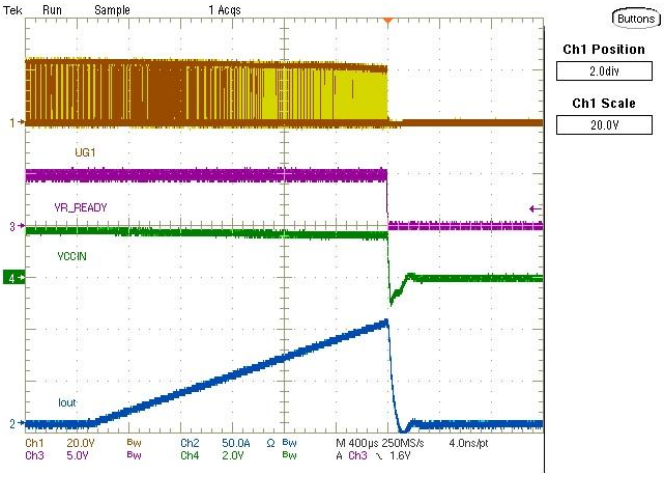
VCCIN=1.8V, I_{OUT}=16A~65A

VR Over Voltage Protection



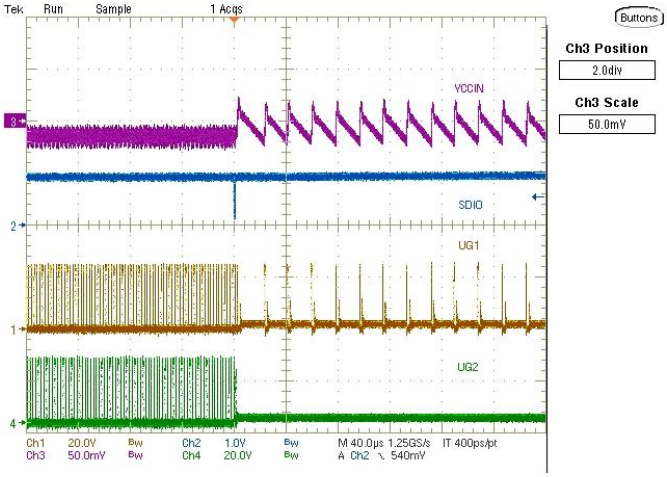
V_{IN}=19V VCCIN=1.8V I_{OUT}=0A

VR Over Current Protection



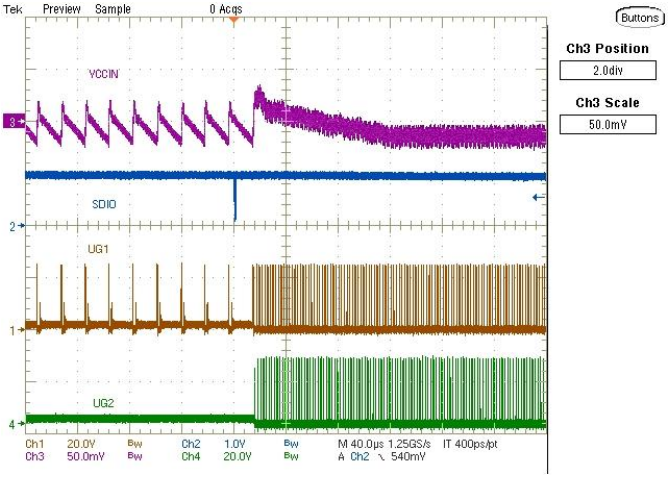
V_{IN}=19V VCCIN=1.8V

VR PSI Transition



V_{IN}=19V, VCCIN=1.8V,PS0 to PS2, I_{OUT}=1A

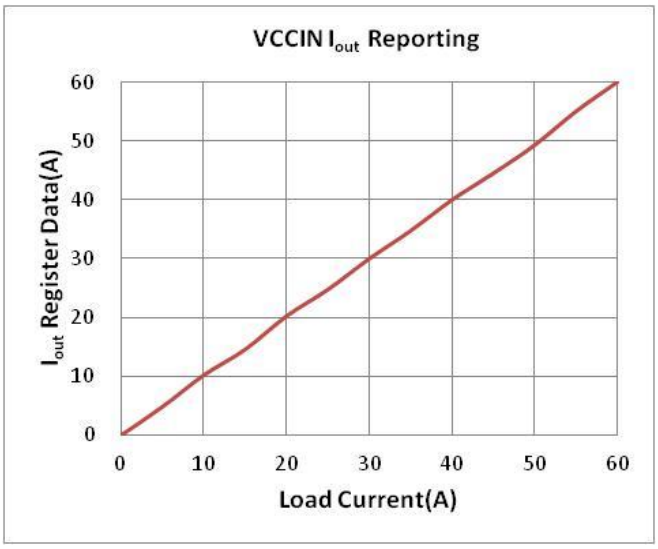
VR PSI Transition



V_{IN}=19V, VCCIN=1.8V,PS2 to PS0, I_{OUT}=1A

Typical Operation Characteristics

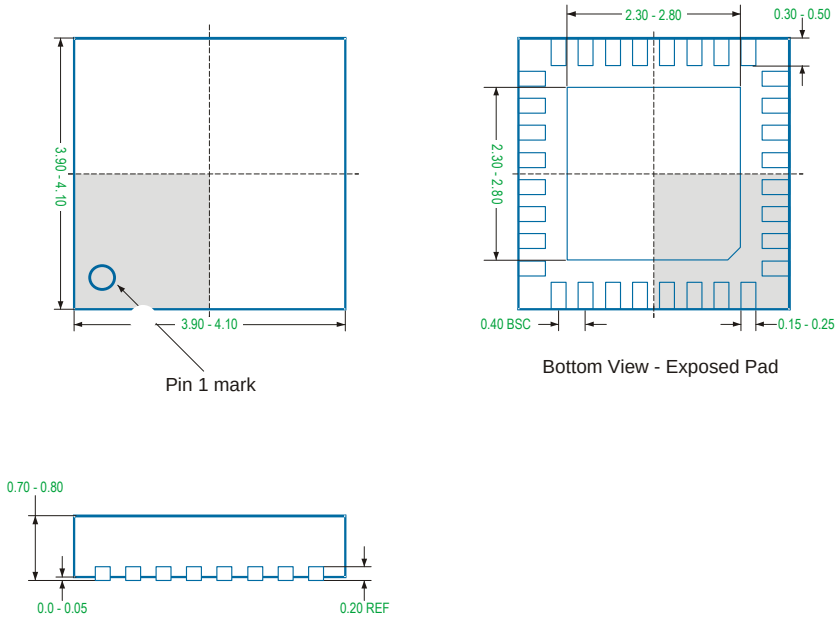
VCCIN I_{OUT} Reporting



uP9523R

Package Information

WQFN4x4-32L



Note

1. Package Outline Unit Description:
   MIN: Minimum dimension specified.
   NOM: Nominal. Provided as a general value.
   MAX: Maximum dimension specified.
   BSC: Basic. Represents theoretical exact dimension or dimension target.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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