3A Ultra Low Dropout Linear Regulator for DDR4 Memory VTT Termination

General Description

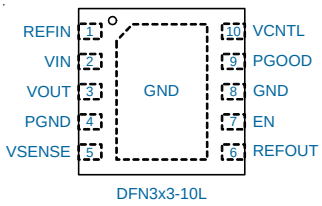
The uP8815 is an ultra low dropout regulator for Double Date Rate (DDR) termination system. It is specifically designed for low input voltage and low external component count systems. The uP8815 is capable of sinking/sourcing up to 3A output current, providing fast load transient and only requires a minimum 3x10uF ceramic output capacitor. The uP8815 supports a remote sensing function and all power requirements for DDR VTT bus termination, DDR4 especially. Other features include an EN signal that can be used to discharge VTT, thermal protection, bi-directional current limit protection. The uP8815 is available in a WDFN3x3-10L package.

Ordering Information

Order Number	Package	Top Marking
uP8815PDDA	WDFN3x3-10L	uP8815P

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration



DFN3x3-10L

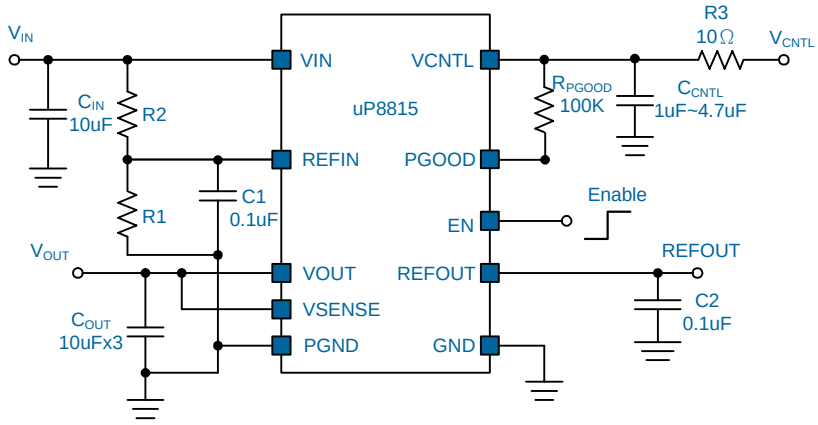
Features

- VIN Input Voltage Range: 1V to 3.6V
- VCNTL Input Voltage: 2.9V to 5.5V
- Power Good to Monitor Output Regulation
- 10mA Source/Sink Buffer Reference
- Output Voltage Remote Sense
- Low External Component
- Discharge MOSFETs at VOUT Shutdown
- Enable Control
- Up to 3A Source/Sink Current
- Support DDR3 and Low Power DDR3/DDR4
- Stable with Pure MLCC as Output Cap
- RoHS Compliant and Halogen Free

Applications

- DDR Memory Termination
- Desktop PCs, Notebook Computers, and Server

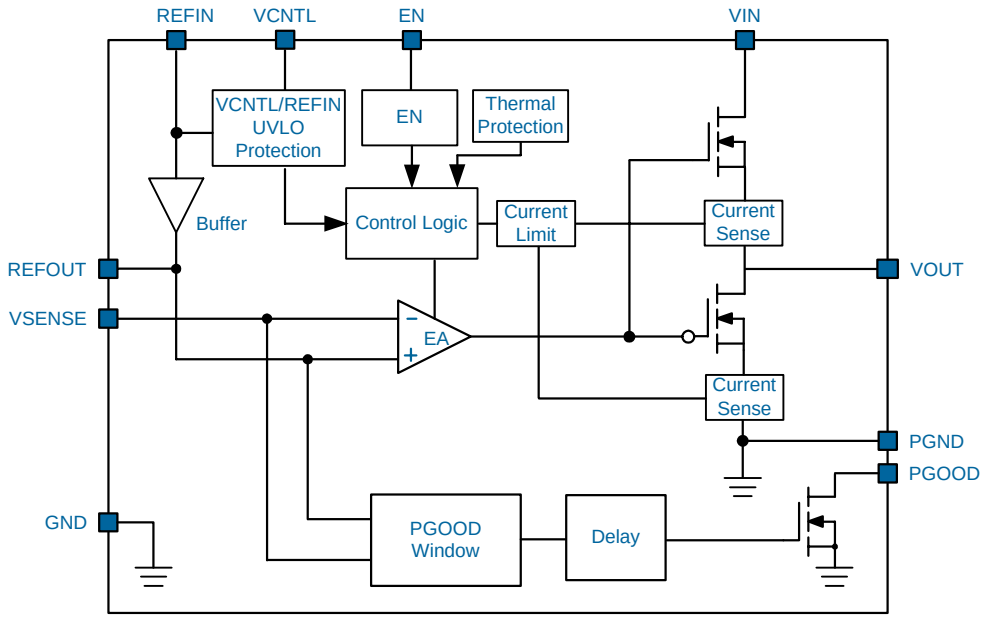
Typical Application Circuit



Functional Pin Description

Pin No.	Name	Pin Function
1	REFIN	**Reference Input.**
2	VIN	**Input Voltage.** This is the drain input to the power device that supplies current to the output pin. Use a ceramic capacitor of at least 10uF on the uP8815 input for stability and improving transient response.
3	VOUT	**Output Voltage.** This pin is the power output of the device. A minimum capacitance of 10uFx3 output capacitor is recommended. And the maximum is 50uF capacitor.
4	PGND	**Power Ground of Regulator.**
5	VSENSE	**Output Voltage Remote Sense for the LDO.**
6	REFOUT	**Reference Output.** Connect a 0.1uF ceramic capacitor from this pin to ground.
7	EN	**EN Input.** If the EN pin is pull high, the IC will enable. If the EN pin is pull low, the IC will disable and then discharge the output voltage through internal resistance.
8 Exposed Pad	GND	**Signal Ground.** All voltage levels are measured with respect to this pin.
9	PGOOD	**Power Good Indication.** This pin is an open-drain output and is set as the high impedance once VOUT enters power good window.
10	VCNTL	**Supply Input for Control Circuit.** This pin provides bias voltage to the control circuitry and driver for the pass transistor. The driving capability of output current is proportioned to the $V_{CNTL.}$ For the device to regulate, the voltage on this pin must be at least 1.5V greater than the output voltage, and no less than V_{CNTL_MIN}

Functional Block Diagram



Source/Sink Current Limit

The uP8815 monitor sourcing and sinking output currents and it has a constant over current limit by reducing Power MOSFET gate voltage. Note that the current limit level will be folded back to be one half when the output voltage is lower than 0.3V. This reduction is a non-latch protection.

Power Good

The PGOOD is an open drain that asserts high with 2 ms (typ) delay time after the VOUT enters power good window which is V_{SENSE} within ±20% of REFOUT. When the V_{SENSE} is out of the PGOOD window, PGOOD de-asserts within 10us (typ).

REFOUT

This buffer generates the DDR VTT reference and is capable of supporting both a sourcing and sinking load of 10mA. REFOUT is independent of the EN pin state.

VCNTL UVLO Protection

The V_{CNTL} UVLO protection through monitor V_{CNTL}. If V_{CNTL} is less than the UVLO threshold voltage, Both V_{OUT} and REFOUT regulators are powered off.

REFIN

The RFFIN has UVLO protection. And It can be set by external equivalent ratio voltage divider connected to the memory supply bus (VDDQ).

EN Control

The uP8815 features an enable pin for enable/disable control of the chip. Pulling V_{EN} lower than 0.3V disables, an internal discharge MOSFET of 18Ω $R_{DS(ON)}$ turns on to pull output voltage to ground. Pulling V_{EN} higher than 1.7V enables the output voltage.

Absolute Maximum Rating

(Note 1)

Control Input Voltage, V_{CNTL}
- DC ---------- -0.3V to +6.5V
- <200ns ---------- -0.3V to +7.0V

Power Input Voltage, V_{IN}
- DC ---------- -0.3V to +6.5V
- <200ns ---------- -0.3V to +7.0V

Other Pins ---------- -0.3V to (V_{CNTL} + 0.3V)
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
- HBM (Human Body Mode) ---------- 2kV
- MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
- WDFN3x3-10L θ_{JA} ---------- 68°C/W
- WDFN3x3-10L θ_{JC} ---------- 6°C/W

Power Dissipation, P_D @ T_A = 25°C
- WDFN3x3-10L ---------- 1.47W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{IN} ---------- +1V to +3.6V
Supply Input Voltage, V_{CNTL} ---------- +2.9V to +5.5V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The case temp location for measuring θ_{JC} is on the top of the package.

Note 5. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(V_{CNTL} = 5V, C_{OUT} = 10uFx3, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VCNTL Supply Input						
VCNTL POR Threshold	$V_{CNTLRTH}$	$V_{CNTLRTH}$ rising	2.5	2.7	2.85	V
VCNTL POR Hysteresis	$V_{CNTLHYS}$	$V_{CNTLRTH}$ falling	--	0.2	--	V
VCNTL Shutdown Current	I_{SD_VCNTL}	V_{EN}=V_{REFIN}= 0V, I_{OUT}=0A	--	65	80	uA
VCNTL Standby Current	I_{SB_VCNTL}	V_{EN}= 0V, V_{REFIN} > 0.4V, I_{OUT}=0A	--	200	400	uA
VCNTL Input Current	I_{VCNTL}	V_{EN}=V_{CNTL}= 5V, I_{OUT}=0A, V_{REFIN} > 0.4V	--	0.7	1	mA
VIN Supply Input						
VIN Supply Current	I_{VIN}	V_{EN}=V_{CNTL}= 5V, I_{OUT}=0A, V_{REFIN} > 0.4V	--	1	50	uA
VIN Shutdown Current	I_{SHDN_VIN}	V_{EN}=V_{REFIN}= 0V, No Load	--	0.1	50	uA
VIN Standby Current	I_{SB_VIN}	V_{EN}= 0V, V_{REFIN} > 0.4V, I_{OUT}=0A	--	--	50	uA
Output Voltage						
Output Voltage	V_{OUT}	V_{IN} = 1.5V, V_{REFIN} = 0.75V; I_{OUT} =0A	0.735	0.75	0.765	V
		V_{IN} = 1.35V, V_{REFIN} = 0.675V; I_{OUT} =0A	0.66	0.675	0.69	
		V_{IN} = 1.2V, V_{REFIN} = 0.6V; I_{OUT} =0A	0.585	0.6	0.615	
VOUT Voltage Offset to REFOUT	V_{OUT_OS}	I_{OUT} = ±2A, V_{IN}=1.5V, V_{REFOUT}=0.75V	-25	--	25	mV
		I_{OUT} = ±2A, V_{IN}=1.35V, V_{REFOUT}=0.675V	-25	--	25	
		I_{OUT} = ±2A, V_{IN} = 1.2V, V_{REFOUT} = 0.6V	-25	--	25	
Load Regulation	ΔV_{LOAD}	-1A < I_{OUT} <1A	-20	--	20	mV
VOUT Discharge Resistance	$R_{DISCHARGE}$	V_{REFIN} = 0V, V_{OUT} = 0.3V, V_{EN} = 0V	--	18	25	Ω
VOUT Source Current Limit	$I_{LIM\_VOUT\_SR}$	V_{OUT} in PGOOD Window	3.5	4.5	5.5	A
VOUT Sink Current Limit	$I_{LIM\_VOUT\_SK}$	V_{OUT} in PGOOD Window	3.5	4.5	5.5	A
REFIN/REFOUT						
REFIN Logic High Threshold	V_{ENH}	REFIN rising to enable the device	360	390	420	mV
REFIN Logic Low Threshold	V_{ENL}	REFIN falling to disable the device	--	20	--	mV
REFIN Input Current	I_{REFIN}	V_{EN} = V_{CNTL}	--	--	1	uA
REFIN Voltage Range	V_{REFIN}		0.5	--	1.8	V
REFOUT Voltage Tolerance to REFIN	V_{TOL_REFOUT}	-10mA <I_{REFOUT} <10mA, V_{REFIN} = 0.75V	-15	--	15	mV
		-10mA <I_{REFOUT} <10mA, V_{REFIN} = 0.675V	-15	--	15	
		-10mA <I_{REFOUT} <10mA, V_{REFIN} = 0.6V	-15	--	15	
REFOUT Source Current Limit	$I_{LIM\_REFOUT\_SR}$	V_{REFOUT} = 0V	10	40	--	mA
REFOUT Sink Current Limit	$I_{LIM\_REFOUT\_SK}$	V_{REFOUT} = V_{REFIN} +1V	10	40	--	mA

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Thermal Protection						
Thermal Shutdown Temperature	T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis	T_{SDH_HYS}		--	30	--	°C
PGOOD						
PGOOD Threshold	V_{TH_PGOOD}	V_{SENSE} lower threshold with respect to REFOUT	-25	-20	-15	%
		V_{SENSE} upper threshold with respect to REFOUT	15	20	25	
		PGOOD Hysteresis	--	5	--	
PGOOD Start-up Delay	$T_{PGDELAY1}$	Start-up rising delay, V_{SENSE} within PGOOD range	--	2	--	ms
Output Low Voltage	V_{LOW_PGOOD}	I_{PGOOD} = 4mA	--	--	0.4	V
PGOOD Falling Delay	$T_{PGDELAY2}$	Falling delay, V_{SENSE} is out of PGOOD range	--	10	--	us
Leakage Current	$I_{LEAKAGE\_PGOOD}$	V_{SENSE} = V_{REFIN} (PGOOD high impedence). V_{PGOOD} = VIN +3.0V	--	--	1	uA
EN Threshold						
EN Input Voltage	V_{EN}		1.7	--	--	V
	V_{SD}		--	--	0.3	V

Application Information

The uP8815 is an ultra low dropout linear regulator specifically designed to provide termination voltage for DDR memory system. Designed with low on-resistance NMOSFETs, this device is capable of sinking/sourcing up to 3A output current. The output voltage is tightly regulated to track reference voltage input with fast to line/load transient.

Supply Voltage for Control Circuit VCNTL

This uP8815 works with dual supplies, a control input for the control circuitry and a power input as low as 1.0V for providing current to output. The control input provides bias current for control circuit and gate voltage for turning on and off the NMOSFETs. It is highly recommended to keep the control input 1.5V higher than the output voltage for optimal performance. The control voltage should be locally bypassed by a minimum 1uF ceramic capacitor plus a 10Ω resistor.

Power Input Capacitor (C_{IN}) and Control Input Capacitor (C_{CNTL})

The VIN pin supplies current to output when the upper MOSFET turns on. The uP8815 is designed to work with minimum 10uF ceramic input capacitor. When work with large output capacitor, the uP8815 may demand large input current during soft start. Make sure the power input is capable of delivering up to 3A.

Table 1 Component Recommended Value

Component	Recommended Value
C_{CNTL}	1uF ~ 4.7uF Ceramic Capacitor
C_{IN}	10uF or greater Ceramic Capacitor

Reference Input

The output voltage is regulated to track the reference input at REFIN pin. The reference input can be obtained from power input by voltage divider or from an independent voltage reference. A ceramic capacitor physically near the IC is required to filter the reference voltage.

Output Voltage and Output Capacitor, C_{OUT}

The uP8815 is designed to work with low ESR ceramic capacitors. Attach three, 10-uF ceramic capacitors in parallel to minimize the effect of equivalent series resistance (ESR) and equivalent series inductance (ESL).

Thermal Consideration

The uP8815 integrates internal thermal limiting function to protect the device from damage during fault conditions. However, continuously keeping the junction near the thermal shutdown temperature may remain possibility to affect device reliability. It is highly recommended to keep the junction temperature below the recommended operation condition 125°Cfor maximum reliability. Power dissipation in the device is calculated as:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{CNTL} \times I_{CNTL}$$

It is adequate to neglect power loss with respective to control circuit V_{CNTL} x I_{CNTL} when considering thermal management in uP8815. This power dissipation is conducted through the package into the ambient environment, and, in the process, the temperature of the die (T_J) rises above ambient. Large power dissipation may cause considerable temperature raise in the regulator in large dropout applications. The geometry of the package and of the printed circuit board (PCB) greatly influence how quickly the heat is transferred to the PCB and away from the chip. The most commonly used thermal metrics for IC packages are thermal resistance from the chip junction to the ambient air surrounding the package (ΔT_{JA}):

$$\theta_{JA} = (T_J - T_A) / P_D$$

θ_{JA} specified in the Thermal Information section is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-5 thermal measurement standard. Given power dissipation P_D, ambient temperature and thermal resistance θ_{JA}, the junction temperature is calculated as:

$$T_J = T_A + \Delta T_{JA} = T_A + P_D \times \theta_{JA}$$

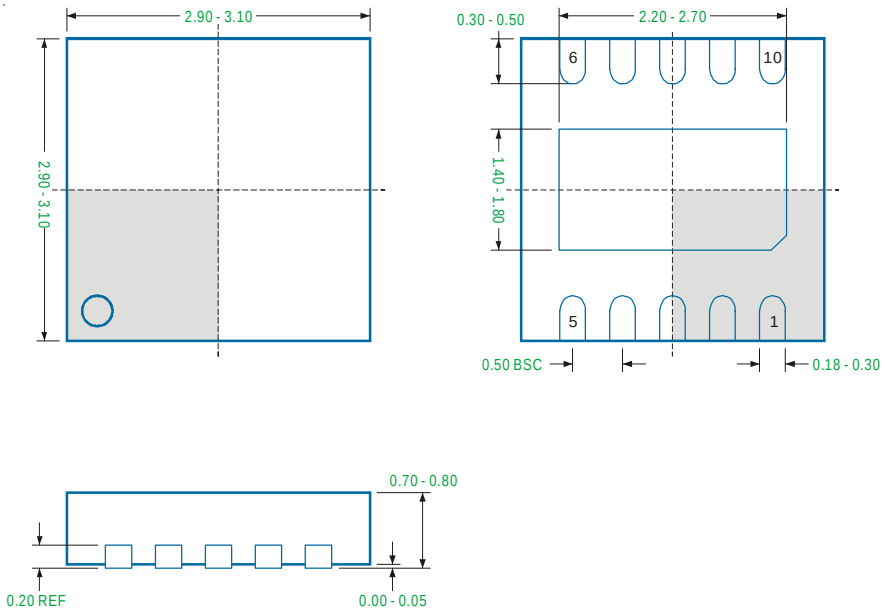
To limit the junction temperature within its maximum rating, the allowable maximum power dissipation is calculated as:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

Package Information

WDFN3x3 - 10L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Important Notice

uPI and its subsidiaries reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

uPI products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment. However, no responsibility is assumed by uPI or its subsidiaries for its use or application of any product or circuit; nor for any infringements of patents or other rights of third parties which may result from its use or application, including but not limited to any consequential or incidental damages. No uPI components are designed, intended or authorized for use in military, aerospace, automotive applications nor in systems for surgical implantation or life-sustaining. No license is granted by implication or otherwise under any patent or patent rights of uPI or its subsidiaries.

uPI Semiconductor Corp.
Headquarter
9F.,No.5, Taiyuan 1st St. Zhubei City,
Hsinchu Taiwan, R.O.C.
TEL : 886.3.560.1666 FAX : 886.3.560.1888

Sales Branch Office
12F-5, No. 408, Ruiguang Rd. Neihu District,
Taipei Taiwan, R.O.C.
TEL : 886.2.8751.2062 FAX : 886.2.8751.5064