

Ultra Low Noise, Fast Response, High PSRR 1A Low Dropout Linear Regulator

General Description

The uP8808 is an ultra low noise, fast response, high power supply rejection ratio (PSRR) low dropout regulator specifically designed to continuously deliver up to 1A output current. Designed with a P-channel MOSFET series pass transistor, the uP8808 yields extremely low dropout voltage (e.g. 240mV at 1A) and maintains very low ground current (200uA).

The uP8808 is designed and optimized to work with low-value, low-cost ceramic capacitors. Only a 10uF ceramic output capacitor is required for stable operation for any load conditions, ideal suitable for portable RF and wireless applications where PCB size are specially concerned. A bypass pin is provided to reduce output noise voltage and improve PSRR to 40dB at 100kHz.

Other features include foldback overcurrent protection, quick soft start, and overtemperature protection. The uP8808 is available in fixed output voltage from 0.8V to 3.3V with 0.1V per step. The device comes in PSOP-8L, SOT23-5L, TSOT223-3L, WDFN3x3-8L and VQFN5x5-24L packages.

Ordering Information

Order Number	Package	Top Marking
uP8808PSU8-XX	PSOP-8L	uP8808PXX
uP8808AMA5-XX	SOT23-5L	SA8AXX
uP8808AJA3-XX	SOT223-3L	SA9AXX
uP8808BJA3-XX		SA9BXX
uP8808AJT3-XX	TSOT223-3L	N66AXX
uP8808BJT3-XX		N66BXX
uP8808PDE8-XX	WDFN3x3-8L	8808PXX
uP8808PQBG-XX	VQFN5x5-24L	uP8808PXX
XX: 00: Adjustable Output Voltage 08: 0.8V; 10: 1.0V; 12: 1.2V; 15: 1.5V; 18: 1.8V; 25: 2.5V; 33: 3.3V, 1L: 1.34V		
Status: In Production: uP8808PSU8-00 Others: Please check the sample/production availability with uPI representatives		

Note:

(1) Please check the sample/production availability with uPI representatives.

(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

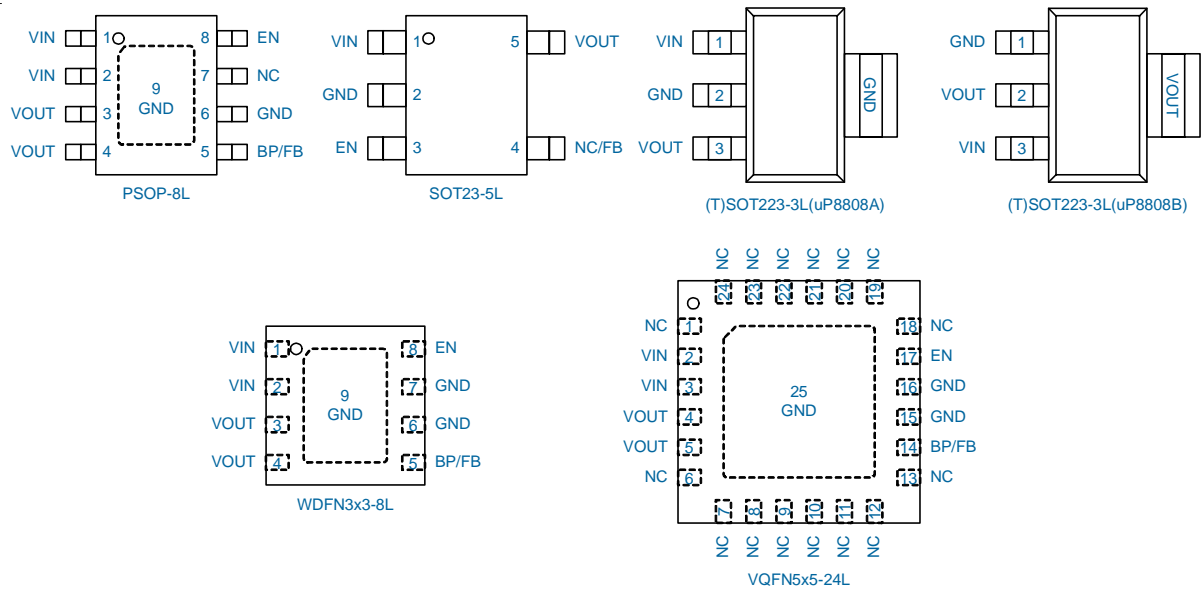
Features

- Wide Input Voltage Range from 2.5 to 5.5V
- Ultra Low Dropout Voltage: 240mV @ 1A
- High Power Supply Rejection Ratio
 - 60dB at 100Hz
 - 40dB at 100kHz
- Ultra Low Output Noise Voltage: 100uV_(RMS)
- Ultra Fast Response to Line/Load Transient
- Low Ground Current: 200uA
- Low Shutdown Current: < 1uA
- Foldback Output Current Limit
- High Output Accuracy
 - 1.5% Initial Accuracy
 - Fixed Output Voltages: 0.8V to 3.3V with 0.1V Per Step
- Over-Temperature Protection
- RoHS Compliant and Halogen Free

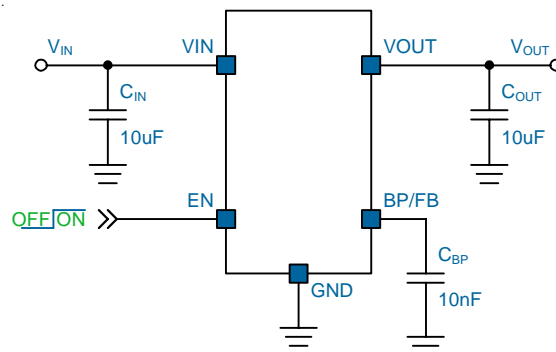
Applications

- Cellular and Cordless Phones
- Bluetooth Portable Radios and Accessories
- Battery-Powered Equipments
- Laptop, Palmtops, Notebook Computers
- Hand-Held Instruments
- PCMCIA Cards
- Portable Information Appliances

Pin Configuration



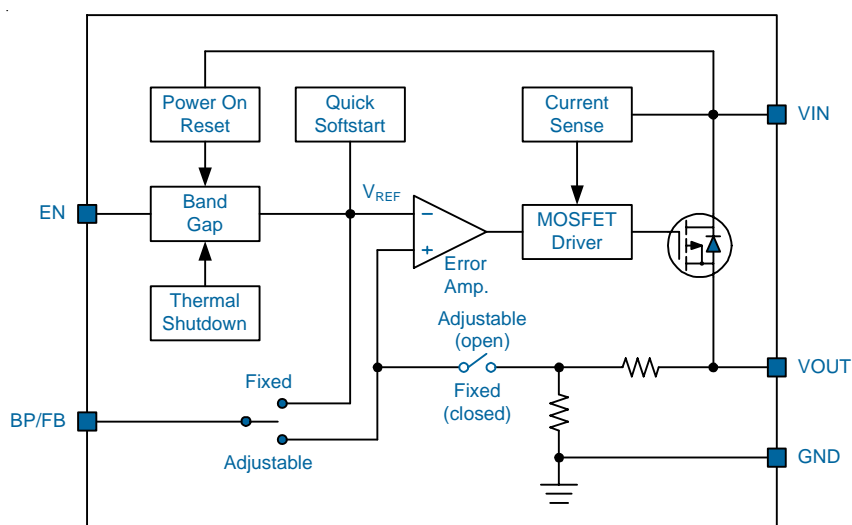
Typical Application Circuit



Functional Pin Description

Name	Pin Function
VIN	Input Voltage. This pin connects to the source of the internal pass transistor that supplies current to the output pin. Bypass VIN to GND with a 10uF ceramic capacitor. Place the decoupling capacitor physically as close as possible to the device.
VOUT	Output Voltage. This pin is power output of the device. Bypass this pin with a 10uF ceramic capacitor.
BP/FB	Bypass Pin for Fixed Voltage Version or Feedback Pin for Variable Voltage Version. Place a minimum 10nF capacitor physically near the bypass pin to reduce the output noise voltage. Connect a voltage divider at the feedback pin to program the output voltage. The feedback pin voltage is regulated to internal 0.8V reference voltage.
GND	Ground.
NC/FB	Not Internally Connected for Fix Voltage Version or Feedback Pin for Variable Voltage Version. Connect a voltage divider at the feedback pin to program the output voltage. The feedback pin voltage is regulated to internal 0.8V reference voltage.
EN	Enable Input. Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. Pull this pin higher than 2V for normal operation.
Exposed Pad	Ground and Thermal Pad. This pin should be well soldered to the PCB with adequate thermal pad for heat dissipation.

Functional Block Diagram



Functional Description

Definitions

Some important terminologies for LDO are specified below.

Dropout Voltage

The input/output Voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 2% below its nominal value, dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Load Regulation

The change in output voltage for a change in load current at constant chip temperature. The measurement is made under conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Maximum Power Dissipation

The maximum total device dissipation for which the regulator will operate within specifications.

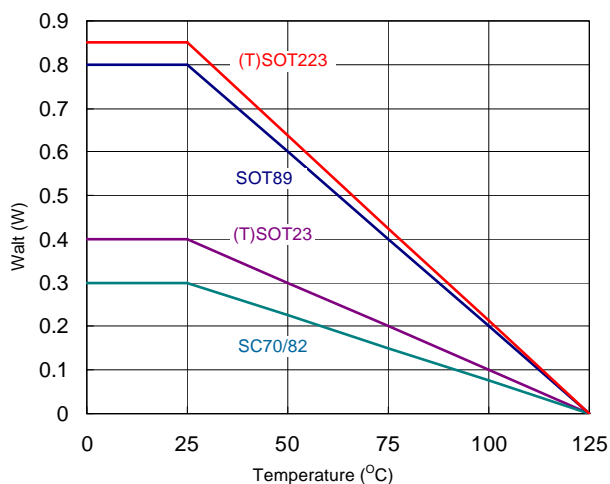


Figure 1. Power Dissipation vs. Temperature

Quiescent Bias Current

Current which is used to operate the regulator chip and is not delivered to the load. The quiescent current I_Q is defined as the supply current used by the regulator itself that does not pass into the load. It typically includes all bias currents required by the LDO and any drive current for the pass transistor.

The uP8808 is an ultra low noise, fast response, high power supply rejection ratio (PSRR) low dropout regulator specifically designed to continuously deliver up to 1A output current for space-limited applications. Designed with a P-channel MOSFET series pass transistor, the uP8808 yields extremely low dropout voltage (e.g. 240mV at 1A) and maintains very low ground current (80uA). A bypass capacitor to the BP/FB pin effectively reduces output noise voltage to 100uV_(RMS) and improves PSRR to 40dB at 100kHz. The uP8808 is designed and optimized to work with low-value, low-cost ceramic capacitors. Only a 10uF ceramic output capacitor is required for stable operation for any load conditions. Other features include foldback overcurrent protection, quick soft start, and overtemperature protection. The uP8808 is available in fixed output voltages from 0.8V to 3.3V with 0.1V increments.

As shown in the *Functional Block Diagram*, the uP8808 consists of a bandgap for reference voltage, error amplifier, P-channel MOSFET pass transistor and internal feedback voltage divider. The 0.8V bandgap reference voltage is connected to the inverting input of error amplifier. The error amplifier compares this reference voltage with the feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the pass-transistor gate is pulled low. This allows more current to pass to the output and increases the output voltage. If the feedback voltage is too high, the pass transistor gate is pulled high, allowing less current to pass to the output. The output voltage is fed back through an internal resistor voltage-divider connected to the VOUT pin. Additional blocks include a current limiter, thermal sensor, and shutdown logic.

Supply Input Power On Reset

The input voltage supplies current to the output voltage and supplies current for control circuit. The input voltage is monitored for power on reset (POR) to ensure the regulator is not enabled until the input voltage is high enough for normal operation. The POR threshold level is typical 2.3V at V_{IN} rising.

Enable/Shutdown

The uP8808 features an active-high enable pin that allows the regulator to be disabled. Forcing the enable pin lower than 0.4V shuts down the regulator and reduces its quiescent current less than 1uA. The voltage reference, error amplifier, gate-driver circuit and pass transistor are disabled in the shutdown state.

Forcing the enable pin higher than 2V enables the output voltage (once the input voltage is higher than its POR threshold level). If the enable function is not needed in a specific application, it may be tied to VIN to keep the regulator in an always on state. The enable pin uses CMOS technology and cannot be left floating, as this may cause an indeterminate state on the output.

Current Limit and Short-Circuit Protection

The uP8808 includes a current limiter that monitors and controls the gate voltage of pass transistor to limit the output current to 2A typically. A short circuit protector monitors the output voltage and asserts output short circuit if V_{OUT} is lower than 40% of V_{NOM} . The current limit level is reduced to 1A and overtemperature threshold level is lowered to 100°C when output short circuit occurs. This limits the junction temperature to a safe level and allows the output to be shorted to ground for an indefinite duration without damaging the device. The output voltage is rebuilt after short circuit is removed.

Overtemperature Protection

The overtemperature protection limits total power dissipation in the uP8808. When the junction temperature exceeds $T_J = 170^\circ\text{C}$, the thermal sensor signals the shutdown logic, turns off the pass transistor and allows the device to cool down. The thermal sensor turns on the pass transistor again after the device's junction temperature drops by 40 °C, resulting in a pulsed output during continuous during continuous thermal-overload conditions. The overtemperature protection is designed to protect the device in the event of a fault condition. For continual operation, do not exceed the recommended temperature of $T_J = 125^\circ\text{C}$ for maximum reliability.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage V_{IN}	-0.3V to +6.5V
Other Pins	-0.3V to ($V_{IN} + 0.3V$)
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	260°C
ESD Rating (Note 2)	
HBM (Human Body Mode)	2kV
MM (Machine Mode)	200V

Thermal Information

Package Thermal Resistance (Note 3)

PSOP8-8L θ_{JA}	50°C/W
PSOP8-8L θ_{JC}	5°C/W
SOT23-5L θ_{JA}	250°C/W
SOT23-5L θ_{JC}	140°C/W
TSOT223-3L θ_{JA}	117°C/W
TSOT223-3L θ_{JC}	15°C/W
WDFN3x3-8L θ_{JA}	68°C/W
WDFN3x3-8L θ_{JC}	6°C/W
VQFN5x5-24L θ_{JA}	36°C/W
VQFN5x5-24L θ_{JC}	3°C/W

Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$

PSOP8-8L	2W
SOT23-5L	0.4W
TSOT223-3L	0.85W
WDFN3x3-8L	1.47W
VQFN5x5-24L	2.78W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range	-40°C to +125°C
Operating Ambient Temperature Range	-40°C to +85°C
Supply Input Voltage, V_{IN}	+2.5V to +5.5V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at $T_A = 25^\circ\text{C}$ on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

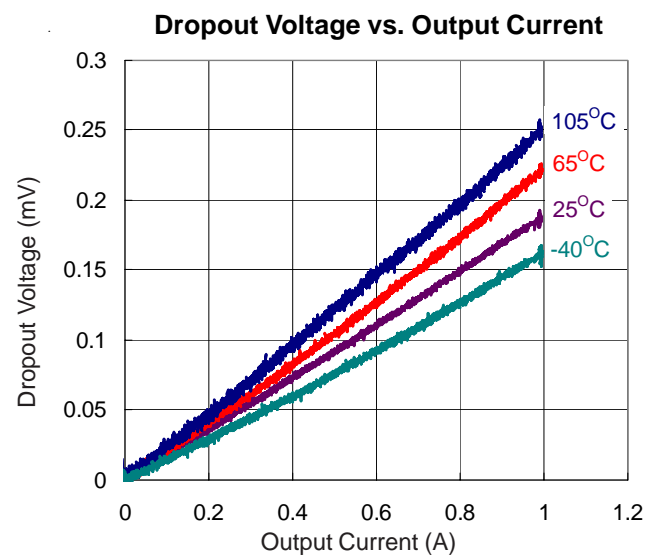
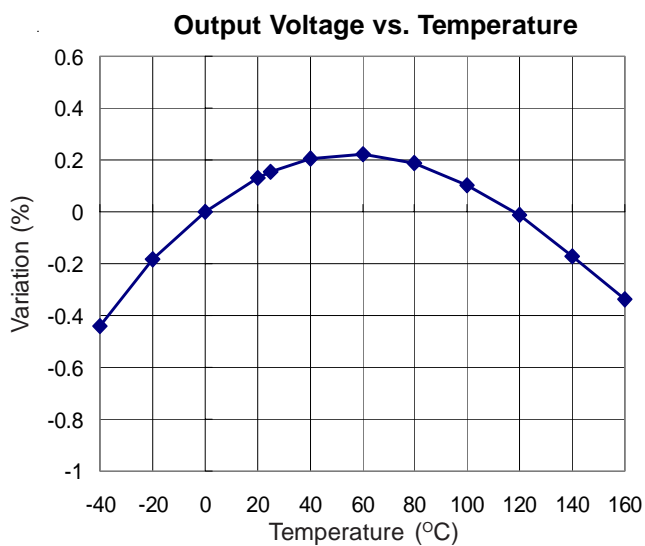
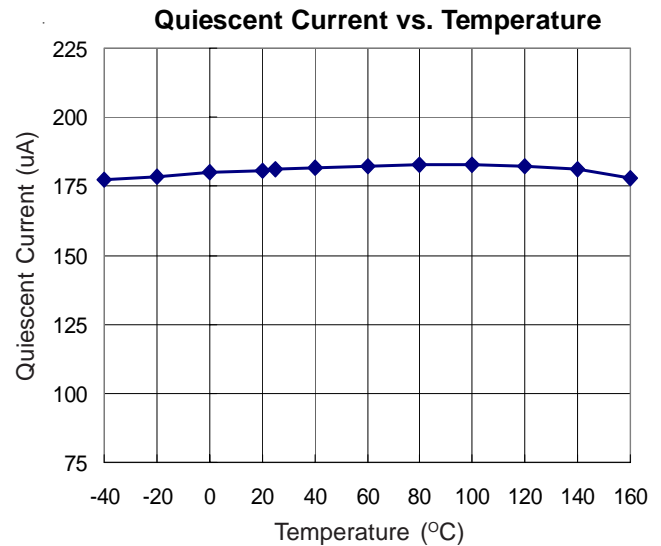
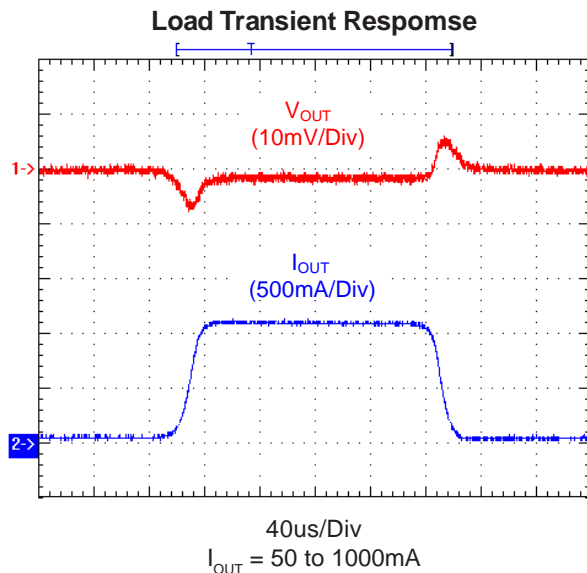
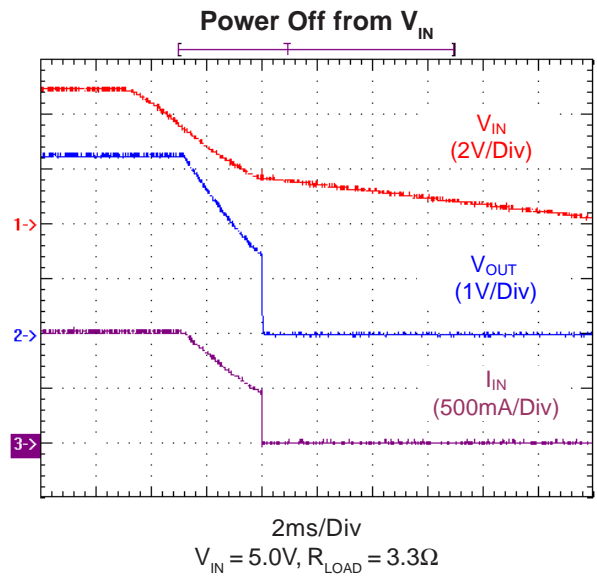
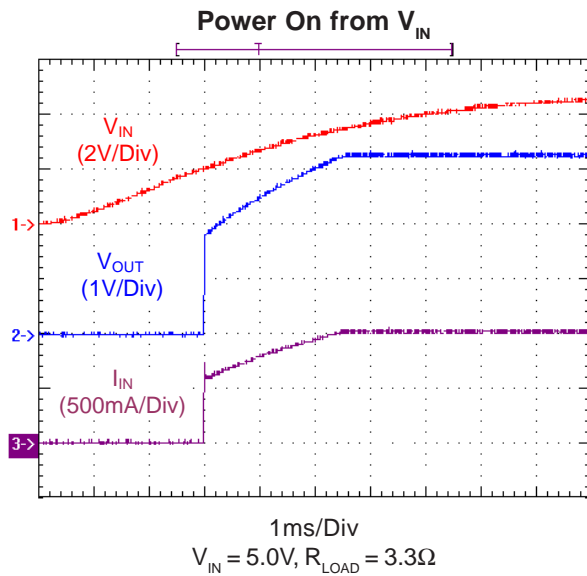
Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

($V_{IN} = 5V$, $T_A = 25^\circ C$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input Voltage						
Supply Input Voltage	V_{IN}		2.5	--	5.5	V
POR Threshold	V_{PORTH}		--	2.0	--	V
POR Hysteresis	V_{PORHYS}		--	0.2	--	V
Quiescent Current	I_Q	$V_{EN} = 5V$, $I_{OUT} = 0mA$	--	200	300	μA
Shutdown Current	I_{SHDN}	$V_{EN} = 0V$	--	0.1	1	μA
Output Voltage						
Output Voltage Accuracy	V_{OUT}	$V_{IN} = V_{NOM} + 1.0V$; $I_{OUT} = 1mA$	-1.5	--	1.5	%
Output Line Regulation	$\Delta V_{OUT(LINE)}$	$2.5V < V_{IN} < 5.5V$, $I_{OUT} = 1mA$	--	0.01	0.1	%/V
Output Load Regulation	$\Delta V_{OUT(LOAD)}$	$1mA < I_{OUT} < 300mA$, $V_{IN} = V_{NOM} + 1.0V$	--	0.4	1	%/A
Output Voltage Noise		10Hz to 1MHz; $C_{OUT} = 3.3\mu F$, ESR < 100m Ω	--	100	--	$\mu V_{(RMS)}$
Power Supply Rejection Ratio	PSRR	$I_{OUT} = 300mA$; 100Hz	--	60	--	dB
		$I_{OUT} = 300mA$; 10kHz	--	50	--	
		$I_{OUT} = 300mA$; 100kHz	--	40	--	
Dropout Voltage	V_{DROP}	$I_{OUT} = 1A$, $2.5V < V_{NOM} < 3.3V$	--	240	360	mV
Feedback Voltage (Adjustable Version)						
BP/FB Pin Voltage	V_{FB}	$V_{NOM} = V_{FB}$, $I_{OUT} = 1mA$	0.784	0.8	0.816	V
BP/FB Pin Bias Current	I_{FB}	$V_{FB} = 0.8V$	--	10	100	nA
Enable						
Enable High Level	V_{EN}		2	--	--	V
Disable Low Level	V_{SD}		--	--	0.4	V
EN Input Current	I_{EN}	$V_{IN} = 5.5V$, $V_{EN} = 5.5V$ or $0V$	-1	--	1	μA
Enable Delay Time	T_{DELAY}	from $V_{EN} > 2V$ to $V_{OUT} > 10\%V_{NOM}$	--	15	--	μs
Output Voltage Ramp Up Time	T_{SS}	from $V_{OUT} = 10\%$ to 90% , $C_{BP} = 1nF \sim 100nF$	--	20	--	μs
Protection						
Current Limit Threshold	I_{LIM}		1.6	2.3	3	A
Short Circuit Current	I_{SHORT}		--	1	--	A
Thermal Shutdown Temperature	T_{SD}	$I_{OUT} = 0mA$, $V_{IN} = V_{EN} = 5.5V$	--	170	--	$^\circ C$
Thermal Shutdown Hysteresis	T_{SDHYS}	$I_{OUT} = 0mA$, $V_{IN} = V_{EN} = 5.5V$	--	40	--	$^\circ C$
Startup Overshoot		$I_{OUT} = 300mA$, $C_{OUT} = 10\mu F$	--	--	0.5	%

Typical Operation Characteristics



Application Information

The uP8808 is specially designed to provide low-noise, high PSRR output voltage without a bypassing capacitor on its reference voltage. However, input and output capacitor should be well considered for optimal performance.

Input Capacitors

The uP8808 requires well-decoupled supply input for optimal performance. A minimum 1uF capacitor is required from input-to-ground to provide stability. Input capacitors greater than 10uF offer superior input line transient response and will assist in maximizing the highest possible power supply ripple rejection ratio (PSRR). Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{IN} . There is no specific capacitor ESR requirement for C_{IN} . However, low-ESR ceramic capacitors provide optimal performance at a minimum of space and are highly recommended due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices. Additional high frequency capacitors, such as small-valued NPO dielectric type capacitors, help filter out high-frequency noise and are good design practice in any RF-based circuit. Place the capacitors physically as close as possible to the device with wide and direct PCB traces.

Output Capacitors and Stability

For proper load voltage regulation and operational stability, a capacitor is required to put between VOUT and GND pins. The uP8808 is designed and optimized to work with low-value, low-cost ceramic capacitors in space saving and performance consideration. Typical output capacitor values for maximum output current conditions is 10uF. Larger capacitors are recommended for applications expecting low output noise and optimum power supply ripple rejection characteristics. Place the capacitors physically as close as possible to the device with wide and direct PCB traces.

X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X7R type capacitors loss capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U or Y5V dielectric capacitors loss their capacitance by 50% and 60% respectively over their operating temperature range. If Y5V or Z5U capacitors are used as output capacitors, the capacitance must be much higher than that of X7R capacitors to ensure the same minimum capacitance over the operating temperature range.

No Load Stability

The uP8808 is designed to maintain output voltage regulation and stability under operational no load conditions. This is important characteristic for CMOS RAM keep-alive applications where the output current may drop to zero.

The uP8808 integrates internal thermal limiting function to protect the device from damage during fault conditions. However, continuously keeping the junction near the thermal shutdown temperature may remain possibility to affect device reliability. It is highly recommended to keep the junction temperature below the recommended operation condition 125°C for maximum reliability. Power dissipation in the device is calculated as:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

This power dissipation is conducted through the package into the ambient environment and in the process, the temperature of the die (T_J) rises above ambient. Large power dissipation may cause considerable temperature raise in the regulator in large dropout applications. The geometry of the package and of the printed circuit board (PCB) greatly influenced how quickly the heat is transferred to the PCB and away from the chip. The most commonly used thermal metrics for IC packages are thermal resistance from the chip junction to the ambient air surrounding the package (θ_{JA}):

$$\theta_{JA} = (T_J - T_A) / P_D$$

θ_{JA} specified in the *Thermal Information* section is measured in the natural convection at $T_A = 25^\circ\text{C}$ on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard. The case point of ~JC is on the exposed pad. Given power dissipation P_D , ambient temperature and thermal resistance θ_{JA} , the junction temperature is calculated as:

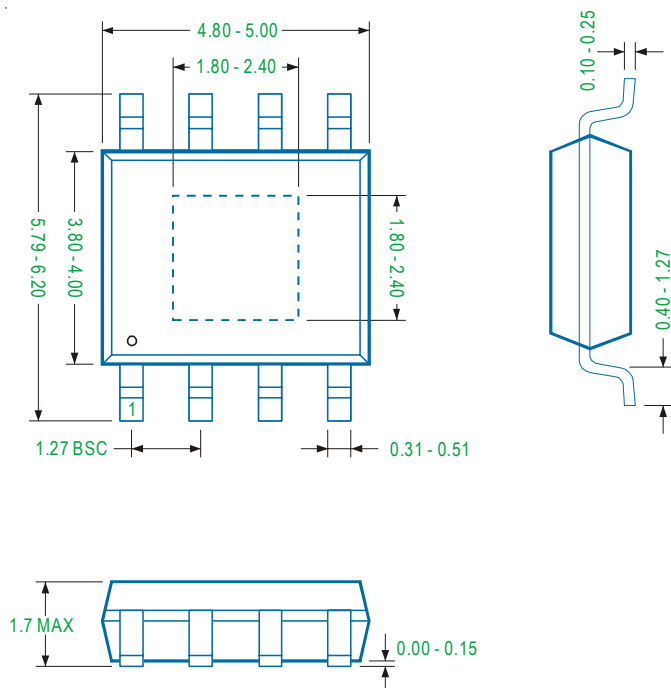
$$T_J = T_A + \Delta T_{JA} = T_A + P_D \times \theta_{JA}$$

To limit the junction temperature within its maximum rating, the allowable maximum power dissipation is calculated as:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

PSOP-8L



Note

1. Package Outline Unit Description:

BSC: Basic. Represents theoretical exact dimension or dimension target

MIN: Minimum dimension specified.

MAX: Maximum dimension specified.

REF: Reference. Represents dimension for reference use only. This value is not a device specification.

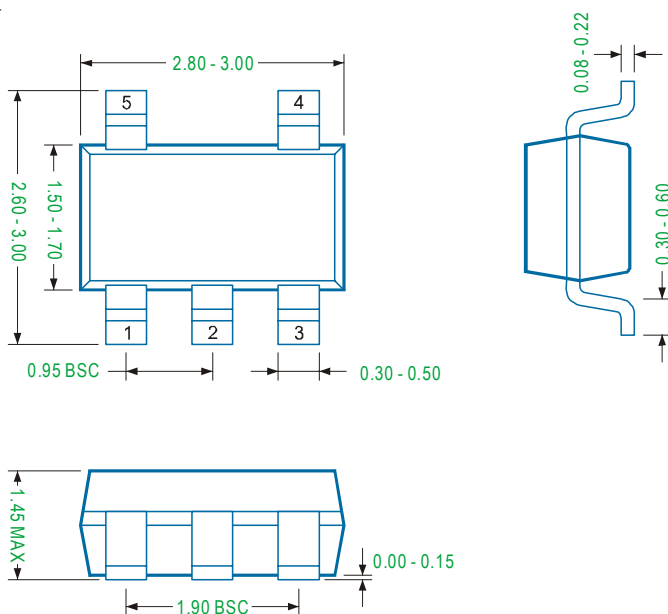
TYP: Typical. Provided as a general value. This value is not a device specification.

2. Dimensions in Millimeters.

3. Drawing not to scale.

4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

SOT23-5L



Note

1. Package Outline Unit Description:

BSC: Basic. Represents theoretical exact dimension or dimension target

MIN: Minimum dimension specified.

MAX: Maximum dimension specified.

REF: Reference. Represents dimension for reference use only. This value is not a device specification.

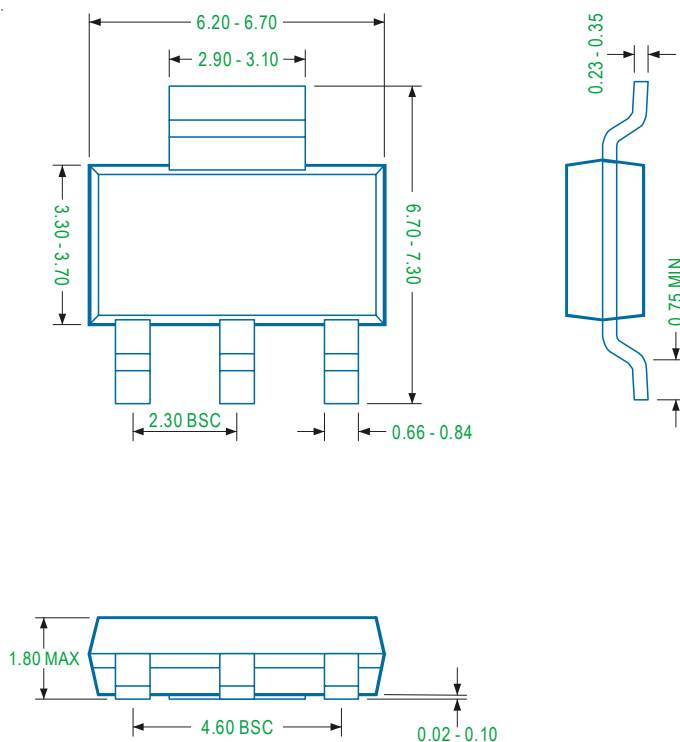
TYP: Typical. Provided as a general value. This value is not a device specification.

2. Dimensions in Millimeters.

3. Drawing not to scale.

4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

SOT223-3L



Note

1. Package Outline Unit Description:

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MIN: Minimum dimension specified.

MAX: Maximum dimension specified.

REF: Reference. Represents dimension for reference use only. This value is not a device specification.

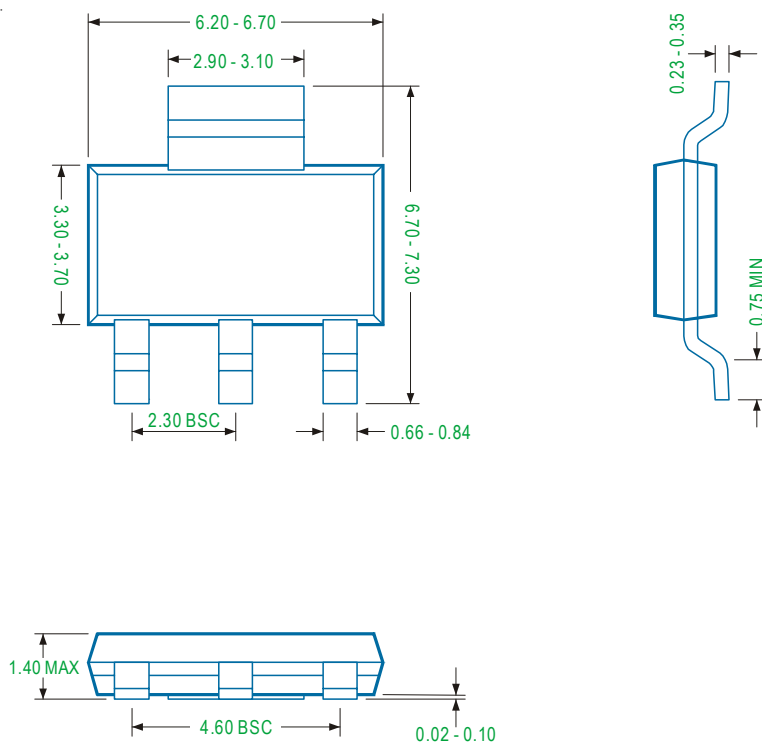
TYP: Typical. Provided as a general value. This value is not a device specification.

2. Dimensions in Millimeters.

3. Drawing not to scale.

4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

TSOT223-3L



Note

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MAX: Maximum dimension specified.

REF: Reference. Represents dimension for reference use only. This value is not a device specification.

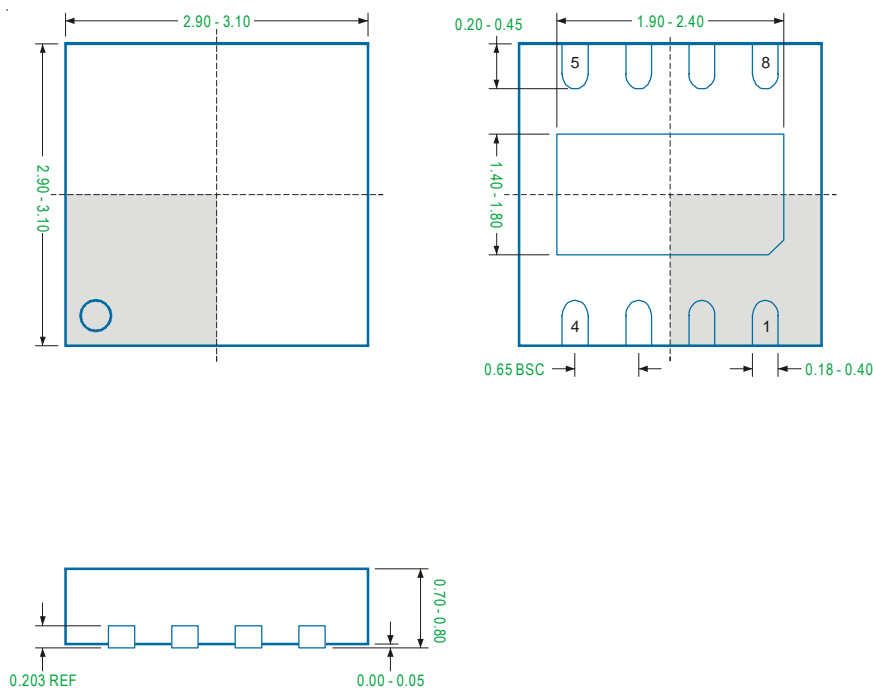
TYP: Typical. Provided as a general value. This value is not a device specification.

2. Dimensions in Millimeters.

3. Drawing not to scale.

4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

WDFN3x3 - 8L



Note

1. Package Outline Unit Description:

BSC: Basic. Represents theoretical exact dimension or dimension target

MIN: Minimum dimension specified.

MAX: Maximum dimension specified.

REF: Reference. Represents dimension for reference use only. This value is not a device specification.

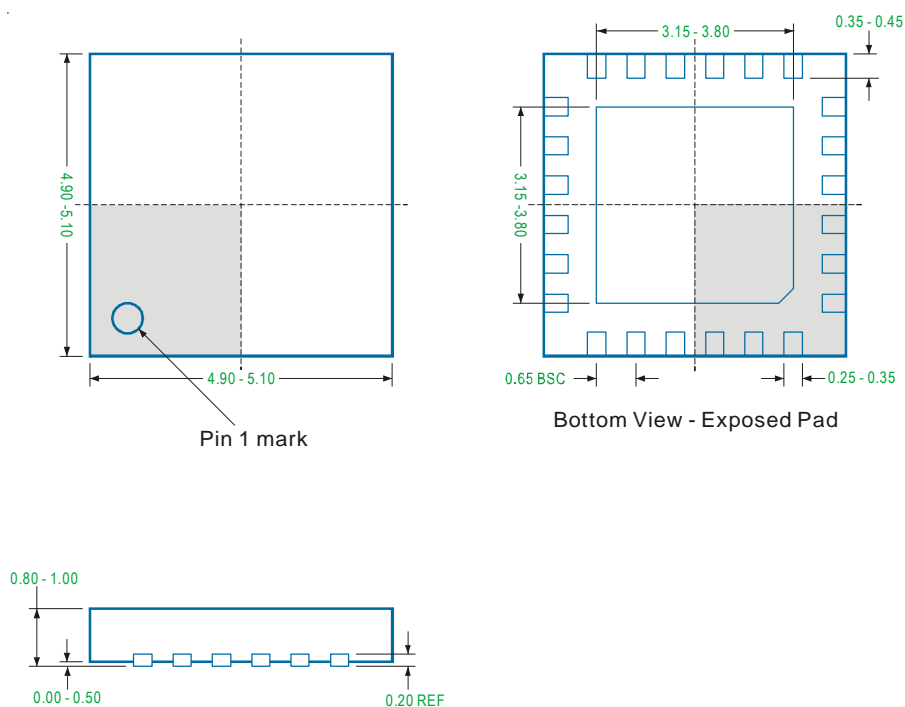
TYP: Typical. Provided as a general value. This value is not a device specification.

2. Dimensions in Millimeters.

3. Drawing not to scale.

4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

VQFN5x5-24L



Note

1. Package Outline Unit Description:

BSC: Basic. Represents theoretical exact dimension or dimension target

MIN: Minimum dimension specified.

MAX: Maximum dimension specified.

REF: Reference. Represents dimension for reference use only. This value is not a device specification.

TYP: Typical. Provided as a general value. This value is not a device specification.

2. Dimensions in Millimeters.

3. Drawing not to scale.

4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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