Ultra Low Noise, Fast Response, High PSRR 300mA Low Dropout Linear Regulator

General Description

The uP8806J is an ultra low noise, fast response, high power supply rejection ratio (PSRR) low dropout regulator specifically designed to continuously deliver up to 300mA output current. Designed with a P-channel MOSFET series pass transistor, the uP8806J yields extremely low dropout voltage (e.g. 300mV at 300mA).

The uP8806J does not require a bypass capacitor, hence achieving the smallest PCB area. This device reduces output voltage noise under 70uV$_{(RMS)}$ and improves PSRR to 40dB at 100kHz.

The uP8806J is designed and optimized to work with low-value, low-cost ceramic capacitors. Only a 1uF ceramic output capacitor is required for stable operation for any load conditions.

Other features include foldback overcurrent protection, quick soft start, and over temperature protection. The uP8806J is available in fixed output voltage from 0.8V to 4.75V with 0.1V per step.

The device comes in UTDFN1x1-4L package.

Ordering Information

Order Number	Package	Top Marking
uP8806JDS4-12	UTDFN1x1-4L	F6
uP8806JDS4-15		F7
uP8806JDS4-18		F8
uP8806JDS4-25		F9
uP8806JDS4-28		FA
uP8806JDS4-30		FB
uP8806JDS4-33		FC
uP8806JDS4-11		FD

Status:
In Production: uP8806JDS4-18, uP8806JDS4-33
Others: Please check the sample/production availability with uPI representatives

Note:
uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

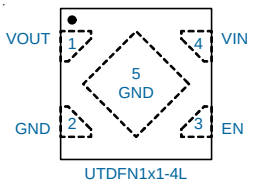
Features

- **Wide Input Voltage Range from 2.4 to 5.5V**
- **Ultra Low Dropout Voltage: 300mV @ 300mA**
- **High Power Supply Rejection Ratio Up to 74dB @1kHz**
- **Ultra Fast Response in Line/Load Transient**
- **Stable with 1uF Ceramic Output Capacitor**
- **Low Shutdown Current: < 1uA**
- **Foldback Output Current Limit**
- **High Output Accuracy**
  - **1.5% Initial Accuracy**
  - **Fixed Output Voltages: 0.8V to 4.75V with 0.1V Per Step**
- **Over Temperature Protection**
- **RoHS Compliant and Halogen Free**

Applications

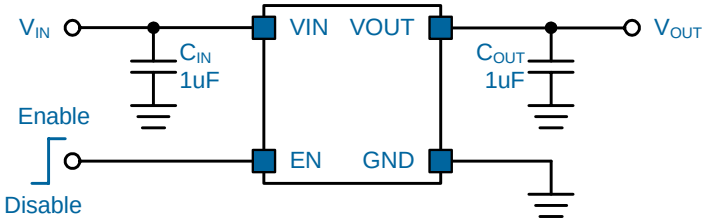
- **Cellular and Cordless Phones**
- **Bluetooth Portable Radios and Accessories**
- **Battery-Powered Equipment**
- **Laptop, Palmtops, Notebook Computers**
- **Hand-Held Devices**
- **PCMCIA Cards**
- **Portable Information Appliances**

Pin Configuration



UTDFN1x1-4L

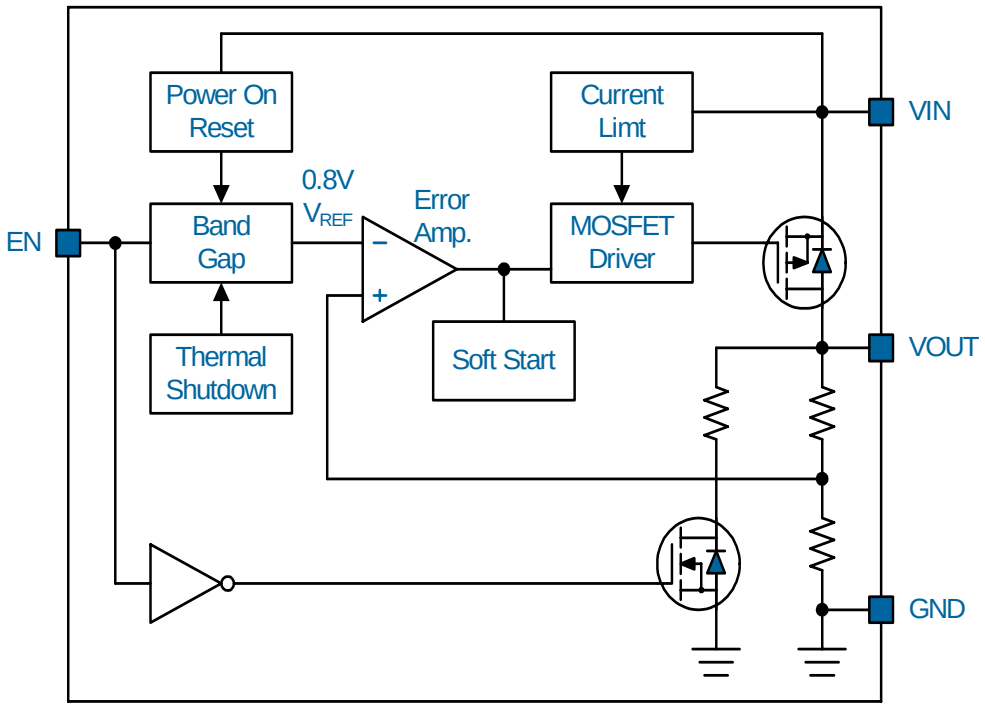
Typical Application Circuit



Functional Pin Description

No.	Pin Name	Pin Function
1	VOUT	**Output Voltage.** This pin is power output of the device. Bypass this pin with a minimum 1uF ceramic capacitor.
2	GND	**Ground.**
3	EN	**Enable Input.** Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. Pull this pin hiegher than 1.4V for for normal operation.
4	VIN	**Input Voltage.** This pin connects to the sourrce of the internal pass transistor that supplies current to the output pin. Bypass VIN to GND with a minimum 1uF ceramic capacitor. Place the decoupling capacitor physically as close as possible to the device.
5	GND	**Ground.** The exposed pad is the mainly path for heat convection and should be well soldered to the PCB for best thermal performance.

Functional Block Diagram



Functional Description

Definitions

Some important terminologies for LDO are specified below.

Dropout Voltage

The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 2% below its nominal value, dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Load Regulation

The change in output voltage for a change in load current at constant chip temperature. The measurement is made under conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Maximum Power Dissipation

The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Bias Current

Current which is used to operate the regulator chip and is not delivered to the load. The quiescent current I_Q is defined as the supply current used by the regulator itself that does not pass into the load. It typically includes all bias currents required by the LDO and any drive current for the pass transistor.The uP8806J is an ultra low noise, fast response, high power supply rejection ratio (PSRR) low dropout regulator specifically designed to continuously deliver up to 300mA output current for space-limited applications. Designed with a P-channel MOSFET series pass transistor, the uP8806J yields extremely low dropout voltage (e.g. 150mV at 150mA and 300mV at 300mA). The uP8806J does not require a bypass capacitor, hence achieving the smallest PCB area. This device reduces output voltage noise under $70uV_{(RMS)}$ and improves PSRR to 40dB at 100kHz. The uP8806J is designed and optimized to work with low-value, low-cost ceramic capacitors. Only a 1uF ceramic output capacitor is required for stable operation for any load conditions. Other features include foldback overcurrent protection, quick soft start, and overtemperature protection. The uP8806J is available in adjustable and fixed output voltages from 0.8V to 4.75V with 0.1V increments.

As shown in the *Functional Block Diagram*, the uP8806J consists of a bandgap for reference voltage, error amplifier, P-channel MOSFET pass transistor and internal feedback voltage divider. The 0.8V bandgap reference voltage is connected to the inverting input of error amplifier. The error amplifier compares this reference voltage with the feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the pass-transistor gate is pulled low. This allows more current to pass to the output and increases the output voltage. If the feedback voltage is too high, the pass transistor gate is pulled high, allowing less current to pass to the output. The output voltage is fed back through an internal resistor voltage-divider connected to the VOUT pin. Additional blocks include a current limiter, thermal sensor, and shutdown logic.

Supply Input Power On Reset

The input voltage supplies current to the output voltage and supplies current for control circuit. The input voltage is monitored for power on reset (POR) to ensure the regulator is not enabled until the input voltage is high enough for normal operation. The POR threshold level is typical 1.9V at V_{IN} rising.

Enable/Shutdown

The uP8806J features an active-high enable pin that allows the regulator to be disabled. Forcing the enable pin lower than 0.4V shuts down the regulator and reduces its quiescent current less than 1uA. The voltage reference, error amplifier, gate-driver circuit and pass transistor are disabled in the shutdown state.

Forcing the enable pin higher than 1.4V enables the output voltage (once the input voltage is higher than its POR threshold level). If the enable function is not needed in a specific application, it may be tied to VIN to keep the regulator in an always on state. The enable pin uses CMOS technology and cannot be left floating, as this may cause an indeterminate state on the output.

Current Limit and Short-Circuit Protection

The uP8806J includes a current limiter that monitors and controls the gate voltage of pass transistor to limit the output current to 300mA typically. A short circuit protector monitors the output voltage and asserts output short circuit if V_{OUT} is lower than 40% of V_{NOM}. The current limiting level is reduced to around 110mA and overtemperature threshold level is lowered to 100°C when output short circuit occurs. This limits the junction temperature to a safe level and allows the output to be shorted to ground for an indefinite duration without damaging the device. The output voltage is rebuilt after short circuit is removed.

Over Temperature Protection

The over temperature protection limits total power dissipation in the uP8806J when the junction temperature exceeds TJ=150°C, the thermal sensor signal the shutdowns logic, turning off the pass transistor and allows the device to cool down. The thermal sensor turns on the pass transistor again after the device's junction temperature drops by 30°C, resulting in a pulsed output during continuous thermal-overload conditions.The overtemperature protection is designed to protect the device in the event of a fault condition. For continual operation, do not exceed the recommended temperature of TJ = 125°C for maximum reliability.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage V_{IN} ---------- -0.3V to +6.0V
Other Pins ---------- -0.3V to (V_{IN} + 0.3V)
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
UTDFN1x1-4L θ_{JA} ---------- 250°C/W
UTDFN1x1-4L θ_{JC} ---------- 67°C/W
Power Dissipation, P_D @ T_A = 25°C
UTDFN1x1-4L ---------- 0.40W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{IN} ---------- +2.4V to +5.5V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

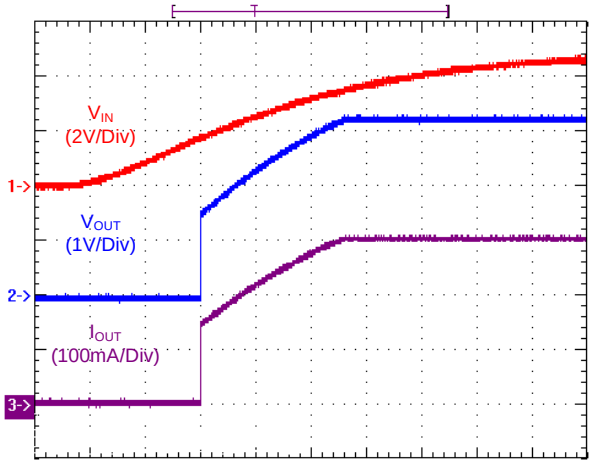
Electrical Characteristics

(V_{IN} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input Voltage						
Supply Input Voltage	V_{IN}		2.4	--	5.5	V
POR Threshold	V_{PORTH}		--	1.9	2.4	V
POR Hysteresis	V_{PORHYS}		--	0.35	--	V
Quiescent Current	I_Q	V_{EN} = 5V, I_{OUT} = 0mA	--	35	50	uA
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	0.1	1	uA
Output Voltage						
Output Voltage Accuracy	V_{OUT}	V_{IN} = V_{NOM} + 1.0V; I_{OUT} = 1mA	-1.5	--	1.5	%V_{NOM}
Output Line Regulation	$\Delta V_{OUT(LINE)}$	2.5V < V_{IN} < 5.5V, I_{OUT} = 1mA	--	0.01	0.1	%/V
Output Load Regulation	$\Delta V_{OUT(LOAD)}$	1mA < I_{OUT} < 300mA, V_{IN} = V_{NOM} + 1.0V	--	0.5	1	%/A
Output Voltage Noise		10Hz to 1MHz; C_{OUT} = 1uF	--	70	--	$uV_{(RMS)}$
Power Supply Rejection Ratio	PSRR	I_{OUT} = 30mA; 1kHz, V_{OUT} = 1.2V	--	74	--	dB
		I_{OUT} = 30mA; 1kHz, V_{OUT} = 3.0V	--	63	--	
		I_{OUT} = 30mA; 100kHz	--	40	--	
		I_{OUT} = 30mA; 1MHz	--	35	--	
Dropout Voltage	V_{DROP}	I_{OUT} = 150mA, 2.5V < V_{NOM} < 3.3V	--	150	--	mV
		I_{OUT} = 300mA, 2.5V < V_{NOM} < 3.3V	--	300	--	mV
Enable						
Enable High Level	V_{EN}		1.1	--	--	V
Disable Low Level	V_{SD}		--	--	0.4	V
EN Input Current	I_{EN}	V_{IN} = 5.5V, V_{EN} = 5.5V or 0V	-1	0	1	uA
Enable Delay Time		from V_{EN} > 2V to V_{OUT} > 10%V_{MON}	10	25	50	us
Output Pull Low Resistance When Turn Off		V_{IN} = 5V, V_{OUT} = 0.5V	300	500	700	Ω
Protection						
Current Limit Threshold	I_{LIM_TH}		330	450	--	mA
Short Circuit Current	I_{LIM_SC}		--	105	--	mA
Thermal Shutdown Temperature	T_{SD}	I_{OUT} = 0mA, V_{IN} = V_{EN} 5.5V	--	150	--	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	I_{OUT} = 0mA, V_{IN} = V_{EN} 5.5V	--	30	--	°C

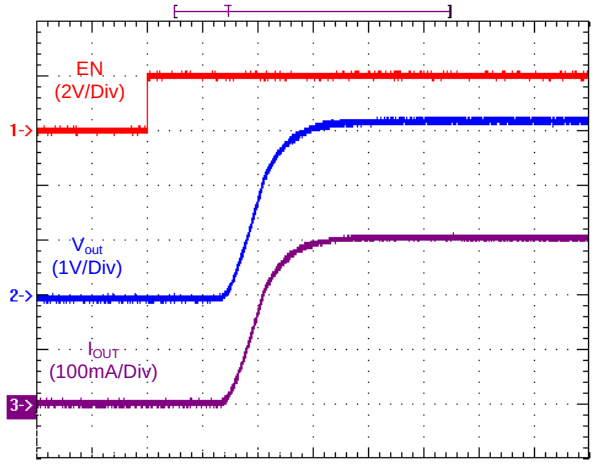
Typical Operation Characteristics

Power On Waveforms



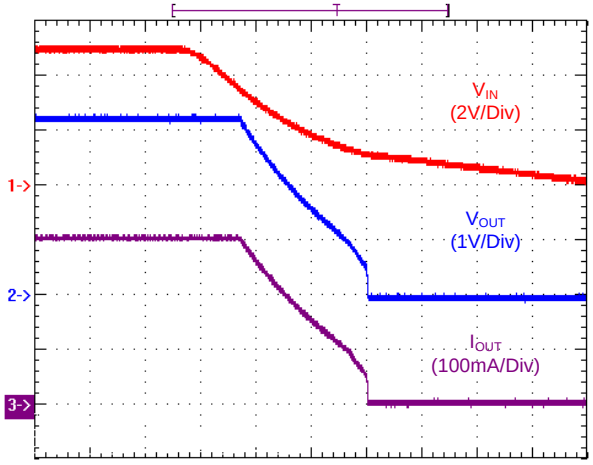
Time: 1ms/Div
$C_{IN} = C_{out} = 1uF$, $V_{out} = 3.3V$, $R_{OUT} = 11\Omega$

Turn On Waveforms



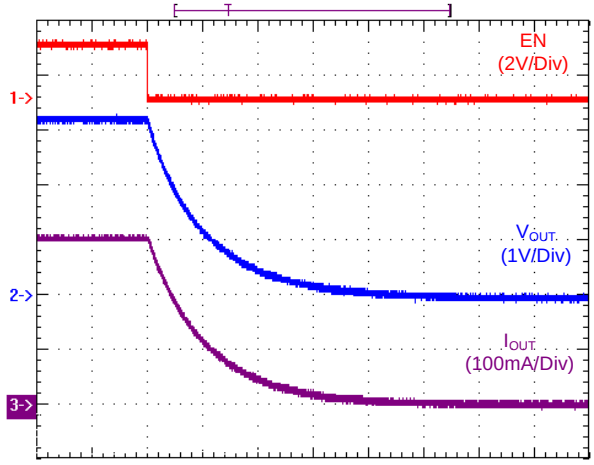
Time: 20us/Div
$C_{IN} = C_{out} = 1uF$, $V_{out} = 3.3V$, $R_{OUT} = 11\Omega$

Power Off Waveforms



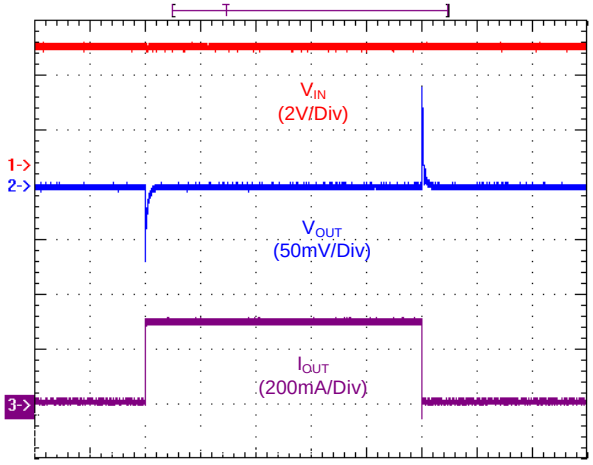
Time: 2ms/Div
$C_{IN} = C_{out} = 1uF$, $V_{out} = 3.3V$, $R_{OUT} = 11\Omega$

Turn Off Waveforms



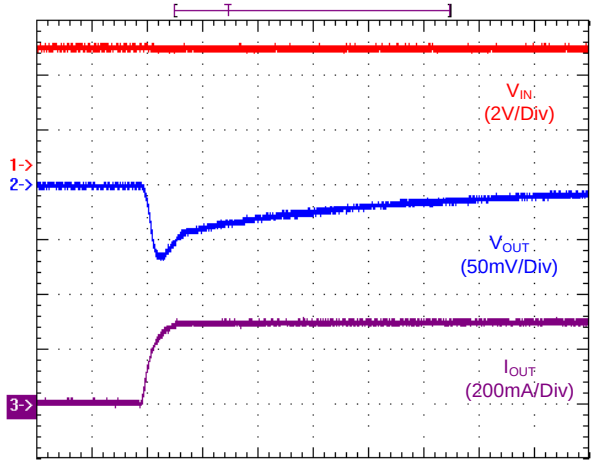
Time: 10us/Div
$C_{IN} = C_{out} = 1uF$, $V_{out} = 3.3V$, $R_{OUT} = 11\Omega$

Load Transient Response



Time: 200us/Div
$C_{IN} = C_{out} = 1uF$, $V_{out} = 3.3V$, $R_{OUT} = 11\Omega$

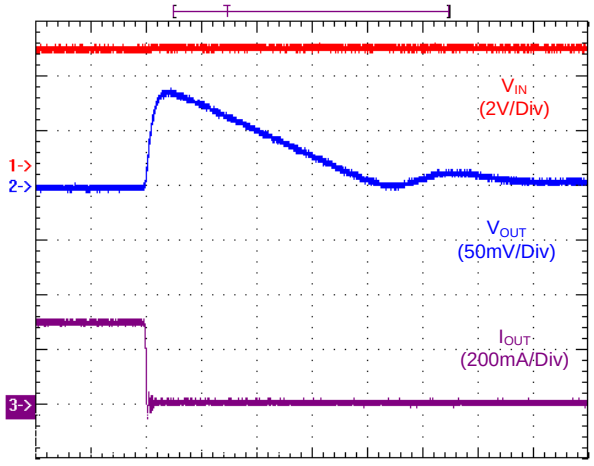
Load Regulation On Response



Time: 2us/Div
$C_{IN} = C_{out} = 1uF$, $V_{out} = 3.3V$, $R_{OUT} = 11\Omega$

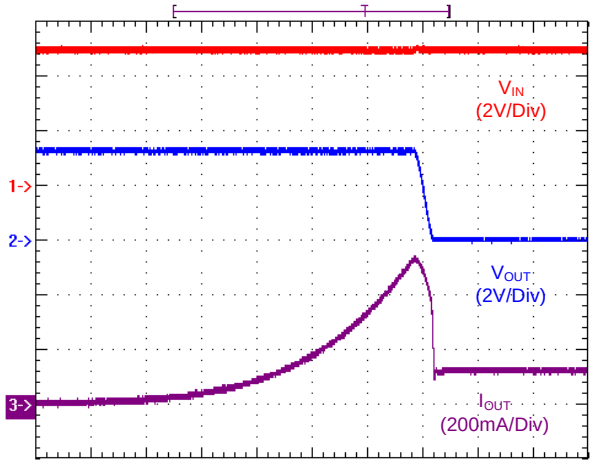
Typical Operation Characteristics

Load Transient Off Response



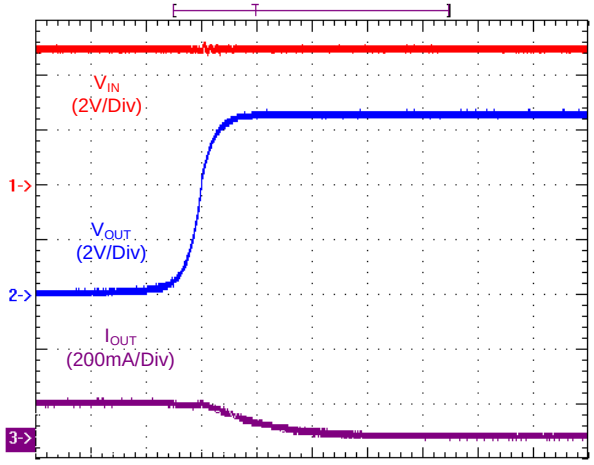
Time: 1ms/Div
$C_{IN} = C_{out} = 1uF$, $V_{out} = 4.3V$, $R_{OUT} = 11\Omega$

Short Circuit Protection



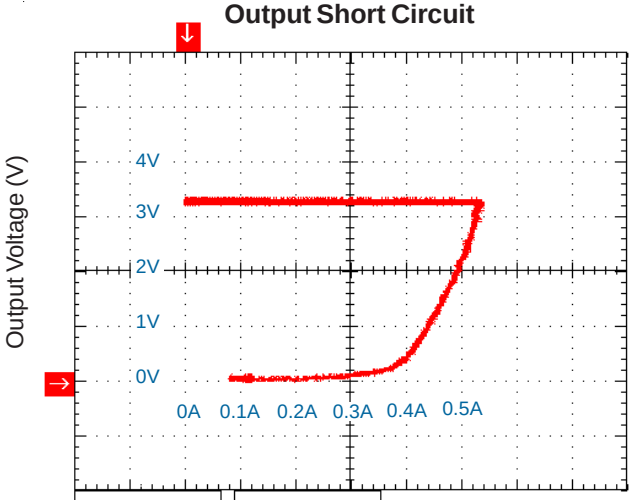
Time: 40us/Div
$C_{IN} = C_{out} = 1uF$, $V_{out} = 3.3V$, $V_{IN} = 4.3V$

Short Circuit Protection Recover



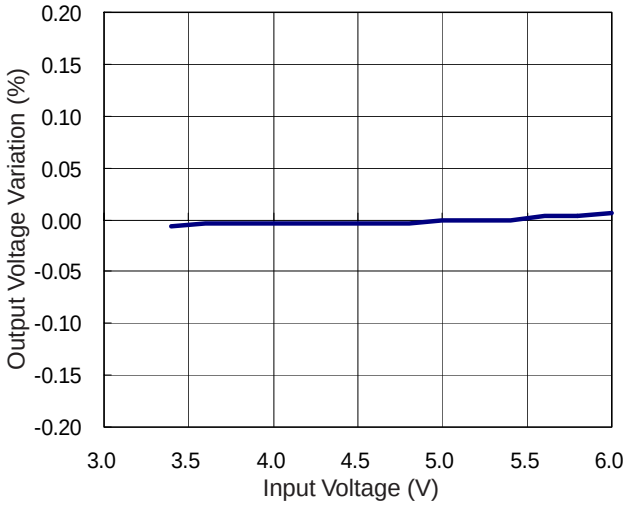
Time: 40us/Div
$C_{IN} = C_{out} = 1uF$, $V_{out} = 3.3V$, $V_{IN} = 4.3V$

Output Short Circuit

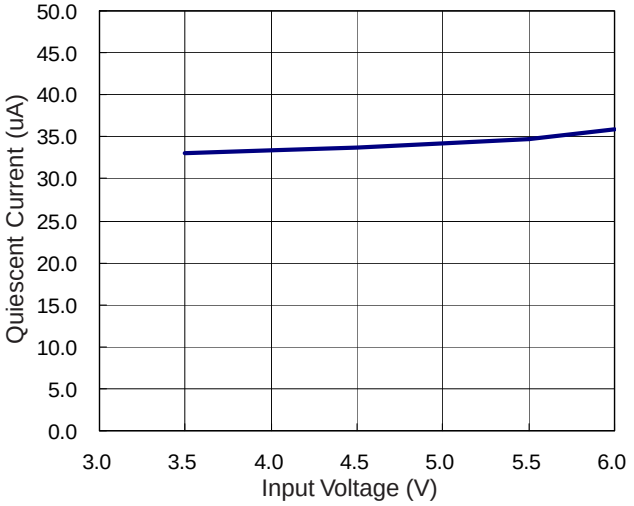


$V_{OUT} = 3.3V$

Output Voltage Line Regulation

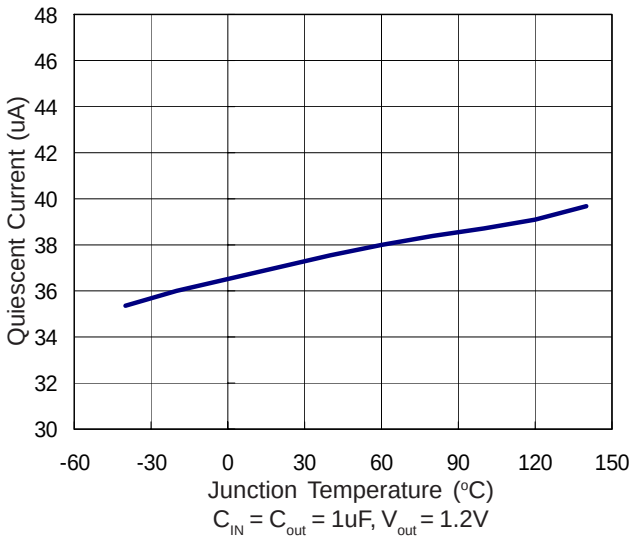


Quiescent Current vs. Input Voltage



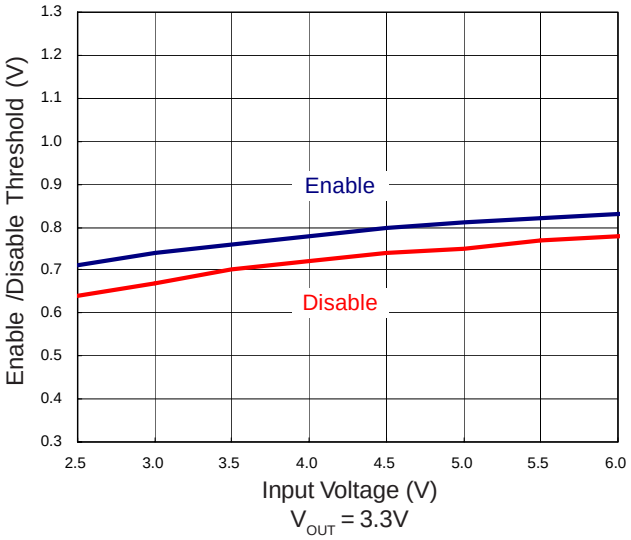
Typical Operation Characteristics

Quiescent Current vs. Temperature



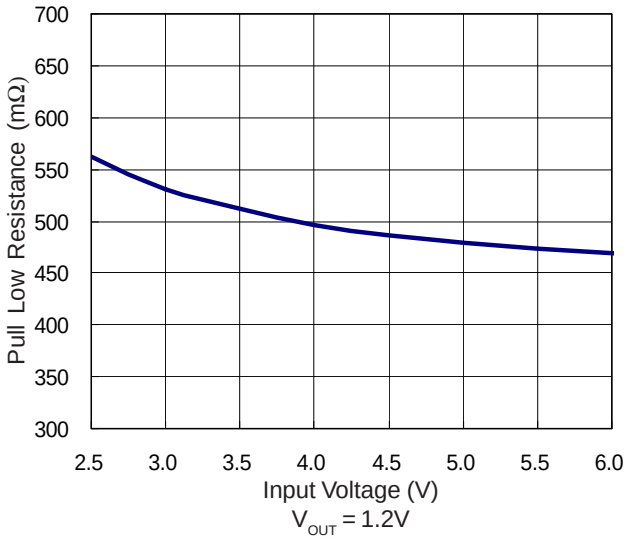
$C_{IN} = C_{out} = 1uF, V_{out} = 1.2V$

Enable /Disable vs. Input Voltage



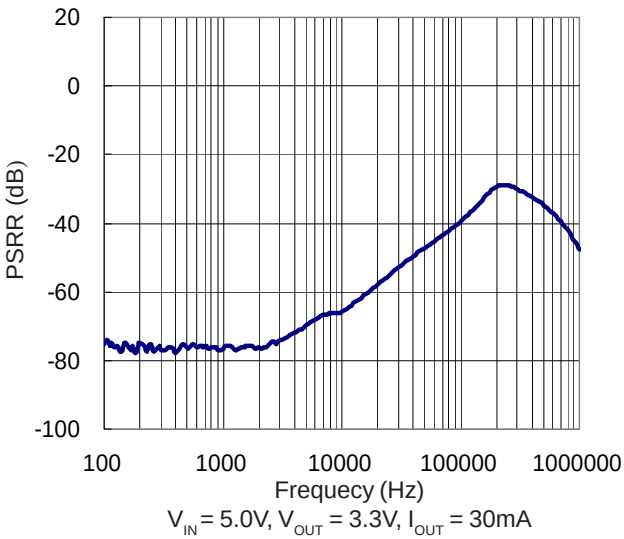
$V_{OUT} = 3.3V$

Output Pull Low Resistance vs. Input Voltage



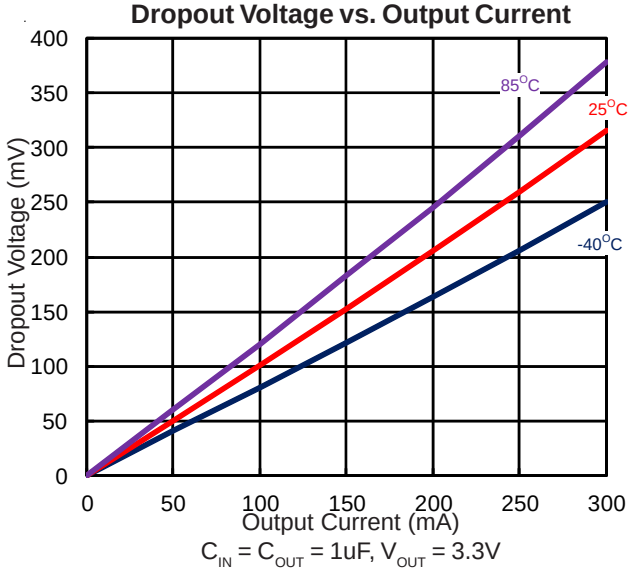
$V_{OUT} = 1.2V$

PSRR



$V_{IN} = 5.0V, V_{OUT} = 3.3V, I_{OUT} = 30mA$

Dropout Voltage vs. Output Current



$C_{IN} = C_{OUT} = 1uF, V_{OUT} = 3.3V$

Application Information

The uP8806J is specially designed to provide low-noise, high PSRR output voltage without a bypassing capacitor on its reference voltage. However, input and output capacitor should be well considered for optimal performance.

Input Capacitors

The uP8806J requires well-decoupled supply input for optimal performance. A minimum 1uF capacitor is required from-input-to-ground to provide stability. Input capacitors greater than 1uF offer superior input line transient response and will assist in maximizing the highest possible power supply ripple rejection ratio (PSRR). Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for CIN. There is no specific capacitor ESR requirement for CIN. However, low-ESR ceramic capacitors provide optimal performance at a minimum of space and are highly recommended due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices. Additional high frequency capacitors, such as small-valued NPO dielectric type capacitors, help filter out high-frequency noise and are good design practice in any RF-based circuit. Place the capacitors physically as close as possible to the device with wide and direct PCB traces.

Output Capacitors and Stability

For proper load voltage regulation and operational stability, a capacitor is required between VOUT and GND pins. The uP8806J is designed and optimized to work with low-value, low-cost ceramic capacitors in space saving and performance consideration. Typical output capacitor values for maximum output current conditions range from 1uF to 10uF. Larger capacitors are recommended for applications expecting low output noise and optimum power supply ripple rejection characteristics. Place the capacitors physically as close as possible to the device with wide and direct PCB traces.

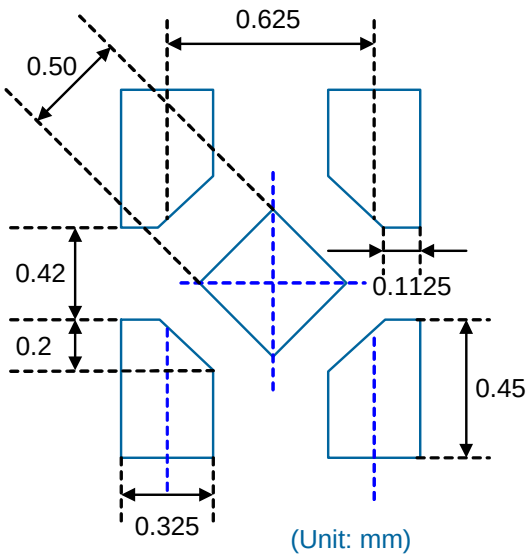
X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X7R type capacitors loss capacitance by 15% over their operating temperature rand and are the most stable type of ceramic capacitors. Z5U or Y5V dielectric capacitors loss their capacitance by 50% and 60% respectively over their operating temperature ranges. If Y5V or Z5U capacitors are used as output capacitors, the capacitance must be much higher than that of X7R capacitors to ensure the same minimum capacitance over the operating temperature range.

ESR of output capacitors should be well considered to ensure stable operation of the device. High ESR capacitors may cause high frequency oscillation.

No Load Stability

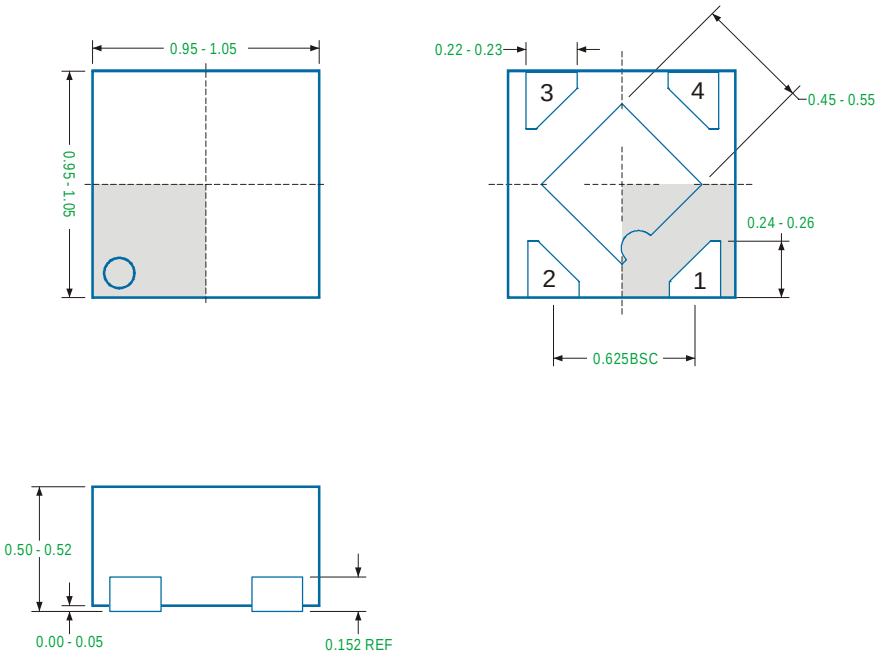
The uP8806J is designed to maintain output voltage regulation and stability under operational no load conditions. This is important characteristic for CMOS RAM keep-alive applications where the output current may drop to zero.

Recommended Footprint



Package Information

UTDFN1x1-4L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.

Important Notice

uPI and its subsidiaries reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

uPI products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment. However, no responsibility is assumed by uPI or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of uPI or its subsidiaries.

uPI Semiconductor Corp.
Headquarter
9F.,No.5, Taiyuan 1st St. Zhubei City,
Hsinchu Taiwan, R.O.C.
TEL : 886.3.560.1666 FAX : 886.3.560.1888

Sales Branch Office
12F-5, No. 408, Ruiguang Rd. Neihu District,
Taipei Taiwan, R.O.C.
TEL : 886.2.8751.2062 FAX : 886.2.8751.5064