Current-Limited, Power Distribution Switches

General Description

The uP7558 is a current limited high-side switch designed for applications where heavy capacitive loads and short-circuits are likely to be met. This device operates with inputs from 2.7V to 5.5V for both 3V and 5V systems. Its low quiescent current and shutdown current(<1uA) conserve battery power in portable.

The power switch is controlled by a logic enable input and driven by an internal charge pump circuit. When the output load exceeds the current-limit threshold or a short is present, the uP7558 asserts over current protection and limits the output current to a safe level by driving the power switch into saturation mode.

The uP7558 features glitch-blank fault flag that is asserted by over current and over temperature. The 8ms glitch-blanking time allows momentary faults to be ignored, thus preventing false alarms to the host system.

Other features include soft-start to limit inrush current during plug-in, thermal shutdown to prevent catastrophic switch failure from high-current loads, under-voltage lockout (UVLO) to ensure that the device remains off unless there is a valid input voltage present, and output reverse voltage to turn off the power switch when the output voltage is higher than input voltage. The uP7558 is available in TSOT23-5L, TSOT23-5L(Flip-Chip), SOT23 - 5L, and MSOP-8L packages.

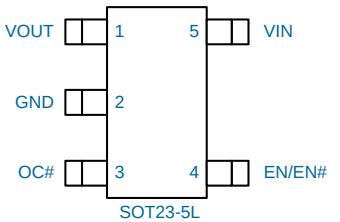
Features

- Compliant to USB Specifications
- Operating Range: 2.7 V to 5.5 V
- 75mΩ (5V Input) High Side MOSFET Switch
- 100uA Typical Quiescent Current
- <1uA Typical Shutdown Current
- Over Current/ Short Circuit Protection
- Output Reverse Voltage/Current Protection
- Fast Short-Circuit Response Time: 2us (typ.)
- Thermal Shutdown Protection
- Deglitched Open Drain Fault Flag
- Slow Turn On and Fast Turn Off
- Enable Active-High or Active-Low
- Pb-Free (RoHS Compliant)
- UL Approved E316940
- TuV R 50254704 Certification
- CB IEC60950-1 Certification

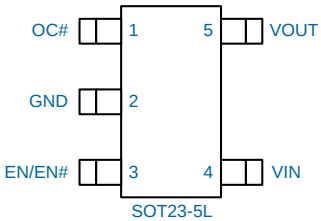
Applications

- Notebook and Desktop PCs
- USB Power Management
- ACPI Power Distribution
- Hot-Plug Power Supplies
- Battery-Powered Equipments
- Battery-Charger Circuits

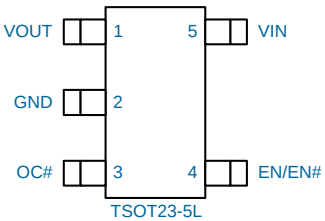
Pin Configuration



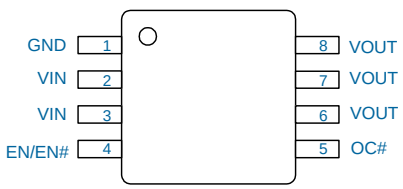
SOT23-5L
(uP7558PMA5/uP7558QMA5)



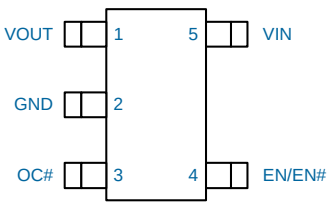
SOT23-5L
(uP7558RMA5/uP7558SMA5)



TSOT23-5L
(uP7558PMT5/uP7558QMT5)



MSOP-8L
(uP7558PRA8/uP7558QRA8)



TSOT23-5L Flip-Chip
(uP7558PMD5/uP7558QMD5)

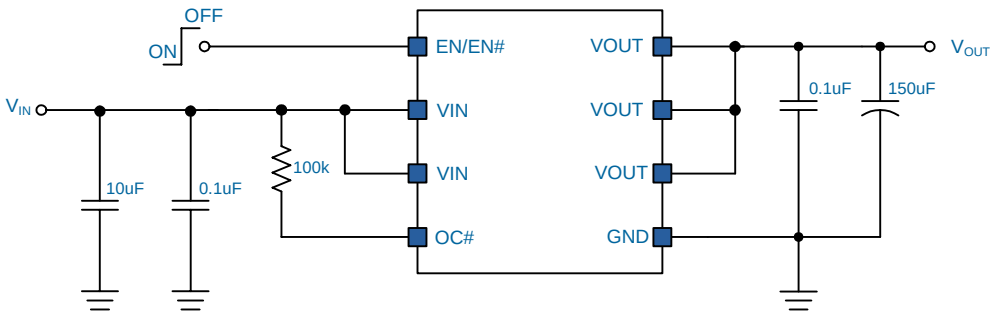
Ordering Information

Order Number	Package	Remark
uP7558PRA8-XX	MSOP-8L	Enable Active High
uP7558QRA8-XX	MSOP-8L	Enable Active Low
uP7558PMA5-XX	SOT23-5L	Enable Active High
uP7558QMA5-XX	SOT23-5L	Enable Active Low
uP7558RMA5-XX	SOT23-5L	Enable Active High
uP7558SMA5-XX	SOT23-5L	Enable Active Low
uP7558PMT5-XX	TSOT23-5L	Enable Active High
uP7558QMT5-XX	TSOT23-5L	Enable Active Low
uP7558PMD5-XX	TSOT23-5L (Flip-Chip)	Enable Active High
uP7558QMD5-XX	TSOT23-5L (Flip-Chip)	Enable Active Low

Code XX	Typical Current Limit (A)	Typical Short Circuit Current (A)
05	0.8	0.5
10	1.5	0.9
15	2.1	1.0
20	2.5	1.5
25	3.3	2.0
30	4.3	2.6

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

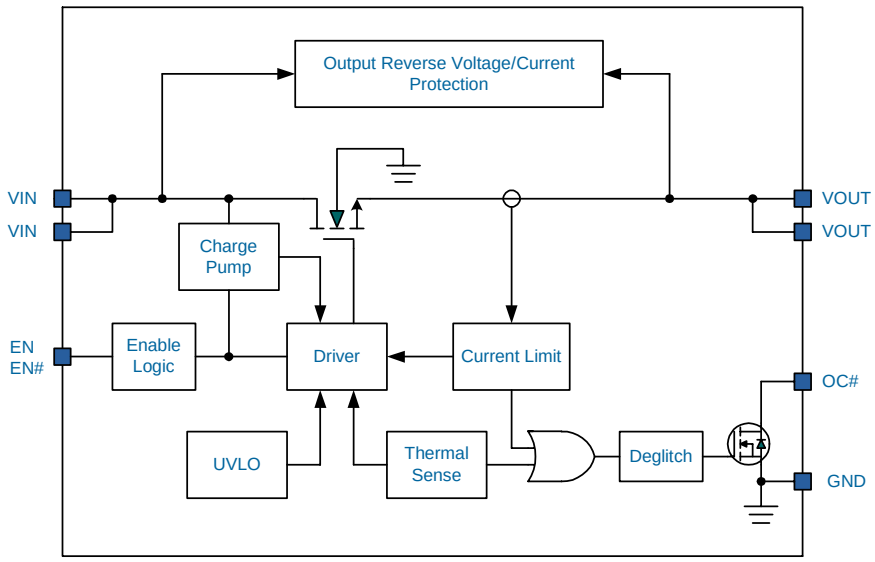
Typical Application Circuit



Functional Pin Description

Pin Name	Pin Function
OC#	**Fault Flag.** This is an active-low, open-drain fault flag output for the power switch. A 8ms deglitch on both the rising and falling edges avoids false triggering at startup and during transients.
VOUT	**Output Voltage.** This pins is output from N-Channel MOSFET Source. Bypass this pin with a minimum 22uF capacitor to ground.
GND	**Ground.**
EN/EN#	**Enable Input.** This is the enable input to turn on/off the power switch.
VIN	**Supply Input.** This is the input pin to N-Channel MOSFET Drain and supply to control circuit. Bypass this pin with a 10uF capacitor to ground.

Functional Block Diagram



Functional Description

Power Switch

The power switch is an N-channel MOSFET with a low on-state resistance. Configured as a high-side switch, the power switch prevents current flow from VOUT to VIN and VIN to VOUT when disabled. The power switch is controlled by a logic enable input and driven by an internal charge pump circuit. When the output load exceeds the current-limit threshold or a short is present, the uP7558 asserts over current protection and limits the output current to a safe level by driving the power switch into saturation mode.

Charge Pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltage.

Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

Chip Enable

Refer to Ordering Information,the uP7558 has active high (EN) or active low (EN#).The EN pin receives a TTL or CMOS compatible input to enable/disable the uP7558 Logic low disables the power switch, charge pump, gate driver and other circuitry and reduces the supply current down to less than 1uA.Logic high restores bias to the drive and control circuits and turns the switch on.

The EN# pin receives a TTL or CMOS compatible input to enable/disable the uP7558. Logic high disables the power switch, charge pump, gate driver and other circuitry and reduces the supply current down to less than 1uA. Logic low restores bias to the drive and control circuits and turns the switch on.

Soft Start

The uP7558 features soft start function to eliminate the inrush current into downstream and voltage droop of upstream when hot-plug-in with capacitive loads. The soft start interval is 0.9ms typically. The uP7558 current limit function may be active during the plug-in of extreme large capacitive load. The fault flag is masked during the softstart interval.

Under Voltage Lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2.2V, a control signal turns off the power switch.

Over Current Limit

The uP7558 continuous monitors the output current for over current protection to protect the system power, the power switch, and the load from damage during output short circuit or soft start interval. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

Fault Flag

The uP7558 asserts fault condition and pulls low OC# when over current, over temperature condition is encountered. The output remains asserted until the over current and over temperature condition is removed. A 8ms deglitch on both the rising and falling edges avoids false triggering at startup and during transients. If an over temperature shutdown or over current occurs,the OC# is asserted instantaneously.

Over Temperature Protection

The uP7558 continuously monitor the operating temperature of the power switch for over temperature protection. The uP7558 asserts over temperature and turns off the power switch to prevent the device from damage if the junction temperature rises to approximately 135^{O}C due over current or short-circuit conditions. Hysteresis is built into the thermal sense, the switch will not turns back on until the device has cooled approximately 20 degrees. The open-drain false reporting output (OC#) is asserted (active low) when an over temperature shutdown or over current occurs.

Output Voltage Discharge When Disabled

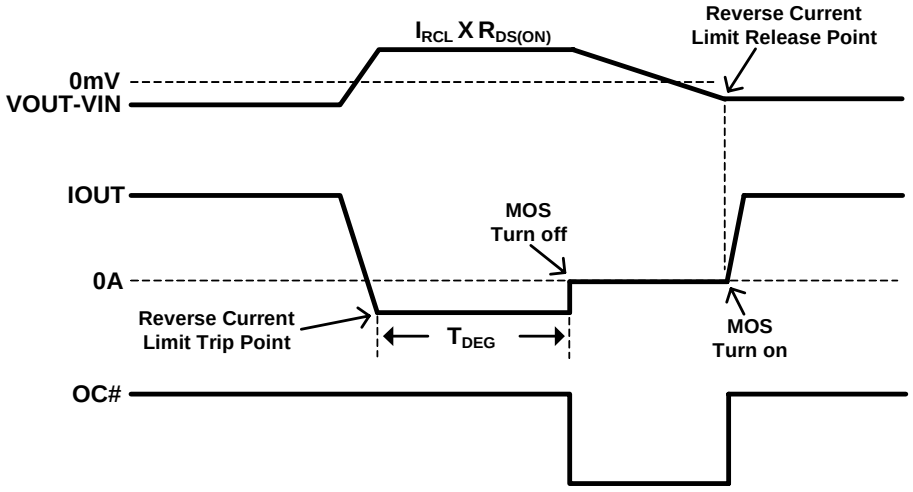
The output voltage is discharged through an internal resistor when the output voltage is disabled.

Functional Description

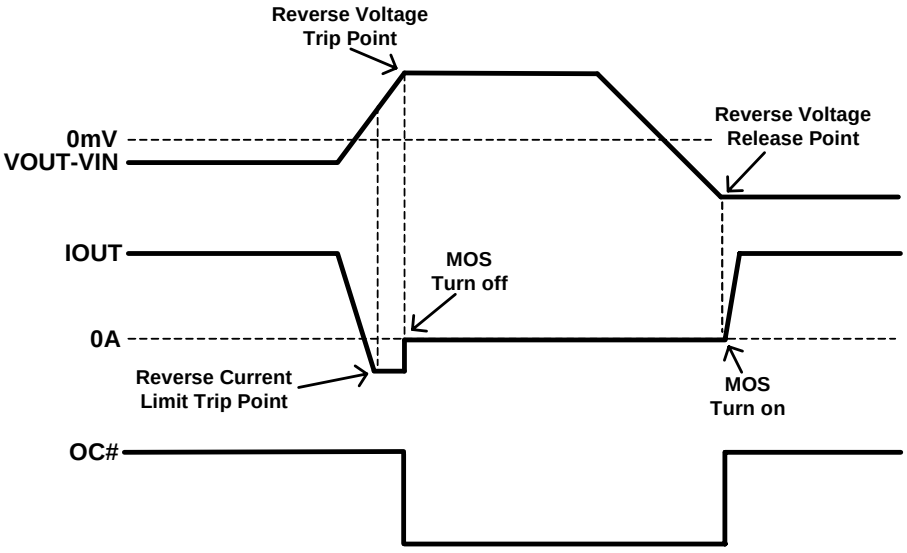
Reverse-Current Limit and Reverse-Voltage Protection

The uP7558 has a reverse current limit feature that protects the input source against significant back current flow from output to input when the output side voltage is higher than the input side. This feature is activated and clamped to a reverse-current level (200mA typical) at a deglitch time of 4ms when the output side voltage is higher than the input side. After 4ms deglitch time, the N-channel MOSFET is turned off, no current flows from the output to the input. The N-channel MOSFET will be turned on if the output side voltage is lower than the input side (5mV typical).

In addition to reverse current limit, reverse voltage protection is also implemented. A reverse voltage comparator controls the N-channel MOSFET to be turned ON or OFF. The N-channel MOSFET is turned off after 40us (typical) deglitch time as soon as VOUT-VIN exceeds 60mV. It turns on within 40us (typical) deglitch time until the voltage VOUT-VIN falls below -40mV. The following Figures show typical protection behavior implementation using the uP7558.



Reverse Current Limit Protection



Reverse Voltage Protection

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VIN ---------- -0.3V to +6V
Other Pins ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
- HBM (Human Body Mode) ---------- 2kV
- MM (Machine Mode) ---------- 200V
- CDM (Charged Device Mode) ---------- 1000V

Thermal Information

Package Thermal Resistance (Note 3)
- TSOT23-5L θ_{JA} ---------- 250°C/W
- TSOT23-5L θ_{JC} ---------- 100°C/W
- TSOT23-5L (Flip-Chip) θ_{JA} ---------- 126.5°C/W
- SOT23-5L θ_{JA} ---------- 250°C/W
- SOT23-5L θ_{JC} ---------- 140°C/W
- MSOP-8L θ_{JA} ---------- 160°C/W
- MSOP-8L θ_{JC} ---------- 40°C/W

Power Dissipation, P_D @ T_A = 25°C
- TSOT23-5L ---------- 0.40W
- TSOT23-5L (Flip-Chip) ---------- 0.79W
- SOP23-5L ---------- 0.40W
- MSOP-8L ---------- 0.63W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{IN} ---------- +2.7V to +5.5V

Electrical Characteristics

(V_{IN}= 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Suppy Input Voltage			2.7	--	5.5	V
Under Voltage Lockout	V_{UVLO}	V_{IN} rising	2.0	2.2	2.4	V
UVLO Hysteresis	ΔV_{UVLO}		--	75	--	mV
Shutdown Current	I_{SD}	No load on V_{OUT}, disabled.	--	0.1	1	uA
Quiescent Current	I_Q	No load on V_{OUT}, enabled.	--	--	100	uA

Electrical Characteristics

Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
Chip Enable							
Logic High Threshold		2.7V < V_{IN} < 5.5V		1.4	--	--	V
Logic Low Threshold		2.7V < V_{IN} < 5.5V		--	--	0.4	V
Enable Input Current		0V < V_{EN}, $V_{EN\#}$ < 5.5V		-0.5	--	0.5	uA
Turn On Time (Note 5)	T_{ON}	C_L = 1uF, R_L = 10Ω		--	1	--	ms
Turn Off Time (Note 5)	T_{OFF}	C_L = 1uF, R_L = 10Ω		--	0.1	--	ms
Output Rise Time	T_R	C_L = 1uF, R_L = 10Ω		0.6	0.9	1.2	ms
Output Fall Time	T_F	C_L = 1uF, R_L = 10Ω		--	0.1	0.3	ms
Output Discharge Resistance when Disabled		V_{IN} = 5V, V_{OUT} = 5V,disabled.	uP7558XXXX-XX	--	40	--	Ω
		V_{IN} = 5V, V_{OUT} = 5V,disabled.	uP7558PMD5-XX	200	--	300	
		V_{IN} = 5V, V_{OUT} = 5V,disabled.	uP7558QMD5-XX	200	--	300	
Power Switch							
N-MOSFET ON Resistance (Note 6)	$R_{DS(ON)}$	Test current = 0.5A	uP7558XXXX-XX	--	--	75	mΩ
N-MOSFET ON Resistance for TSOT23-5L Flip-Chip Package Only (Note 6)	$R_{DS(ON)}$	Test current = 0.5A	uP7558PMD5-XX	--	40	--	mΩ
			uP7558QMD5-XX	--	40	--	
Current Limit							
Short Circuit Output Current	I_{SC}	V_{IN} = 5.0V, V_{OUT} connected to GND, device enabled into short-circuit	uP7558XXXX-05	--	0.5	--	A
			uP7558XXXX-10	--	0.9	--	
			uP7558XXXX-15	--	1.0	--	
			uP7558XXXX-20	--	1.5	--	
			uP7558XXXX-25	--	2.0	--	
			uP7558XXXX-30	--	2.6	--	
Over Current Trip Threshold	I_{SC_TRI}	V_{IN} = 5.0V, current ramp < 100A/s on V_{OUT}	uP7558XXXX-05	0.55	0.8	1.1	A
			uP7558XXXX-10	1.1	1.5	2.0	
			uP7558XXXX-15	1.6	2.1	2.7	
			uP7558XXXX-20	2.1	2.5	3.1	
			uP7558XXXX-25	3.1	3.3	5.0	
			uP7558XXXX-30	3.6	4.3	5.0	
Output Reverse Voltage Protection							
Output Reverse Voltage Trigger Point		V_{OUT} - V_{IN}		--	60	--	mV
Output Reverse Voltage Release Trigger Point		V_{IN} - V_{OUT}		--	40	--	mV
VOUT Shutdown Current	I_{SD_OUT}	V_{OUT} = 5.5V, VIN Short to GND		--	--	5	uA

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Reverse Current Protection						
Output Reverse Current Threshold			--	0.2	--	A
Output Reverse Current Deglitch Time			--	4	--	ms
Over Temperature Protection						
Shutdown-Level Threshold		Guarantee by design	--	135	--	°C
Thermal Shutdown Hysteresis		Guarantee by design	--	20	--	°C
Fault Flag (OC#)						
Output Low Voltage	V_{OL}	$I_{OC\#}$ = 5mA	--	--	0.4	V
Off State Current		$V_{OC\#}$ = 5.5V	--	--	1	uA
OC# Deglitch		OC# assertion and deassertion delay	5	8	15	ms

Note 1. Stresses beyond those listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operation Condition* section of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

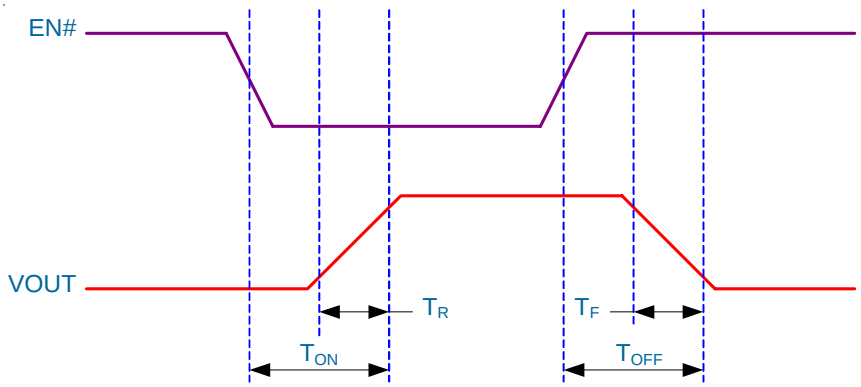
Note 2. Devices are ESD sensitive. Handling precaution recommended.

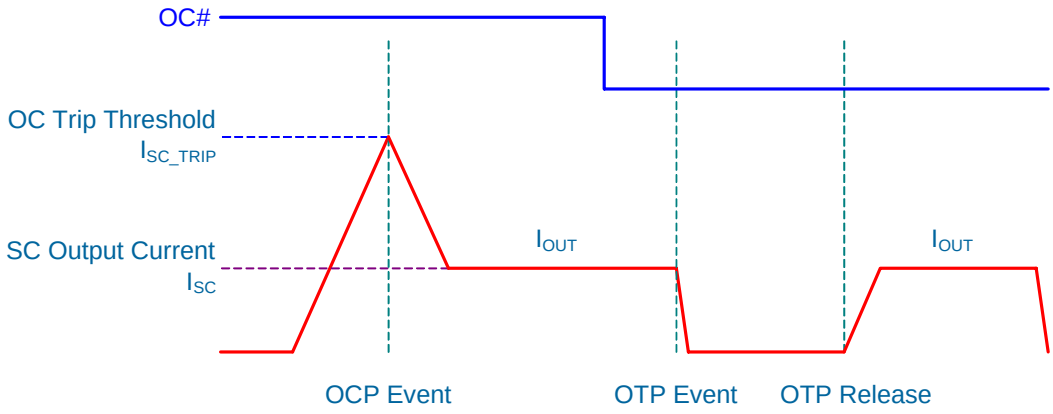
Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. These items are not tested in production, specified by design.

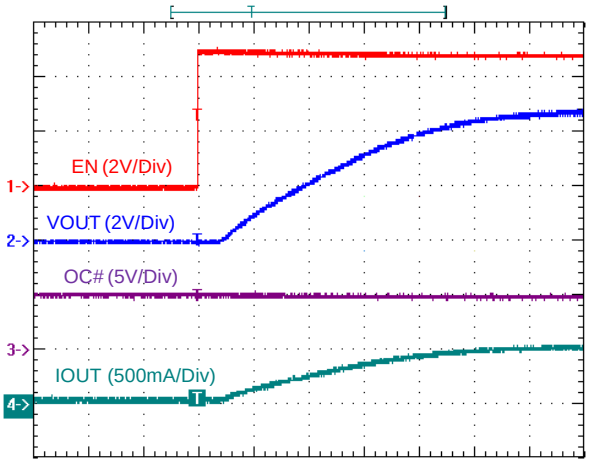
Note 6. Catalog by pulsed current, duration ≤ 1mS, Frequency ≤ 100Hz.


EN#
VOUT
TR
TF
TON
TOFF


OC#
OC Trip Threshold
ISC_TRIP
SC Output Current
ISC
IOUT
IOUT
OCP Event
OTP Event
OTP Release

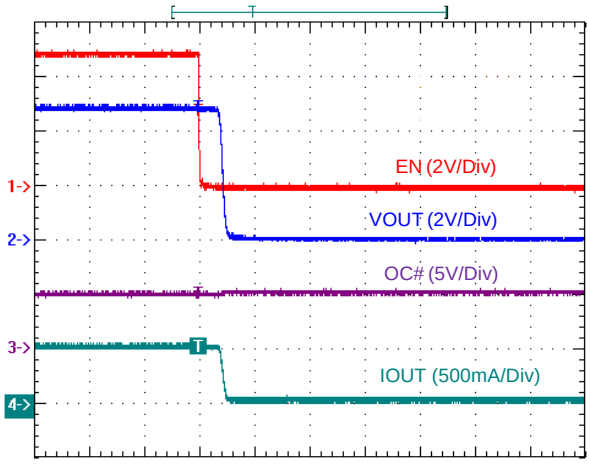
Typical Operation Characteristics

Turn On



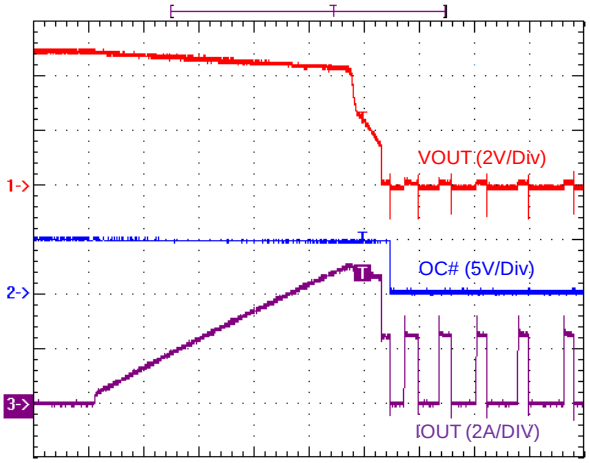
Time：200us/Div
VIN = 5V, VOUT = 5V, CL = 1uF, RL = 10Ω

Turn Off



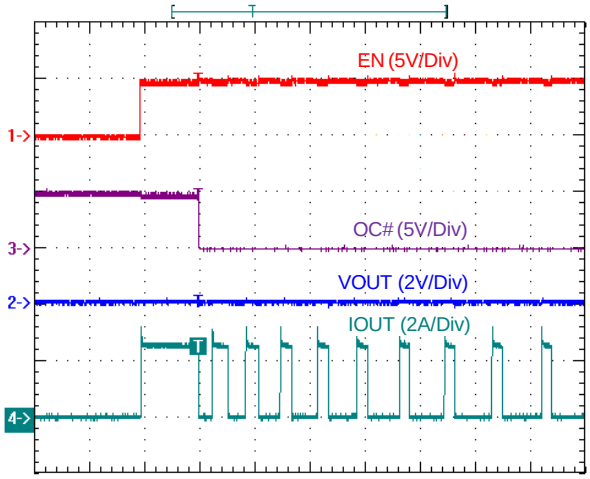
Time：200us/Div
VIN = 5V, VOUT = 5V, CL = 1uF, RL = 10Ω

OC# Response



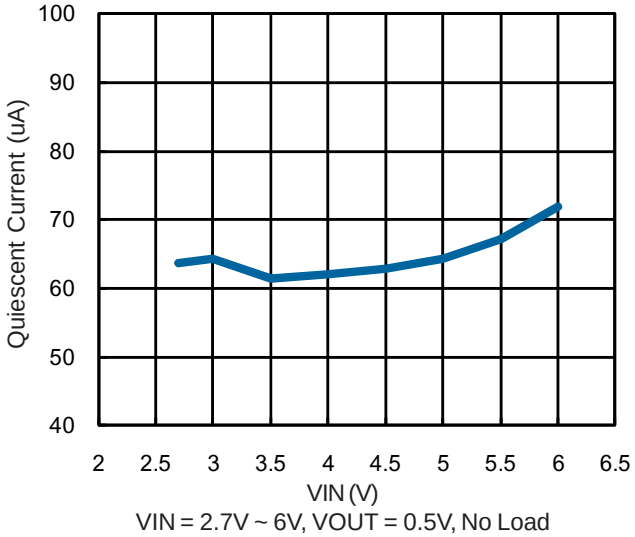
Time：10ms/Div
VIN = 5V, VOUT = 5V, CL = 1uF

Turn On at Short-Circuit



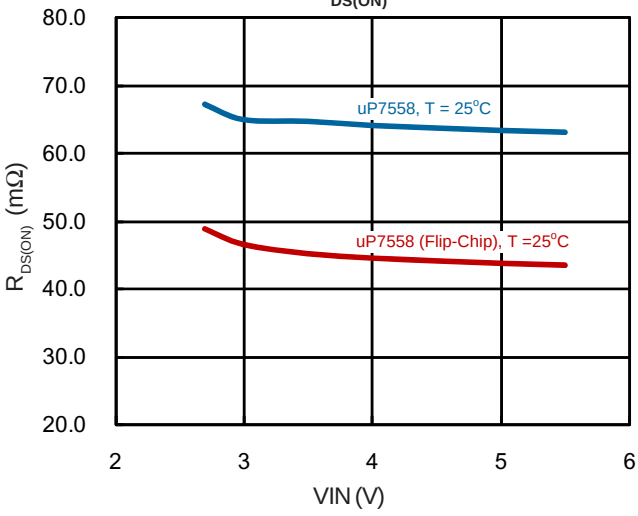
Time：10ms/Div
VIN = 5V, VOUT = 5V, CL = 1uF

Quiescent Current vs. VIN



VIN = 2.7V ~ 6V, VOUT = 0.5V, No Load

$R_{DS(ON)}$



VIN = 2.7V ~ 5.5V, IOUT = 0.5A

Application Information

Supply Input Filtering

VIN pins supply power to the power switch and internal circuit. Both of them should be connect to upstrem power supply with short and wide trace on the PCB.

Events such as hot-plug/unplug, output short circuit and over temperature result in step change of input current with sharp edges, which in turn causes voltage transient at supply input due to di/dit effect of parasitic inductance on the current path. A 0.1uF ceramic capacitor from VIN to GND, physically located near the device is strongly recommended to control the supply input transient. Minimizing the parasitic inductance along the current path also alleviate the voltage transient at the supply input.

Output Voltage Filtering

Bypassing the output voltage with a 0.1uF ceramic capacitor improves the immunity of the device against output short circuit and hot plug/unplug of load. A lower ESR capacitor results in lower voltage drop against a step load change. A large electrolytic capacitor from VOUT to GND is also recommended. This capacitor reduces power supply transient that may cause ringing on the input.

USB supports dynamic attachment (hot plug-in) of peripherals. A current surge is caused by the input capacitance of downstream device. Ferrite beads are recommended in series with all power and ground connector pins. Ferrite beads reduce EMI and limit the inrush current during hot-attachment by filtering high-frequency signals. The DC resistance of the ferrite bead should be specially taken care to reduce the voltage drop.

Voltage Drop and Power Dissipation

Temperature effect should be well considered when dealing with voltage drop and power dissipation. The maximum $R_{DS(ON)}$ of the power switch is 75mΩ under 25°C junction temperature. If the device is expected to operate at 125°C junction temperature, the $R_{DS(ON)}$ will become

$$75m\Omega \times [1 + (125°C - 25°C) \times 0.35\%/°C] = 101.25m\Omega$$

where 0.35%/°C is the approximated temperature coefficient of the $R_{DS(ON)}$.

If the maximum load current is expected to be 1.2A, the maximum voltage will become

$$1.2A \times 101.25m\Omega = 121.5mV$$

This in turn will cause power dissipation as

$$1.2A \times 121.5mV = 145.8mW$$

The temperature raise is calculated as

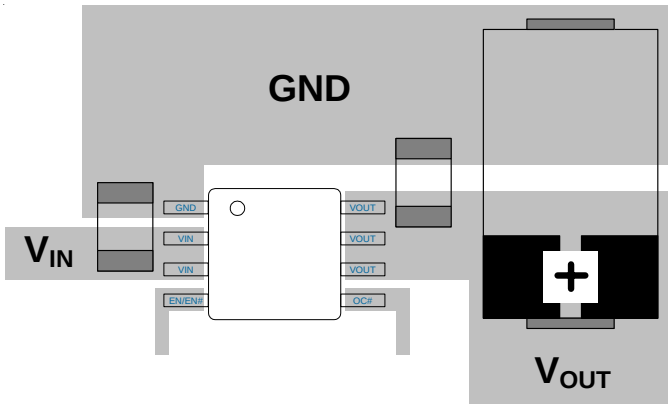
$$145.8m\Omega \times 160°C/W = 24°C$$

The junction temperature is calculated as T_A + 24°C, where T_A is the expected maximum ambient temperature. A few iterations are required until get final solutions.

Layout Consideration

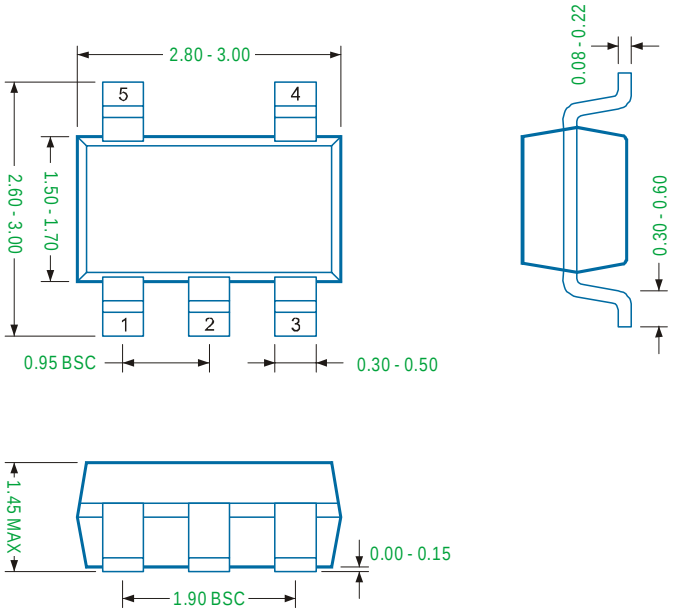
The power circuitry of USB printed circuit boards requires a customized layout to maximize thermal dissipation and to minimized voltage drop and EMI

- Place the device physically as close to the USB port as possible. Keep all traces wide, short and direct to minimized the parasitic inductance. This optimizes the switch response time to output short circuit conditions.
- Place both input and output bypass capacitors near to the device.
- All VOUT pins should be connected together on the PCB. All VIN pins should be connected together on the PCB.



Package Information

SOT23-5L Package

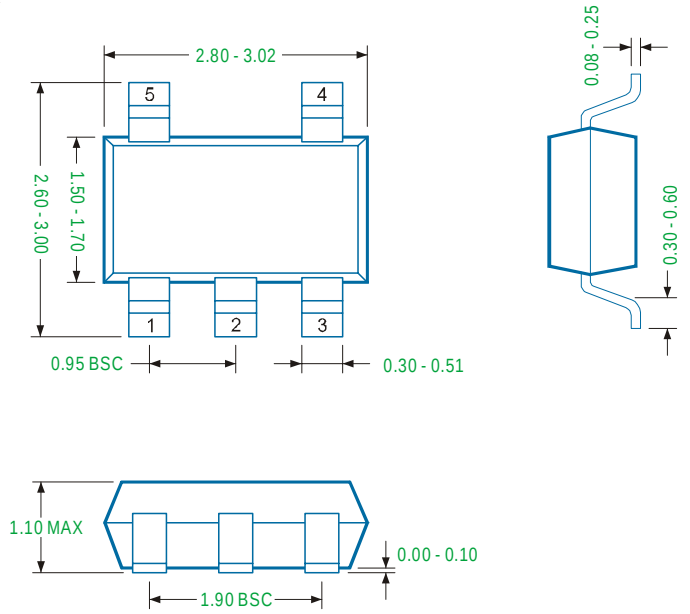


Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Package Information

TSOT23 - 5L Package

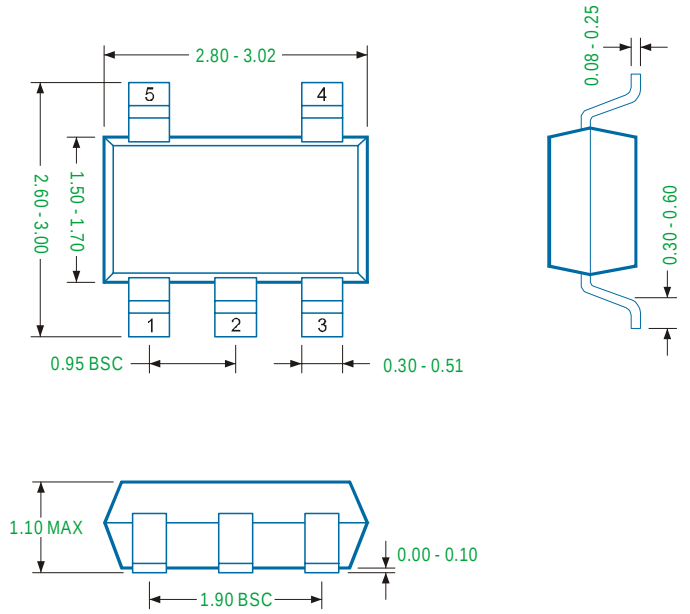


Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Package Information

TSOT23 - 5L (Flip-Chip) Package

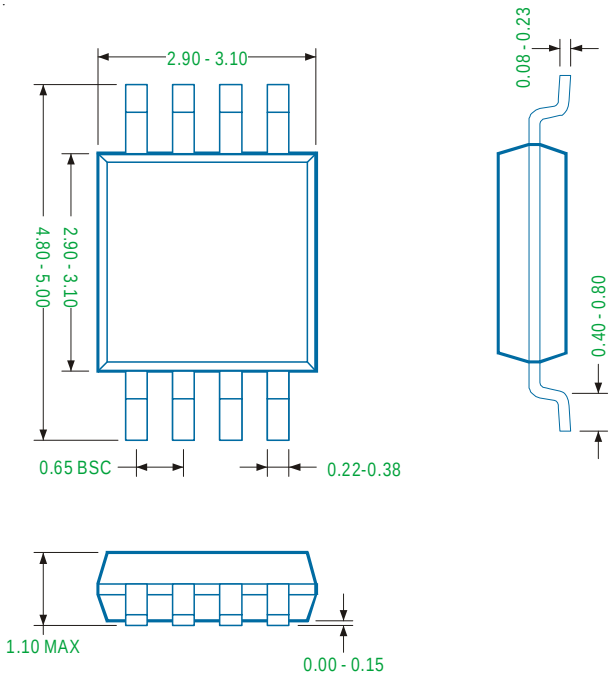


Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Package Information

MSOP - 8L Package



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Important Notice

uPI and its subsidiaries reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

uPI products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment. However, no responsibility is assumed by uPI or its subsidiaries for its use or application of any product or circuit; nor for any infringements of patents or other rights of third parties which may result from its use or application, including but not limited to any consequential or incidental damages. No uPI components are designed, intended or authorized for use in military, aerospace, automotive applications nor in systems for surgical implantation or life-sustaining. No license is granted by implication or otherwise under any patent or patent rights of uPI or its subsidiaries.

uPI Semiconductor Corp.
Headquarter
9F.,No.5, Taiyuan 1st St. Zhubei City,
Hsinchu Taiwan, R.O.C.
TEL : 886.3.560.1666 FAX : 886.3.560.1888

Sales Branch Office
12F-5, No. 408, Ruiguang Rd. Neihu District,
Taipei Taiwan, R.O.C.
TEL : 886.2.8751.2062 FAX : 886.2.8751.5064