Multi-Phase Synchronous-Rectified Buck Controller for Next Generation CPU Core Power

General Description

The uP6213A/B is a multi-phase synchronous-rectified Buck controller specifically designed to deliver high quality output voltage for high-performance Intel microprocessors. It integrates a 8-bit DAC that supports Intel VR10 and VR11 tables to set the output voltage between 0.5V and 1.6V.

The uP6213A provides programmable 3/4 phase operation. The uP6213B provides programmable 1/2 phase operation. The uP6213A/B also supports dynamic phase selection by PS1/2/3 pins. Operation with phase reduction at light load conditions achieves high efficiency over a wide range of output current.

The uP6213A/B includes programmable no-load offset and droop slope functions to adjust the output voltage as a function of the load current, optimally positioning it for a system transient.

Other features include accurate and reliable short-circuit protection, adjustable over current protection, and a delayed power OK output. The uP6213A is available in VQFN6x6-40L package and uP6213B in VQFN4x4-28L package.

Ordering Information

Order Number	Package Type	Remark
uP6213AQAJ	VQFN6x6 - 40L	3/4 phase operation
uP6213BQJH	VQFN4x4 - 28L	1/2 phase operation

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 requirements. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

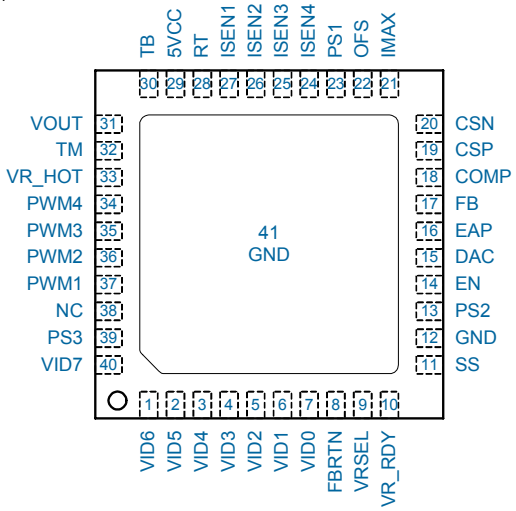
Features

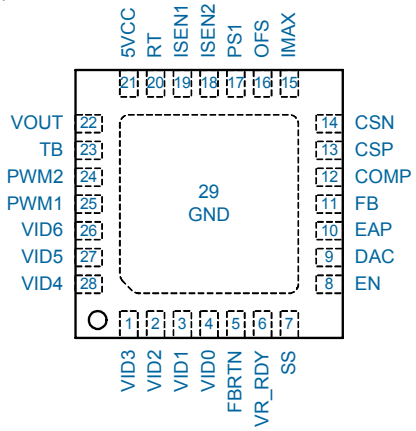
- Selectable Phase Number of Operation
  - uP6213A: 3/4 Phase
  - uP6213B: 1/2 Phase
- 8-bit DAC, Supporting Intel VR10 and VR11 CPUs
- Programmable Dynamic Power Saving Mode Operation
- Simple Single-Loop Voltage-Mode Control
- Lossless $R_{DS(ON)}$ Current Sensing for Current Balance
- Adjustable Operation Frequency form 50kHz to 1MHz Per Phase
- External Compensation
- Adjustable Over Current Protection
- Adjustable Soft Start
- VR_HOT and VR_RDY Indication
- uP6213A in VQFN6x6 - 40L Package
- uP6213B in VQFN4x4 - 28L Package
- RoHS Compliant and 100% Lead (Pb)-Free

Applications

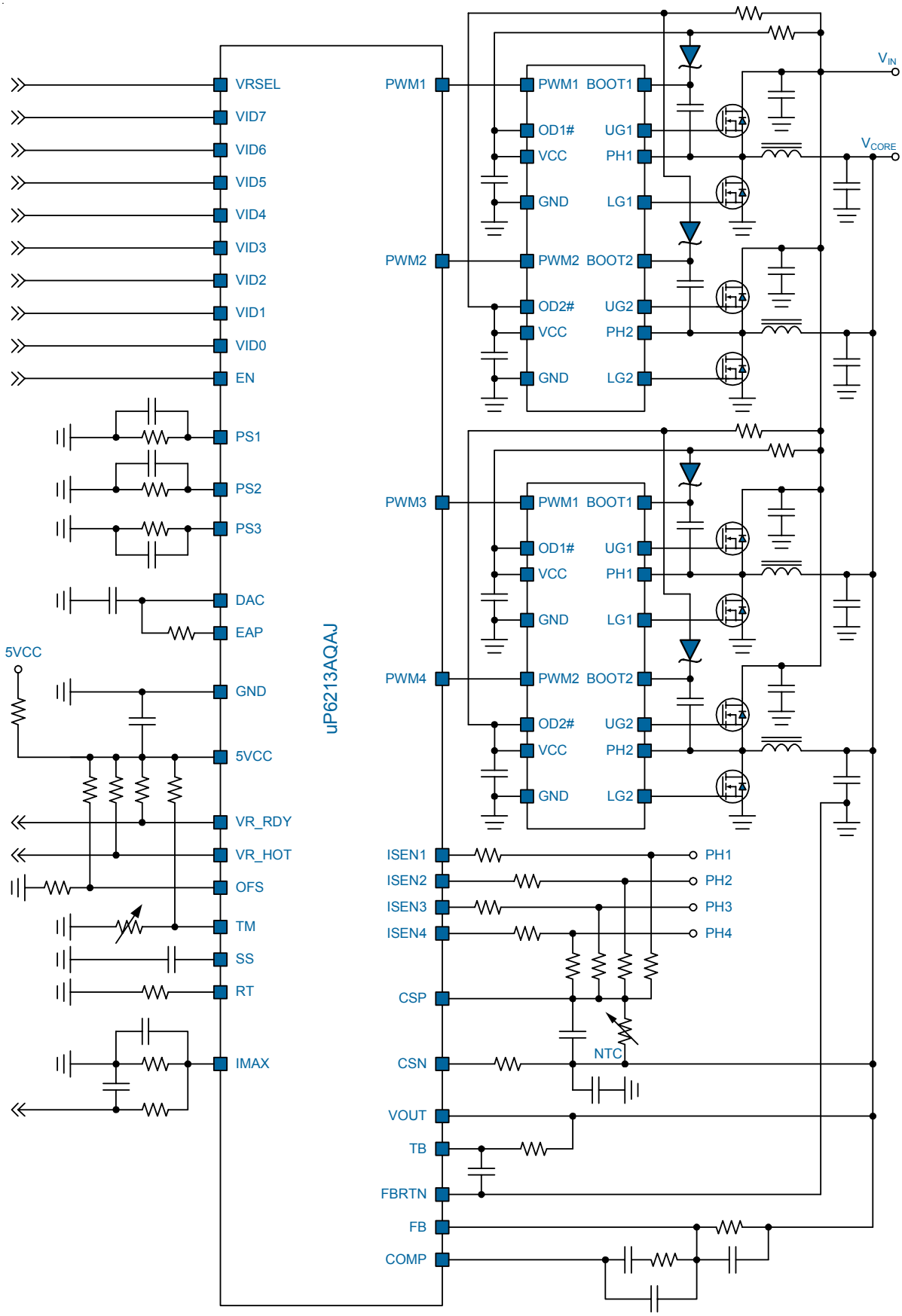
- Desktop PC Core Power Supplies
- Middle/High End Graphic Cards
- Low Output Voltage, High Power Density DC/DC Converters
- Voltage Regulator Modules

Pin Configuration

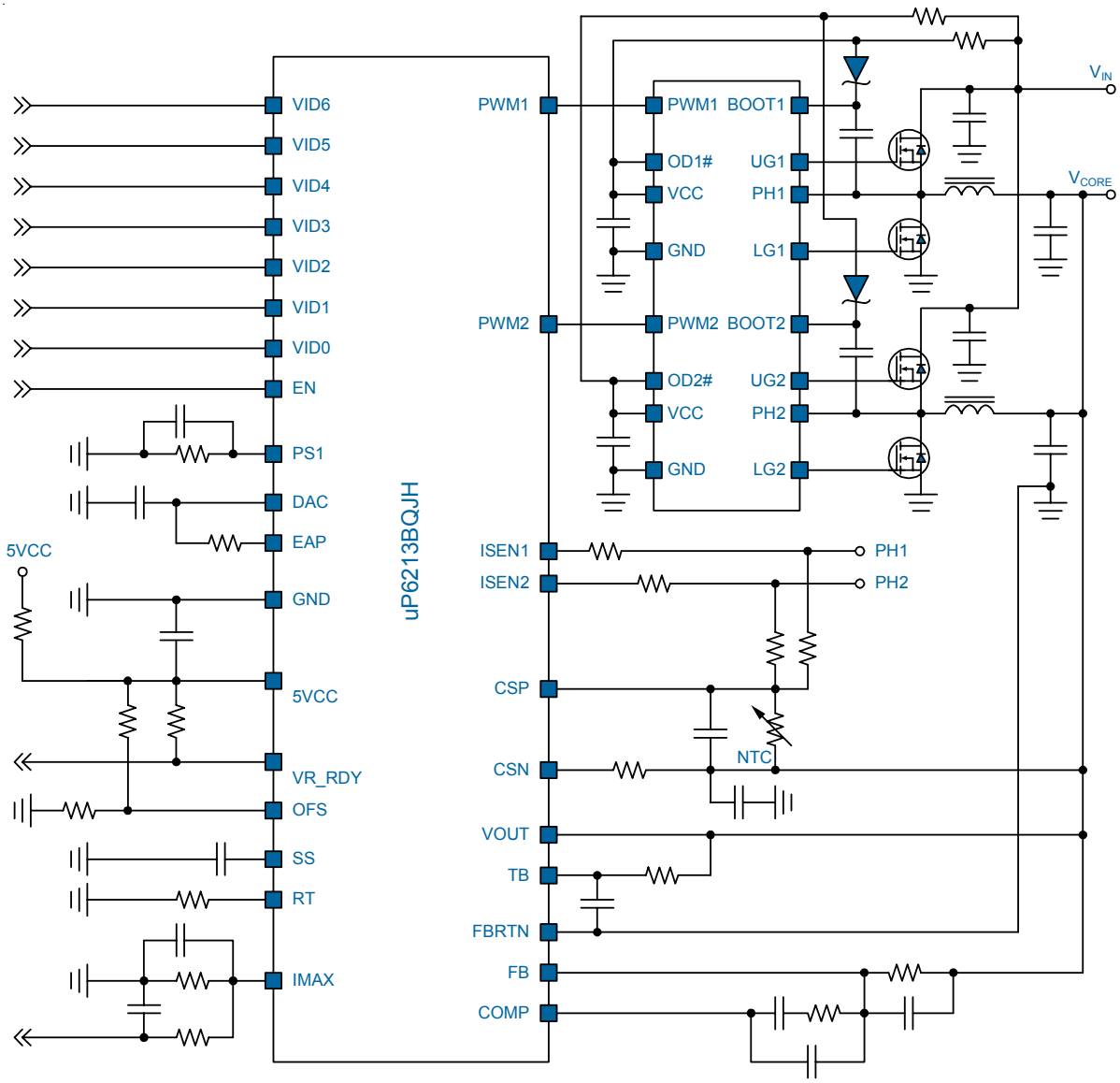




Typical Application Circuit



Typical Application Circuit



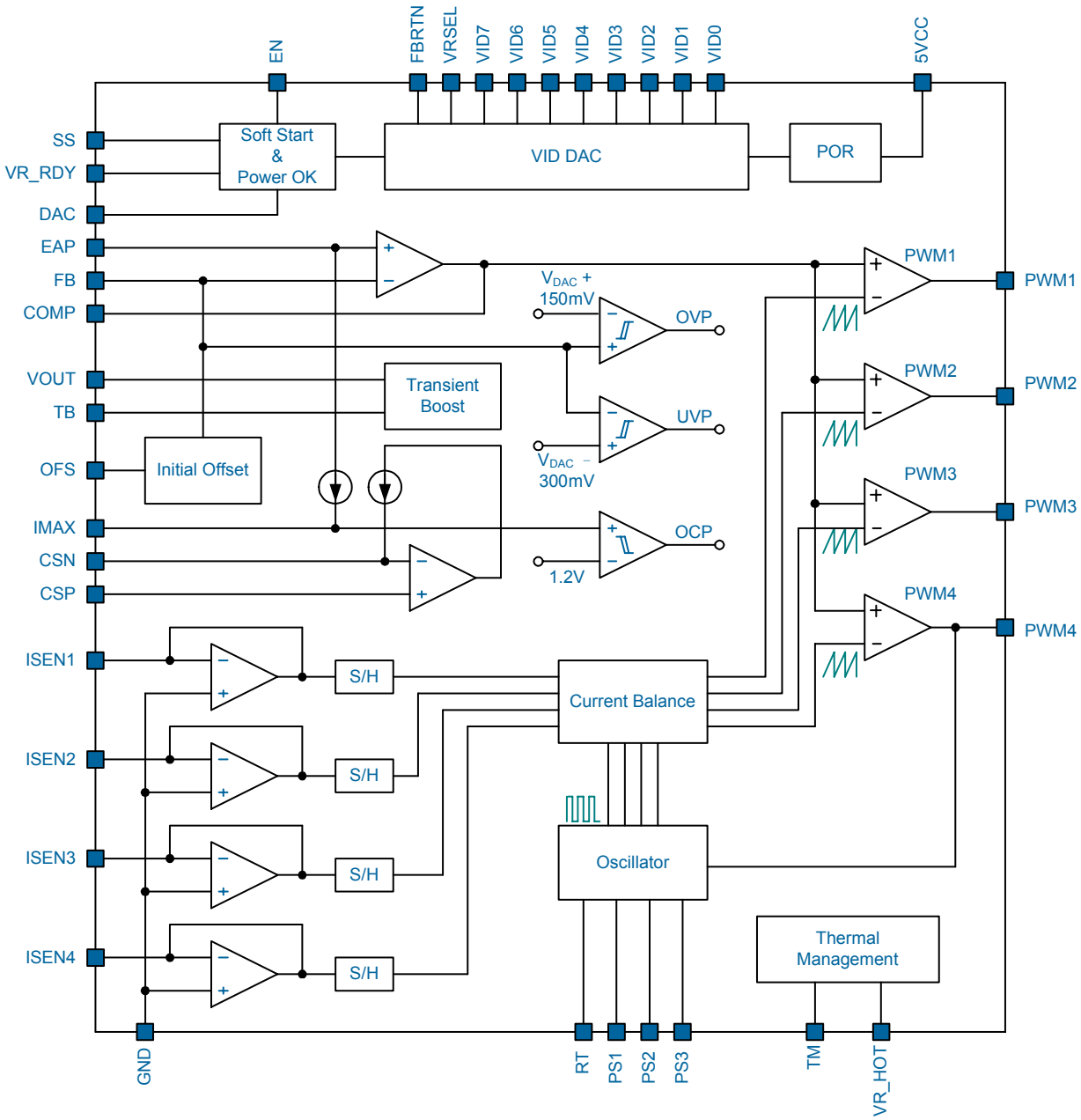
Functional Pin Description

No.		Name	Pin Function
VQFN6x6	VQFN4x4		
1	26	VID6	**Bit 6 of DAC Input.**
2	27	VID5	**Bit 5 of DAC Input.**
3	28	VID4	**Bit 4 of DAC Input.**
4	1	VID3	**Bit 3 of DAC Input.**
5	2	VID2	**Bit 2 of DAC Input.**
6	3	VID1	**Bit 1 of DAC Input.**
7	4	VID0	**Bit 0 of DAC Input.**
8	5	FBRTN	**Return for the DAC Circuit.** Connect this pin to the point where output voltage is to be regulated.
9	NA	VRSEL	**VID Table Selection.** Connect this pin to 5VCC for VR11 VID table, and to GND for VR10 VID table.
10	6	VR_RDY	**VR Ready Indication.**
11	7	SS	**Soft Start.** Connect a capacitor from this pin to GND to set the soft start time.
12	NA	GND	**Ground.**
13	NA	PS2	**Power Saving Mode Setting Input 2.** Connect a resistor from this pin to GND to set the phase reduction threshold level.
14	8	EN	**Chip Enable.** Pulling this pin lower than 0.4V shuts down the device**.**
15	9	DAC	**DAC Output.** Output of the internal DAC. Connect a resistor form this pin to EAP to set the load line slope.
16	10	EAP	**Non-Inverting Input of the Error Amplifier.** Connect a resistor from this pin to DAC to set the load line slope.
17	11	FB	**Feedback Pin.** This pin is the inverting input of the error amplifier.
18	12	COMP	**Compensation Output.** This pin is the output of the error amplifier
19	13	CSP	**Positive Input of the Current Sensing GM Amplifier.**
20	14	CSN	**Negative Input of the Current Sensing GM Amplifier.**

Functional Pin Description

Pin No.		Name	Pin Function
VQFN6x6	VQFN4x4		
21	15	IMAX	**Output Current Indication.** Connect a resistor from this pin to GND to set the over current protection level.
22	16	OFS	**Zero Current Offset.** Connect a resistor form this pin to 5VCC or GND to set the output offset voltage.
23	17	PS1	**Power Saving Mode Setting Input 1.** Connect a resistor from this pin to ground to set the phase reduction threshold level.
24	NA	ISEN4	**Current Sensing for Phase4.**
25	NA	ISEN3	**Current Sensing for Phase 3.**
26	18	ISEN2	**Current Sensing for Phase 2.**
27	19	ISEN1	**Current Sensing for Phase 1.**
28	20	RT	**Switching Frequency Programming.** Connect a resistor from this pin to GND to set the switching frequency.
29	21	5VCC	**5V Supply Input.** This pin receives a 5V voltage source to power the control circuit. Connect this pin to ATX 5VCC.
30	23	TB	**Transient Boost.** This pin along with the VOUT pin set the transient boost behavior.
31	22	VOUT	**Output Voltage Sensing.** This pin along with the TB pin set the transient boost behavior.
32	NA	TM	**Thermal Monitoring.** Connect NTC network to this pin for thermal monitoring.
33	NA	VR_HOT	**VR HOT Output.**
34	NA	PWM4	**PWM Output of Phase 4.** Connect this pin to input pin of the companion gate driver, such as uP6281.
35	NA	PWM3	**PWM Output of Phase 3.** Connect this pin to input pin of the companion gate driver, such as uP6281.
36	24	PWM2	**PWM Output of Phase 2.** Connect this pin to input pin of the companion gate driver, such as uP6281.
37	25	PWM1	**PWM Output of Phase 1.** Connect this pin to input pin of the companion gate driver, such as uP6281.
38	NA	NC	**Not Internally Connected.**
39	NA	PS3	**Power Saving Mode Setting Input 3.** Connect a resistor from this pin to GND to set the phase reduction threshold level.
40	NA	VID7	**Bit 7 of DAC Input.** This pin is internally pulled high for uP6213B.
Exposed Pad GND			**Ground.** Tie this pin to the ground island/plane through the lowest impedance connection available.

Functional Block Diagram



Functional Description

The uP6213A/B is a multi-phase synchronous-rectified Buck controller specifically designed to deliver high quality output voltage for high-performance Intel microprocessors. It integrates a 8-bit DAC that supports Intel VR10 and VR11 tables to set the output voltage between 0.5V and 1.6V.

The uP6213A provides programmable 3/4 phase operation. The uP6213B provides programmable 1/2 phase operation. The uP6213A/B also supports dynamic phase selection by PS1/2/3 pins. Operation with phase reduction at light load conditions achieves high efficiency over a wide range of output current.

The uP6213A/B includes programmable no-load offset and droop slope functions to adjust the output voltage as a function of the load current, optimally positioning it for a system transient.

Other features include accurate and reliable short-circuit protection, adjustable over current protection, and a delayed power OK output. The uP6213A is available in VQFN6x6-40L package and uP6213B in VQFN4x4-28L package.

Supply Input and Power on Reset

The 5VCC pin receives a well-decoupled 5V voltage source to power the internal control circuit. Place a minimum 1uF ceramic capacitor physically near the 5VCC pin for locally bypassing the 5VCC voltage. The 5VCC voltage is continuously monitored for power on reset. The POR level is typical 4.2V at 5VCC rising.

Operation Phase Selection

The uP6213A supports 3/4 phase operation and uP6213B supports 1/2 phase operation. PWM4 and PWM2 status is checked at POR for operation phase selection. Connect PWM4 to 5VCC for 3-phase operation of uP6213A and connect PWM2 to 5VCC for 1-phase operation of uP6213B. Let the unused current sensing pins ISEN4 or ISEN2 float or short them to GND when selecting 3/1-phase operation. (*See the related section for Dynamic Phase Reduction.*)

VID Table Selection

The uP6213A supports both VR10 and VR11 VID tables. Pulling the VRSEL pin lower than 0.4V select VR10 table as shown in Table 2 while pulling the VRSEL pin higher than 0.8V select the VR11 table as shown in Table 1. The uP6213B supports only VR11 table with VID7 = High.

Oscillation Frequency Programming

A resistor R_{RT} connected to RT pin programs the oscillation frequency as:

$$f_{OSC} = 300\left(\frac{33k\Omega}{R_{RT}(k\Omega)}\right)^{0.92} \quad (kHz)$$

Figure 1 shows the relationship between oscillation frequency and R_{RT}.

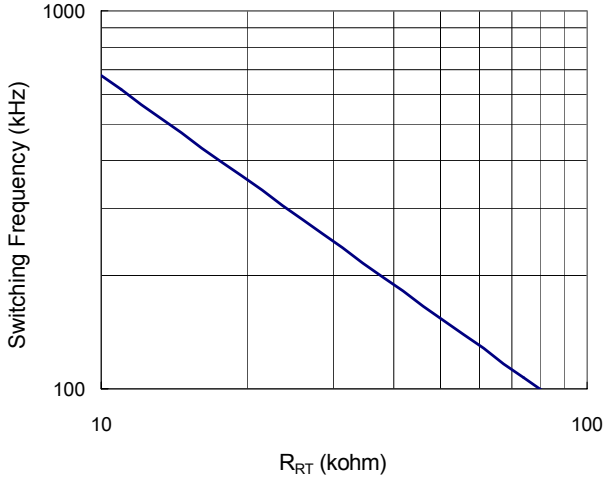


Figure 1. Switching Frequency vs. R_{RT}

Output Current Sensing

Figure 2 illustrates the output current sensing block of the uP6213A/B. The voltage V_{CS} across the current sensing capacitor C_{CS} can be expressed as:

$V_{CS} = I_{OUT} \times DCR/P$

if the following condition is true.

$P \times L / DCR = R_{CSP} \times C_{CS}$

where P is the phase number of operation (P = 3 for three phase operation, P = 4 for four phase operation), L is the output inductor of the buck converter, DCR is the parasitic resistance of the inductor, R_{CSP} and C_{CS} are the external RC network for current sensing.

The GM amplifier will source a current I_{AVG} to the CSN pin to let its inputs virtually short circuit.

$I_{AVG} \times R_{CSN} = V_{CS}$

Therefore the output current signal I_{AVG} can be expressed as:

$$I_{AVG} = \frac{I_{OUT} \times DCR}{P \times R_{CSN}}$$

The output current signal I_{AVG} is used as droop turning and output over current protection. Please see the related section for details.

Note that the constant P is only dependent of the power stage topology. It is programmed by the PWM4/PWM2 configuration. Dynamic phase reduction will not affect the value of P.

Functional Description

Table 1. VR11 VID Table (VRSEL = 5VCC)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	OFF
0	0	0	0	0	0	1	0	1.60000
0	0	0	0	0	0	1	1	1.59375
0	0	0	0	0	1	0	0	1.58750
0	0	0	0	0	1	0	1	1.58125
0	0	0	0	0	1	1	0	1.57500
0	0	0	0	0	1	1	1	1.56875
0	0	0	0	1	0	0	0	1.56250
0	0	0	0	1	0	0	1	1.55625
0	0	0	0	1	0	1	0	1.55000
0	0	0	0	1	0	1	1	1.54375
0	0	0	0	1	1	0	0	1.53750
0	0	0	0	1	1	0	1	1.53125
0	0	0	0	1	1	1	0	1.52500
0	0	0	0	1	1	1	1	1.51875
0	0	0	1	0	0	0	0	1.51250
0	0	0	1	0	0	0	1	1.50625
0	0	0	1	0	0	1	0	1.50000
0	0	0	1	0	0	1	1	1.49375
0	0	0	1	0	1	0	0	1.48750
0	0	0	1	0	1	0	1	1.48125
0	0	0	1	0	1	1	0	1.47500
0	0	0	1	0	1	1	1	1.46875
0	0	0	1	1	0	0	0	1.46250
0	0	0	1	1	0	0	1	1.45625
0	0	0	1	1	0	1	0	1.45000
0	0	0	1	1	0	1	1	1.44375
0	0	0	1	1	1	0	0	1.43750
0	0	0	1	1	1	0	1	1.43125
0	0	0	1	1	1	1	0	1.42500
0	0	0	1	1	1	1	1	1.41875
0	0	1	0	0	0	0	0	1.41250
0	0	1	0	0	0	0	1	1.40625
0	0	1	0	0	0	1	0	1.40000
0	0	1	0	0	0	1	1	1.39375
0	0	1	0	0	1	0	0	1.38750
0	0	1	0	0	1	0	1	1.38125
0	0	1	0	0	1	1	0	1.37500
0	0	1	0	0	1	1	1	1.36875
0	0	1	0	1	0	0	0	1.36250
0	0	1	0	1	0	0	1	1.35625
0	0	1	0	1	0	1	0	1.35000
0	0	1	0	1	0	1	1	1.34375
0	0	1	0	1	1	0	0	1.33750

Table 1. VR11 VID Table (Cont.) (VRSEL = 5VCC)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	1	0	1	1	0	1	1.33125
0	0	1	0	1	1	1	0	1.32500
0	0	1	0	1	1	1	1	1.31875
0	0	1	1	0	0	0	0	1.31250
0	0	1	1	0	0	0	1	1.30625
0	0	1	1	0	0	1	0	1.30000
0	0	1	1	0	0	1	1	1.29375
0	0	1	1	0	1	0	0	1.28750
0	0	1	1	0	1	0	1	1.28125
0	0	1	1	0	1	1	0	1.27500
0	0	1	1	0	1	1	1	1.26875
0	0	1	1	1	0	0	0	1.26250
0	0	1	1	1	0	0	1	1.25625
0	0	1	1	1	0	1	0	1.25000
0	0	1	1	1	0	1	1	1.24375
0	0	1	1	1	1	0	0	1.23750
0	0	1	1	1	1	0	1	1.23125
0	0	1	1	1	1	1	0	1.22500
0	0	1	1	1	1	1	1	1.21875
0	1	0	0	0	0	0	0	1.21250
0	1	0	0	0	0	0	1	1.20625
0	1	0	0	0	0	1	0	1.20000
0	1	0	0	0	0	1	1	1.19375
0	1	0	0	0	1	0	0	1.18750
0	1	0	0	0	1	0	1	1.18125
0	1	0	0	0	1	1	0	1.17500
0	1	0	0	0	1	1	1	1.16875
0	1	0	0	1	0	0	0	1.16250
0	1	0	0	1	0	0	1	1.15625
0	1	0	0	1	0	1	0	1.15000
0	1	0	0	1	0	1	1	1.14375
0	1	0	0	1	1	0	0	1.13750
0	1	0	0	1	1	0	1	1.13125
0	1	0	0	1	1	1	0	1.12500
0	1	0	0	1	1	1	1	1.11875
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625
0	1	0	1	0	0	1	0	1.10000
0	1	0	1	0	0	1	1	1.09375
0	1	0	1	0	1	0	0	1.08750
0	1	0	1	0	1	0	1	1.08125
0	1	0	1	0	1	1	0	1.07500
0	1	0	1	0	1	1	1	1.06875
0	1	0	1	1	0	0	0	1.06250
0	1	0	1	1	0	0	1	1.05625

Table 1. VR11 VID Table (Cont.) (VRSEL = 5VCC)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	1	0	1	1	0	1	0	1.05000
0	1	0	1	1	0	1	1	1.04375
0	1	0	1	1	1	0	0	1.03750
0	1	0	1	1	1	0	1	1.03125
0	1	0	1	1	1	1	0	1.02500
0	1	0	1	1	1	1	1	1.01875
0	1	1	0	0	0	0	0	1.01250
0	1	1	0	0	0	0	1	1.00625
0	1	1	0	0	0	1	0	1.00000
0	1	1	0	0	0	1	1	0.99375
0	1	1	0	0	1	0	0	0.98750
0	1	1	0	0	1	0	1	0.98125
0	1	1	0	0	1	1	0	0.97500
0	1	1	0	0	1	1	1	0.96875
0	1	1	0	1	0	0	0	0.96250
0	1	1	0	1	0	0	1	0.95625
0	1	1	0	1	0	1	0	0.95000
0	1	1	0	1	0	1	1	0.94375
0	1	1	0	1	1	0	0	0.93750
0	1	1	0	1	1	0	1	0.93125
0	1	1	0	1	1	1	0	0.92500
0	1	1	0	1	1	1	1	0.91875
0	1	1	1	0	0	0	0	0.91250
0	1	1	1	0	0	0	1	0.90625
0	1	1	1	0	0	1	0	0.90000
0	1	1	1	0	0	1	1	0.89375
0	1	1	1	0	1	0	0	0.88850
0	1	1	1	0	1	0	1	0.88125
0	1	1	1	0	1	1	0	0.87500
0	1	1	1	0	1	1	1	0.86875
0	1	1	1	1	0	0	0	0.86250
0	1	1	1	1	0	0	1	0.85625
0	1	1	1	1	0	1	0	0.85000
0	1	1	1	1	0	1	1	0.84375
0	1	1	1	1	1	0	0	0.83750
0	1	1	1	1	1	0	1	0.83125
0	1	1	1	1	1	1	0	0.82500
0	1	1	1	1	1	1	1	0.81875
1	0	0	0	0	0	0	0	0.81250
1	0	0	0	0	0	0	1	0.80625
1	0	0	0	0	0	1	0	0.80000
1	0	0	0	0	0	1	1	0.79375
1	0	0	0	0	1	0	0	0.78750
1	0	0	0	0	1	0	1	0.78125
1	0	0	0	0	1	1	0	0.77500

Table 1. VR11 VID Table (Cont.) (VRSEL = 5VCC)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
1	0	0	0	0	1	1	1	0.76875
1	0	0	0	1	0	0	0	0.76250
1	0	0	0	1	0	0	1	0.75625
1	0	0	0	1	0	1	0	0.75000
1	0	0	0	1	0	1	1	0.74375
1	0	0	0	1	1	0	0	0.73750
1	0	0	0	1	1	0	1	0.73125
1	0	0	0	1	1	1	0	0.72500
1	0	0	0	1	1	1	1	0.71875
1	0	0	1	0	0	0	0	0.71250
1	0	0	1	0	0	0	1	0.70625
1	0	0	1	0	0	1	0	0.70000
1	0	0	1	0	0	1	1	0.69375
1	0	0	1	0	1	0	0	0.68750
1	0	0	1	0	1	0	1	0.68125
1	0	0	1	0	1	1	0	0.67500
1	0	0	1	0	1	1	1	0.66875
1	0	0	1	1	0	0	0	0.66250
1	0	0	1	1	0	0	1	0.65625
1	0	0	1	1	0	1	0	0.65000
1	0	0	1	1	0	1	1	0.64375
1	0	0	1	1	1	0	0	0.63750
1	0	0	1	1	1	0	1	0.63125
1	0	0	1	1	1	1	0	0.62500
1	0	0	1	1	1	1	1	0.61875
1	0	1	0	0	0	0	0	0.61250
1	0	1	0	0	0	0	1	0.60625
1	0	1	0	0	0	1	0	0.60000
1	0	1	0	0	0	1	1	0.59375
1	0	1	0	0	1	0	0	0.58750
1	0	1	0	0	1	0	1	0.58125
1	0	1	0	0	1	1	0	0.57500
1	0	1	0	0	1	1	1	0.56875
1	0	1	0	1	0	0	0	0.56250
1	0	1	0	1	0	0	1	0.55625
1	0	1	0	1	0	1	0	0.55000
1	0	1	0	1	0	1	1	0.54375
1	0	1	0	1	1	0	0	0.53750
1	0	1	0	1	1	0	1	0.53125
1	0	1	0	1	1	1	0	0.52500
1	0	1	0	1	1	1	1	0.51875
1	0	1	1	0	0	0	0	0.51250
1	0	1	1	0	0	0	1	0.50625
1	0	1	1	0	0	1	0	0.50000
1	1	1	1	1	1	1	0	OFF
1	1	1	1	1	1	1	1	OFF

Functional Description

Table 1. VRD10 + VID6 VID Table (VRSEL = GND)

VID4	VID3	VID2	VID1	VID0	VID5	VID6	Voltage
0	1	0	1	0	1	1	1.60000
0	1	0	1	0	1	0	1.59375
0	1	0	1	1	0	1	1.58750
0	1	0	1	1	0	0	1.58125
0	1	0	1	1	1	1	1.57500
0	1	0	1	1	1	0	1.56875
0	1	1	0	0	0	1	1.56250
0	1	1	0	0	0	0	1.55625
0	1	1	0	0	1	1	1.55000
0	1	1	0	0	1	0	1.54375
0	1	1	0	1	0	1	1.53750
0	1	1	0	1	0	0	1.53125
0	1	1	0	1	1	1	1.52500
0	1	1	0	1	1	0	1.51875
0	1	1	1	0	0	1	1.51250
0	1	1	1	0	0	0	1.50625
0	1	1	1	0	1	1	1.50000
0	1	1	1	0	1	0	1.49375
0	1	1	1	1	0	1	1.48750
0	1	1	1	1	0	0	1.48125
0	1	1	1	1	1	1	1.47500
0	1	1	1	1	1	0	1.46875
1	0	0	0	0	0	1	1.46250
1	0	0	0	0	0	0	1.45625
1	0	0	0	0	1	1	1.45000
1	0	0	0	0	1	0	1.44375
1	0	0	0	1	0	1	1.43750
1	0	0	0	1	0	0	1.43125
1	0	0	0	1	1	1	1.42500
1	0	0	0	1	1	0	1.41875
1	0	0	1	0	0	1	1.41250
1	0	0	1	0	0	0	1.40625
1	0	0	1	0	1	1	1.40000
1	0	0	1	0	1	0	1.39375
1	0	0	1	1	0	1	1.38750
1	0	0	1	1	0	0	1.38125
1	0	0	1	1	1	1	1.37500
1	0	0	1	1	1	0	1.36875
1	0	1	0	0	0	1	1.36250
1	0	1	0	0	0	0	1.35625
1	0	1	0	0	1	1	1.35000
1	0	1	0	0	1	0	1.34375
1	0	1	0	1	0	1	1.33750
1	0	1	0	1	0	0	1.33125
1	0	1	0	1	1	1	1.32500
1	0	1	0	1	1	0	1.31875

Table 1. VRD10 + VID6 VID Table (Cont.) (VRSEL = GND)

VID4	VID3	VID2	VID1	VID0	VID5	VID6	Voltage
1	0	1	1	0	0	1	1.31250
1	0	1	1	0	0	0	1.30625
1	0	1	1	0	1	1	1.30000
1	0	1	1	0	1	0	1.29375
1	0	1	1	1	0	1	1.28750
1	0	1	1	1	0	0	1.28125
1	0	1	1	1	1	1	1.27500
1	0	1	1	1	1	0	1.26875
1	1	0	0	0	0	1	1.26250
1	1	0	0	0	0	0	1.25625
1	1	0	0	0	1	1	1.25000
1	1	0	0	0	1	0	1.24375
1	1	0	0	1	0	1	1.23750
1	1	0	0	1	0	0	1.23125
1	1	0	0	1	1	1	1.22500
1	1	0	0	1	1	0	1.21875
1	1	0	1	0	0	1	1.21250
1	1	0	1	0	0	0	1.20625
1	1	0	1	0	1	1	1.20000
1	1	0	1	0	1	0	1.19375
1	1	0	1	1	0	1	1.18750
1	1	0	1	1	0	0	1.18125
1	1	0	1	1	1	1	1.17500
1	1	0	1	1	1	0	1.16875
1	1	1	0	0	0	1	1.16250
1	1	1	0	0	0	0	1.15625
1	1	1	0	0	1	1	1.15000
1	1	1	0	0	1	0	1.14375
1	1	1	0	1	0	1	1.13750
1	1	1	0	1	0	0	1.13125
1	1	1	0	1	1	1	1.12500
1	1	1	0	1	1	0	1.11875
1	1	1	1	0	0	1	1.11250
1	1	1	1	0	0	0	1.10625
1	1	1	1	0	1	1	1.10000
1	1	1	1	0	1	0	1.09375
1	1	1	1	1	0	1	OFF
1	1	1	1	1	0	0	OFF
1	1	1	1	1	1	1	OFF
1	1	1	1	1	1	0	OFF
0	0	0	0	0	0	1	1.08750
0	0	0	0	0	0	0	1.08125
0	0	0	0	0	1	1	1.07500
0	0	0	0	0	1	0	1.06875
0	0	0	0	1	0	1	1.06250
0	0	0	0	1	0	0	1.05625

Table 1. VRD10 + VID6 VID Table (Cont.) (VRSEL = GND)

VID4	VID3	VID2	VID1	VID0	VID5	VID6	Voltage
0	0	0	0	1	1	1	1.05000
0	0	0	0	1	1	0	1.04375
0	0	0	1	0	0	1	1.03750
0	0	0	1	0	0	0	1.03125
0	0	0	1	0	1	1	1.02500
0	0	0	1	0	1	0	1.01875
0	0	0	1	1	0	1	1.01250
0	0	0	1	1	0	0	1.00625
0	0	0	1	1	1	1	1.00000
0	0	0	1	1	1	0	0.99375
0	0	1	0	0	0	1	0.98750
0	0	1	0	0	0	0	0.98125
0	0	1	0	0	1	1	0.97500
0	0	1	0	0	1	0	0.96875
0	0	1	0	1	0	1	0.96250
0	0	1	0	1	0	0	0.95625
0	0	1	0	1	1	1	0.95000
0	0	1	0	1	1	0	0.94375
0	0	1	1	0	0	1	0.93750
0	0	1	1	0	0	0	0.93125
0	0	1	1	0	1	1	0.92500
0	0	1	1	0	1	0	0.91875
0	0	1	1	1	0	1	0.91250
0	0	1	1	1	0	0	0.90625
0	0	1	1	1	1	1	0.90000
0	0	1	1	1	1	0	0.89375
0	1	0	0	0	0	1	0.89750
0	1	0	0	0	0	0	0.88125
0	1	0	0	0	1	1	0.87500
0	1	0	0	0	1	0	0.86875
0	1	0	0	1	0	1	0.86250
0	1	0	0	1	0	0	0.85625
0	1	0	0	1	1	1	0.85000
0	1	0	0	1	1	0	0.84375
0	1	0	1	0	0	1	0.83750
0	1	0	1	0	0	0	0.83125

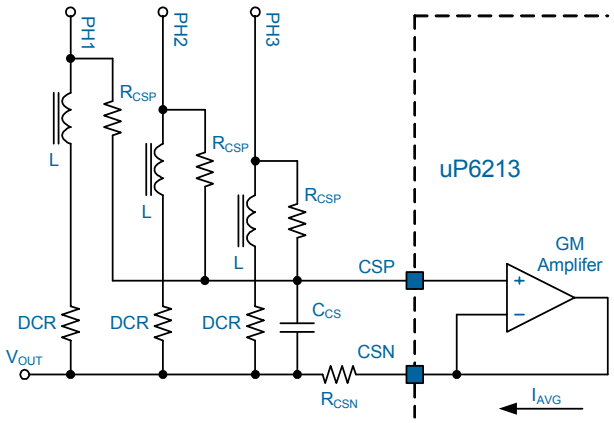


Figure 2. Output Current Sensing of uP6213A/B.

Voltage Control Loop

Figure 3 illustrates the voltage control loop of the uP6213A/B. FB and EAP are negative and positive inputs of the Error Amplifier respectively. The Error Amplifier modulates the COMP voltage V_{COMP} and the duty cycle of buck converter to force FB voltage V_{FB} follows V_{EAP}.

As shown in Figure 3, V_{DAC} is output of the internal VID table. The slew rate of V_{DAC} is limited by the capacitor connected to SS pin during soft start and VID on the fly transition. The sensed current signal is mirrored to the EAP pin and creates voltage at EAP pin as:

$$V_{EAP} = V_{DAC} - R_{DRP} \times I_{AVG}$$

where V_{DAC} is a slew rate limited voltage source, I_{AVG} is a current source proportional to output current, and R_{DRP} is an external resistor for adjusting load line slope.

On the other hand, the inverting input voltage V_{FB} can be written as:

$$V_{FB} = V_{OUT} - R_{FB} \times I_{OFS}$$

where V_{OUT} is the output voltage, I_{OFS} is a current source for initial offset adjustment, R_{OFS} is an external resistor.

Therefore, the output voltage will be:

$$V_{OUT} = V_{DAC} - R_{DRP} \times I_{AVG} + R_{FB} \times I_{OFS}$$

$$V_{OUT} = V_{DAC} - \frac{I_{OUT} \times DCR \times R_{DRP}}{P \times R_{CSN}} + R_{FB} \times I_{OFS}$$

Please see the related section for details.

Functional Description

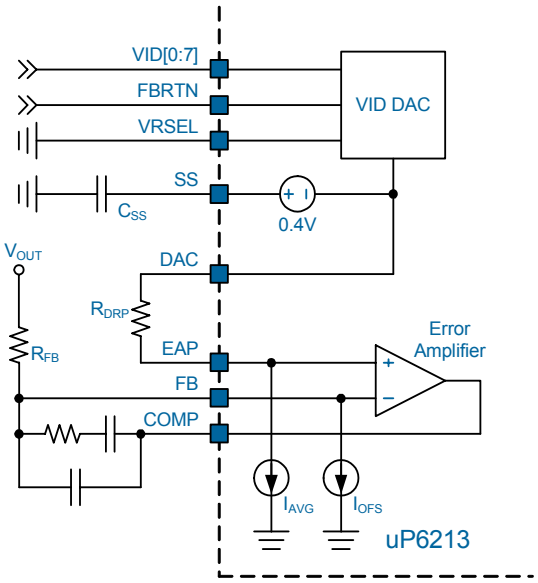


Figure 3. Voltage Control Loop.

Initial Offset Adjustment

Connect a resistor R_{OFS} from OFS pin to 5VCC or GND to set the initial offset voltage. The OFS voltage V_{OFS} is 5_{VCC} - 1.6V or 0.4V when connected to 5VCC or GND respectively. There the current source I_{OFS} can be calculated as:

I_{OFS} = 0.4V / R_{OFS} sourcing, R_{OFS} to GND, positive offset

I_{OFS} = 1.6V / R_{OFS} sinking, R_{OFS} to 5VCC, negative offset.

The offset current source I_{OFS} is mirrored and injected to FB pin for initial offset adjustment. Please see the *Voltage Control Loop* section for details.

Soft Start and Power OK

Figure 4 illustrates typical VR11 compliant soft start cycle of uP6213A/B. A capacitor C_{SS} connected to SS pin is used to adjust the soft start cycle.

A limited current source I_{SS} is used to charge/discharge C_{SS} when VID changes. Since V_{DAC} is 0.4V higher than V_{SS}, this limit the slew rate of V_{SS} and V_{DAC} during soft start and VID on the fly period. This consequently limits the output voltage ramp up/down slew rate.

The uP6213A/B is POR and enabled at T0. There is a 800us time delay (T0 ~ T1) before the current source I_{SS} begins charging the C_{SS}. The DAC voltage V_{DAC} and output voltage V_{OUT} is kept zero during (T0 ~ T2). The V_{DAC} and V_{OUT} ramps up to boot up voltage V_{BOOT} during time delay TD2. The uP6213A/B inserts a time delay TD3 for the VID to get valid. The V_{DAC} and V_{OUT} ramps to its target value according to VID status during TD4. The uP6213A/B asserts soft start end and set VR_RDY to high impedance status at T6.

Before time delay TD3 ends, the I_{SS} is limited to 10uA. After that, the I_{SS} is limited to 160uA. Consequently, critical time periods are calculated as:

(T2 - T1) = 0.4V x C_{SS} / 10uA

TD1 = T2 - T0 = 800us + 0.4V x C_{SS} / 10uA

TD2 = V_{BOOT} x C_{SS} / 10uA = 1.1V x C_{SS} / 10uA

TD4 = |V_{VID} - V_{BOOT}| / 160uA

Time Delay (T1 - T0) = 800us, TD3 = 800us and TD5 = 800us are fixed delay and can not be adjusted externally.

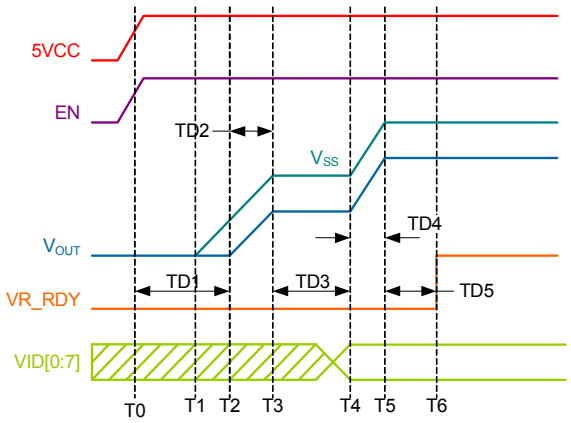


Figure 4. Soft Start Cycle of uP6213.

Transient Boost Mechanism

The uP6213A/B features a novel transient boost mechanism that turns on all high side MOSFETs during a large step load transient as shown in Figure 5. The VOUT and TB are inverting and non-inverting inputs of the transient boost comparator respectively. At steady state, an internal 10uA current source creates a voltage drop between V_{OUT} and V_{TB}:

V_{OUT} - V_{TB} = 10uA x R_{TB}

R_{TB} and C_{TB} form a low pass filter for the V_{TB}. During large step load transient, V_{OUT} abruptly drops while the V_{TB} keeps relatively constant. Once V_{OUT} is smaller than V_{TB}, the transient boost mechanism is activated and turns on all high side MOSFETs to provide current to output capacitors as fast as possible.

Select R_{TB} to decide a suitable threshold level for transient boost. For example, a 4.7kΩ R_{TB} will triggered the transient boost mechanism if output voltage is abruptly drops by around 50mV. Also keep the R_{TB} x C_{TB} time constant around 2us.

Functional Description

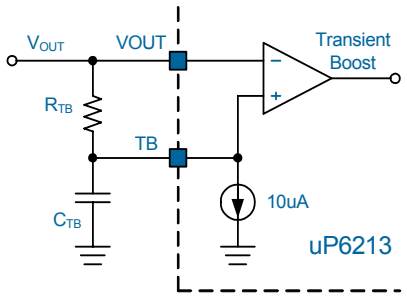


Figure 5. Transient Boost Mechanism

Channel Current Sensing

The uP6213A/B extracts phase currents for current balance and over current protection by parasitic on-resistance of the lower switches when turn on as shown in Figure 6. The ISEN1/2/3/4 pins sense the corresponding phase current when the low side MOSFETs are turned on.

$I_{SENX} = ((I_{PHX} \times R_{DS(ON)}) + V_{DC}) / R_{SENX}$

where I_{SENX} is the sampled and held phase current signal, I_{PHX} is phase current, $R_{DS(ON)}$ is the on-resistance of the low side MOSFETs, and V_{DC} = 20mV is an offset voltage for the current balance circuit. The current balance circuit increases the duty cycle of the phase whose phase current is smaller than others and decrease the duty cycle of the phase whose phase current is larger than others.

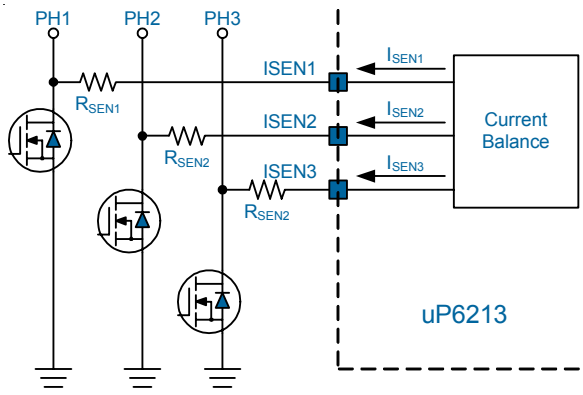


Figure 6. Phase Current Sensing and Current Balance.

Select R_{SENX} to set the current balance gain. A rule of thumb is to keep I_{SENX} = 5uA at rated output current.

Output Over Current Protection

I_{AVG} is mirrored and injected to the IMAX pin and create a voltage V_{IMAX} at IMAX pin.

$V_{IMAX} = R_{IMAX} \times I_{AVG} = R_{IMAX} \times I_{OUT} \times DCR / R_{CSN} / P$

The over current protection is activated and shuts down the uP6213A/B if the IMAX voltage is higher than 1.2V.

Output Over Voltage Protection

The OVP is activated and turns on the low side MOSFETs if (V_{FB} - V_{DAC}) > 160mV

The uP6213A/B turns on the lower gate drivers when OVP is detected. The over voltage protection is latch-off and can only be reset by POR or toggling the EN pin.

Under Voltage Protection

The under voltage protection is activated if FB voltage V_{FB} is 300mV lower than the DAC voltage V_{DAC}. The uP6213 A/B turns off both higher and lower gate drivers when UVP is detected. The under voltage protection is latch-off and can only be reset by POR or toggling the EN pin.

Operation Phase Selection

The uP6213A/B sources 10uA current sources out of PS1, PS2 and PS3 pins. Connecting resistors R_{PS1}, R_{PS2} and R_{PS3} at PS1, PS2 and PS3 pins creates voltage levels V_{PS1} , V_{PS2} and V_{PS3} for power saving mode operation.

$V_{PS1} = 10uA \times R_{PS1}$

$V_{PS2} = 10uA \times R_{PS2}$

$V_{PS3} = 10uA \times R_{PS3}$

Table 3 shows the operation phase of uP6213A according to V_{IMAX}, V_{PS1}, V_{PS2}, V_{PS3} and PWM3/PWM4 status. The uP6213A/B operates in 4-phase configuration if all PWM outputs are connected to inputs of respective pre-drivers, in 3-phase of PWM4 is connected 5VCC, in 2-phase if PWM3/PWM4 are connected to 5VCC.

The uP6213 also supports dynamic phase-selection according to PS1, PS2 and PS3 status.

Let PS1/PS2/PS3 >0.8V to force the uP6213A/B into single phase operation. Let PS1/PS2/PS3 <0.2V to force the uP6213A/B into full-phase operation (set by PWM3/PWM4).

Automatic Phase Reduction

The uP6213A/B compares V_{IMX} with V_{PS1}/V_{PS2}/V_{PS3} to decide the operation dynamically. if $V_{IMX} < V_{PS1}$ the uP6213 operates in single phase regarless the status of V_{PS2} and V_{PS3}; if $V_{PS1} < V_{IMX} < V_{PS2}$ the uP6213 operates in dual phase regarless the status of V_{PS3}. Take PWM4 = 5VCC, V_{PS1} = 0.2V, V_{PS2} = 0.3V, V_{PS3} = 0.2V and V_{IMAX} = 0.25V for example, the uP6213 turns off phase 3 and operates the converter in 2-phase.

The uP6213A/B always keeps out-of-phase interleaved operation. When operating in 3 phase, Phase1/2/3 are kept 120^{O} out-of phase. When operating in 2 phase, Phase 1/2 are kept 180^{O} of phase.

When setting PS1, PS2 and PS3, always keep V_{PS1} < V_{PS2}, V_{PS3} with difference larger than 80mV. Violating

Table 3. Operation Phase Selection.

		PS1	PS2	PS3	Operation Phase
2-Phase Configuration, PWM3, PWM4 to VCC5	Auto PSI Mode	PS1 > V_{IMAX}	open		1
		V_{IMAX} > PS1	open		2
	Forced 1 phase	< 0.2V			1
	Forced 2-phase	> 0.8V			2
3-Phase Configuration, PWM4 to VCC5	Auto PSI Mode	PS2, PS1 > V_{IMAX}		open	1
		PS2 > V_{IMAX} > PS1		open	2
		V_{IMAX} > PS2, PS1		open	3
	Forced 1-phase	< 0.2V			1
	Forced 3-phase	> 0.8V			3
4-Phase Configuration	Auto PSI Mode	PS3, PS2, PS1 > V_{IMAX}			1
		PS3, PS2 > V_{IMAX} > PS1			2
		PS3 > V_{IMAX} > PS2, PS1			3
		V_{IMAX} > PS3, PS2, PS1			4
	Forced 1-phase	< 0.2V			1
	Forced 4-phase	> 0.8V			4
Always Keep PS1 < PS2 < PS3					

this rule may lead to unkown status and should be avoided.

The automatic phase reduction reduces the switching and conduction losses at light load condition and enables high efficiency over a wide range of output current.

Short PS1, PS2 and PS3 to GND to disable the automatic phase reduction.

Temperature Monitoring

The uP6213 monitors the converter temperature at TM pin as shown if Figure 7. VR_HOT is activated if V_{TM} < 28% of 5VCC and sets the VR_HOT pin high impedance. VR_HOT is pulled low if V_{TM} > 33% of 5VCC.

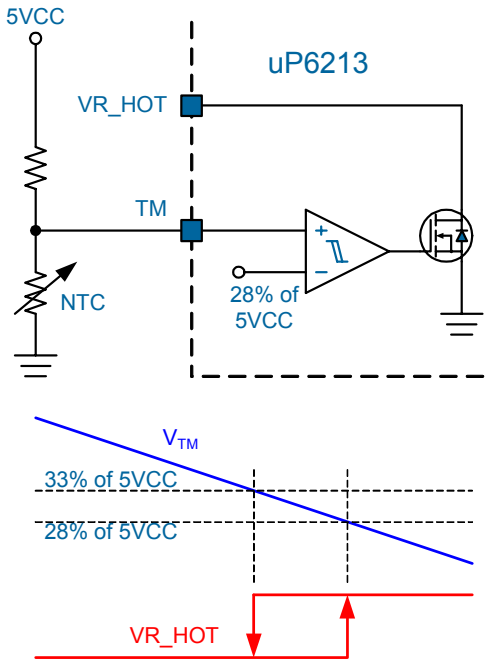


Figure 7. Temperature Monitoring of uP6213.

Absolute Maximum Rating

Supply Input Voltage, 5VCC (Note 1) ---------- -0.3V to +6V
Other Pins ---------- -0.3V to +5VCC + 0.3V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
VQFN6x6 - 40L θ_{JA} ---------- 35°C/W
VQFN4x4 - 28L θ_{JA} ---------- 40°C/W
VQFN6x6 - 40L θ_{JC} ---------- 3°C/W
VQFN4x4 - 28L θ_{JC} ---------- 4°C/W
Power Dissipation, P_D @ T_A = 25°C
VQFN6x6 - 40L ---------- 2.8W
VQFN4x4 - 28L ---------- 2.5W

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4) ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{CC5} ---------- 4.5V to 5.5V

Electrical Characteristics

(5VCC = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Input Voltage	V_{CC5}		4.5	--	5.5	V
Supply Current	I_{CC5}	PWMx open; Switching	2	4	6	mA
5VCC POR Threshold	V_{CC5RTH}	V_{CC5} Rising.	4.0	4.2	4.4	V
5VCC POR Hysteresis	V_{CC5HYS}		--	0.4	--	V
Soft Start						
Soft Start Current	I_{SS}	V_{SS} = 0V	9.0	10.4	11.8	uA
VID on the Fly Maximum Current	I_{SS}		--	160	--	uA
Transient Boost (TB)						
TB Sinking Current	I_{TB}		9	10	11	uA
Thermal Management						
VR_HOT Threshold Level			26	28	30	%V_{CC5}
VR_HOR Hysteresis			--	5	--	%V_{CC5}

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Total Current Sensing						
Maximum Sourcing Current			100	--	--	uA
Input Offset Voltage			-0.4	0.6	1.6	mV
IMAX Current Mirror Accuracy		I_{IMAX}/I_{AVG}	95	100	105	%
Droop Current Mirror Accuracy		I_{DRP}/I_{AVG}	95	100	105	%
Enable Control						
Logic Low Threshold	V_{IL}		--	--	0.4	V
Logic High Threshold	V_{IH}		0.8	--	--	V
Oscillator						
Switching Frequency	f_{OSC}	R_{RT} = 24kΩ	270	300	330	kHz
Adjustable Frequency Range			50	--	1000	kHz
Ramp Amplitude			--	4	--	V
Maximum Duty			70	75	80	%
RT Pin Voltage	V_{RT}		0.97	1.02	1.07	V
PWM Output						
Output Low Voltage	V_{OL}	I_{SINK} = 4mA	--	--	0.2	V
Output High Voltage	V_{OH}	I_{SRC} = 4mA	4.7	--	--	V
Reference Voltage and DAC						
DAC Accuracy	V_{FB}	0.5V to 0.8V	-10	--	10	mV
		0.8V to 1.0V	-8	--	8	
		1.0V to 1.6V	-0.5	--	0.5	%
DAC Input Logic Low Threshold	V_{IL}		--	--	0.4	V
DAC Input Logic High Threshold	V_{IH}		0.8	--	--	V
OFS Voltage		R_{OFS} = 10kΩ to 5VCC. V_{CC5} - V_{OFS}	1.49	1.62	1.75	V
		R_{OFS} = 10kΩ to GND.	0.38	0.41	0.44	
Error Amplifier						
Open Loop DC Gain	AO	Guaranteed by Design	70	80	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF.	30	--	--	MHz
Slew Rate	SR	Guaranteed by Design	3	6	--	V/us
Trans-conductance	GM	R_{LOAD} = 20kΩ	1400	1800	--	uA/V
Maximum Current (Source & Sink)	I_{COMP}	V_{COMP} = 1.6V	300	360	--	uA

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Saving Mode						
PS1/PS2/PS3 Soucing Current	I_{PSX}	R_{PS1} = R_{PS2} =R_{PS3}= 47k	9	10	11	uA
Protection						
Total Curren Protection Threshold	V_{IMAX}		1.1	1.2	1.3	V
FB Over Voltage Protection		V_{FB} - V_{DAC}	130	160	190	mV
FB Under Voltage Protection		V_{FB} - V_{DAC}	-380	-300	-250	mV
Over Temperature Protection Threshold			--	160	--	°C
Over Temperature Protection Hysteresis			--	20	--	°C
Output Pin Capability						
VR_HOT Sinking Capability	V_{HOT}	I_{HOT} = 4mA.	--	0.05	0.2	V
VR_RDY Sinking Capability	V_{RDY}	I_{RDY} = 4mA.	--	0.05	0.2	V

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

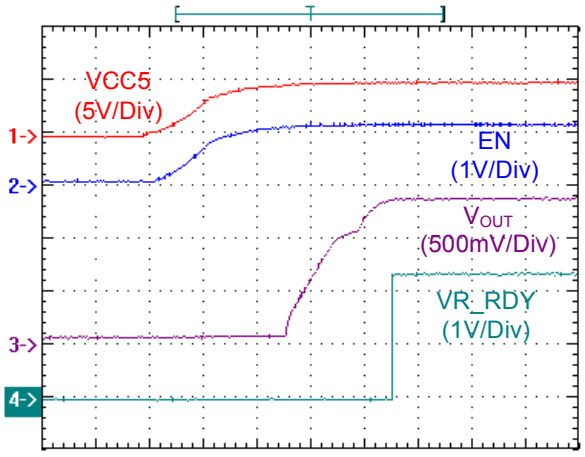
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

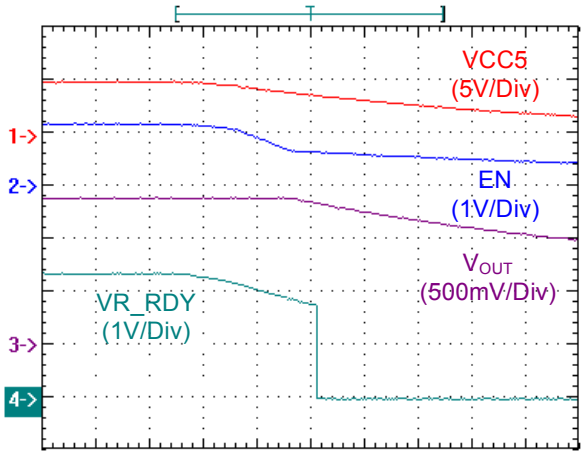
Typical Operation Characteristics

Power On Waveforms



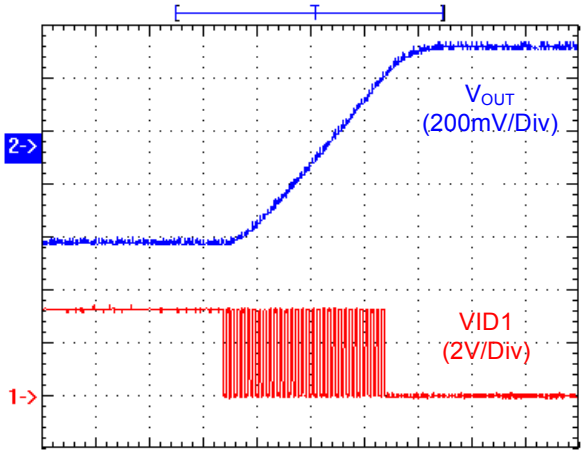
Time (4ms/Div)

Power Off Waveforms



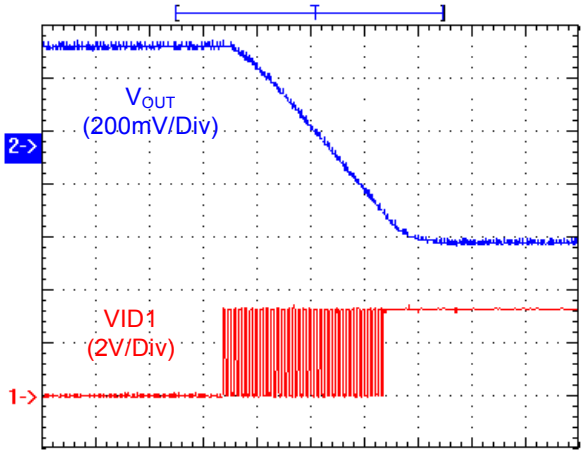
Time (100ms/Div)

DVID Rising



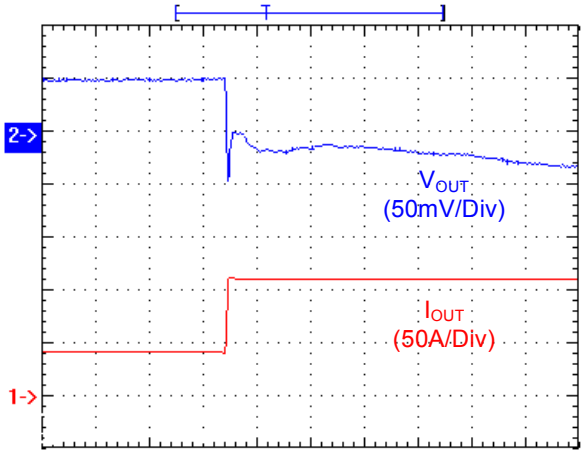
Time (100us/Div)

DVID Falling



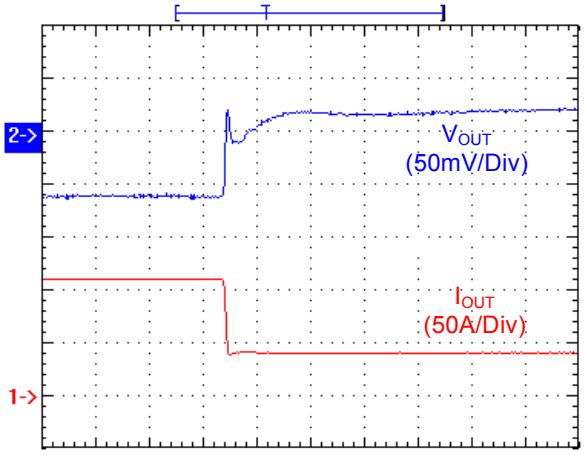
Time (100us/Div)

Load Transient Response Rising



Time (1us/Div)

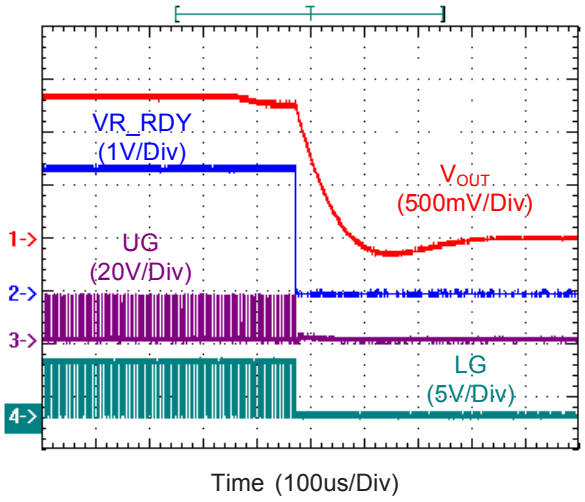
Load Transient Response Falling



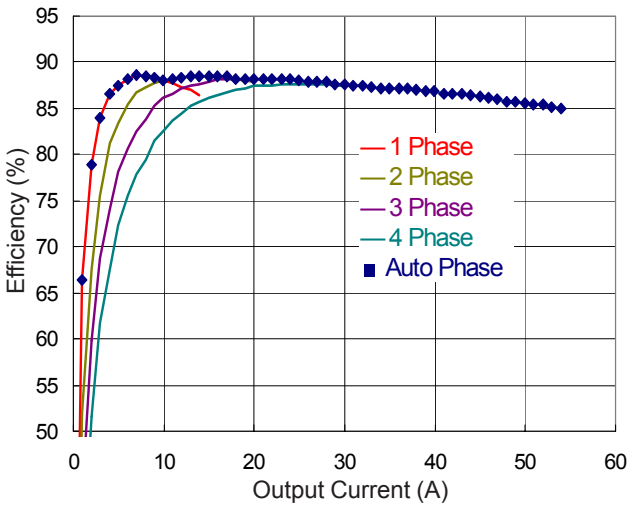
Time (1us/Div)

Typical Operation Characteristics

Over Current Protection



Auto Phase Efficiency



Total Current Sensing

In the real application, PCB trances are not ideal and have certain parasitic resistances R_{PCB1} and R_{PCB2} as shown in Figure 1. When these parasistic resistances are not identical, the voltages at inductor terminals are not the same, contributing meausrement error on total current sensing. Two 1Ω resistors, connecting directly to inductor terminals are recommended to elimiate the effects of parasitic resistance.

A 0.1uF capacitor C_{BYP} is also recommended to bypassing noise when the uP6213A/B is far away from the output inductors. Place the C_{BYP} physically near the IC.

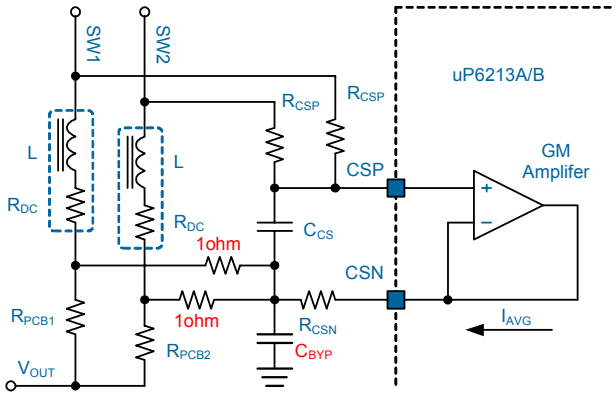
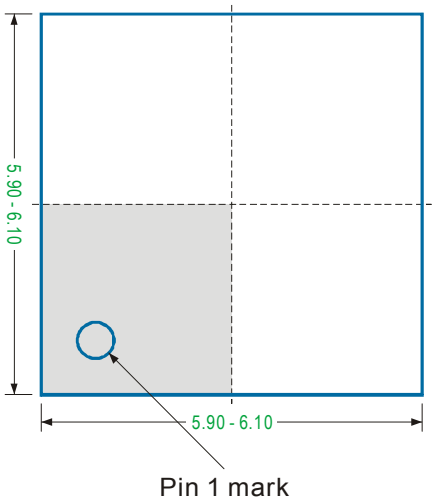
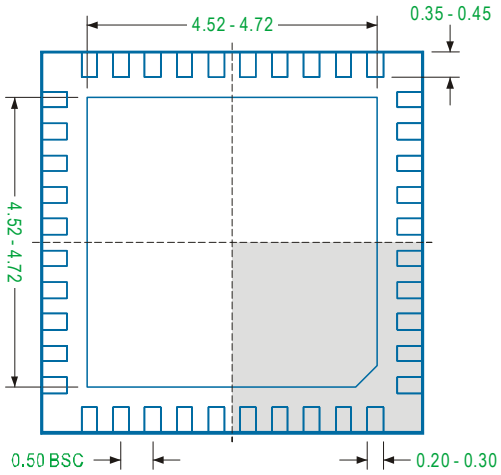


Figure 1. Parasitic Resistance of PCB

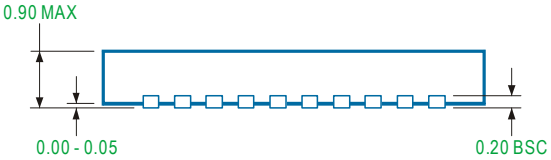
Package Information

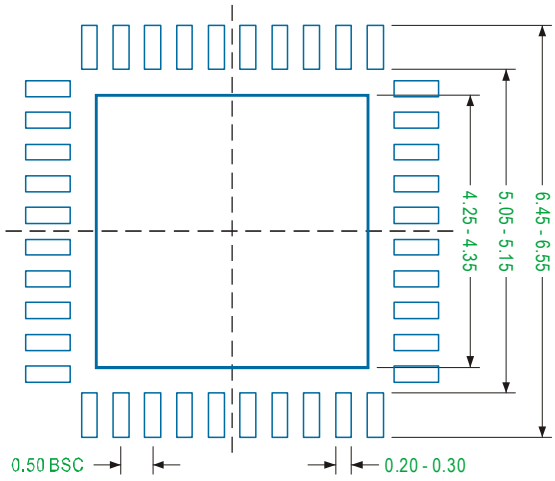
VQFN6x6 - 40L Package





Bottom View - Exposed Pad





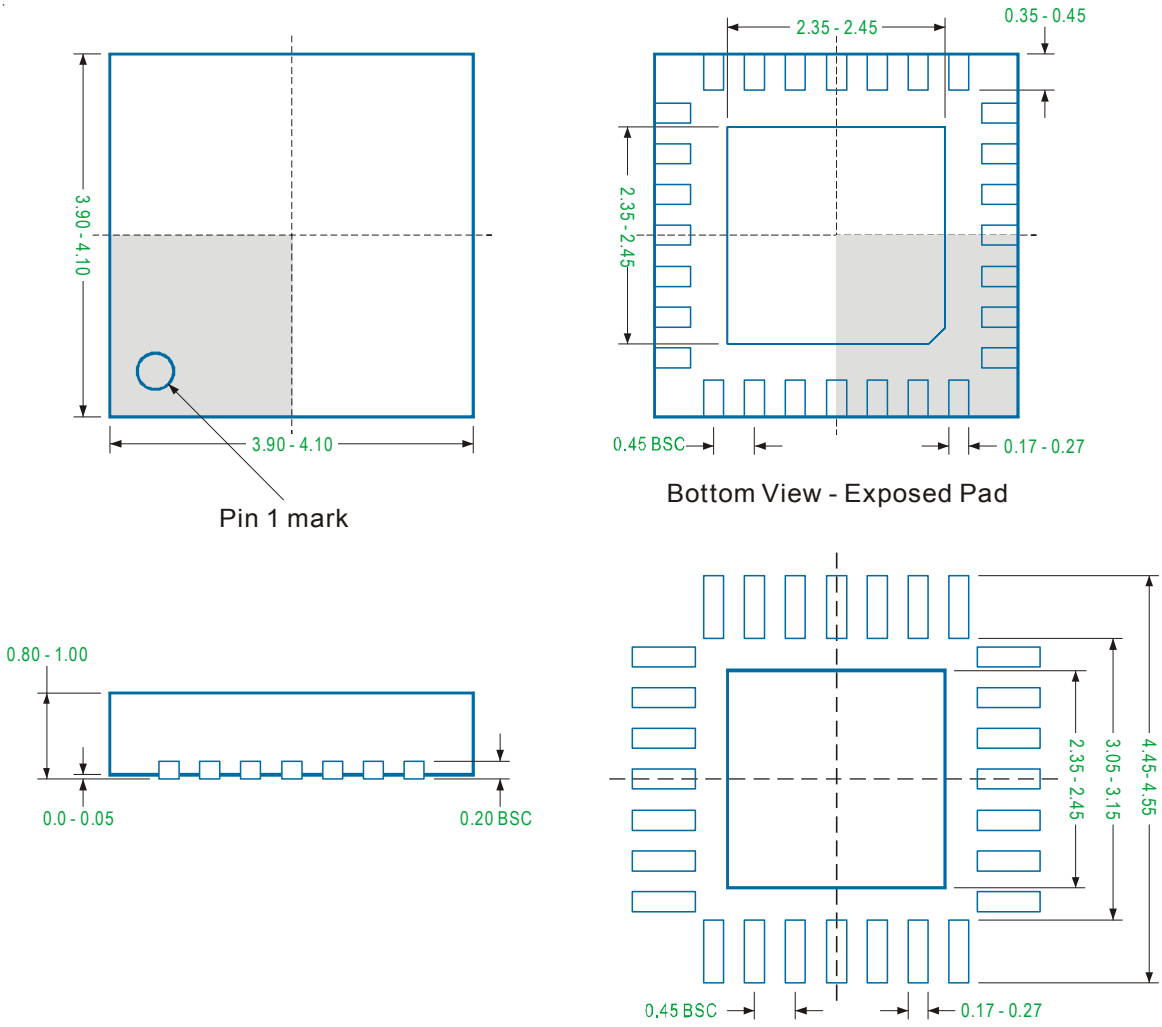
Recommended Solder Pad Pitch and Dimensions

Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.

Package Information

VQFN4x4 - 28L Package



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.