Single Phase PWM Controller for Mobile Applications

General Description

The uP6111A/B is a high performance synchronous-rectified buck controller specifically designed for POL voltage regulation in notebook PC application. The controller operates with 5V bias voltage and converts 2V~26V input voltage to 0.75V~5.5V output voltage.

The uP6111A/B adopts constant-on-time PWM scheme that features easy-to-use, low external component count, fast transient response and quasi constant frequency operation over the operation range. Selectable Forced Continuous Conduction Mode (FCCM) or Power Saving Mode (PSM) enables the flexibility for low noise operation or high efficiency conversion over wide output current range.

Lossless current sensing by $R_{DS(ON)}$ of lower switch achieves programmable over current protection. Other features include internal soft start, integrated bootstrap diode and thermal shutdown. The uP6111A is available in WQFN3x3 -16L and WQFN4x4-16L packages. The uP6111B is available in VQFN3.5x3.5- 14L and TSSOP-14L packages.

Applications

- **Power Supplies for Microprocessors or Subsystem Power Supplies**
- **Cable Modems, Set Top Boxes, and DSL Modems**
- **Industrial Power Supplies; General Purpose Supplies**
- **2V to 26V Input DC-DC Regulators**
- **Low-Voltage Distributed Power Supplies**

Features

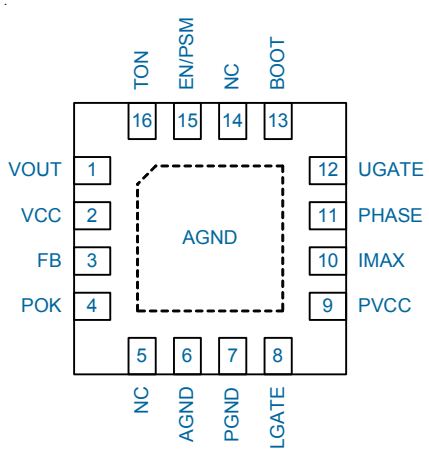
- **Wide Input Voltage Range 2V ~ 26V**
- **Wide Output Voltage Range 0.75V ~ 5.5V**
  - **1.0% Initial Accuracy**
- **Constant On Time PWM**
  - **Quasi Constant Switching Frequency**
  - **Adjustable Frequency from 200kHz to 500kHz**
  - **Ultra Fast Transient Response**
- **Integrated Bootstrap Diode**
- **Integrated MOSFET Drivers with Shoot-Through Protection**
- **Configurable Forced Continuous Current Mode or Power Saving Mode**
- **Lossless, Programmable Overcurrent Protection**
  - **Use Low-Side MOSFET $R_{DS(ON)}$**
- **Internal Soft Start**
- **Over Voltage and Under Voltage Protection**
- **Power OK Indication**
- **WQFN4x4 - 16L, WQFN3x3 - 16L, VQFN3.5X3.5 - 14L, or TSSOP - 14L Packages**
- **RoHS Compliant and 100% Lead Free**

Ordering Information

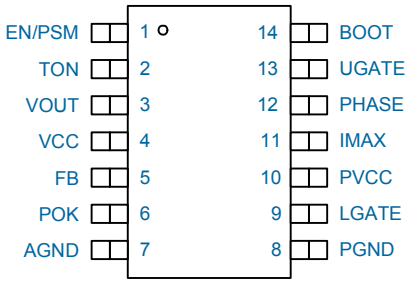
Order Number	Package Type	Remark
uP6111AQED	WQFN4x4 - 16L	Refer to IMAX and TON pin description on P. 5.
uP6111AQDD	WQFN3x3 - 16L	
uP6111BQHC	VQFN3.5x3.5 - 14L	
uP6111BTAC	TSSOP - 14L	

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

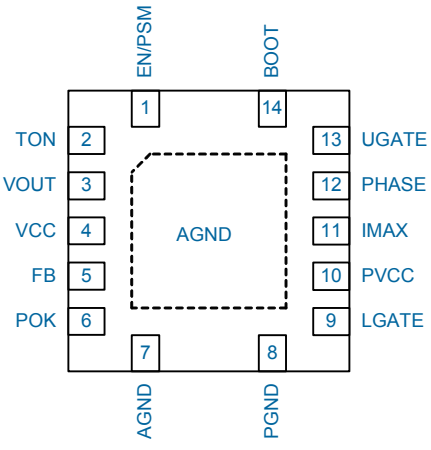
Pin Configuration



WQFN 3x3 or 4x4 – 16L
uP6111A

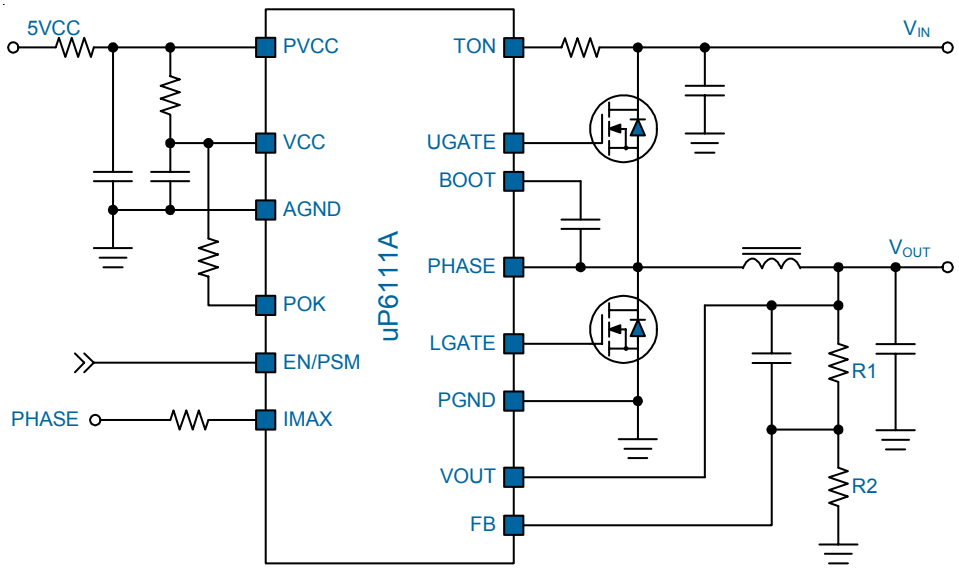


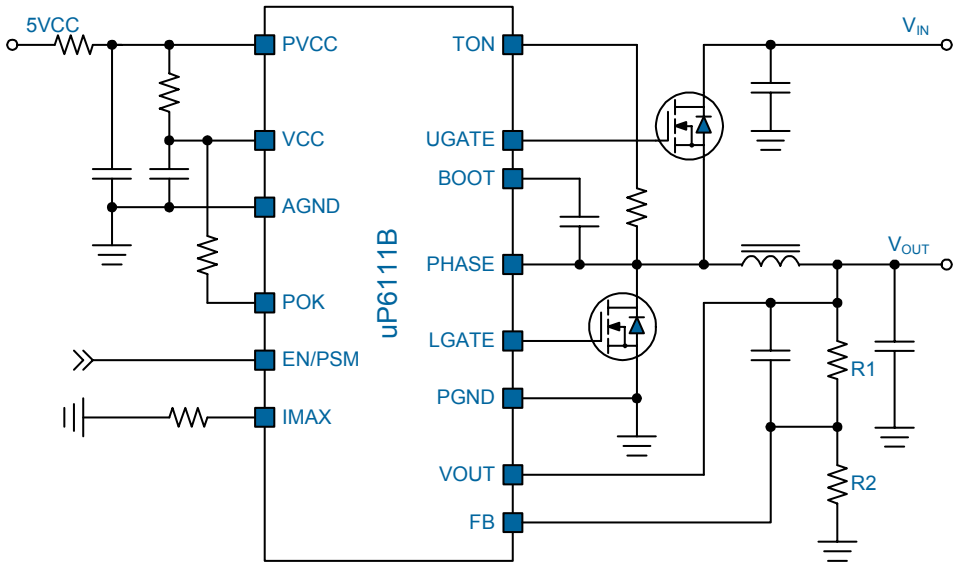
TSSOP-14
uP6111B



VQFN 3.5x3.5-14L
uP6111B

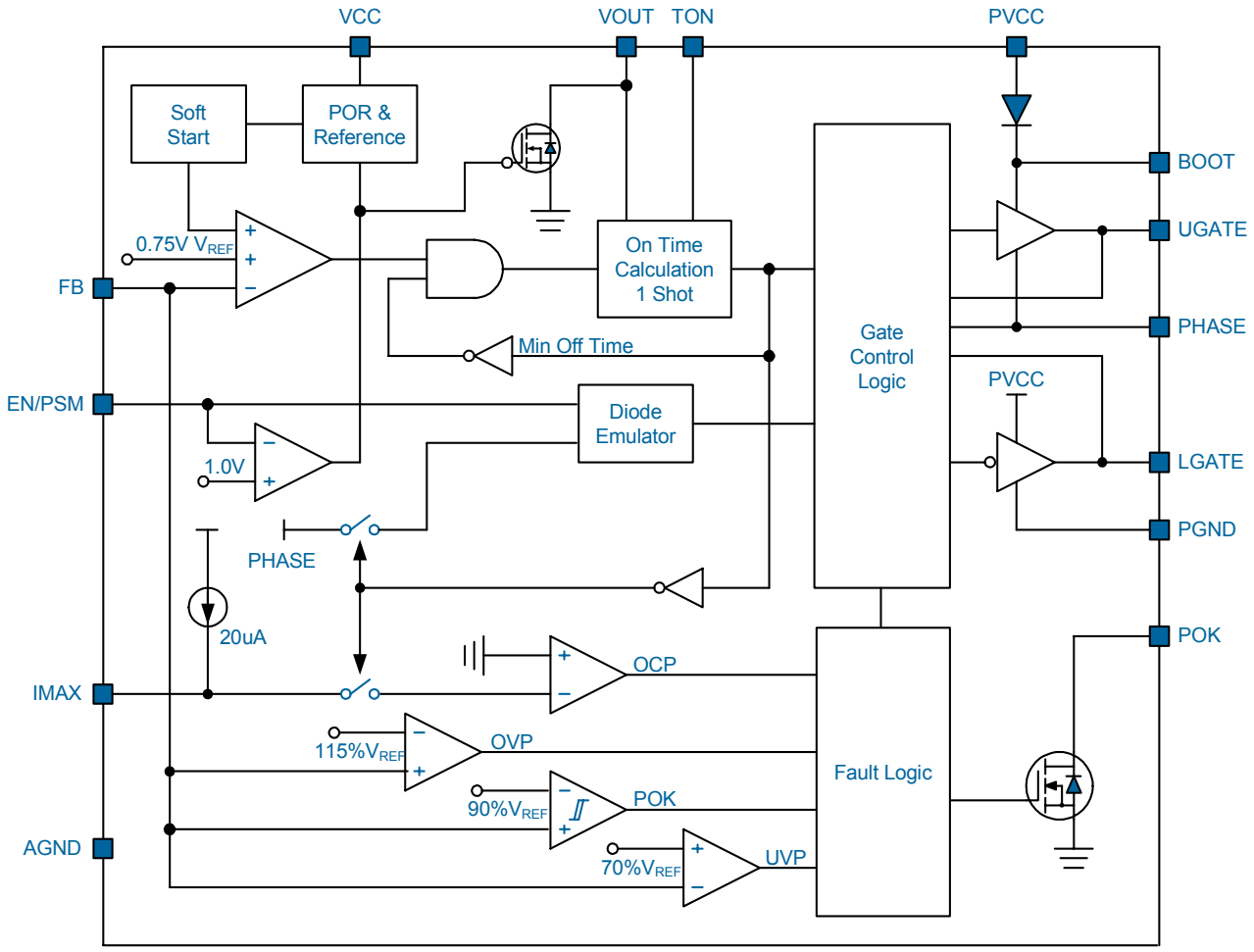
Typical Application Circuit





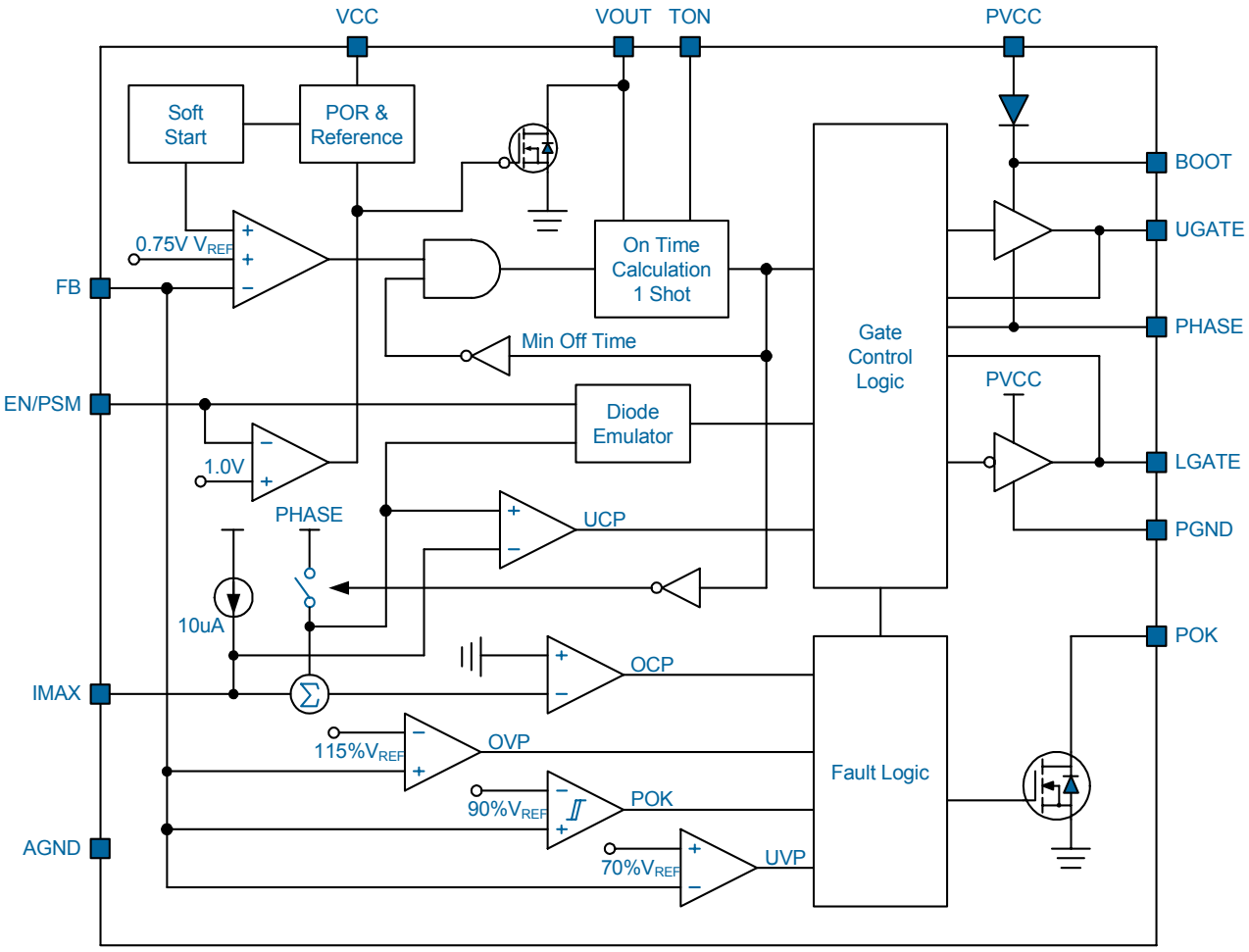
Functional Block Diagram

uP6111A



Functional Block Diagram

uP6111B



Functional Pin Description

Pin Name	Pin Function
VOUT	**Output Voltage Detection.** Connect this pin directly to the converter output voltage for output voltage sensing.
VCC	**Supply Voltage for the IC.** This pin provides bias voltage for the IC. Connect this pin to 5V voltage source and bypass it with a R/C filter.
FB	**Feedback Voltage for Buck Converter.** This pin is the inverting input to the error amplifier. A resistor divider from the output to GND is used to set the regulation voltage.
POK	**Output Voltage OK Indication.** This pin is an open drain output for indicating output voltage status. It is set high impedance when the output voltage is within regulation and no faults occur.
NC	**Not Internally Connected.**
AGND	**Signal Ground for the IC.** All voltages levels are measured with respect to this pin.
PGND	**Power Ground.** This pin is dedicated for lower MOSFET driver and should be directly connected to the source of the lower MOSFET with an isolated path.
LGATE	**Lower Gate Driver Output.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.
PVCC	**Supply Voltage for the Gate Drivers.** This pin provides current for lower gate driver and bootstrap circuit for upper gate driver. Connect this pin to 5V voltage source and bypass it with a R/C filter.
IMAX	**Current Limit Threshold Setting and Sense.** Connect a resistor to drain of low-side MOSFET for $R_{DS(ON)}$ sensing. (uP6111A)
	Over Current Protection Level Seting. Connect a resistor from this pin to AGND to set the OCP level. (uP6111B)
PHASE	**PHASE Switch Node.** Connect this pin to the source of the high-side MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UGATE driver, and to monitor the voltage drop across the lower MOSFET for over current protection. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
UGATE	**Upper Gate Driver Output.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
BOOT	**Bootstrap Supply** for the floating upper gate driver. Connect the bootstrap capacitor C_{BOOT} between BOOT pin and the PHASE pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Typical values for C_{BOOT} range from 0.1uF to 0.47uF. Ensure that C_{BOOT} is placed near the IC.
EN/PSM	**Chip Enable and Mode Selection.** Pulling this pin lower than 0.4V disables the IC and turns off both upper and lower MOSFETs. Tie this pin to VCC for power saving mode (PSM) operation and let this pin float for force continuous conduction mode (FCCM) operation.
TON	**ON Time Programming.** Connect a resistor from this pin to VIN (uP6111A) or PHASE (uP6111B) to set the on-time for the upper MOSFET. $T_{ON} = 3.85x\ 10^{-12} \times R_{TON} \times V_{OUT}/(V_{IN} - 0.5)$ - uP6111A $T_{ON} = 19x\ 10^{-12} \times R_{TON} \times \{[(2/3)V_{OUT} + 100mV]/V_{IN}\} + 50ns$ - uP6111B
Exposed Pad	**Signal Ground for the IC.** All voltages levels are measured with respect to this pin. This exposed pad should be well soldered to PCB for effective heat conduction.

Functional Description

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The uP6111A/B adopts constant-on-time PWM scheme that features easy-to-use, low external component count, fast transient response and quasi constant frequency operation over the operation range. Selectable Forced Continuous Conduction Mode (FCCM) or Power Saving Mode (PSM) enables the flexibility for low noise operation or high efficiency conversion over wide output current range.

Lossless current sensing by $R_{DS(ON)}$ of lower switch achieves programmable over current protection. Other features include internal soft start, integrated bootstrap diode and thermal shutdown.

UVLO, Soft Start and POK

Undervoltage-lockout (UVLO) circuit inhibits switching and reset the protection faults when VCC is below 4V. Both LGATE and UGATE drivers are turned off during UVLO.

The soft start of uP6111A/B is achieved by internal ramp wave SS with over current limit, results in an internal 1.2ms soft start. The error is an tri-input device, SS or V_{REF} which ever is smaller dominates the behavior of non-inverting input of the error amplifier. On VCC is over its 4V UVLO level and EN/PSM is floating or high, soft start SS begins to ramp up. The SS signal is created digitally by internal circuit. It takes 1.2ms for the SS to ramp up from 0V to 0.75V. The feedback voltage V_{FB} is regulated to follow the SS during the soft start, resulting in smooth ramp up of the output voltage.

The V_{REF} takes over the control after SS is over 0.75V. The SS keeps ramping up to 1.6V, taking about extra 1.5ms. The uP6111A/B asserts soft start end when the SS reaches about 1.6V.

The POK is an open drain output. The uP6111A/B asserts POK high impedance output if the output voltage is within regulation with about 45us time delay after soft start end. If the output voltage is out of 10% of the target value, the POK signal will become low immediately.

Output Voltage Setting

The output voltage can be adjusted from 0.75V to 5.5V by setting the feedback resistors R1 and R2 (see the Typical Application Circuit). The following equaion is for adjudting the ouput voltage.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{FB} is 0.75V (typ.) and keep R2 about 10kΩ to choose R1 value.

Operation Mode

The uP6111A/B supports selectable froced continuous conduction mode (FCCM) and power saving mode (PSM) operations. If EN/PSM is grounded, the switching regulator is disabled. If the EN/PSM pin is connected to 3.3V or 5V, the regulator is enabled with PSM selected. If the EN/PSM pin is floated, it is internally pulled up to 1.9V, and the regulator is enabled with FCCM.

The uP6111A/B features a control loop as adaptive on-time and minimum off-time pulse width modulation (PWM). The upper MOSFET is turned on at the beginning of each cycle. It is turned off after the internal one-shot timer expires. Another cycle initiates when the feedback voltage V_{FB} is lower than the internal reference voltage V_{REF} and the minimum off-time expires. This regulates the valley of V_{FB} at V_{REF}.

For uP6111A, the one-shot timer is programmed by a resistor R_{TON} connected from TON pin to V_{IN} as:

$$T_{ON} = 3.85pF \times R_{TON} \times \frac{V_{OUT}}{V_{IN} - 0.5V}$$

where 3.85pF is the internal timing capacitor.

For uP6111B, the one-shot timer is programmed by a resistor R_{TON} connected from TON pin to PHASE pin as:

$$T_{ON} = 19pF \times R_{TON}\left(\frac{(2/3)V_{OUT} + 100mV}{V_{IN}}\right) + 50ns$$

where 19pF is the internal timing capacitor, and 50ns represents the turn-off delay time caused by the internal circuit and high-side MOSFET.

The on-time is determined by V_{IN} and V_{OUT} and is kept fairly constant over a wide input and output voltage range at steady state. These equations provide a good approximation to start with, but the accuracy will be affected by design and selection of high-side MOSFET.

Figure 1 and 2 illustrate the switching frequency vs. R_{TON} relationship for uP6111A and uP6111B respactively.

Functional Description

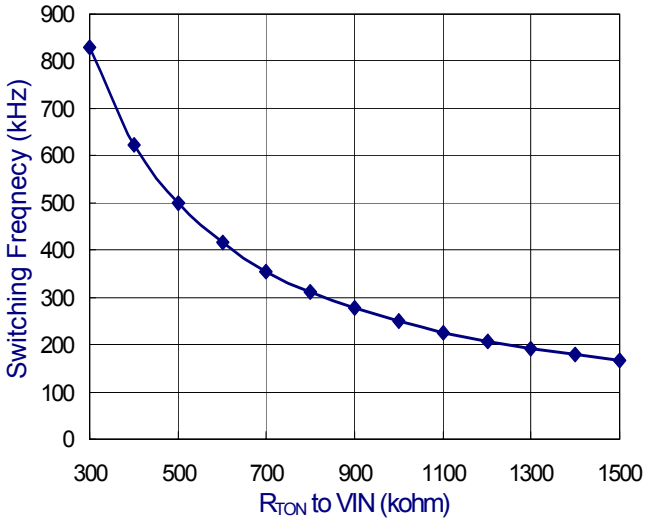


Figure 1. Switching Frequency vs. $R_{TON.}$ (uP6111A)

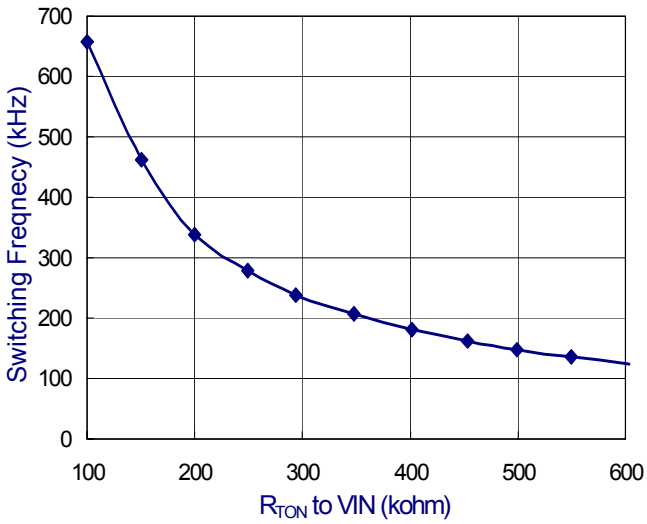


Figure 2. Switching Frequency vs. $R_{TON.}$ (uP6111B)

Power Saving Mode Operation

The uP6111A/B automatically reduces switching frequency at light load to maintain high efficiency when PSM is selected by connecting EN/PSM to VCC. The frequency reduction is achieved smoothly and without increasing V_{OUT} ripple or load regulation.

As the output current decreases from heavy load condition, the inductor current also decreases and eventually comes to the point that its valley touches zero current at the boundary between continuous and discontinuous conduction modes. The uP6111A/B emulates conventional asynchronous buck converter by turning off the lower MOSFET when zero inductor current is detected. As the load current decreased, the converter runs in discontinuous conduction mode and it takes a long time to discharge the output capacitor to next ON cycle.

High/Low Side Gate Drivers

The lower gate driver is designed to work with high-current and low $R_{DS(ON)}$ N-channel MOSFETs. The lower gate driver is powered by PVCC pin. The driving capability is represented by its internal resistance, that is 1.5Ω for sourcing and 1.0Ω for sinking. A dead time to prevent shoot through is internally generated between upper MOSFET off to lower MOSFET on and lower MOSFET off to upper MOSFET on.

The upper gate driver is designed to work with high-current and low $R_{DS(ON)}$ N-channel MOSFETs. The upper gate driver work with bootstrap circuit formed by BOOT and PHASE pins. The bootstrap diode is integrated to simplified circuit and PCB design. An external Schottky diode can be used if the forward drop voltage is critical to achieve best efficiency. The driving capability is represented by its internal resistance, that is 3.0Ω for sourcing and 1.0Ω for sinking.

Output Discharge Control (Soft Stop)

The uP6111A/B features the soft stop function that discharges the output when the converter is disabled or in a fault condition (UVP, OVP, UVLO or thermal shutdown.) The discharge path is through VOUT, internal 20Ω MOSFET and PGND pins. The discharge time constant is a function of the output capacitance and resistance of the discharge MOSFET.

Over Current Protection (uP6111A)

The uP6111A features cycle-by-cycle current limit function. The uP6111A monitors the inductor current by lower MOSFET $R_{DS(ON)}$ when it turns on as shown in Figure 3.

The uP6111A sources a 20uA current source out of IMAX pin and creates a voltage as:

$$V_{IMAX} = R_{IMAX} \times 20uA + V_{PHASE}$$

The high side MOSFET will not turn on if the VIMAX voltage is lower than zero even the voltage loop demands the it to be turned on. The current limit level is calculated as:

$$I_{LIM} = \frac{R_{IMAX} \times 20uA}{R_{DS(ON)}} + \frac{I_{RIPPLE}}{2}$$

where $R_{DS(ON)}$ is the on resistance of lower MOSFET and I_{RIPPLE} is the inductor current ripple.

The output voltage decreases and eventually triggers the under voltage protection if the load continuously demands current larger than the current limit level.

Functional Description

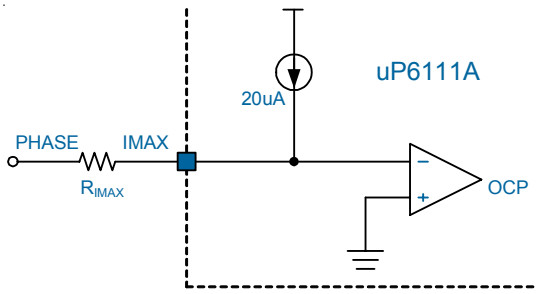


Figure 3. Current Limit of uP6111A.

Over Current Protection (uP6111B)

The uP6111B features cycle-by-cycle current limit function. The uP6111B monitors the inductor current by lower MOSFET $R_{DS(ON)}$ when it turns on as shown in Figure 4.

The uP6111B sources a 10uA current source out of IMAX pin and creates a voltage as:

$$V_{IMAX} = R_{IMAX} \times 10uA$$

The IMAX voltage is added to PHASE pin voltage for current limit function. The high side MOSFET will not turn on if the summation is lower than zero even the voltage loop demands the it to be turned on. The current limit level is calculated as:

$$I_{LIM} = \frac{V_{IMAX}}{R_{DS(ON)}} + \frac{I_{RIPPLE}}{2}$$

where $R_{DS(ON)}$ is the on resistance of lower MOSFET and I_{RIPPLE} is the inductor current ripple.

The output voltage decreases and eventually triggers the under voltage protection if the load continuously demands current larger than the current limit level.

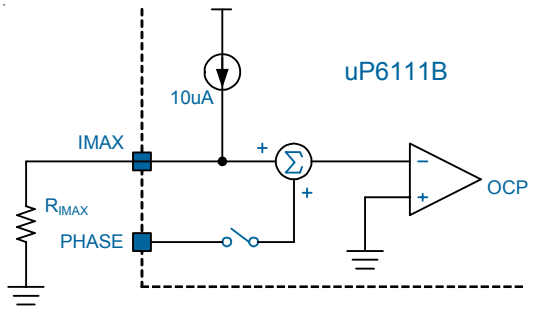


Figure 4. Current Limit of uP6111B.

Over Voltage/Under Voltage Protection

The uP6111A/B monitors feedback voltage V_{FB} for over voltage and under voltage protection. The uP6111A/B asserts over voltage protection and turns on the lower MOSFET and turns off upper MOSFET when the V_{FB} voltage is over 115% of its target value with 30us delay. The OVP protection is latch-off type. It can only be reset by UVLO or toggling the EN/PSM pin.

The uP6111A/B asserts under voltage protection and turns off both upper and lower MOSFETs if the V_{FB} voltage is lower than 70% of its target value with 4us delay. The UVP protection is latch-off type. It can only be reset by UVLO or toggling the EN/PSM pin. The UVP function is disables during soft cycle.

Thermal Protection

The uP6111A/B monitors the temperature of itself. If the temperature exceeds typical 150°C, the uP6111A/B will be turned off .This is non-latch protection. It will be recovered once temperature is lower 130°C.

Absolute Maximum Rating

Supply Input Voltage, VIN (Note 1) ---------- -0.3V to +28V
VCC & PVCC to GND ---------- -0.3V to +6V
BOOT to PHASE ---------- -0.3V to +6V
PHASE to GND
- DC ---------- -0.7V to 28V
- < 200ns ---------- -8V to 36V

BOOT to GND
- DC ---------- -0.3V to PVCC + 28V
- < 200ns ---------- -0.3V to 42V

UGATE to PHASE
- DC ---------- -0.3V to (BOOTx - PHx +0.3V)
- <200ns ---------- -5V to (BOOTx - PHx + 0.3V)

LGATE to GND
- DC ---------- -0.3V to + (PVCC + 0.3V)
- <200ns ---------- -5V to PVCC + 0.3V

Other Pins to GND ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
- HBM (Human Body Mode) ---------- 2kV
- MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
- θ_{JA} WQFN4x4-16L ---------- 37°C/W
- θ_{JA} WQFN3x3-16L ---------- 68°C/W
- θ_{JA} VQFN3.5x3.5-14L ---------- 42 °C/W
- θ_{JA} TSSOP- 14L ---------- 133°C/W
- θ_{JC} WQFN4x4-16L ---------- 3°C/W
- θ_{JC} WQFN3x3-16L ---------- 5°C/W

Power Dissipation, P_D @ T_A = 25°C
- WQFN4x4-16L ---------- 2.70W
- WQFN3x3-16L ---------- 1.47W
- VQFN3.5x3.5-14L ---------- 2.38W
- TSSOP -14L ---------- 0.75W

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4) ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Power Input Voltage, V_{IN} ---------- +2V to 26V
Supply Input Voltage, PV_{CC} , V_{CC} ---------- +4.5V to 5.5V

Electrical Characteristics

(PV_{CC} = V_{CC} = 5.0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Power Input Voltage Range	V_{IN}		2	--	26	V
Supply Input Voltage Range	V_{CC}, PV_{CC}		4.5	--	5.5	V
VCC POR Rising Threshold	V_{CCRTH}	VCC rising	3.7	4.0	4.3	V
VCC POR Hysteresis	V_{CCHYS}		--	0.3	--	V
Supply Current	I_Q	I_{VCC} + I_{PVC}, V_{FB} = 0.8V. EN/PSM = VCC	--	300	--	uA
Shutdown Current	I_{SHDN}	I_{VCC} + I_{PVCC}, TON = floating, EN/PSM = GND	--	5	10	uA
VOUT and FB						
V_{FB} Regulation Voltage Accuracy	V_{FB}		742.5	750	757.5	mV
V_{FB} Regulation Voltage Tolerance	V_{FB_TOL}	T_A = 25°C, bandgap initial accuracy	-1.0	--	1.0	%
		T_A = 0°C to 85 °C	-1.3	--	1.3	
		T_A = -40°C to 85°C	-1.3	--	1.3	
FB Bias Current		V_{FB} = 0.75V	-0.1	--	0.1	uA
Output Voltage Range	V_{OUT}		0.75	--	5.5	V
VOUT Discharging Resistance	R_{OUT}	EN/PSM = GND	--	20	32	Ω
On Time and Internal Soft Start (uP6111A)						
Nominal On Time	T_{ON_N}	V_{IN} = 15V, V_{OUT} = 1.25V, R_{TON} = 1MΩ	264	330	396	ns
Minimum Off Time	$T_{OFF(MIN)}$		--	440	--	ns
Internal Soft Start Time	T_{SS}	from EN/PSM > 1V to V_{FB} >0.71V	0.9	1.2	1.5	ms
On Time and Internal Soft Start (uP6111B)						
Nominal On Time	T_{ON_F}	V_{PHASE} = 12V, V_{OUT} = 2.5V, R_{TON} = 100kΩ	264	330	396	ns
Minimum Off Time	$T_{OFF(MIN)}$		--	440	--	ns
Internal Soft Start Time	T_{SS}	from EN/PSM > 1V to V_{FB} >0.71V	0.9	1.2	1.5	ms
Gate Drivers						
UGATE Driver Sourcing	R_{H_SRC}	I_{H_SRC} = 150mA	--	3.0	6.0	Ω
UGATE Driver Sinking	R_{H_SNK}	I_{H_SNK} = 150mA	--	1.0	2.0	Ω
LGATE Driver Sourcing	R_{L_SRC}	I_{L_SRC} = 150mA	--	1.5	3.0	Ω
LGATE Driver Sinking	R_{L_SNK}	I_{L_SNK} = 150mA	--	1.0	2.0	Ω
Dead Time		by design	--	20	--	ns
Bootstrap Diode						
Forward Voltage	V_{BST_F}	I_F = 10mA	0.7	0.8	0.9	V
Reverse Leakage Current	I_{BST_LK}	V_{BOOT} = 28V	--	0.1	1	uA

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Sense						
IMAX Source Current	I_{IMAX}	uP6111A	18	20	22	uA
		uP6111B	9	10	11	uA
OCP Comparator Offset	V_{OC_OFS}		-10	0	10	mV
Negative OCP Comparator Offset	V_{OC_OFS}	for uP6111B only	-9.5	0.5	10.5	mV
Zero Crossing Comparator Offset	V_{ZC_OF}		-9.5	0.5	10.5	mV
Logic and Protection Level						
EN/PSM Logic Low			--	--	0.7	V
EN/PSM Logic High			2.9	--	--	V
EN/PSM Floating Level			1.6	1.9	2.2	V
EN/PSM Source Current	$I_{EN/PSM}$	EN/PSM = GND	--	1	--	uA
Power OK Threshold From Lower		V_{FB} rising, percentage of V_{REF}	87	90	93	%
Power OK Low Hysteresis		V_{FB} falling, percentage of V_{REF}	--	-3	--	%
Power OK Threshold Fom Higher		V_{FB} falling, percentage of V_{REF}	107	110	113	%
Power OK High Hysteresis		V_{FB} rising, percentage of V_{REF}	--	3	--	%
Power OK Sinking Current	I_{POK}	V_{POK} = 0.5V.	2	--	--	mA
Power OK Delay Time			--	45	--	us
Over Voltage Trip Level	V_{OVP}	percentage of V_{REF}	111	115	119	%
Over Voltage Delay Time			--	30	--	us
Under Voltage Trip Level	V_{UVP}	percentage of V_{REF}	65	70	75	%
Under Voltage Delay Time			--	4	--	us
OTP Temperature Level	T_{OTTH}		--	150	--	°C
OTP Temperature Hysteresis	T_{OTHYS}		--	20	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

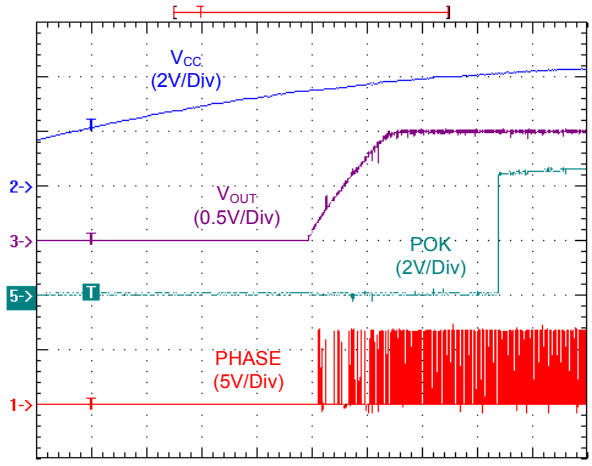
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

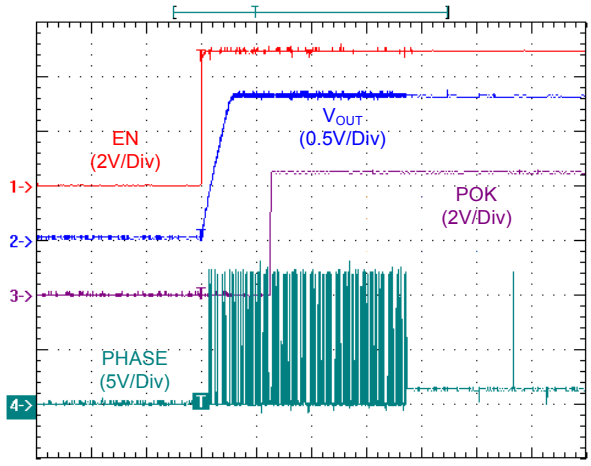
Typical Operation Characteristics

Power On Waveforms



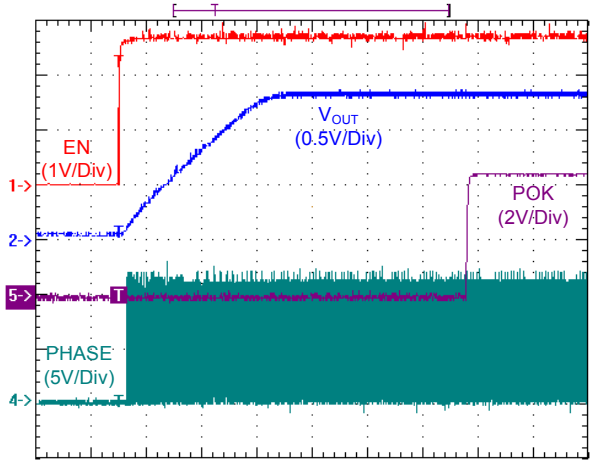
Time: 1ms/Div
V_{IN} = 7.0V, V_{CC} = 5V

Turn On Waveforms @ PSM



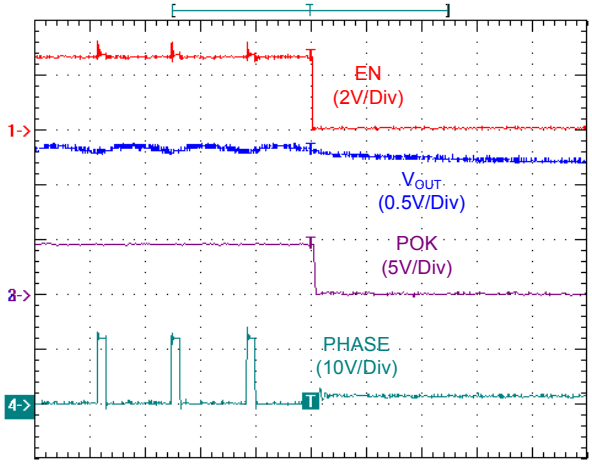
Time: 2.5ms/Div
V_{IN} = 12V, V_{CC} = 5V

Turn On Waveforms @ FCCM



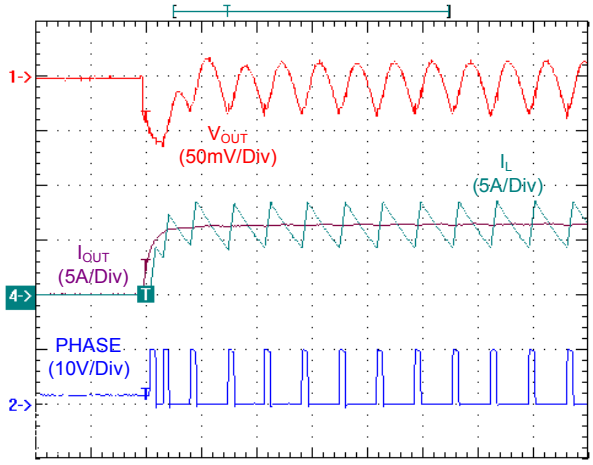
Time: 500us/Div
V_{IN} = 12V, V_{CC} = 5V

Turn Off @ FCCM



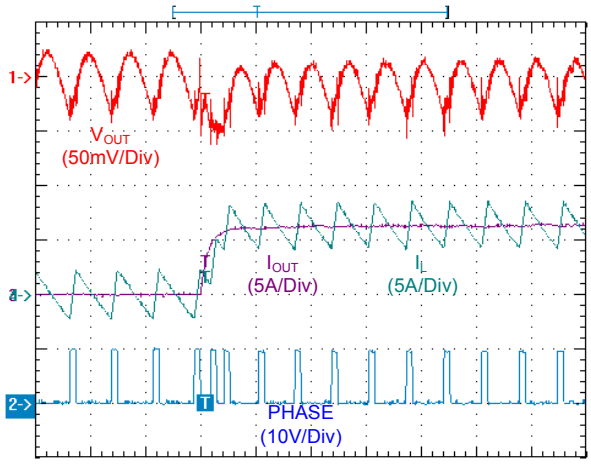
Time: 2.5us/Div
V_{IN} = 12V, V_{CC} = 5V, I_{OUT} = 2A

Load Transient Response



Time: 5us
V_{IN} = 10V, V_{OUT} = 1.5V, I_{OUT} = 0 to 8A transient, PSM

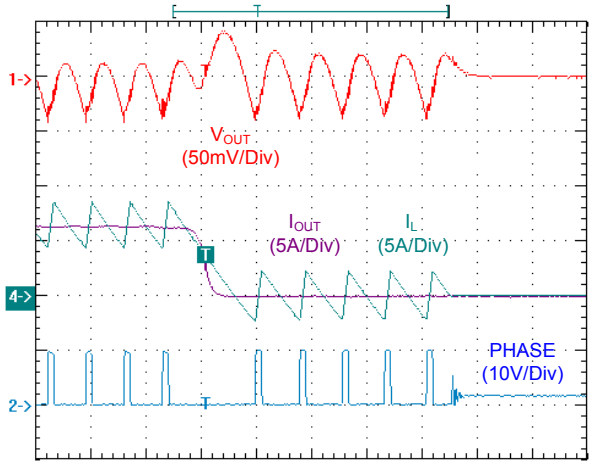
Load Transient Response



Time: 5us
V_{IN} = 10V, V_{OUT} = 1.5V, I_{OUT} = 0 to 8A transient, FCCM

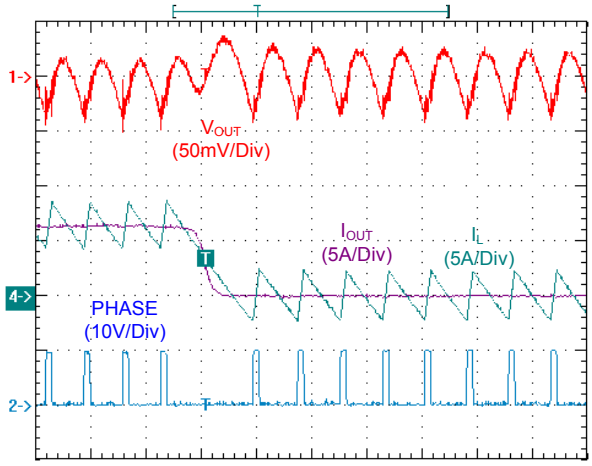
Typical Operation Characteristics

Load Transient Response



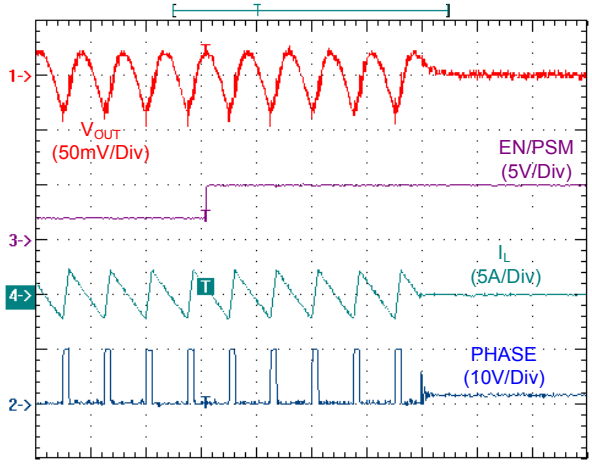
Time: 5us/Div
V_{IN} = 10V, V_{OUT} = 1.5V, I_{OUT} = 8 to 0A transient, PSM

Load Transient Response



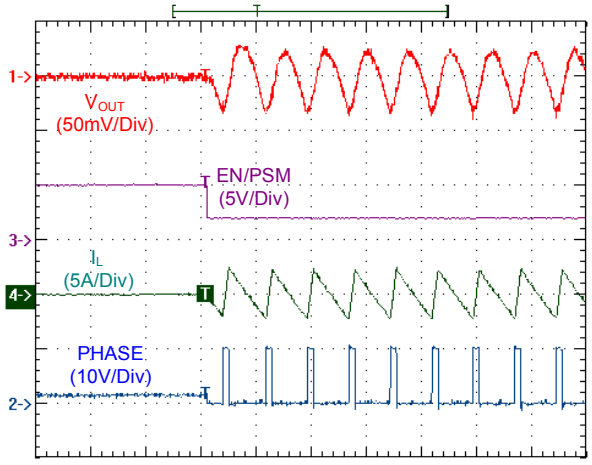
Time: 5us/Div
V_{IN} = 10V, V_{OUT} = 1.5V, I_{OUT} = 8 to 0A transient, FCCM

FCCM toPSM Transition



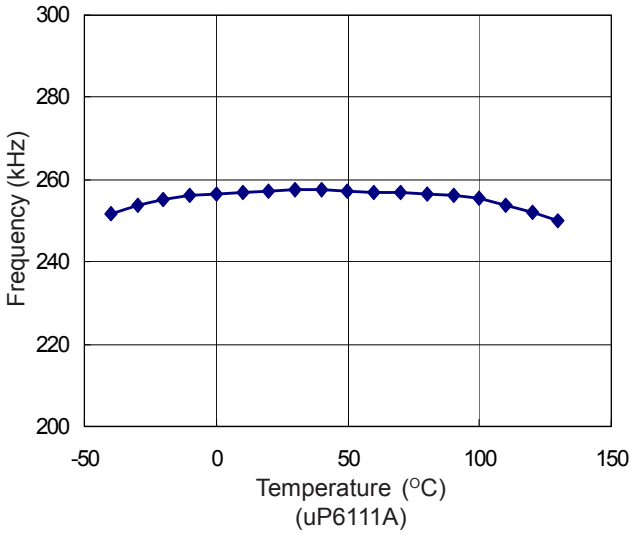
Time: 5us
V_{IN} = 10V, V_{OUT} = 1.5V

PSM to FCCM Transition

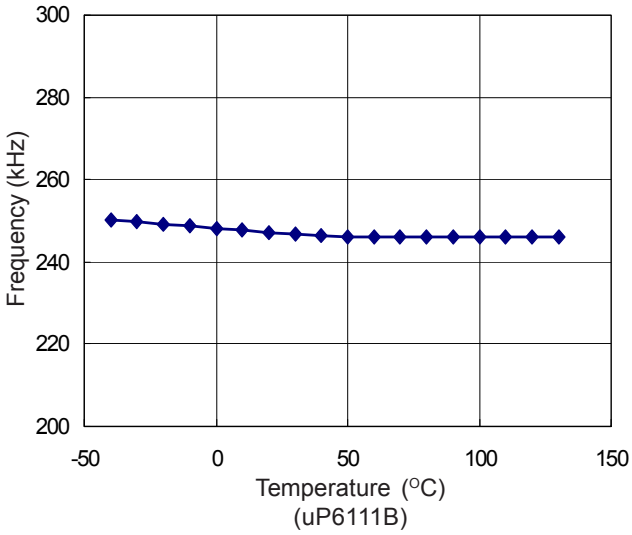


Time: 5us
V_{IN} = 10V, V_{OUT} = 1.5V

Frequency vs. Temperature

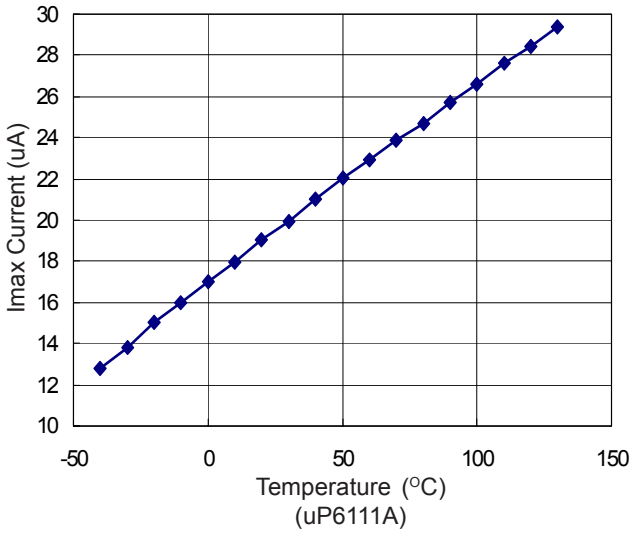


Frequency vs. Temperature

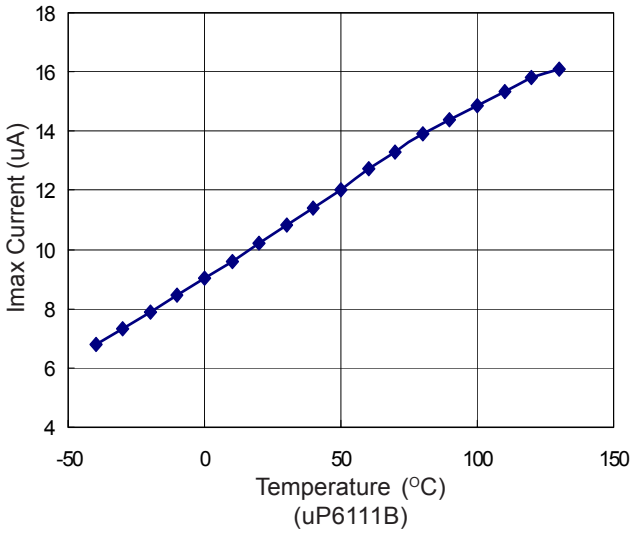


Typical Operation Characteristics

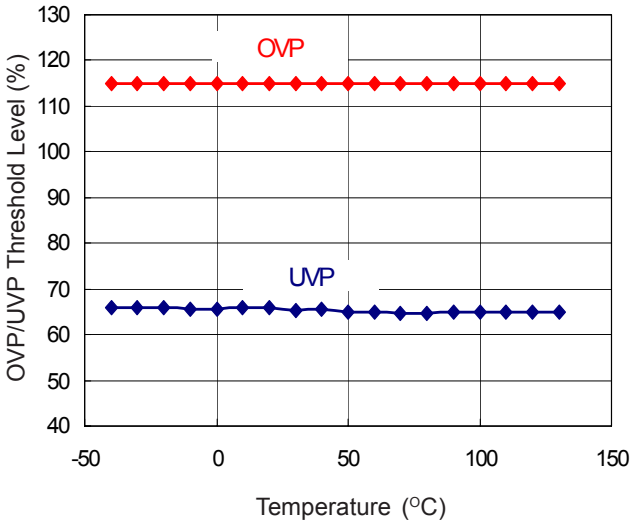
Imax Current vs. Temperature



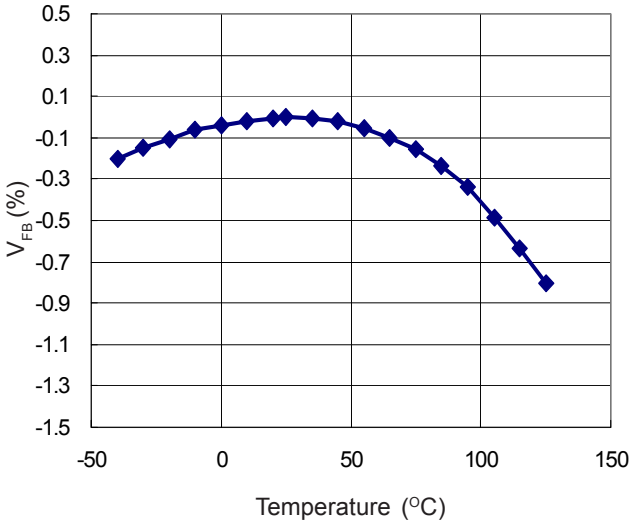
Imax Current vs. Temperature



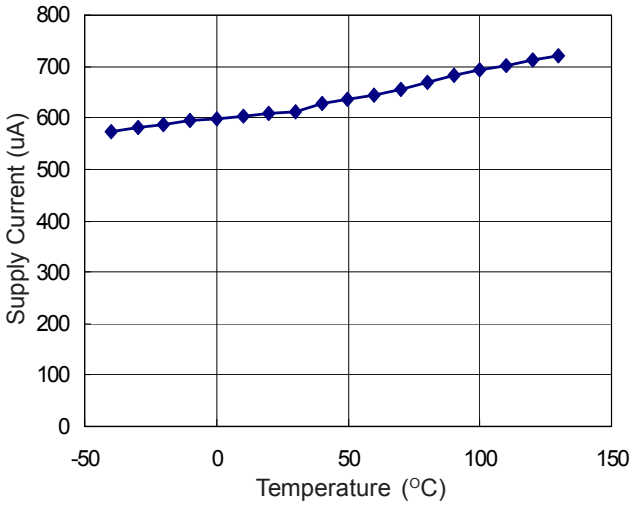
OVP/UVP Threshold vs. Temperature



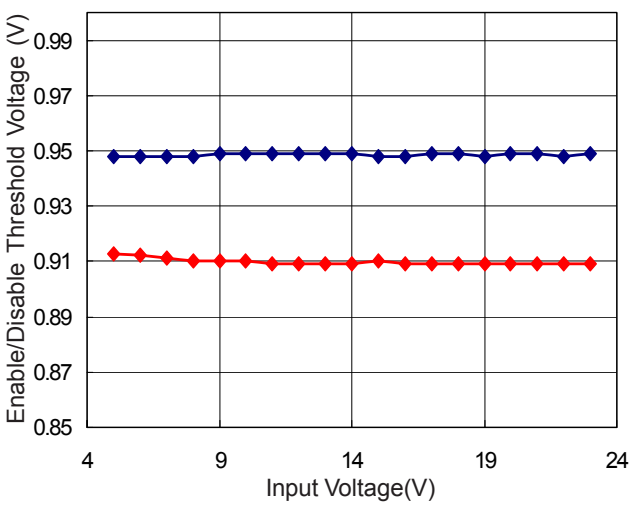
V_{FB} vs. Temperature



Supply Current vs. Temperature

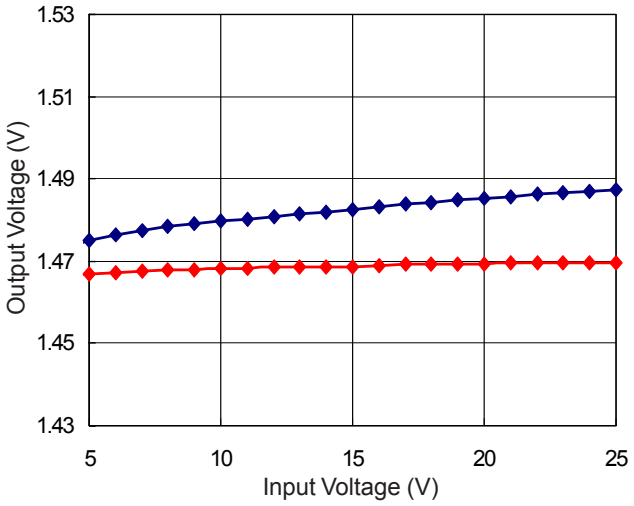


Enable/Disable Threshold Voltage vs. V_{IN}

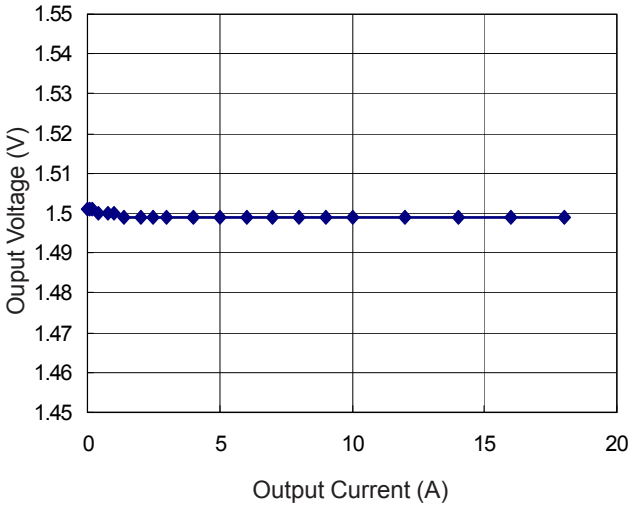


Typical Operation Characteristics

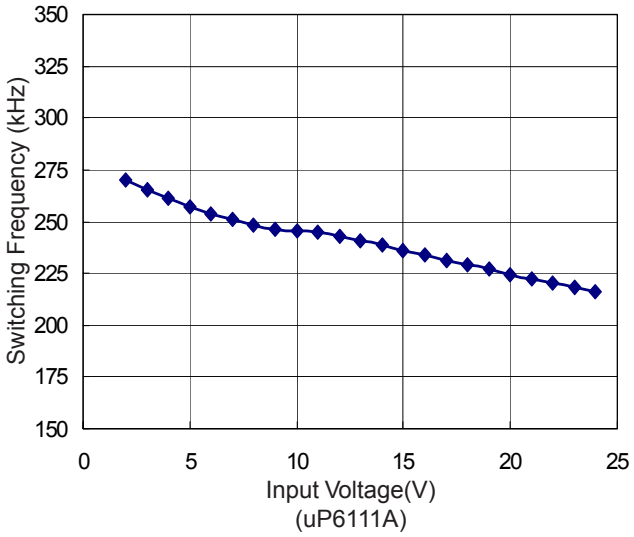
Line Regulation



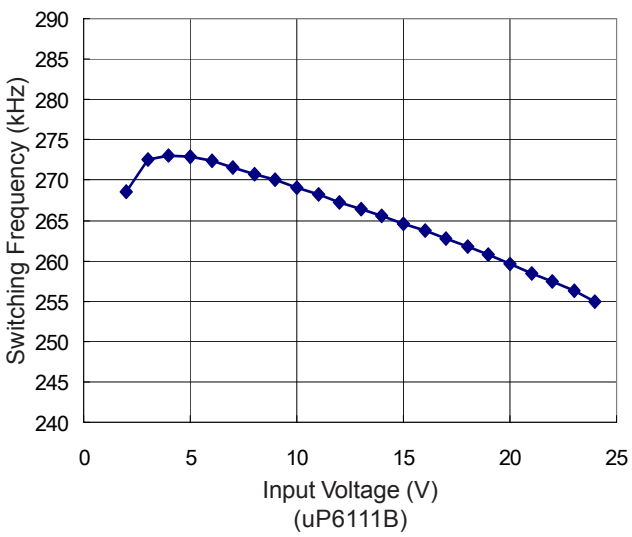
Load Regulation



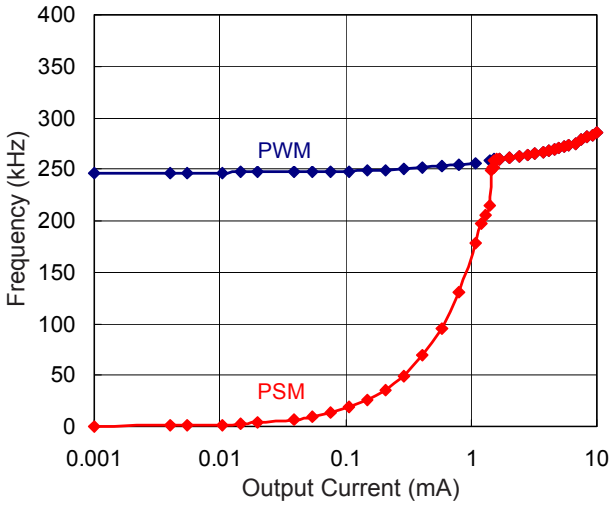
Switchung Frequency vs. Input Voltage



Switching Frequency vs. Input Voltage



Frequency vs. Output Current



Application Information

Component Selection

External component selection is primarily determined by the maximum load current and begins with the selection of power MOSFET switches. The uP6111A/B uses the on-resistance of the lower switch for determining the inductor current. The desired amount of ripple current and operating frequency largely determines the inductor value. Finally, C_{IN} is selected for its ability to handle the large RMS current into the converter and C_{OUT} is chosen with enough ESR to meet the stability, output voltage ripple and transient specification.

Power MOSFET Selection

The uP6111A/B requires two external N-channel power MOSFETs for upper (controlled) and lower (synchronous) switches. Important parameters for the power MOSFETs are the breakdown voltage $V_{(BR)DSS}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, maximum current $I_{DS(MAX)}$, gate supply requirements, and thermal management requirements.

The gate drive voltage is powered by PVCC pin that receives 4.5V~5.5V supply voltage. When operating with a 5V power supply for PVCC, a wide variety of NMOSFETs can be used. .Since the lower MOSFET is used as the current sensing element, particular attention must be paid to its on-resistance. Look for $R_{DS(ON)}$ ratings at lowest gate driving voltage.

Special cautions should be exercised on the lower switch exhibiting very low threshold voltage $V_{GS(TH)}$. The shoot-through protection present aboard the uP6111A/B may be circumvented by these MOSFETs if they have large parasitic impedances and/or capacitances that would inhibit the gate of the MOSFET from being discharged below its threshold level before the complementary MOSFET is turned on. Also avoid MOSFETs with excessive switching times; the circuitry is expecting transitions to occur in under 50 ns or so.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty cycle. Since the uP6111A/B is operating in continuous conduction mode, the duty cycles for the MOSFETs are:

$$D_{UP} = \frac{V_{OUT}}{V_{IN}} ; \quad D_{LO} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The resulting power dissipation in the MOSFETs at maximum output current are:

$$P_{UP} = I_{OUT}^2 \times R_{DS(ON)} \times D_{UP} + 0.5 \times I_{OUT} \times V_{IN} \times T_{SW} \times f_{OSC}$$

$$P_{LO} = I_{OUT}^2 \times R_{DS(ON)} \times D_{LO}$$

where T_{SW} is the combined switch ON and OFF time.

Both MOSFETs have I^2R losses and the top MOSFET includes an additional term for switching losses, which are largest at high input voltages. The bottom MOSFET losses are greatest when the bottom duty cycle is near 100%, during a short-circuit or at high input voltage. These equations assume linear voltage current transitions and do not adequately model power loss due the reverse-recovery of the lower MOSFET's body diode. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

The gate-charge losses are dissipated by the uP6111A/B and don't heat the MOSFETs. However, large gate charge increases the switching interval, T_{SW} that increases the MOSFET switching losses. The gate-charge losses are calculated as:

$$P_G = V_{CC} \times (V_{CC} \times (C_{ISS\_UP} + C_{ISS\_LO}) + V_{IN} \times C_{RSS}) \times f_{OSC}$$

where C_{ISS_UP} is the input capacitance of the upper MOSFET, C_{ISS_LO} is the input capacitance of the lower MOSFET, and C_{RSS_UP} is the reverse transfer capacitance of the upper MOSFET. Make sure that the gate-charge loss will not cause over temperature at uP6111A/B, especially with large gate capacitance and high supply voltage.

Output Inductor Selection

Output inductor is usually selected by considering inductance, rated current value, size requirement and DC resistance (DCR).

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{1}{f_{OSC} \times L_{OUT}} \times V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade off between

Application Information

component size, efficiency and operating frequency. A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$.

There is another trade off between output ripple current/ voltage and response time to a transient load. Increasing the value of inductance reduces the output ripple current and voltage. However, the large inductance values reduce the converter response time to a load transient.

Maximum current ratings of the inductor are generally specified in two methods: permissible DC current and saturation current. Permissible DC current is the allowable DC current that causes 40°C temperature raise. The saturation current is the allowable current that causes 10% inductance loss. Make sure that the inductor will not saturate over the operation conditions including temperature range, input voltage range, and maximum output current.

The size requirements refer to the area and height requirement for a particular design. For better efficiency, choose a low DC resistance inductor. DCR is usually inversely proportional to size.

Different core materials and shapes will change the size/ current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements.

Input Capacitor Selection

The synchronous-rectified buck converter draws pulsed current with sharp edges from the input capacitor resulting in ripples and spikes at the input supply voltage. Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time upper MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of upper MOSET and the source of lower MOSFET to avoid the stray inductance along the connection trace.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck converter is calculated as:

$$I_{IN(RMS)} = I_{OUT(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{IN(RMS)} = I_{OUT(RMS)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

For a through-hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can also be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The output ripple ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}}\right)$$

Since ΔIL increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types.

The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout. Modern components and loads are capable of producing transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

Application Information

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes.

However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading.

Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Bootstrap Capacitor Selection

An external bootstrap capacitor C_{BOOT} connected to the BOOT pin supplies the gate drive voltage for the upper MOSFET. This capacitor is charged through the internal diode when the PHASE node is low. When the upper MOSFET turns on, the PHASE node rises to V_{IN} and the BOOT pin rises to approximately V_{IN} + PV_{CC}. The boot capacitor needs to store about 100 times the gate charge required by the upper MOSFET. In most applications 0.1μF to 0.47μF, X5R or X7R dielectric capacitor is adequate.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} x (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value.

During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

PCB Layout Considerations

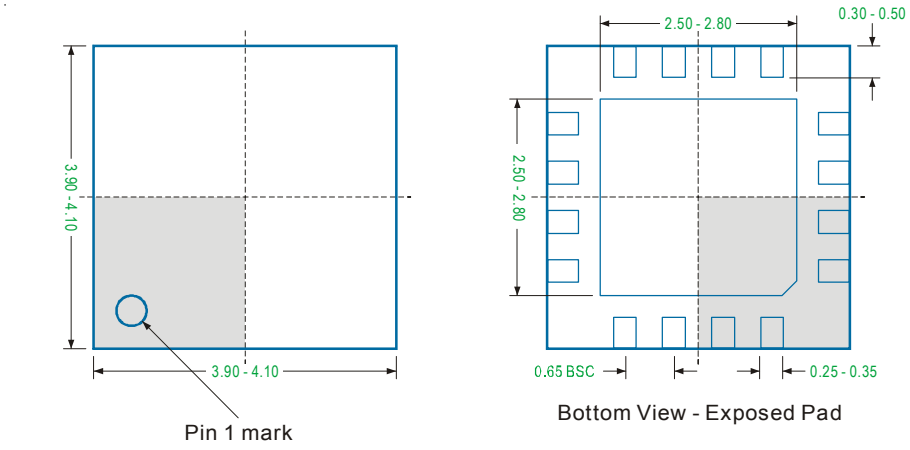
High speed switching and relatively large peak currents in a synchronous-rectified buck converter make the PCB layout a very important part of design. Fast current switching from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency and radiate noise that result in overvoltage stress on devices. Careful component placement and printed circuit design minimize the voltage spikes induced in the converter.

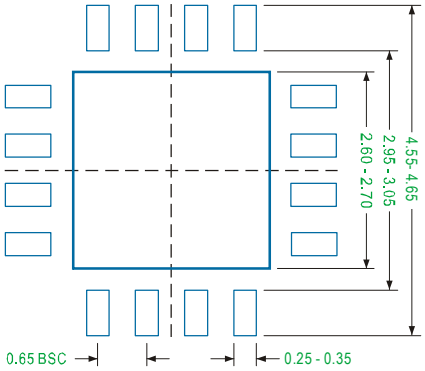
Follow the layout guidelines for optimal performance of uP6111A/B.

1. Place the power components on the top side of PCB, including input/output capacitors, output inductors and power MOSFETs.
2. Use a dedicated grounding plane and use vias to ground all critical components to this layer. The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs. Use an immediate via to connect the components to ground plane including GND of uP6111. Use several bigger vias for power components.
3. Apply another solid layer as a power plane and cut this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes to maintain good voltage filtering and to keep power losses low. Also, for higher currents, it is recommended to use a multilayer board to help with heat sinking power components.
4. The PHASE node is subject to very high dV/dt voltages. Stray capacitance between this island and the surrounding circuitry tend to induce current spike and capacitive noise coupling. Keep the sensitive circuit away from the PHASE node and keep the PCB area small to limit the capacitive coupling. However, the PCB area should be kept moderate since it also acts as main heat convection path of the lower MOSFET.
5. uP6111 sources/sinks impulse current with 2A peak to turn on/off the upper and lower MOSFETs. The connecting trance between the controller and gate/source of the MOSFET should be wide and short to minimize the parasitic inductance along the traces.
6. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power component.
7. Provide local VCC decoupling between VCC and GNDpins. Locate the capacitor, C_{BOOT} as close as practical to the BOOT and PHASE pins.

Package Information

WQFN4x4-16 Package





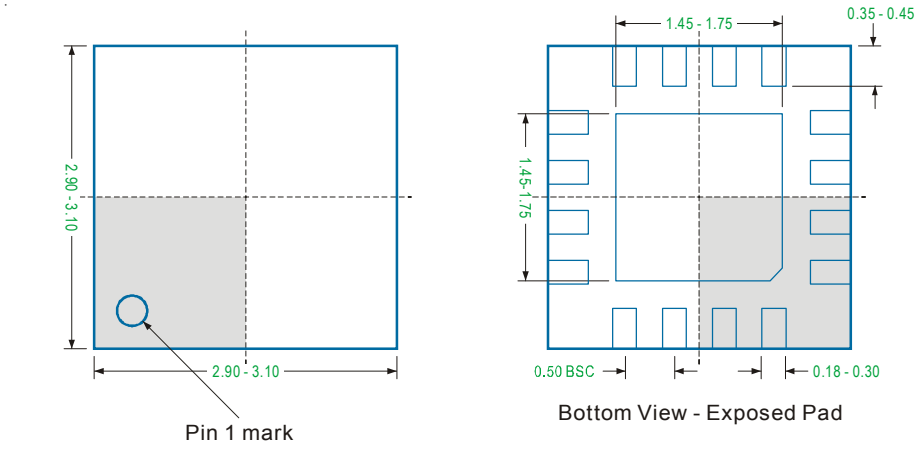
Recommended Solder Pad Pitch and Dimensions

Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.

Package Information

WQFN3x3-16L Package



Note

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   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
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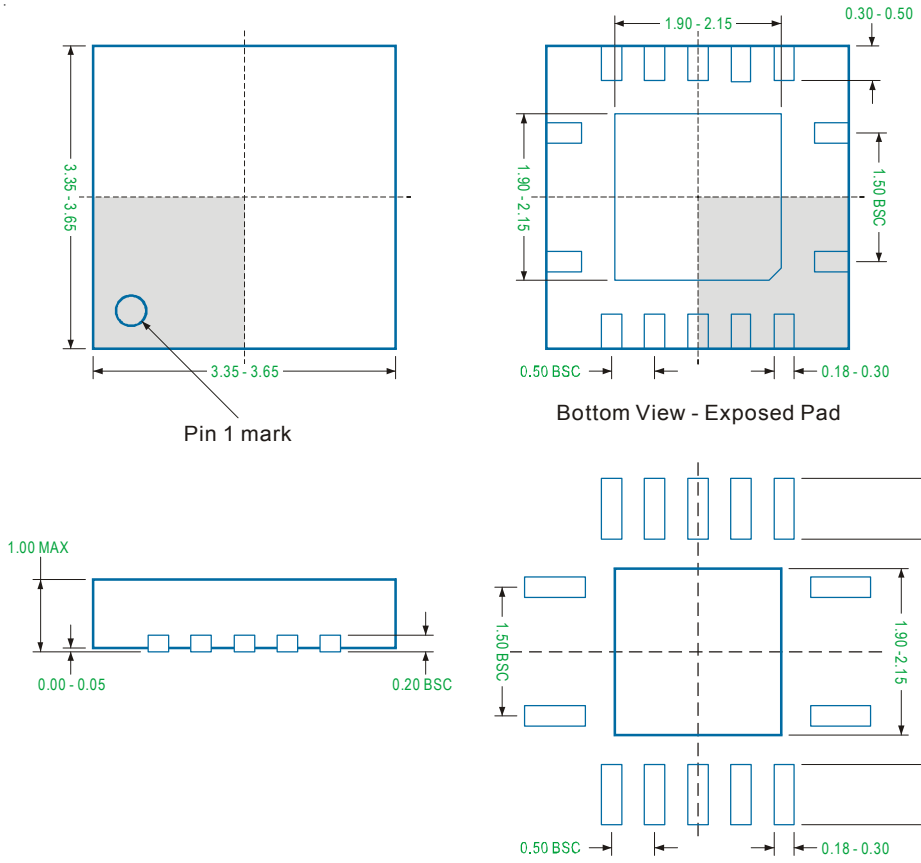
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.

Package Information

VQFN3.5x3.5-14L Package

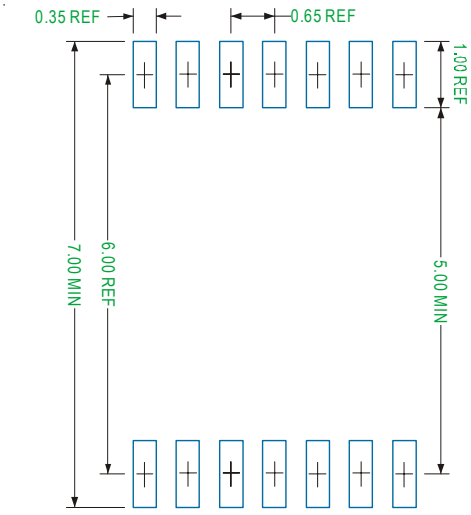


Note

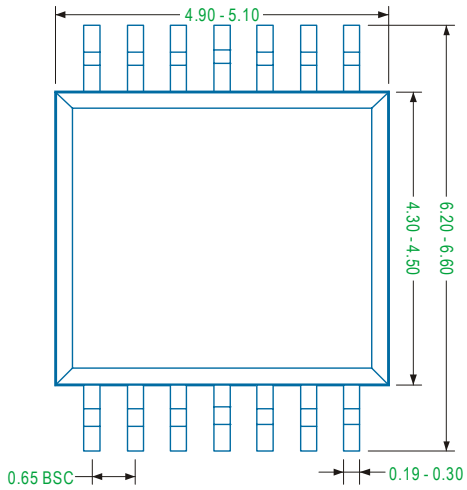
1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.

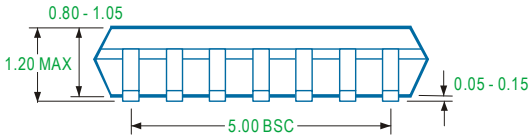
Package Information

TSSOP-14L Package



Recommended Solder Pad Layout





Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.