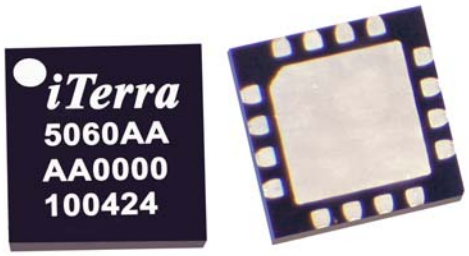
iT5060
12.5 Gb/s, 8 Vpp Modulator Driver
(for use with bias-tee)

Description

The iT5060 is a low-cost, plastic-packaged (QFP-N) broadband GaAs traveling-wave MMIC amplifier with high output voltage. In optical communication systems, it is well suited as a driver for EO/$LiNo_3$ modulators by providing from 3 to 8 Vpp output voltage for NRZ signals up to 12.5 Gb/s. In low-voltage mode, the iT5060 can be used as a pre-driver for a 1.5 to 3 Vpp output voltage. The amplifier can also be used as an optical receiver amplifier gain stage for photodiodes or as a limiting amplifier after the transimpedance amplifier. It can operate from DC to 12.5 GHz with 14 dB linear gain, a +21 dBm P1dB compression point, and +23 dBm Psat. The iT5060 employs GaAs pHEMT technology with silicon nitride as the dielectric of the on-chip MIM capacitors. RF ports of the iT5060 must be AC coupled and drain bias is provided by external choke. Output voltage control is achieved by reducing the Vd power supply. An on-chip power detector allows external temperature compensation to be provided. For low-voltage operation, the iT5060 can be biased through an on-chip resistor, eliminating the need for a bias tee.

Features

- Broad bandwidth: DC to 11 GHz
- Suitable for up to 12.5 Gb/s
- Moderate gain: 14 dB
- Output voltage: 8 Vpp
- Adjustable output voltage: (3 Vpp to 8 Vpp)
- Return Loss: Input –10 dB, output –10 dB
- Bias: 5 V, at 210 mA
- Power dissipation:
  - 1.1 W at Vout = 8 Vpp
  - 400 mW at Vout = 3 Vpp
- On-chip power detector
- Low-cost JEDEC QFP-N (M02-200) package



Absolute Maximum Ratings

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
Vd	Positive voltage			8	V
Vg	Negative voltage	-3			V
Id	Positive supply current			300	mA
Pin	Input RF power			23	dBm
Tch	Operating channel temperature			150	ºC
Tstg	Storage temperature	-65		150	ºC

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Electrical Characteristics

1. Small signal parameters were tested in wafer form with T_{chuck} = 25 °C

2 $J_{rms\_d}=sqrt(J_{rms\_d}^2 - J_{rms\_t}^2)$ where J_{rms_t} is the RMS jitter measured with thru and J_{rms_d} is measured with the device under test.

Test conditions:
Vd = 5 V
Ids(RF) = 210 mA

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
BW	3dB bandwidth	10	11		GHz
S21	Small gain signal	13	14	15	dB
RLin	Input return loss (30 kHz to 11 GHz)	-10			dB
RLout	Output return loss (30 kHz to 11 GHz)	-10			dB
S12	Isolation			-20	dB
GD	Group delay from 0.5 GHz to 15 GHz			±40	ps
Pdiss	Power dissipation at 8 Vpp output		1.1	1.2	W
	Bit rate			12.5	Gb/s
Vout	Saturated output voltage (High-voltage mode) At Vd=5.0 V +/- 5% At Vd=4.5 V +/-5% At Vd=4.0 V +/-5%	 7.5 6.7 6.0	 8 7.2 6.5		 Vpp Vpp Vpp
Rt/Ft	Rise/fall time (20%÷ 80%)		25	30	ps
	RMS jitter degradation (in saturation) (2)		0.5	1.1	ps
	Eye crossing control (via Vg bias)	30		70	%
	Voltage control (by means of Vd) High-voltage mode Low-voltage mode	 3 1.5		 8 3	 V V
Vdet	Power detector transfer function		0.37		V/Vpp
Vdet_o	Power detector output (RF off) at Vd=5 V		5		V
Zdet	Power detector load resistance	100			kΩ

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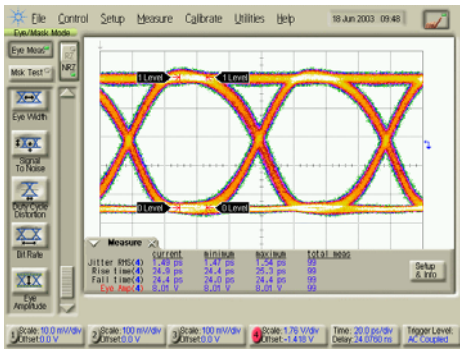
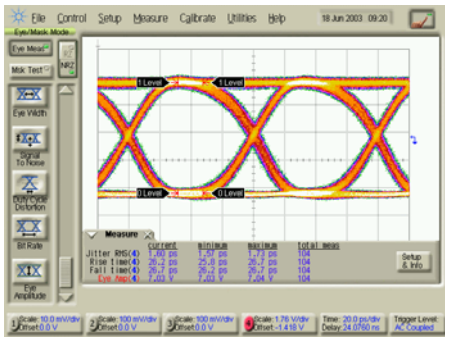
Eye Diagram Performance at 12.5 Gb/s

High-voltage mode
Vd provided by external bias tee
(See assembly diagram)



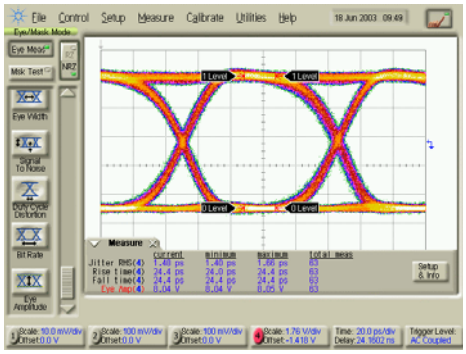
Input = 2.3Vpp, Output = 8 Vpp
V_d= 5 V, I_d=210 mA



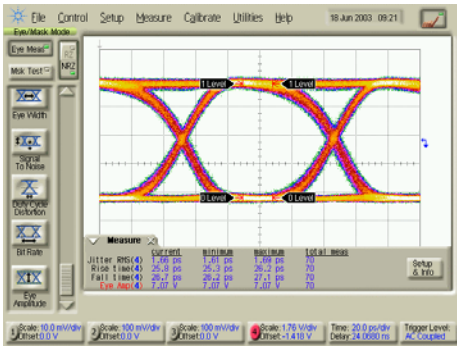
Input = 1.8 Vpp, Output = 7 Vpp
V_d = 4.5 V, I_d = 195 mA

Eye Diagram Performance at 10.7 Gb/s

<u>High-voltage mode</u>
Vd provided by external bias tee
(See assembly diagram)



Input = 2.3 Vpp, Output = 8 Vpp
V_d= 5 V, I_d=210 mA

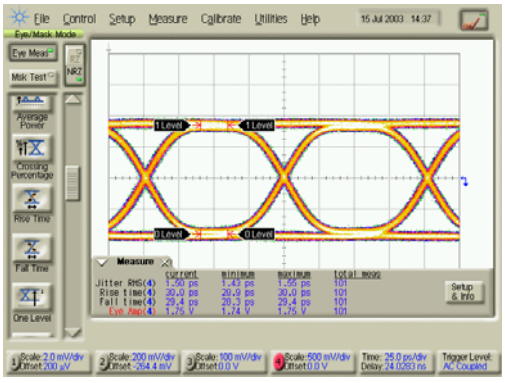


Input = 1.8 Vpp, Output = 7 Vpp
V_d= 4.5 V, I_d= 195 mA

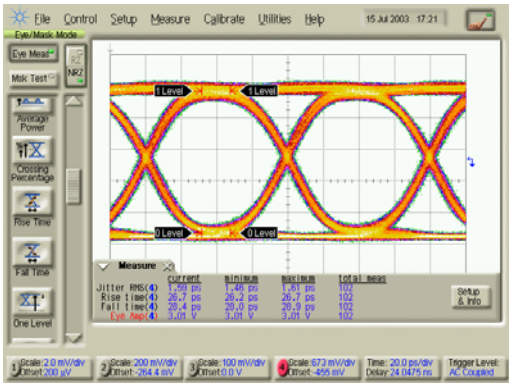
Note: S parameters measured on evaluation board. Effects of board and DC blocks are included.

Eye Diagram Performance at 12.5 Gb/s

<u>Low-voltage mode</u>
Vd provided through VDL1
(See assembly diagram)



Input 0.45 Vpp; Output 1.8 Vpp



Input 1.0 Vpp; Output 3.0 Vpp

Note: S parameters measured on evaluation board. Effects of board and DC blocks are included.

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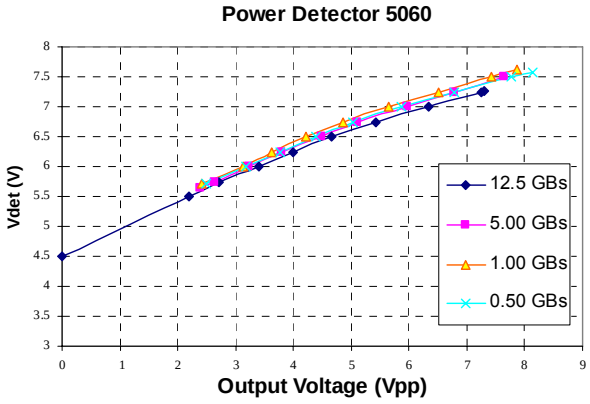
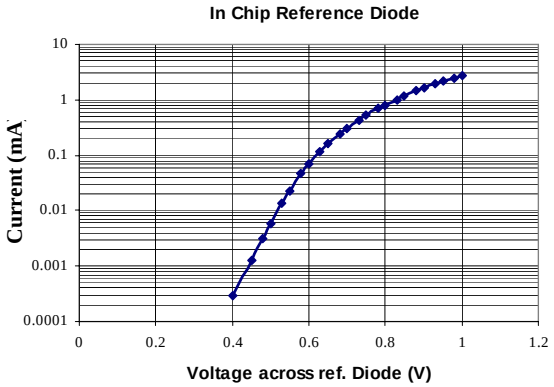
Power Detector Output
(Vdet vs RF Out)



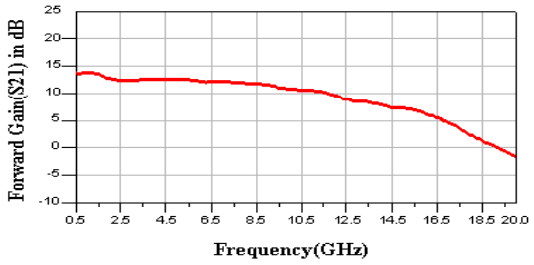


(*) When no RF signal is applied, Vdet_o ~ Vd
(**) Vdet measured with Agilent 34401A multimeter

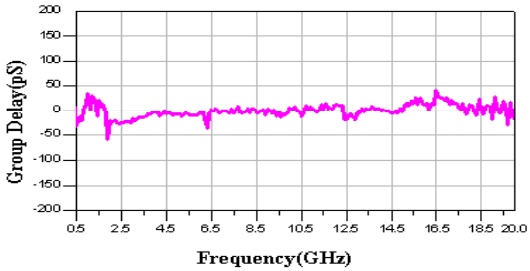
Small Signal Measured Performance

High-voltage mode
Vd = 5 V, Id =210 mA

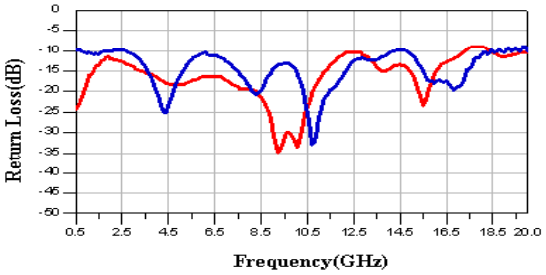
Linear Gain



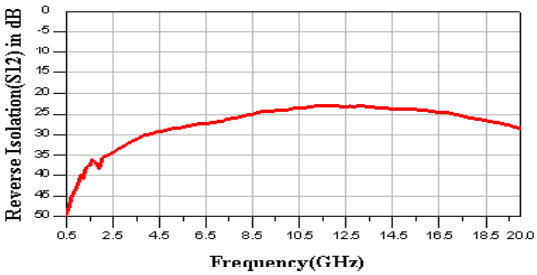
Group Delay



Return Loss



Isolation



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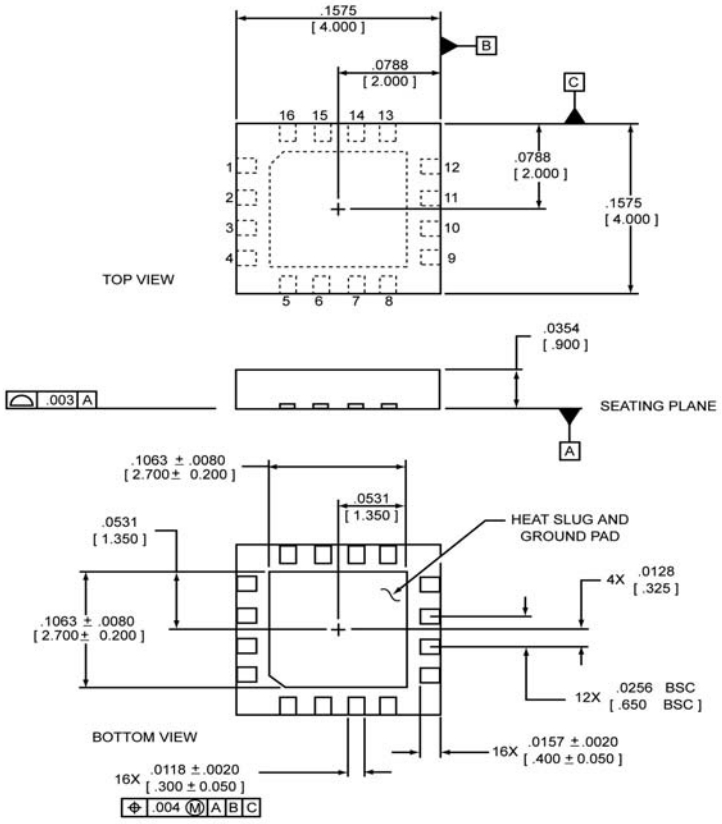
Package Pad Location

1. Dimensions: inches (mm)
2. Tolerance on dimensions is +/- 0.0039 (0.100)

(Unless otherwise specified):



Pinouts

P1:	Not used
P2:	Ground
P3:	RF Input
P4:	Ground
P5:	Not used
P6:	Not used
P7:	Not used
P8:	V_g, negative bias supply, eye crossing control
P9:	Ground
P10:	Ground
P11:	RF output and Vd positive bias supply in case of High-voltage mode
P12:	V_{det}, power detector output
P13	(+) Reference diode
P14	(-) Reference diode
P15:	V_{DL1}, First drain load termination and positive bias supply in case of low-voltage mode
P16:	V_{DL2}, Second drain load termination

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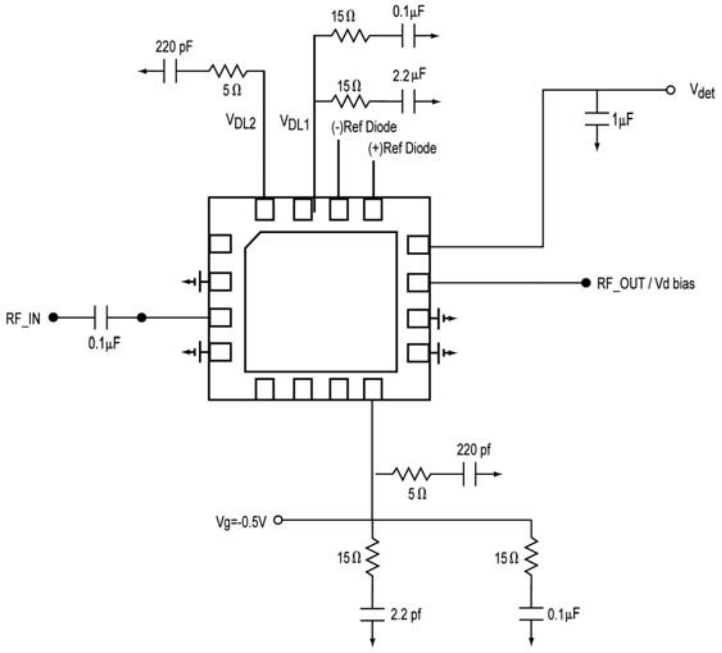
Assembly Diagram

High Voltage Mode
Apply positive bias Vd with external bias-tee at RF output



Bias procedure:

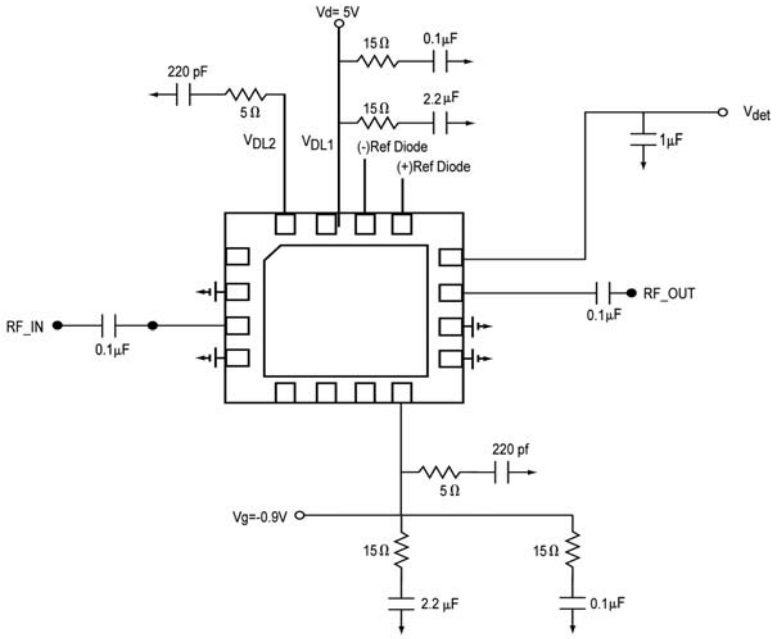
1. Apply V_g =-1 V
2. Apply V_d raising voltage from 0 to 5 V
3. Set V_g approximately at –0.6V (Id=180 mA)
4. Apply RF Input (Id current increases to 210mA at Vout=8Vpp)
5. Adjust V_d for desired output voltage
6. Use V_g to adjust eye crossing

Turn-off procedure:

1. Turn off V_d before V_g

Assembly Diagram

Low Voltage Mode
Apply positive bias Vd through VDL1 pin



Bias procedure:

1. Apply V_g =- 1V
2. Apply V_d at VDL1 raising voltage from 0 to 5 V
3. Set V_g approximately at –0.9 V (Id =75 mA)
4. Apply RF Input (Id current increases to 80m at Vout = 3 Vpp)
5. Adjust V_d for desired output voltage
6. Use V_g to adjust eye crossing

Turn-off procedure:

1. Turn off V_d before V_g

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