iT4033D
100-ps Dual Independent Wideband Phase Delay
(Advanced Information)

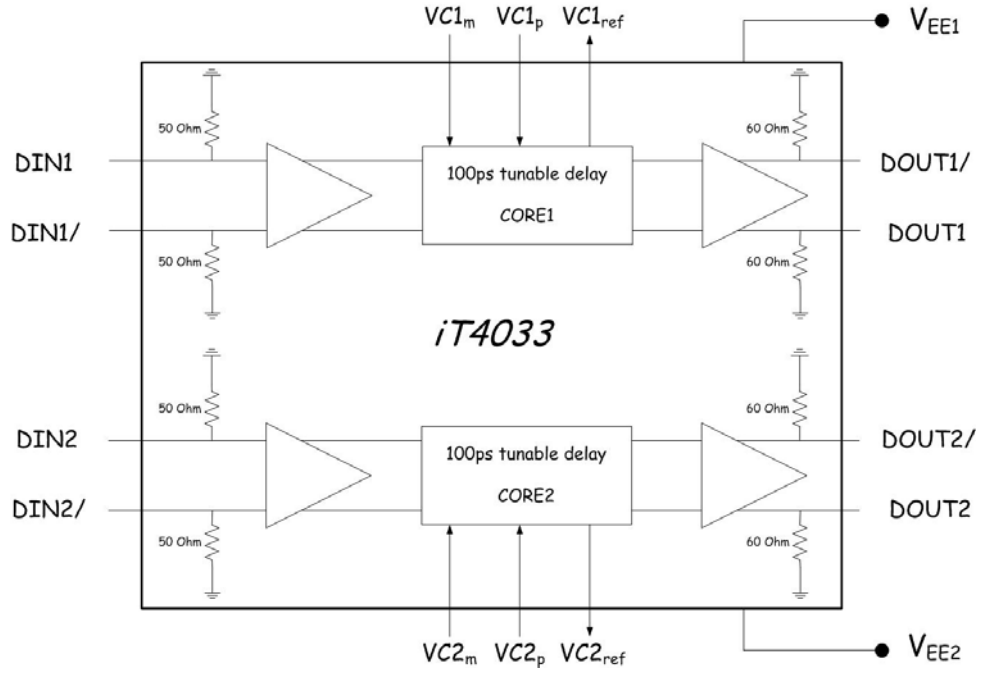
Description

The iT4033D is a dual-independent ultra-wideband phase delay fabricated using 1-um HBT GaAs technology and is based on ECL topology to guarantee high-speed operation. The high output voltage, excellent rise and fall time, and the high eye diagram quality at data rates to 12.5 Gb/s makes the iT4033D suitable for timing adjustment in data and clock distribution at very high speed. Complex digital applications benefit from the iT4033D, including clock data recovery, edge detectors, NRZ-to-RZ converters, MUX/DEMUX, and data restoration. The device features a dual delay element that provides up to 100-ps delay. Delay control can be either differential (using both VCp and VCm) or single-ended (VCm is the active control pad while VCp is shorted to VCref). The control voltage range for the delay input is from -2.2 V to -3.0 V whether the control is single-ended or differential. The device can delay NRZ streams with data rates to 12.5 Gb/s or a clock signal up to 10.7 GHz. Both inputs and outputs are DC-coupled. At the input side, internal 50-ohm resistors avoid the need for external impedance matching terminations. The iT4033D uses SCFL I/O levels and is designed so to allow for either single ended or differential data input.

Features

- Ultra wideband: Up to 12.5 Gb/s NRZ
- Dual independent cores on a single die
- Delay adjustment to 100 ps
- 900 mVpp single-ended output
- Jitter RMS: <1.5 ps
- Output rise time (20% – 80 %): <21 ps
- Output fall time (20% – 80 %): <18 ps
- 50-ohm matched DC-coupled inputs and outputs
- Differential or single ended I/O
- Power consumption: 1.6 W (each core)

Device Diagram



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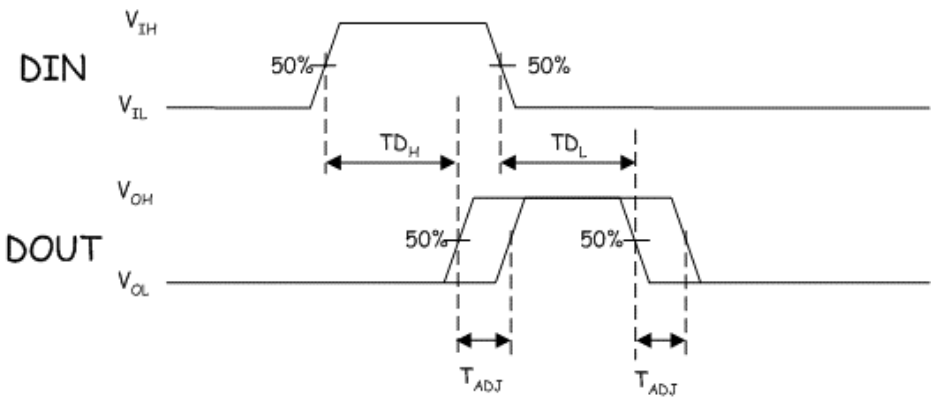
Timing Diagram



Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameters/conditions	Min.	Max.	Units
V_{EE}	Power supply voltage	-5.5	0	V
V_{IH}	Input voltage level, high level	-1.5	1.5	V
V_{IL}	Input voltage level, low level	-1.5	1.5	V
VC	Delay control voltage	-5.0	0	V
T_A	Operating temperature range – die	-15	125	°C
T_{STG}	Storage temperature	-65	150	°C

Recommended Operating Conditions

Symbol	Parameters/conditions	Min	Typ.	Max	Units
T_A	Operating temperature range – die	0		85	°C
V_{EE}	Power supply voltage		-5		V
VC	Delay control voltage	-3.0	-2.6	-2.2	V
V_{IH}	Input voltage level, high level (single ended)		0.0		V
V_{IL}	Input voltage level, low level (single ended)		-0.9		V
V_{INDC}	DC input voltage (with DC-coupled input)		-0.45		V

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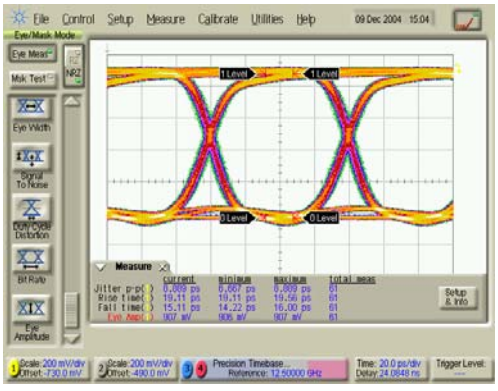
Electrical Characteristics

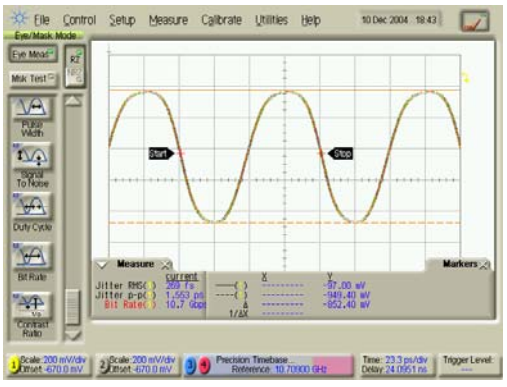
1. Electrical characteristics at ambient temperature.
2. In case of single-ended input the unused pin has to be tied to VINDC.
3. In case of single-ended output, the unused pad must be terminated with 50 ohms to ground.
4. Refer to timing diagram.
5. On a 10.7 Gb/s PRBS pattern.

Symbol	Parameters	Min	Typ	Max	Units
V_{EE}	Power supply voltage	-4.5	-5.00	-5.25	V
V_{IH}	Input voltage level, high level (single ended)		0.0		V
V_{IL}	Input voltage level, low level (single ended)		-0.9		V
V_{INDC}	DC input voltage (with DC-coupled input) (2)		-0.45		V
V_{OUT}	Data output voltage amplidude (3)	0.8	0.9	1.0	V
T_R	Output rise time (20% – 80%)		20		ps
T_F	Output fall time (20% – 80%)		17		ps
TD_H	Output delay low-high transition(4)		250		ps
TD_L	Output delay high-low transition(4)		250		ps
T_{ADJ}	Output phase delay adjustment(4)		100		ps
S_{11}	Input return loss (up to 15 GHz)		24		dB
S_{22}	Output return loss (up to 15 GHz)		8		dB
F_{MAX}	Maximum clock frequency		10.7		GHz
J_{p-p}	Peak-to-peak jitter(5)		9		ps
J_{rms}	RMS jitter(5)		1.5		ps
I_{EE}	Power supply current		642		mA
P_D	Power dissipation		3.21		W

Eye Diagram Performance



Die measurement
Vee: -5.0 V
Input data rate:12.5 GHz
Differential data input: 0/-900 mVpp
Control voltage: VCp = VCref,
VCm = -2.6 V



Die measurement
Vee: -5.0 V
Input CLK frequency: 10.7 GHz
Single-ended CLK input: +/-450 mVpp
Control voltage: VCp = VCref,
VCm = -2.2 to -3.0 V (accumulating)

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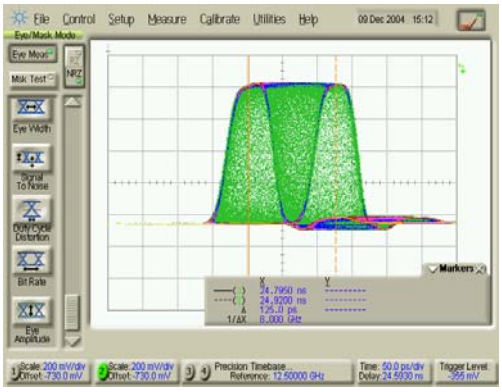
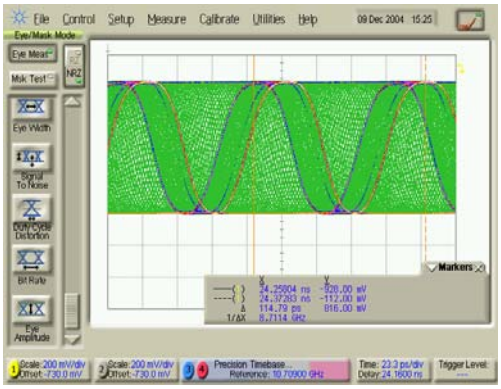
Eye Diagram Performance (cont.)



Die measurement
Vee: -5.0 V
Input data rate: 12.5 GHz
Differential data input: 0/-900 mVpp
Control voltage: VCp = VCref,
VCm = -2.2 to -3.0 V (accumulating)



Die measurement
Vee: -5.0 V
Input CLK frequency: 10.7 GHz
Single-ended CLK input: +/-450 mVpp
Control voltage: VCp = VCref,
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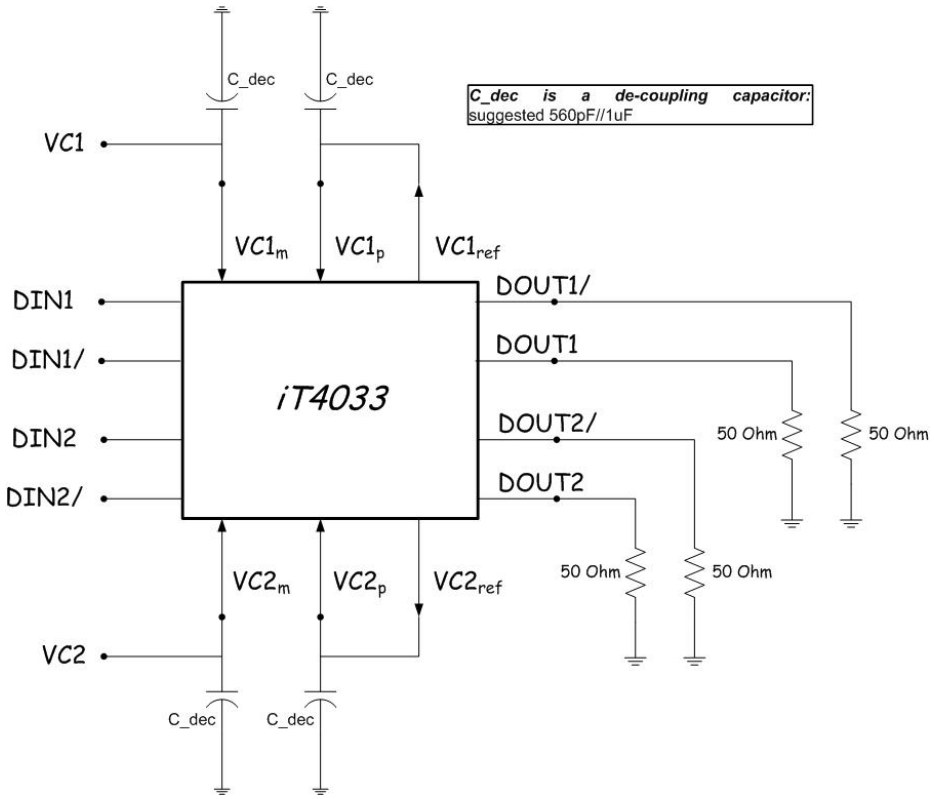
Recommended Operational Setup



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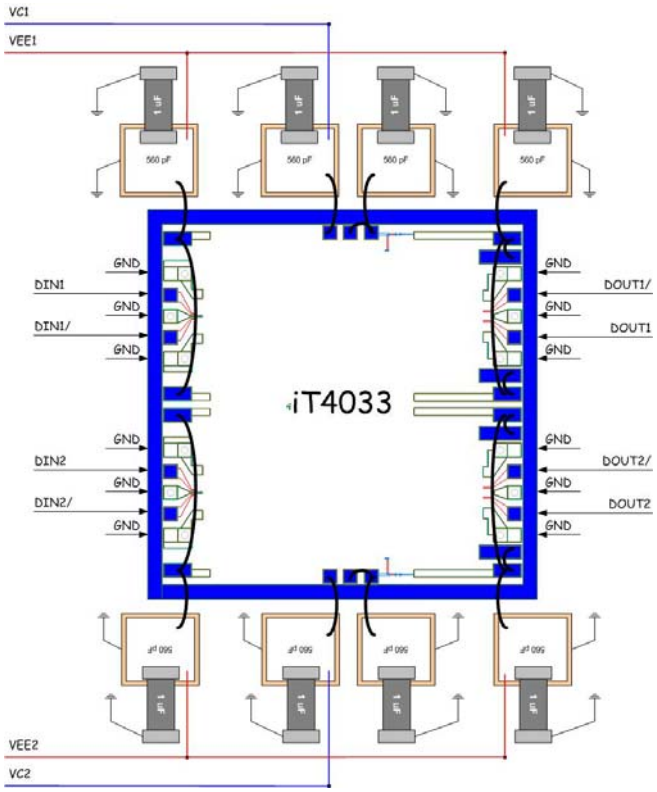
Recommended Chip Mounting

Chip size:
2650 µm ±10 µm
x 2650 µm ±10 µm

Chip thickness:
104 µm ±3 µm

Pad size: 100 µm
x 100 µm

RF pad pitch: 150 µm



Pad Positions and Chip Dimensions

Chip size:
2650 µm ±10 µm
x 2650 µm ±10 µm

Chip thickness:
104 µm ±3 µm

Pad size: 100 µm
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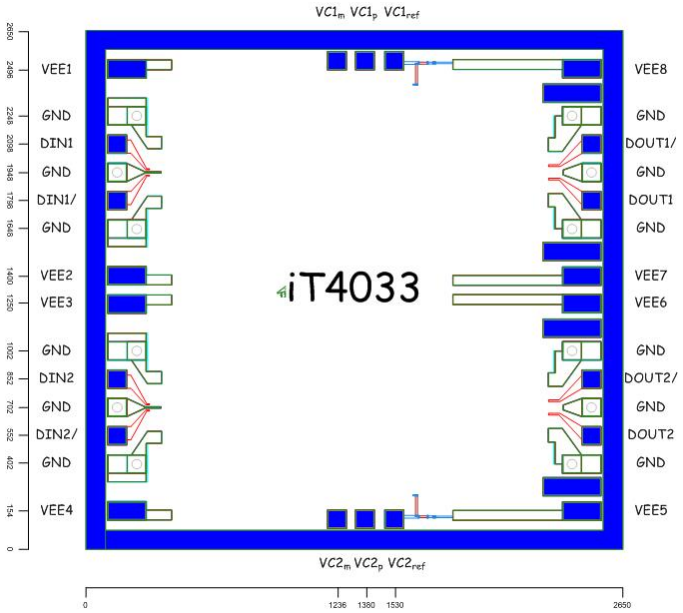
RF pad pitch: 150 µm



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