iT2008

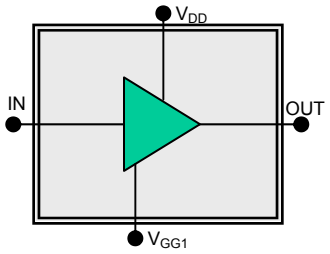
10 MHz – 26.5 GHz High-Power Amplifier

Description

The iT2008 is a broadband GaAs MMIC traveling wave amplifier designed for high output power applications where low-frequency extension capabilities are also required. The iT2008 provides a saturated output power of 1 W up to 7 GHz, greater than 29 dBm up to 15 GHz and greater than 25 dBm at 26.5 GHz. Average gain of 10 dB with flatness of +/-1 dB is provided up to 26.5 GHz. DC power consumption is as low as 3.1 W. Input/output ports are DC coupled.

Features

- Frequency range: 2 GHz – 26.5 GHz with low-frequency extension capability down to 10 MHz
- 30 dBm nominal Psat (2 GHz – 7 GHz)
- 29 dBm nominal Psat (7 GHz – 15 GHz)
- >25 dBm nominal Psat at 26.5 GHz
- 10 dB nominal gain with +/-1 dB flatness
- 3.1 W DC power consumption
- Nominal DC bias conditions: 9 V at 350 mA
- Full chip passivation for high reliability



Absolute Ratings

Symbol	Parameters/conditions	Min.	Max.	Units
V_{DD}	Positive supply voltage		11	V
V_{GG1}	Negative supply voltage	-2	0	V
I_{DD}	Positive supply current		900	mA
I_{GG1}	Negative supply current		1.8	mA
Pin	RF input power		25	dBm
Pdiss_DC	DC power dissipation (no RF)		5	W
Tch	Operating channel temperature		150	°C
Tm	Mounting temperature (30 s)		320	°C
Tst	Storage temperature	-65	150	°C

Electrical Characteristics

(at 25 °C) 50-ohm system, V_{DD}=+9 V, Quiescent current (I_{DQ})=350 mA

(*) Low frequency extension available.

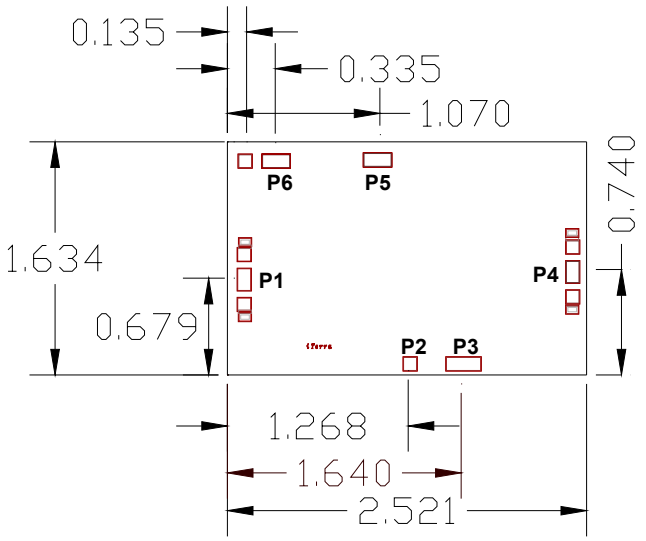
Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
BW	Frequency range*	2		26.5	GHz
S21	Small signal gain	8	10		dB
	Gain flatness		+/-1		dB
S11	Input return loss	10	15		dB
S22	Output return loss	8	12		dB
S12	Isolation	30			dB
Psat	Saturated output power (3 dB gain compression)				
	2 - 10 GHz	27.5	29.5		dBm
	2 - 20 GHz	26.5	28.5		dBm
	2 - 26.5 GHz	23	25		dBm
P_{1dB}	Output power (1 dB gain compression)				
	2 - 10 GHz	27	29		dBm
	2 - 20 GHz	26	28		dBm
	2 - 26.5 GHz	22.5	24.5		dBm

Thermal Characteristics

Symbol	Parameters/conditions	Rth_jb (°C/W)	Tch (°C)	MTFF (h)
Rth_jb	Thermal resistance junction-back side of die No RF: DC bias V_{DD} = 9 V, I_{DQ} = 35 0mA , P_{DC} = 3.1 W Tbase = 70 C	9.2	98.5	>> +1E7
Rth_jb	Thermal resistance junction-back side of die RF applied: Saturated power 1 W, V_{DD} = 9 V, Pdiss = 4.4 W Tbase = 70 C	9.2	110.6	>> +1E7

Chip Layout and Bond Pad Locations

(Back of chip is RF and DC ground)



Chip size tolerance: ± 20 µm
Chip thickness: 4 mil with a tolerance of ± 0.4 mil.

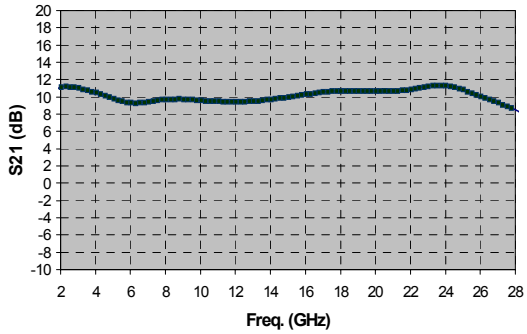
Pinout and pad dimensions:

P1: RF input (100 x 150 µm²)
P2: V_{GG1}, negative voltage (100 x 100 µm²)
P3: Gate low-frequency extension (250 x 100 µm²)
P4: RF output and Vdd bias (option 2) by means of bias-tee (100 x 150 µm²)
P5: Drain low-frequency extension (300 x 100 µm²)
P6: V_{DD} positive voltage (option 1) by means of choke (200 x 100 µm²)

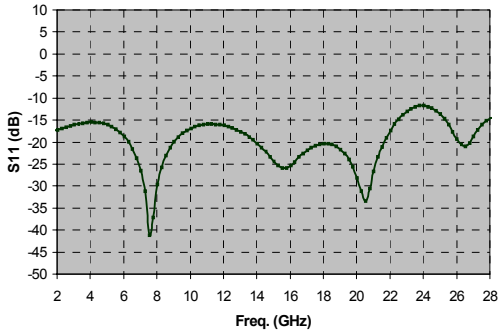
Note: All dimensions are in millimeters

Performance Data, T = 25 °C

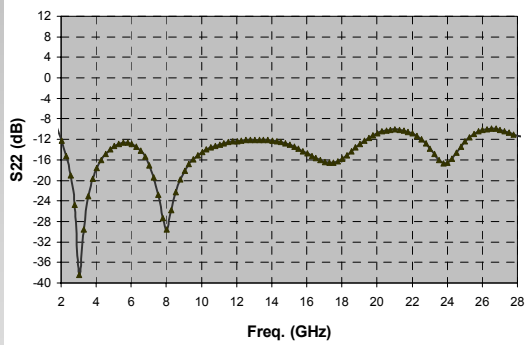
Small Signal Gain, V_{DD} = 9 V, I_{DD} = 350 mA



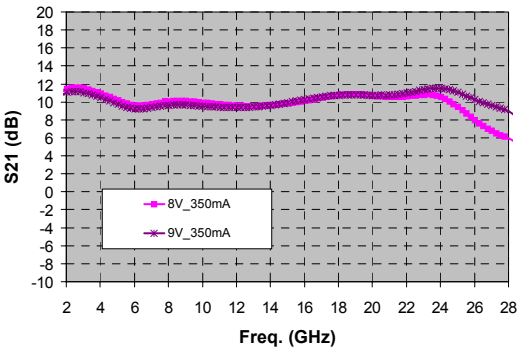
Input Return loss, V_{DD} = 9 V, I_{DD} = 350 mA



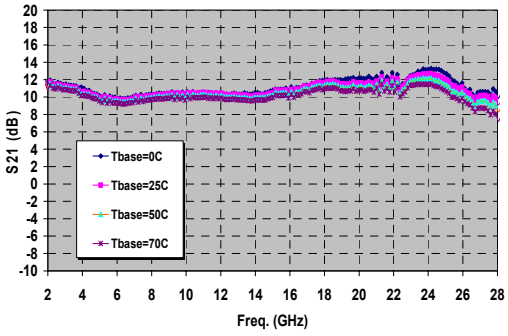
Output Return loss, V_{DD} = 9 V, I_{DD} = 350 mA



Gain vs. Drain Bias V_{DD}, I_{DD} = 350 mA

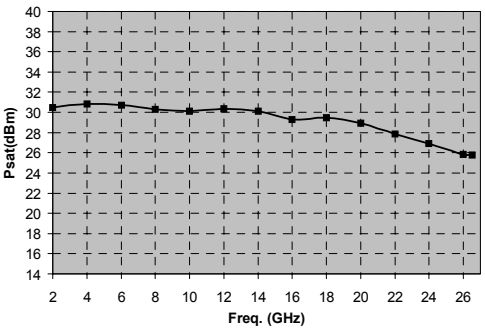


Gain vs. Temperature, V_{DD} =9V

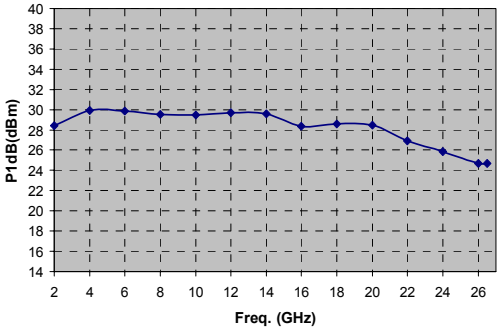


Performance Data, T=25 °C

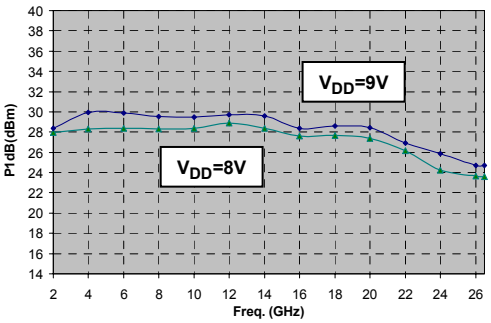
Saturated Power, V_{DD} = 9 V, I_{DD} = 350 mA



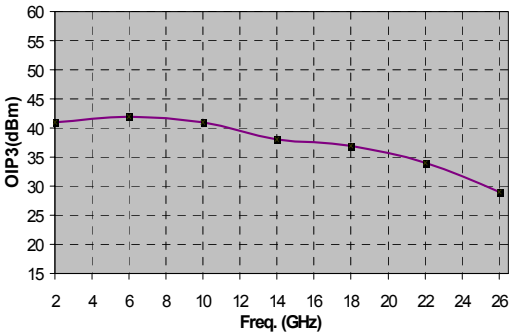
P_{1dB}, V_{DD} = 9V, I_{DD} = 350 mA



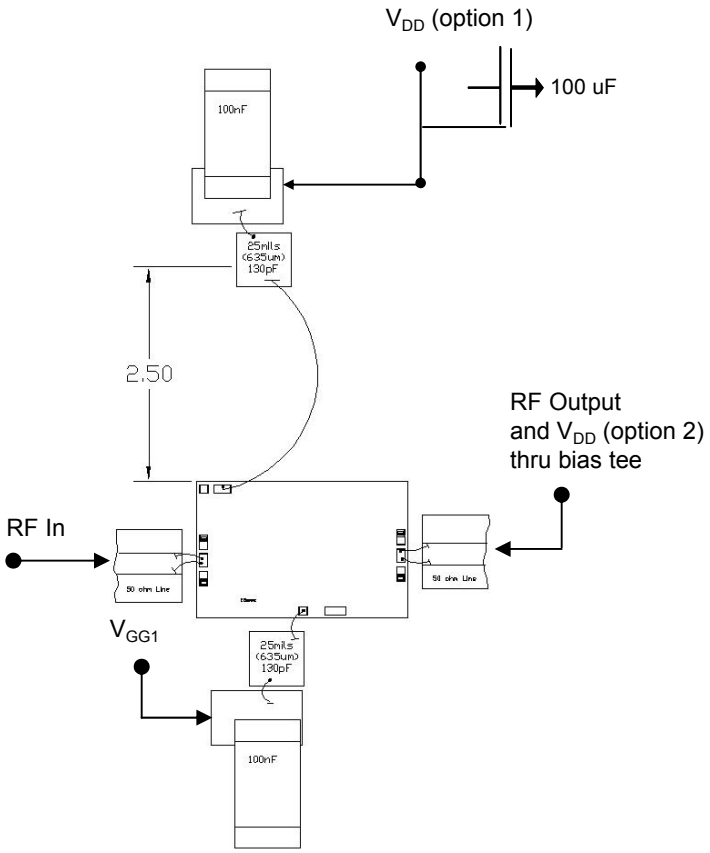
P1dB vs. V_{DD}, I_{DD}=350 mA



Output Third Order Intercept Point, V_{DD} = 9 V, I_{DD} = 350 mA



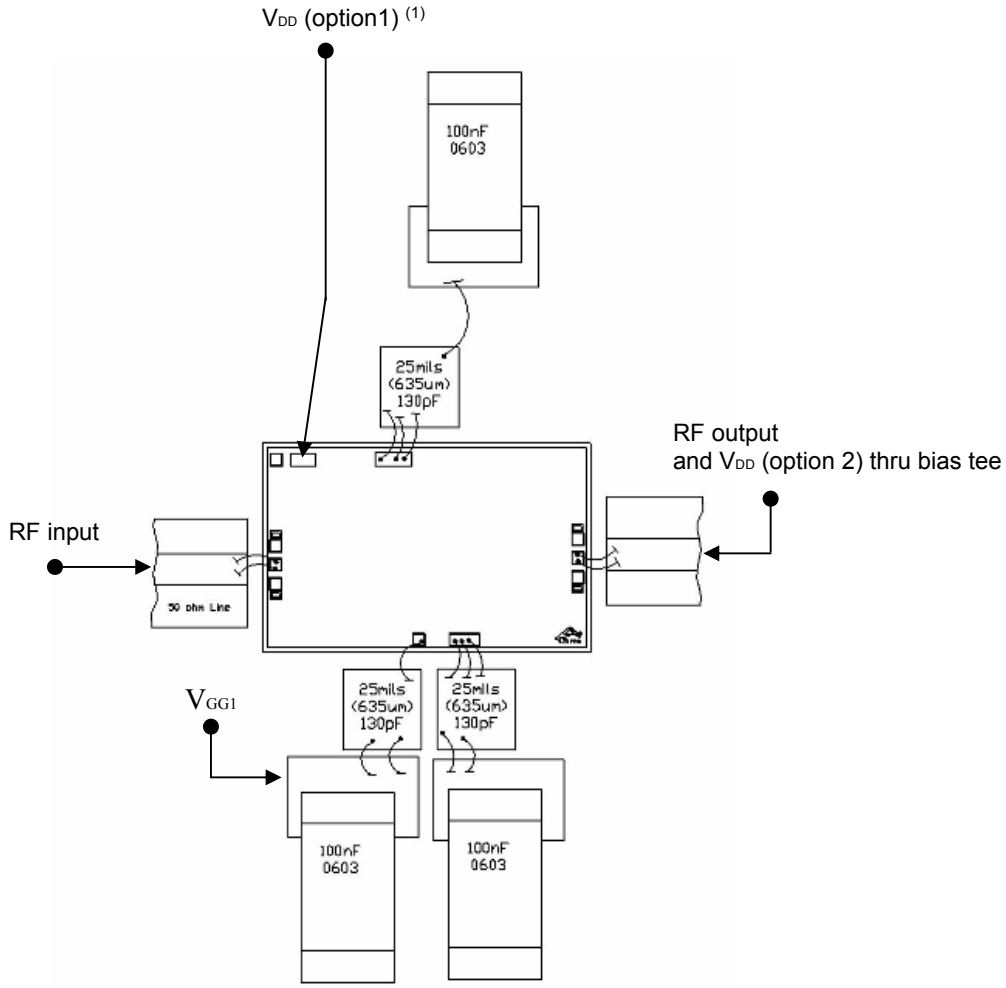
Recommended Assembly Diagram for 2 to 26.5 GHz Applications



1. For applications at 2 GHz and above, only an inductor of Lc> = 3 nH (1 mil long bond wire >2.5 mm) is necessary to provide drain bias.

2. Bypass capacitor must be large enough to isolate bias supply (> = 10 μF)

Recommended Assembly Diagram for 10 MHz to 26.5 GHz Applications



1. Appropriate low-frequency choke must be applied for 10 MHz applications.

Recommended Procedure for Biasing and Operation

CAUTION: LOSS OF GATE VOLTAGE (V_{GG1} and V_{GG2}) WHILE CORRESPONDING DRAIN VOLTAGE (V_{DD}) IS PRESENT CAN DAMAGE THE AMPLIFIER.

The following procedure must be considered to properly test the amplifier.

The iT2008 amplifier is biased with a positive drain supply (V_{DD}) and one negative gate supply (V_{GG1}). The recommended bias conditions for the iT2008 is V_{DD} = 9.0 V, I_{DD} = 350 mA. To achieve this drain current level, V_{GG1} is typically biased between –0.7V and –0.9 V. The gate voltage (V_{GG1}) MUST be applied prior to the drain voltage (V_{DD}) during power up and removed after the drain voltage is removed during the power down. Drain bias V_{DD} can be applied to the drain (P6). Alternatively, the positive power supply can be applied through an external bias tee to the RF Output pad (P4) .

Low Frequency Operation

External coupling capacitors are needed at the RF_IN (P1) and RF_OUT (P4) ports. The auxiliary gate pad (P3) and drain pad (P5) are provided to extend performance below 2 GHz. Connect these pads via large external capacitors to ground to maintain input and output VSWR at low frequencies. Do not apply bias to these pads.

Two options are allowed to provide the positive drain voltage V_{DD}. **Option 1** uses an on-chip pad (P6) where an appropriate value of inductance (choke) must be used to maintain good matching over bandwidth, as reported in the assembly diagram. **Option 2** uses an external bias-tee directly from the pad at the RF output. For application as low as 10 MHz a large value of inductance must be used in parallel with appropriate resistors in order to optimize gain flatness.

Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

Chip carrier material should be selected to have GaAs-compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325° C for 15 min.

Die attachment for power devices should utilize gold/tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the back side of the chip is gold plated and is used as RF and DC ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist-grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3-mil-wide and 0.5-mil-thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 12 mil long corresponding to a typical 2 mil gap between the chip and the substrate material.