GENERAL DESCRIPTION

The ft2830 is a highly efficient 4.5W Class-G audio power amplifier with automatic level control (ALC) for use in battery-powered portable devices. It integrates a filterless Class-D audio power amplifier with a Class-G charge pump regulator based upon proprietary ***Dual-Pump***™ topology. It operates from 3.2V to 4.6V supply. When operating with a 4.2V supply voltage, the ft2830 can deliver into a 4Ω load a maximum output power up to 4.5W with 10% THD+N, or a constant output power at 3.5W with 0.5% THD+N. Its high efficiency, up to 83%, helps extend battery life.

In ft2830, the power supply rail for the amplifier's output stage is internally boosted and regulated at 6.2V by an adaptive charge pump regulator based upon the ***Dual-Pump***™ topology, allowing for a much louder audio output than a stand-alone one directly connected to the battery. It makes ft2830 an ideal audio solution for portable devices that are powered by a single-cell lithium battery while requiring higher audio loudness.

For applications where minimum EMI emission is required, the charge pump regulator can be disabled.

The ft2830 features ALC to constantly monitor and safeguard the audio outputs against the boosted supply voltage, preventing output clipping distortion, excessive power dissipation, or hazardous speaker over-load. Once an over-level condition is detected, the ALC lowers the voltage gain of the audio amplifier proportionally to eliminate output clipping distortion while maintaining a maximum dynamic range of the audio outputs allowed by the boosted supply voltage.

FEATURES

- Proprietary ***Dual-Pump***™ topology
- Filterless Class-D audio amplifier integrated with a Class-G charge pump regulator
- Automatic level control to eliminate output clipping
- Maximum output power (Non-ALC Mode)
  4.5W (V_{DD}=4.2V, THD+N=10%, R_L=4Ω)
  3.6W (V_{DD}=3.6V, THD+N=10%, R_L=4Ω)
- Constant output power (ALC Mode)
  3.5W (V_{DD}=4.2V, THD+N=0.5%, R_L=4Ω)
  3.1W (V_{DD}=3.6V, THD+N=0.5%, R_L=4Ω)
- High efficiency up to 83%
- Low THD+N: 0.05%
  (V_{DD}=3.6V, f=1kHz, R_L=4Ω, Po=1W)
- ALC dynamic range: 10dB
- Low quiescent current: 2.6mA @ V_{DD}=3.6V
- High PSRR: 70dB at 1kHz
- Two gain settings: 24dB and 27.6dB
- One-wire pulse control to set operating mode and voltage gain
- Auto-recovering short-circuit protection
- Available in TSSOP-20L package

APPLICATIONS

- Portable Speakers
- Multimedia Internet Devices
- Mobile Phones
- Portable Consumer Electronic Devices

APPLICATION CIRCUIT

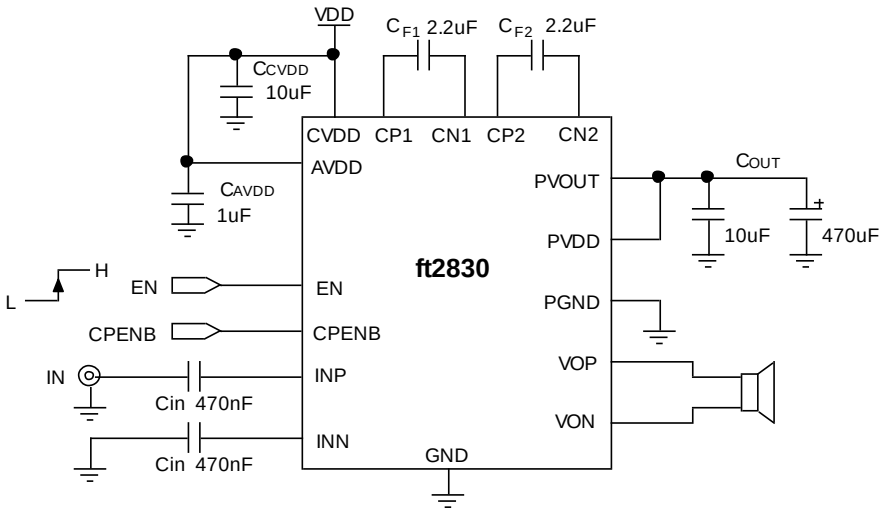
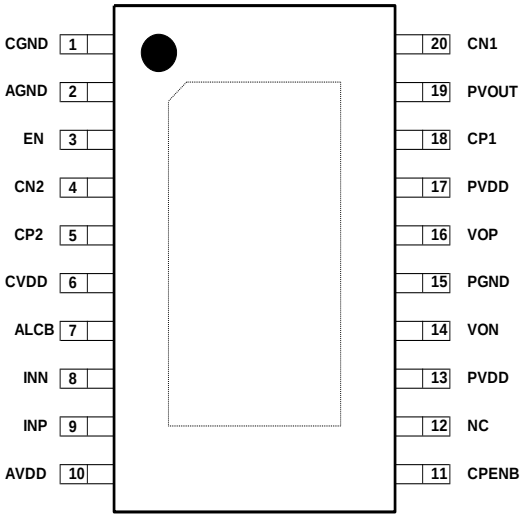


Figure 1: Typical Application Circuit Diagram

PIN ASSIGNMENT AND DESCRIPTION



ft2830P (TOP VIEW)

SYMBOL	PIN #	I/O	DESCRIPTION
CGND	1	G	Ground for the charge pump regulator.
AGND	2	G	Analog ground.
EN	3	DI	Chip Enable & One-wire Pulse Control with a 500kΩ pulldown resistor to ground.
CN2	4	AO	Flying capacitor C_{F2} negative terminal.
CP2	5	AO	Flying capacitor C_{F2} positive terminal.
CVDD	6	P	Power supply for the charge pump regulator.
ALCB	7	DI	ALC Enable (Active-Low) with a 125kΩ pulldown resistor to ground. When pulled low or left unconnected, the ALC control is set by the one-wire pulses applied at the EN pin. When asserted high, the ALC function will be disabled all the time.
INN	8	AI	Negative audio input terminal.
INP	9	AI	Positive audio input terminal.
AVDD	10	P	Analog power supply.
CPENB	11	DI	Charge Pump Enable (Active-Low) with a 300kΩ pulldown resistor to ground. When pulled low or left unconnected, the charge pump regulator is activated adaptively in response to the level of audio outputs. When asserted high, the charge pump regulator will be deactivated all the time.
PVDD	13, 17	P	Power supply rails for the Class-D audio amplifier output stage. They must be externally shorted to PVOUT.
VON	14	AO	Negative BTL audio output.
PGND	15	G	Ground for the Class-D audio amplifier output stage.
VOP	16	AO	Positive BTL audio output.
CP1	18	AO	Flying capacitor C_{F1} positive terminal.
PVOUT	19	AO	Boosted voltage output of the charge pump regulator. It must be externally shorted to PVDD pins on the system board.
CN1	20	AO	Flying capacitor C_{F1} negative terminal.
NC	12	-	No internal connection.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ft2830P	-40°C to +85°C	TSSOP-20L

ABSOLUTE MAXIMUM RATINGS (Note 1)

PARAMETER	VALUE
Supply Voltage, V_{DD} (AVDD, CVDD)	-0.3V to 5.5V
PVOUT, PVDD, CP1, CP2	-0.3V to 6.5V
All Other Pins	-0.3V to V_{DD}+0.3V
ESD Ratings - Human Body Model (HBM)	2000V
Operating Junction Temperature	-40°C to +150°C
Maximum Soldering Temperature (@10 sec duration)	260°C
Storage Temperature	-45°C to +150°C

Note 1: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

POWER DISSIPATION RATINGS (Note 2, 3)

PACKAGE	$T_A \leq$ +25°C	T_A = +70°C	T_A = +85°C	Θ_{JA}
TSSOP-20L	4.8W	3.1W	2.6W	26°C/W

Note 2: The thermal pad of the package must be directly soldered onto a grounded metal island (as a thermal sink) on the system board.
Note 3: The power dissipation ratings are for a two-side, two-plane printed circuit board (PCB).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage, V_{DD}	AVDD, CVDD	3.2		4.6	V
Operating Free-Air Temperature, T_A		-40		85	°C
Minimum Load Resistance, R_{LOAD}		3.2			Ω

IMPORTANT APPLICATION NOTES

1. The ft2830 is a high performance Class-D audio amplifier with an exposed thermal pad underneath the package. The thermal pad must be directly soldered onto a grounded metal island as a thermal sink on the system board for proper power dissipation. Failure to do so may result in the device entering into thermal shutdown.
2. The ft2830 requires adequate power supply decoupling to ensure its optimum performance in output power, efficiency, THD, and EMI emissions. Place respective decoupling capacitors as individually close to the device's AVDD, CVDD, PVOUT, and PVDD pins as possible.
3. It is strongly recommended to employ a ground plane (GND) on the system board for ft2830. The AGND, CGND, and PGND pins are directly shorted to the ground plan.
4. Place a small decoupling resistor (<10Ω) between AVDD and CVDD to prevent high frequency Class-D transient spikes from interfering with the on-chip linear amplifiers.
5. Use a simple ferrite bead filter for further EMI suppression. Choose a ferrite bead with a rated current at 2A or greater for applications with a load resistance less than 4Ω. Also, place the respective ferrite beard filters as close to VOP and VON pins as possible.
6. To avoid excessive load current flowing back into the boosted voltage PVOUT via the Class-D high-side output stage, use speakers with limited phase shift (between voltage and phase) or add a 6.5V Zener diode between PVOUT and ground to ensure the PVOUT voltage does not exceed its absolute maximum rating.
7. Although the output stage of the Class-D audio amplifier can withstand a short between VOP and VON, do not connect either output directly to GND, AVDD, CVDD, PVOUT, or PVDD, CVDD, as this might damage the device.

FUNCTIONAL BLOCK DIAGRAM

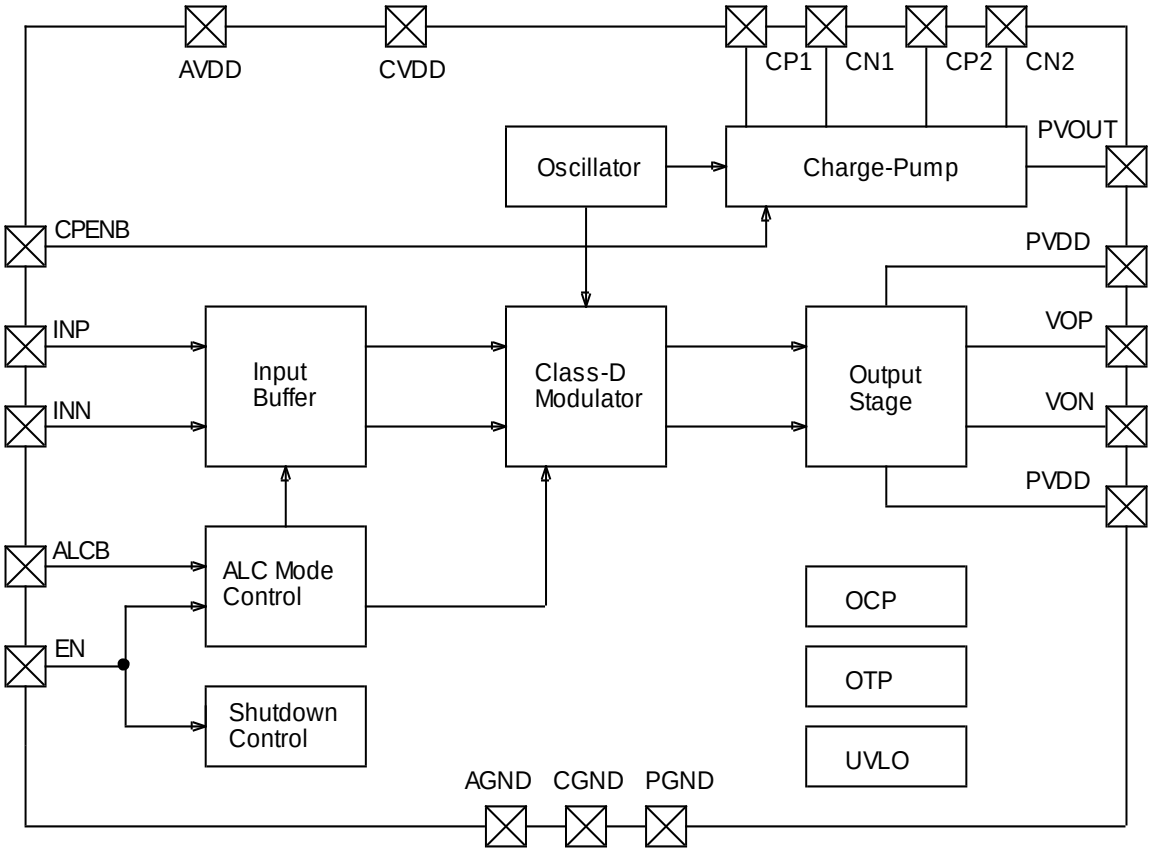


Figure 2: Simplified Functional Block Diagram of ft2830

REVISION HISTORY

Initial Release (October 2015)

Changed from Initial 1.0 (October 2015) to Revision 1.1 (June 2017)

1. Revised Typical Application Circuit Diagrams in Figure 1, 42, 43, 44, 45, and 46.
2. Changed Minimum Load Resistance from 3.0Ω to 3.2Ω in Recommended Operating Conditions on Page 3.

ELECTRICAL CHARACTERISTICS

VDD=3.6V, Mode 1, ALCB=Low, CPENB=Low, C_{IN}=1μF, R_{IN}=0kΩ (A_V=27.6dB), C_{AVDD}=1μF, C_{CVDD}=10μF, $C_{F1/2}$=2.2μF, C_{OUT}=10μF//220μF, C_{PVDD}=10μF, f=1kHz, R_L=4Ω+33μH, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage	AVDD, CVDD	3.2		4.6	V
V_{UVLOUP}	Power-Up Threshold Voltage	V_{DD} from Low to High		2.3		V
V_{UVLODN}	Power-Off Threshold Voltage	V_{DD} from High to Low		2.0		V
I_{DD}	Supply Quiescent Current Inputs AC-Grounded, No Load	V_{DD}=3.6V	1.8	2.6	3.4	mA
		V_{DD}=4.6V	2.0	2.8	3.6	mA
	Supply Quiescent Current V_{in}=300mV_{RMS}, No Load	V_{DD}=3.6V, CPENB Low	6.0	8.5	11	mA
		V_{DD}=4.6V, CPENB Low	7.0	9.5	12	mA
I_{SD}	Shutdown Current	V_{DD}=3.2V ~ 4.6V, EN Low		0.1	1	μA
V_H	Digital High Input Voltage	EN	1.2			V
		ALCB, CPENB	0.8 x V_{DD}			V
V_L	Digital Low Input Voltage	EN			0.4	V
		ALCB, CPENB			0.2 x V_{DD}	V
T_{OTSD}	Over-Temperature Threshold			160		°C
T_{HYS}	Over-Temperature Hysteresis			20		°C
η	Power Efficiency	P_O=0.5W, Load=4Ω+33μH		83		%
		P_O=2.0W, Load=4Ω+33μH		75		%
Class-G CHARGE PUMP REGULATOR						
PVOUT	Charge Pump Output Voltage	I_{PVOUT}=100mA	6.0	6.2	6.4	V
I_{OUT}	Max. DC Output Current	V_{DD}=4.2V, PVDD=5.2V			1.2	A
f_{PUMP}	Switching Frequency			1		MHz
CLASS-D AUDIO AMPLIFIER						
$P_{O, MAX}$ (Mode 3) ALC Off	Maximum Output Power Load=8Ω+33μH	V_{DD}=4.2V, THD+N=10%		2.7		W
		V_{DD}=4.2V, THD+N=1%		2.2		W
		V_{DD}=3.6V, THD+N=10%		2.6		W
		V_{DD}=3.6V, THD+N=1%		2.1		W
	Maximum Output Power Load=4Ω+33μH	V_{DD}=4.2V, THD+N=10%		4.5		W
		V_{DD}=4.2V, THD+N=1%		3.7		W
		V_{DD}=3.6V, THD+N=10%		3.6		W
		V_{DD}=3.6V, THD+N=1%		3.2		W
	Maximum Output Power Load=3Ω+33μH	V_{DD}=4.2V, THD+N=10%		5.0		W
		V_{DD}=4.2V, THD+N=1%		4.2		W
		V_{DD}=3.6V, THD+N=10%		3.8		W
		V_{DD}=3.6V, THD+N=1%		3.5		W
$P_{O, ALC}$ (Mode 1 & 2) ALC On	Constant Output Power Load=8Ω+33μH	V_{DD}=4.2V, V_{in}=300mV_{RMS}		2.1		W
		V_{DD}=3.6V, V_{in}=300mV_{RMS}		2.0		W
	Constant Output Power Load=4Ω+33μH	V_{DD}=4.2V, V_{in}=300mV_{RMS}		3.5		W
		V_{DD}=3.6V, V_{in}=300mV_{RMS}		3.1		W
	Constant Output Power Load=3Ω+33μH	V_{DD}=4.2V, V_{in}=300mV_{RMS}		4.0		W
		V_{DD}=3.6V, V_{in}=300mV_{RMS}		3.4		W
THD+N	Load=4Ω+33μH Mode 3, ALC Off	P_O=0.5W		0.05		%
		P_O=2.0W		0.04		%
	Load=4Ω+33μH, V_{in}=0.3mV_{RMS} Mode 1 & 2, ALC On	V_{DD}=4.2V, P_O=3.5W		0.5		%
		V_{DD}=3.6V, P_O=3.1W		0.4		%

ELECTRICAL CHARACTERISTICS (Cont'd)

VDD=3.6V, Mode 1, ALCB=Low, CPENB=Low, C_{IN}=1μF, R_{IN}=0kΩ (A_V=27.6dB), C_{AVDD}=1μF, C_{CVDD}=10μF, $C_{F1/2}$=2.2μF, C_{OUT}=10μF//220μF, C_{PVDD}=10μF, f=1kHz, R_L=4Ω+33μH, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_V	Maximum Voltage Gain	Mode 1 (ALC On)		27.6		dB
		Mode 2 (ALC On)		24		dB
		Mode 3 (ALC Off)		24		dB
R_{IN}	Input Resistance	@ INP, INN		24		kΩ
R_O	Output Resistance in Shutdown	EN Low @ VOP, VON		3		kΩ
V_{OS}	Output Offset Voltage	Inputs AC-Grounded, No Load		±10		mV
V_N	Output Voltage Noise	A_V=24dB, A-weighted Inputs AC-Grounded		180		μV_{RMS}
PSRR	Power Supply Rejection Ratio	200mV_{PP}, f=217Hz		78		dB
		200mV_{PP}, f=1kHz		70		
CMRR	Common Mode Rejection Ratio			75		dB
SNR	Signal-To-Noise Ratio	Maximum Output (3.5V_{RMS}) with THD+N<1%, A_V=24dB, A-weighted		87		dB
f_{PWM}	PWM Switching Frequency	V_{DD}=3.6V		1		MHz
T_{SETUP}	Startup Time	V_{DD}=3.6V		40		ms
I_{LIMIT}	Over-Current Limit	VDD=PVDD=3.6V		1.4		A
T_{HICCUP}	Over-Current Recovery Time			200		ms
AUTOMATIC LEVEL CONTROL (ALC)						
A_{MAX}	Maximum ALC Attenuation			10		dB
T_{ATT}	ALC Attack Time			10		ms
T_{REL}	ALC Release Time			2		s
MODE CONTROL						
T_{LO}	Time of EN Low		0.5		10	μs
T_{HI}	Time of EN High		0.5			μs
T_{RST}	Time for Mode Reset, Active Low		50		500	μs
T_{SHDN}	Time for Shutdown, Active Low		5			ms

Note:

(1) A 33μH inductor was placed in series with the load resistor to emulate a small speaker for efficiency measurements.

(2) The 33kHz lowpass filter is required even if the analyzer has an internal lowpass filter. An RC lowpass filter (100Ω, 47nF) is used on each output for the data sheet graphs.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD=3.6V, Mode 1, ALCB=Low, CPENB=Low, C_{IN}=1μF, R_{IN}=0kΩ (AV=27.6dB), C_{AVDD}=1μF, C_{CVDD}=10μF, $C_{F1/2}$=2.2μF, C_{OUT}=10μF//220μF, C_{PVDD}=10μF, f=1kHz, R_L=4Ω+33μH, T_A=25°C, unless otherwise specified.

List of Performance Characteristic Plots

DESCRIPTION	CONDITIONS	FIGURE #
ALC Output Power vs. Supply Voltage	R_L=8Ω+33μH/4Ω+33μH, Mode 1 (ALC On)	3
	R_L=8Ω+33μH/4Ω+33μH, Mode 2 (ALC On)	4
Output Power vs. Supply Voltage	R_L=8Ω+33μH, THD+N=1%, 10%, Mode 3 (ALC Off)	5
	R_L=4Ω+33μH, THD+N=1%, 10%, Mode 3 (ALC Off)	6
Output Power vs. Input Voltage	V_{DD}=3.6V, R_L=8Ω+33μH, Mode 1 & 2	7
	V_{DD}=3.6V, R_L=8Ω+33μH, Mode 2 & 3	8
	V_{DD}=4.2V, R_L=8Ω+33μH, Mode 1 & 2	9
	V_{DD}=4.2V, R_L=8Ω+33μH, Mode 2 & 3	10
	V_{DD}=3.6V, R_L=4Ω+33μH, Mode 1 & 2	11
	V_{DD}=3.6V, R_L=4Ω+33μH, Mode 2 & 3	12
	V_{DD}=4.2V, R_L=4Ω+33μH, Mode 1 & 2	13
	V_{DD}=4.2V, R_L=4Ω+33μH, Mode 2 & 3	14
Output Power (on Activation of Charge Pump Regulator) vs. Supply Voltage	R_L=8Ω+33μH & 4Ω+33μH, Mode 1 (ALC On)	15
	R_L=8Ω+33μH & 4Ω+33μH, Mode 3 (ALC Off)	16
Power Dissipation vs. Output Power	R_L=8Ω+33μH, Mode 1, V_{DD}=3.6V, 4.2V	17
	R_L=4Ω+33μH, Mode 1, V_{DD}=3.6V, 4.2V	18
Efficiency vs. Output Power	R_L=8Ω+33μH, Mode 1, V_{DD}=3.6V, 4.2V	19
	R_L=4Ω+33μH, Mode 1, V_{DD}=3.6V, 4.2V	20
THD+N vs. Output Power	R_L=8Ω+33μH, Mode 3, V_{DD}=3.6V, 4.2V	21
	R_L=4Ω+33μH, Mode 3, V_{DD}=3.6V, 4.2V	22
THD+N vs. Input Voltage	R_L=8Ω+33μH, Mode 1, V_{DD}=3.6V, 4.2V	23
	R_L=4Ω+33μH, Mode 1, V_{DD}=3.6V, 4.2V	24
	R_L=8Ω+33μH, Mode 2, V_{DD}=3.6V, 4.2V	25
	R_L=4Ω+33μH, Mode 2, V_{DD}=3.6V, 4.2V	26
THD+N vs. Input Frequency	V_{DD}=3.6V, R_L=8Ω+33μH, Mode 1, P_O=0.25W, 0.5W	27
	V_{DD}=4.2V, R_L=8Ω+33μH, Mode 1, P_O=0.25W, 0.5W	28
	V_{DD}=3.6V, R_L=4Ω+33μH, Mode 1, P_O=0.5W, 1.0W	29
	V_{DD}=4.2V, R_L=4Ω+33μH, Mode 1, P_O=0.5W, 1.0W	30
PSRR vs. Input Frequency	R_L=8Ω+33μH, Input AC-Grounded, Mode 1, V_{DD}=3.6V, 4.2V	31
	R_L=4Ω+33μH, Input AC-Grounded, Mode 1, V_{DD}=3.6V, 4.2V	32
Quiescent Current vs. Supply Voltage	Input AC-Grounded, No Load, Mode 1	33
ALC Attack Time	V_{DD}=4.2V, Vin=0.14V_{RMS} ~ 0.44V_{RMS}, R_L=4Ω+33μH, Mode 1	34
ALC Release Time	V_{DD}=4.2V, Vin=0.44V_{RMS} ~ 0.14V_{RMS}, R_L=4Ω+33μH, Mode 1	35
Charge Pump Mode Transition Waveforms	V_{DD}=4.2V, Vin=50mV_{RMS} ~100mV_{RMS}, R_L=4Ω+33μH, Mode 1	36
(VOP-VON) Startup Waveforms	V_{DD}=4.2V, R_L=4Ω+33μH, Mode 1	37
(VOP-VON) Shutdown Waveforms	V_{DD}=4.2V, R_L=4Ω+33μH, Mode 1	38

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

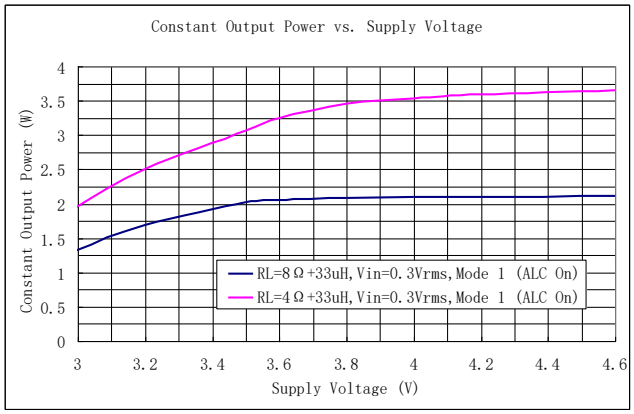


Figure 3: ALC Output Power vs. Supply Voltage

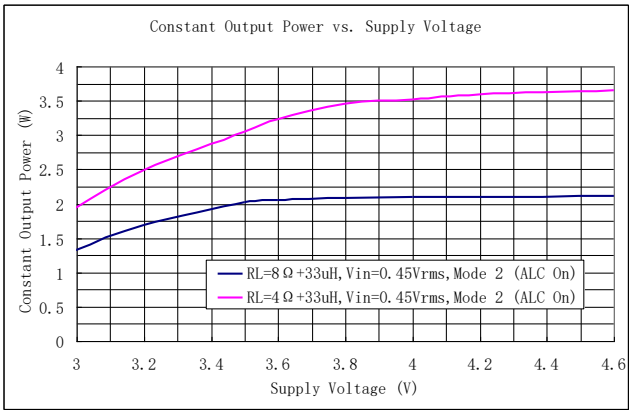


Figure 4: ALC Output Power vs. Supply Voltage

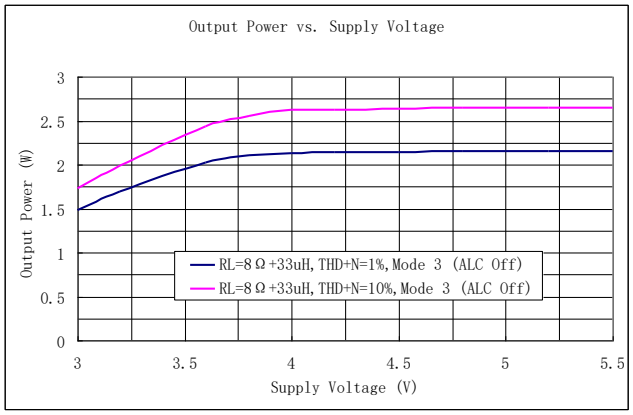


Figure 5: Output Power vs. Supply Voltage

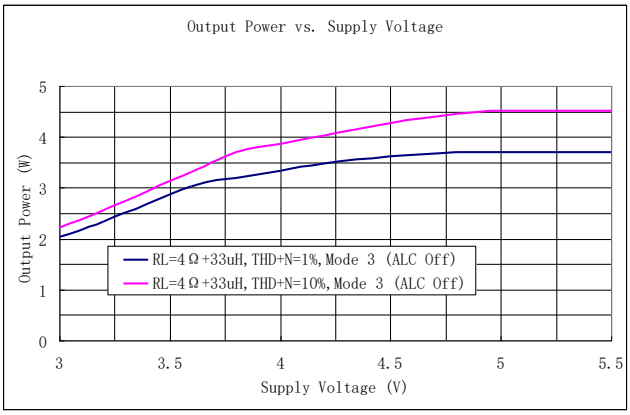


Figure 6: Output Power vs. Supply Voltage

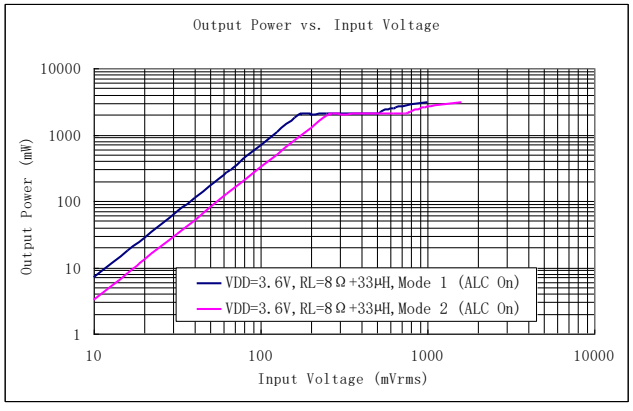


Figure 7: Output Power vs. Input Voltage

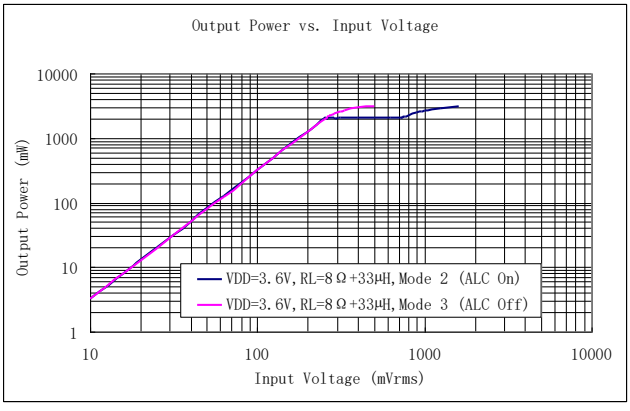


Figure 8: Output Power vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

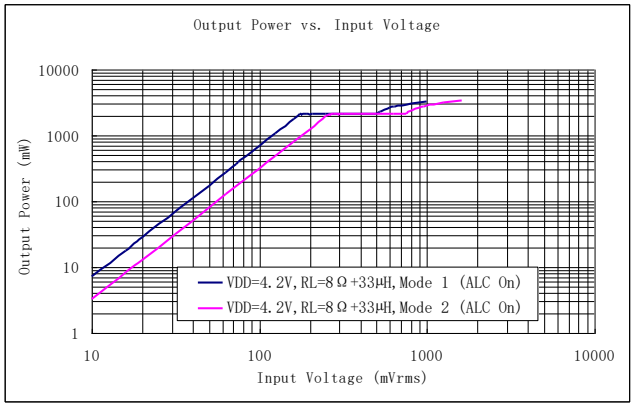


Figure 9: Output Power vs. Input Voltage

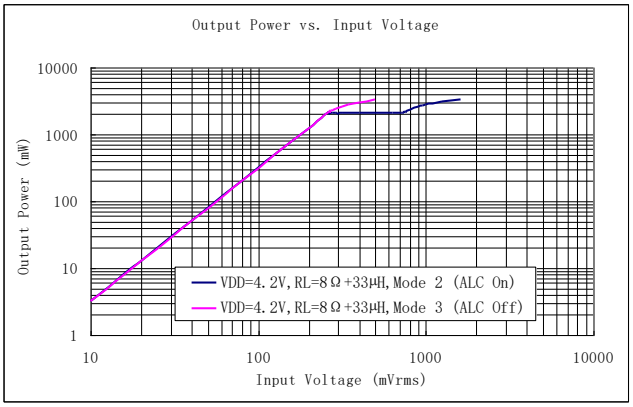


Figure 10: Output Power vs. Input Voltage

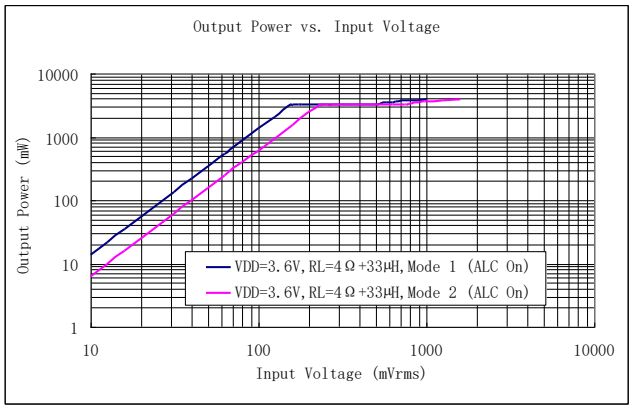


Figure 11: Output Power vs. Input Voltage

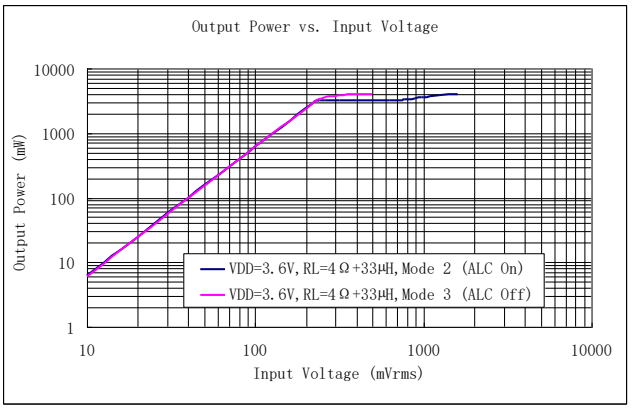


Figure 12: Output Power vs. Input Voltage

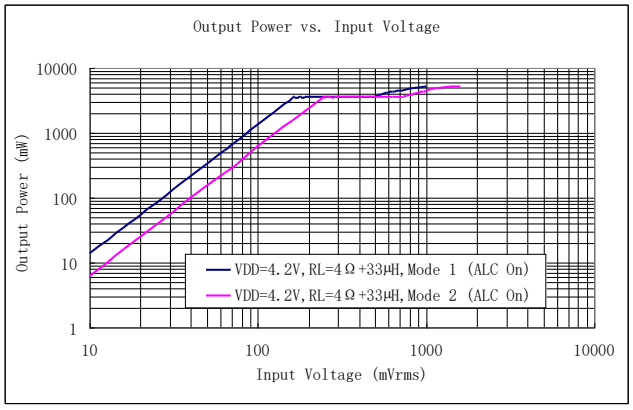


Figure 13: Output Power vs. Input Voltage

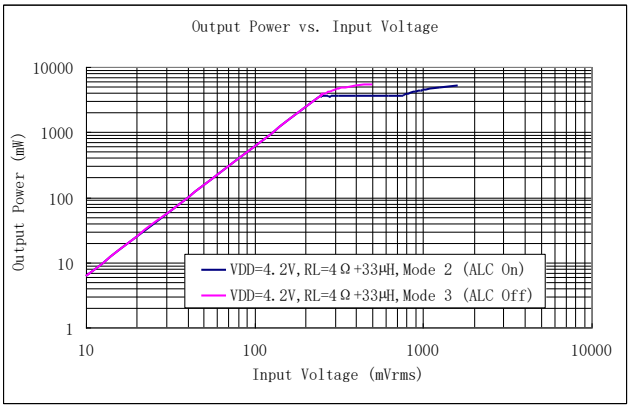


Figure 14: Output Power vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

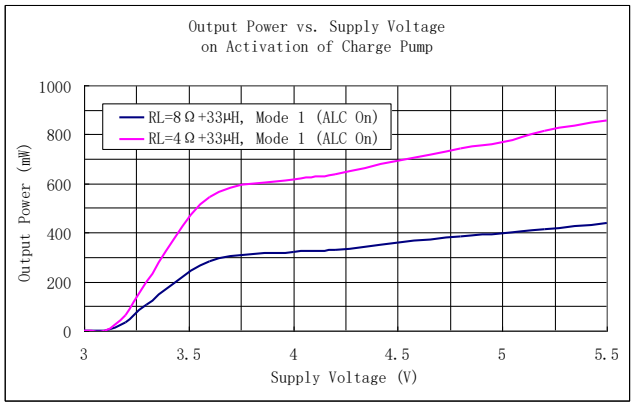


Figure 15: Output Power (on Activation of Charge Pump Regulator) vs. Supply Voltage

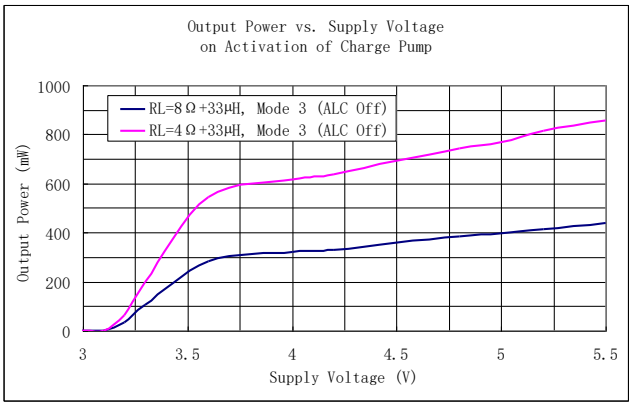


Figure 16: Output Power (on Activation of Charge Pump Regulator) vs. Supply Voltage

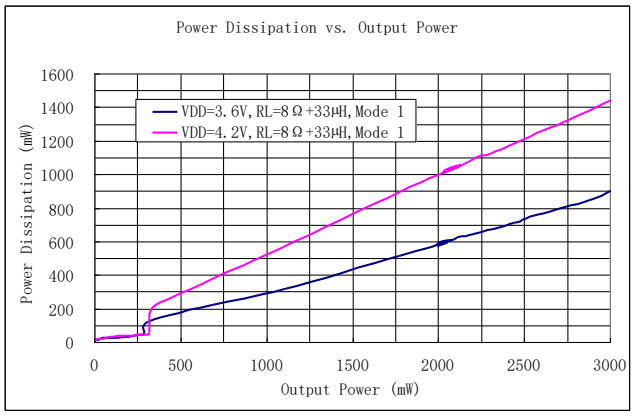


Figure 17: Power Dissipation vs. Output Power

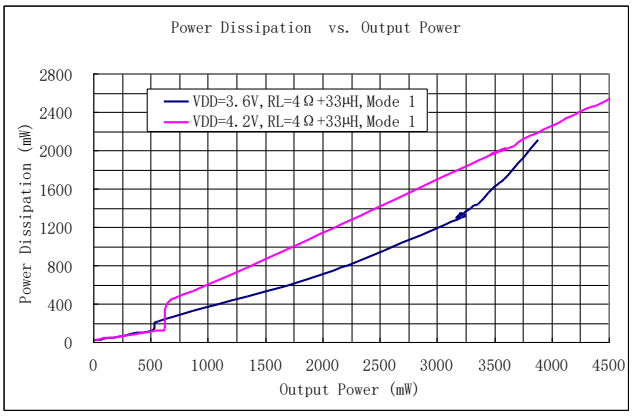


Figure 18: Power Dissipation vs. Output Power

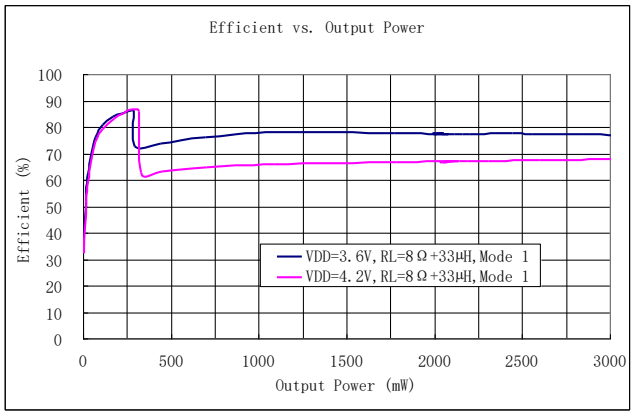


Figure 19: Efficiency vs. Output Power

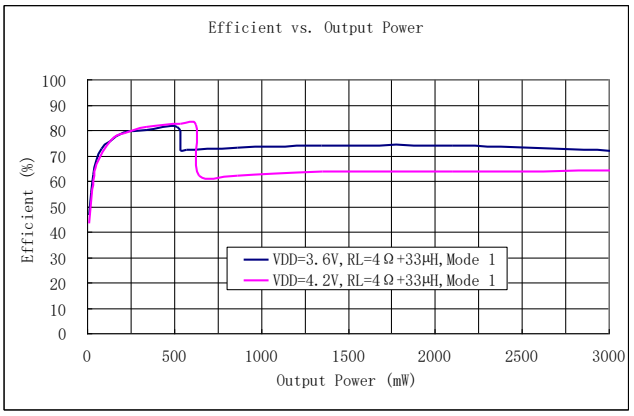


Figure 20: Efficiency vs. Output Power

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

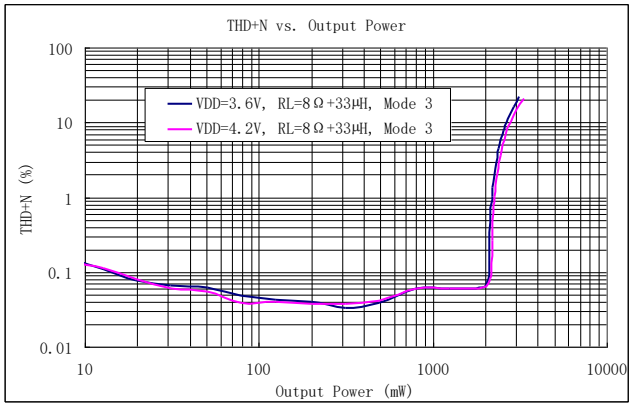


Figure 21: THD+N vs. Output Power

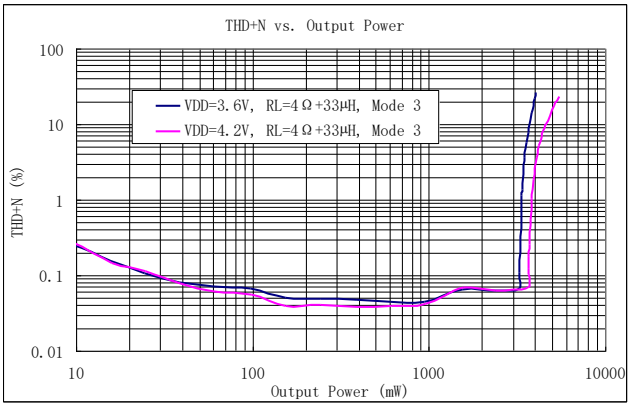


Figure 22: THD+N vs. Output Power

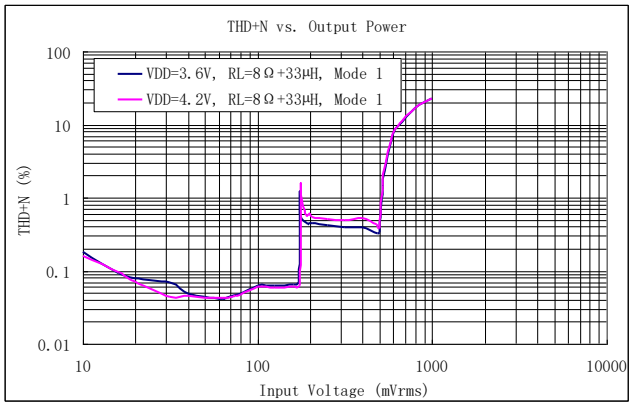


Figure 23: THD+N vs. Input Voltage

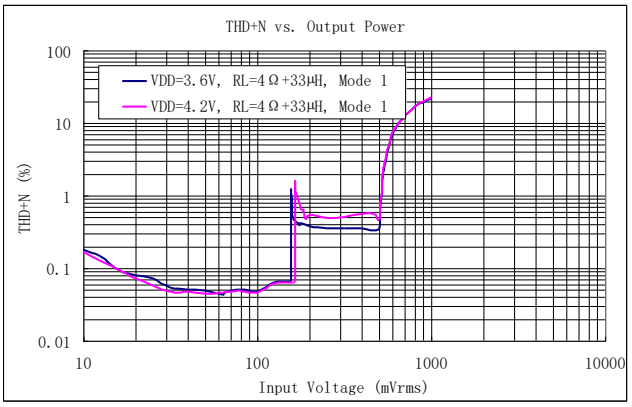


Figure 24: THD+N vs. Input Voltage

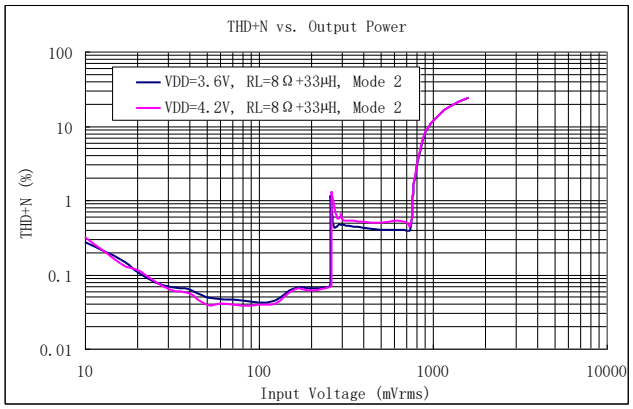


Figure 25: THD+N vs. Input Voltage

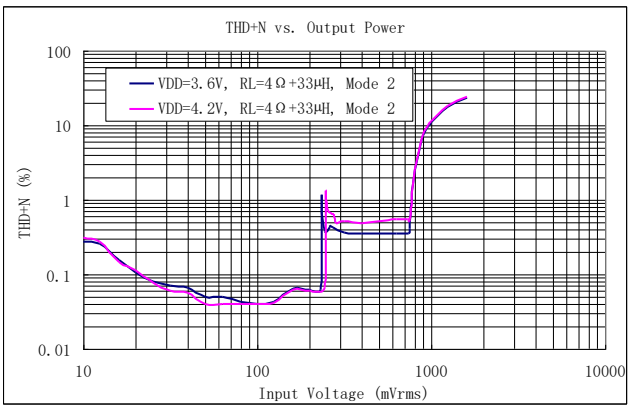


Figure 26: THD+N vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

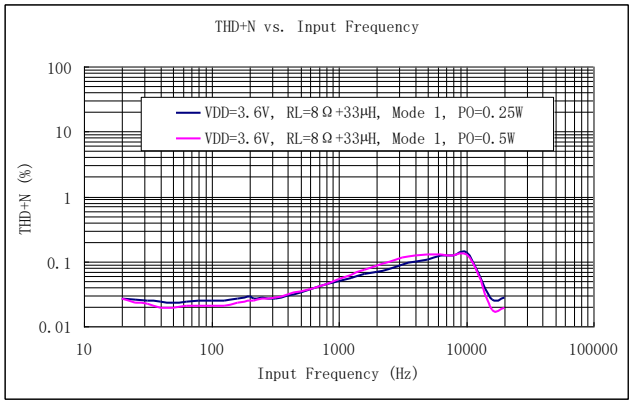


Figure 27: THD+N vs. Input Frequency

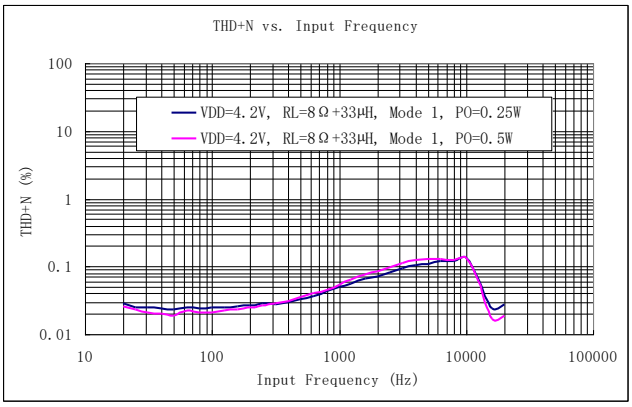


Figure 28: THD+N vs. Input Frequency

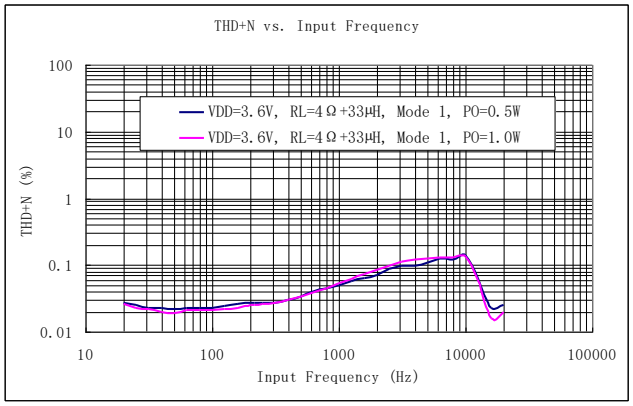


Figure 29: THD+N vs. Input Frequency

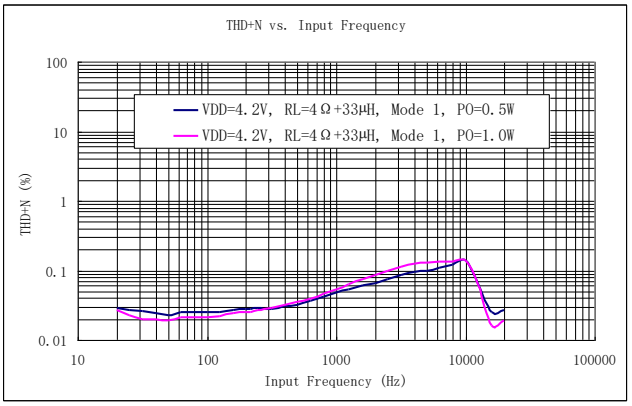


Figure 30: THD+N vs. Input Frequency

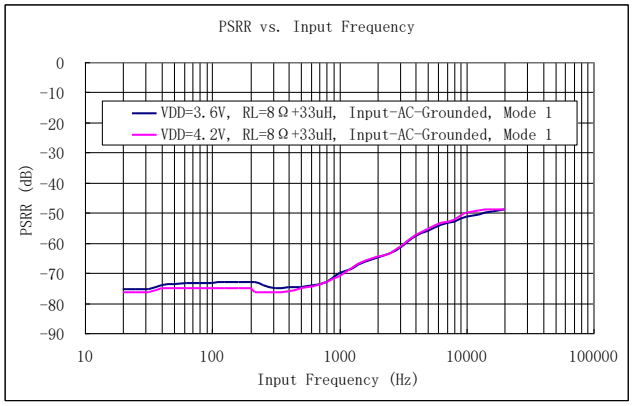


Figure 31: PSRR vs. Input Frequency

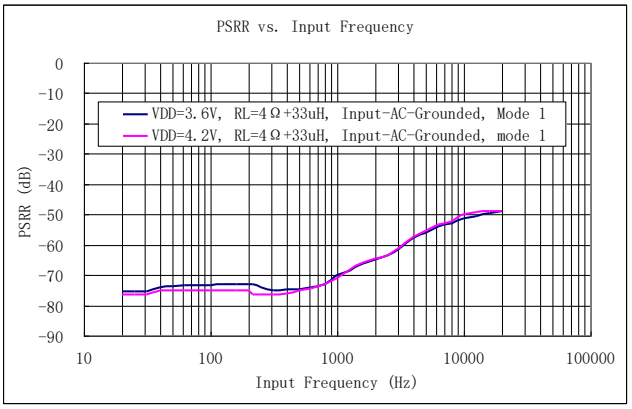


Figure 32: PSRR vs. Input Frequency

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

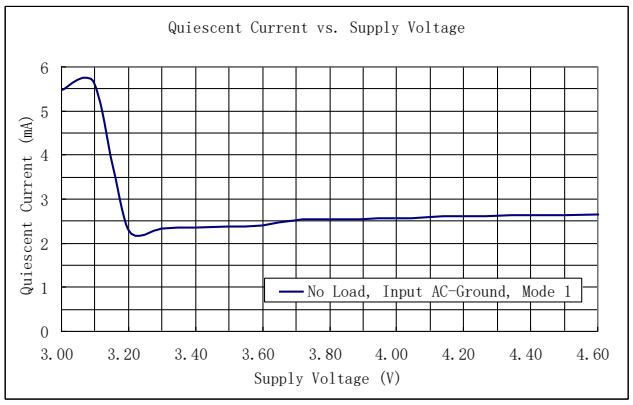


Figure 33: Quiescent Current vs. Supply Voltage

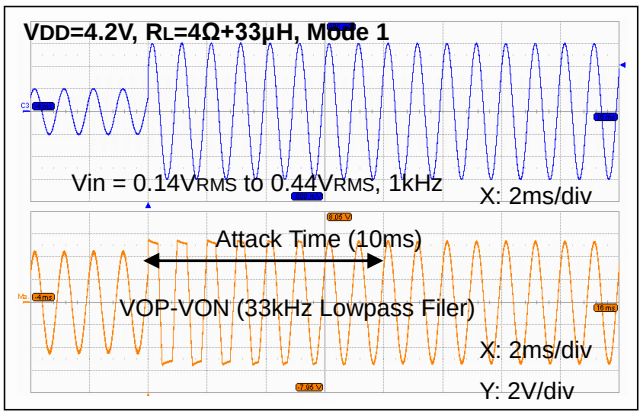


Figure 34: ALC Attack Time

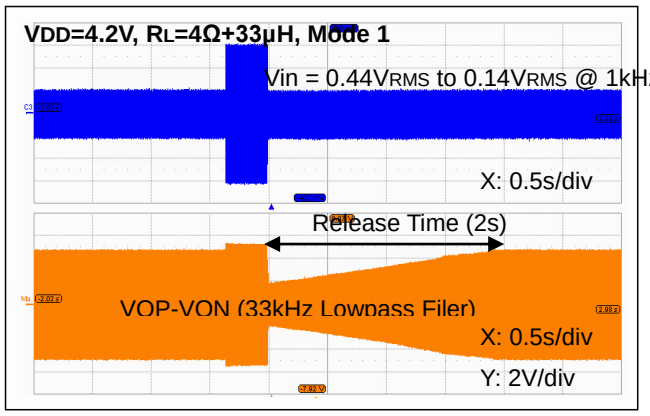


Figure 35: ALC Release Time

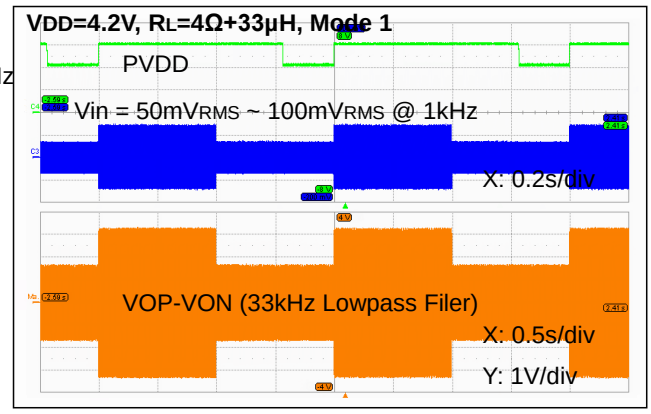


Figure 36: Charge Pump Mode Transition Waveforms

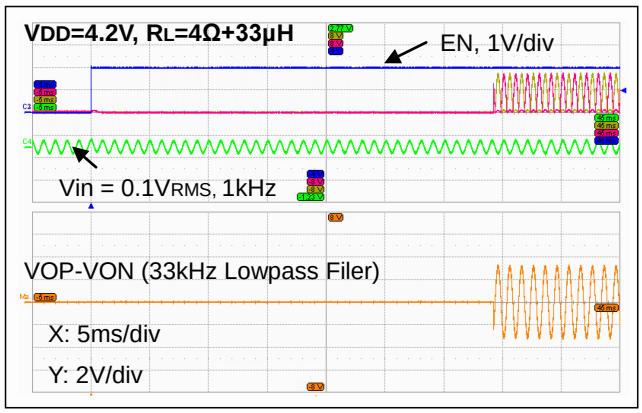


Figure 37: (VOP-VON) Startup Waveforms

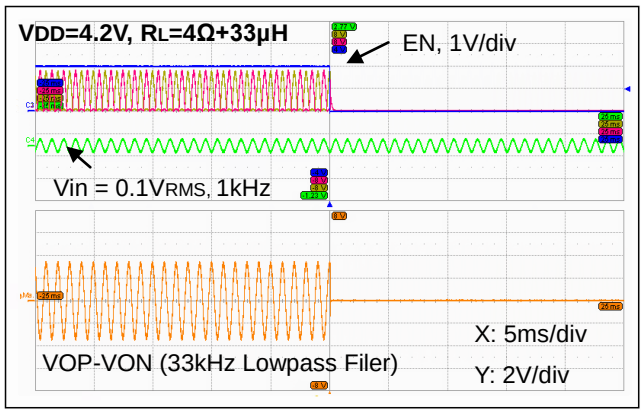


Figure 38: (VOP-VON) Shutdown Waveforms

APPLICATION INFORMATION

The ft2830 is a highly efficient 4.5W Class-G audio power amplifier with automatic level control (ALC) for use in battery-powered portable devices. It integrates a filterless Class-D audio amplifier with a Class-G charge pump regulator based upon proprietary ***Dual-Pump***^{TM} topology. It operates from 3.2V to 4.6V supply. When operating with a 4.2V supply voltage, the ft2830 can deliver into a 4Ω load a maximum output power up to 4.5W with 10% THD+N, or 3.7W with 1% THD+N. With a 3Ω load, it can deliver a maximum output power up to 5W with 10% THD+N, or 4.2W with 1% THD+N. Its high efficiency, up to 83%, helps extend battery life.

In ft2830, the power supply rail of the amplifier output stage is internally boosted and regulated at 6.2V by an adaptive charge pump regulator based upon the ***Dual-Pump***^{TM} topology, allowing for a much louder audio output than a stand-alone one directly connected to the battery. It makes ft2830 an ideal audio solution for portable devices, which are powered by a single-cell lithium battery while requiring higher audio loudness.

The ft2830 features ALC to constantly monitor and safeguard the audio outputs against the boosted supply voltage, preventing output clipping distortion, excessive power dissipation, or hazardous speaker over-load. Once an over-level condition is detected, the ALC lowers the voltage gain of the audio amplifier proportionally to eliminate output clipping distortion while maintaining a maximum dynamic range of the audio outputs allowed by the boosted supply voltage. In ALC mode, with a 4.2V supply voltage, the ft2830 can deliver a constant output power at 3.5W into a 4Ω load, or 4W into a 3Ω load, with 0.5% THD+N.

As specifically designed for portable device applications, the ft2830 incorporates a shutdown mode to minimize the power consumption by holding the EN pin to ground. It also includes comprehensive protection features against various operating faults such as over-current, short-circuit, over-temperature, and under-voltage for a safe and reliable operation.

CLASS-G CHARGE PUMP REGULATOR

To allow for a much louder audio output, an integrated adaptive charge pump regulator is employed to boost PVDD, the power rail for the amplifier output stage. Whenever the audio outputs are higher than a prescribed level for an extended period of time, the charge pump regulator will be activated to boost and regulate PVOUT at 6.2V. In this case, the charge pump regulator operates in the regulation mode. For a proper operation, the boosted voltage PVOUT generated by the charge pump regulator must be externally shorted to PVDD pins via a sufficiently wide metal trace on the system board.

On the other hand, when the audio outputs are less than a prescribed level for an extended period of time, the charge pump regulator will be de-biased and forced into the standby mode. In the standby mode, the amplifier output stage is powered directly by VDD, the battery voltage, through an internal power switch. This adaptive nature of the charge pump regulator can greatly improve the power efficiency of ft2830 when playing audio and thus extends battery life.

DUAL-PUMP^{TM} TECHNOLOGY

In order to maximize the output power, the ft2830 employs a proprietary ***Dual-Pump***^{TM} topology for the internal charge pump regulator using two flying capacitors to boost the supply voltage to a higher value. To limit the inrush current to an acceptable value when the supply voltage is first applied to the device, the charge pump regulator incorporates soft-start function. Furthermore, when a short-circuit condition at the boosted voltage is detected, the ft2830 limits the charging current to about 100mA for a safe operation.

Compared with a conventional charge pump topology using a single flying capacitor, the output current capability of the ***Dual-Pump***^{TM} can be largely enhanced and the output voltage ripples minimized. In this manner, the performance of the Class-D audio amplifier can be significantly improved, particularly for the speakers whose impedance is less than 6Ω. With the ***Dual-Pump***^{TM} topology, the ft2830 can deliver up to 4.5W into a 4Ω load with 10% THD+N when powered by a single-cell lithium battery.

Selection of Charge Pump Flying Capacitors (C_{F1} & C_{F2})

A nominal value of 2.2μF is recommended for the flying capacitors (C_{F1} and C_{F2}) of the charge pump regulator,

but other values can be used. A low equivalent-series-resistance (ESR) ceramic capacitor, such as X7R or X5R, is recommended.

Selection of Charge Pump Output Capacitor (COUT)

For best performance, a 10µF low ESR ceramic capacitor in parallel with a tantalum or electrolytic capacitor (220µF or higher) is recommended for the output capacitor (COUT) of the charge pump regulator, but other values can be used.

CHARGE PUMP REGULATOR CONTROL

For applications where minimum EMI emission is desired, it may become necessary to disable the charge pump regulator by asserting the CPENB pin high. In this manner, the ft2830 operates as a conventional Class-D amplifier and its maximum output power is limited by the supply voltage. On the contrary, with the CPENB pin pulled low or left unconnected, the ft2920 operates as a Class-G audio amplifier with the charge pump regulator to be adaptively activated in response to the level of audio outputs.

CPENB	Description
Low or unconnected	Charge pump regulator is adaptively activated on the level of audio outputs.
High	Charge pump regulator is disabled all the time.

Table 1: Charge Pump Regulator Control

OPERATING MODE CONTROL AND GAIN SETTING

To support for a wide range of applications, the ft2830 incorporates one-wire pulse control to configure the operating mode and the voltage gain. By applying a string of pulses to the EN pin, users can enable (Constant Output Power mode) or disable (Maximum Output Power mode) the ALC function as well as set the voltage gain. The operating mode is advanced and updated on each low-to-high transition of the pulses applied onto the EN pin. The detailed timing diagram of the one-wire pulse control to select the operating mode is shown in Figure 39.

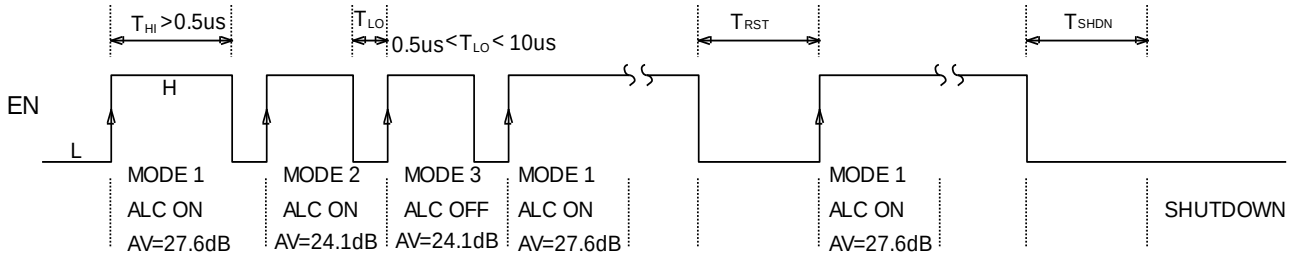


Figure 39: Operating Mode Control Diagram

Three operating modes are configured by the application of a string of pulses onto the EN pin. After an initial application of the power supply, the first low-to-high transition at the EN pin will set the device into Mode 1, where the voltage gain is set at 27.6dB and the ALC function enabled. On the next low-to-high transition, the device advances into Mode 2, where the voltage gain is set at 24dB and the ALC function remains enabled. Finally, on the third low-to-high transition, the device advances into Mode 3, where the ALC function is disabled and the voltage gain remains at 24dB. The operating modes will be cycled and repeated in the same manner as described above for consecutive pulses applied.

Note that each individual pulse must be longer than a minimum of 0.5µs to be recognized. Any pulses shorter than 0.5µs may be ignored. The state of the mode operation can be reset back to Mode 1 by holding the EN pin low more than 50µs but less than 500µs, regardless of the state it is currently operating. Whenever the EN pin held low for more than 5ms, the device enters into the shutdown mode, where all the internal circuitry is de-biased. Once the device is forced into shutdown mode, one or multiple pulses are required for the ft2830 to return to the desired mode of operation.

Mode	# of Pulses	Voltage Gain	ALC Function
Mode 1	1	27.6dB (24X)	Enable
Mode 2	2	24dB (16X)	Enable
Mode 3	3	24dB (16X)	Disable

Table 2: Mode of Operation

Operating Mode Reset

The state of the mode operation can be reset back to the default mode, Mode 1 (Av=27.6dB, ALC On) by holding the EN pin low for more than 50μs but less than 500μs, regardless of the state it is currently operating.

Shutdown Mode

When the EN pin is held low for 5ms (typical) or longer, the ft2830 will be forced into the shutdown mode. During the shutdown mode, the supply current will be significantly reduced to less than 1μA.

AUTOMATIC LEVEL CONTROL (ALC)

The automatic level control is to maintain the output signal level for a maximum output swing without distortion when an excessive input that may cause output clipping is applied. With the ALC function, the ft2830 lowers the gain of the amplifier to an appropriate value such that the clipping at the output is avoided. It also eliminates the clipping of the output signal due to the decrease of the power-supply voltage.

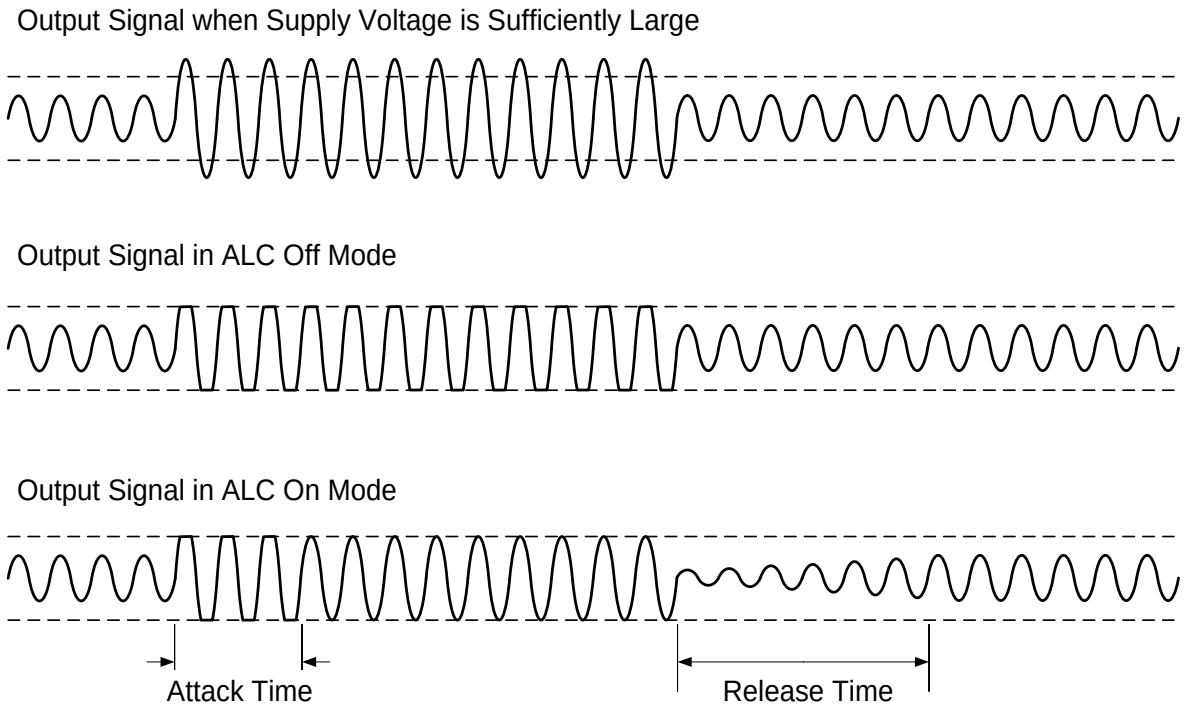


Figure 40: Automatic Level Control Function Diagram

The attack time is defined as the time interval required for the gain to fall to its steady-state gain less 3dB approximately, presumed that a sufficiently large input signal is applied. The release time is the time interval required for the amplifier to exit out of the present mode of operation. See Table 3.

Mode	Attack Time (ms)	Release Time (s)
Mode 1 & 2 (ALC On)	10	2.0

Table 3: Attack Time & Release Time

ALC CONTROL

When the ALCB pin is pulled low or left unconnected, the ALC control is set by the one-wire pulses applied at the EN pin. When the ALCB pin is asserted high, the ALC function will be disabled all the time.

ALCB	Description
Low or unconnected	ALC control is set by the one-wire pulses applied at the EN pin.
High	ALC function is disabled all the time.

Table 4: ALC Control

VOLTAGE GAIN SETTING

The overall voltage gain of the audio amplifier can be externally adjusted by inserting additional input resistors, R_{IN}, in series with the input capacitors. The value of R_{IN} for a given voltage gain is calculated by Equation 1.

$$A_V = 576 / (R_{IN} + 24), \text{ for Mode 1} \quad (1)$$
$$A_V = 384 / (R_{IN} + 24), \text{ for Mode 2 and 3}$$

In Equation 1, A_V is the desired voltage gain of the amplifier and R_{IN} is expressed in kΩ. Table 5 shows suitable resistor values of R_{IN} that can be used for various voltage gains.

RIN, kΩ	0	5	10	22	33	47	66
AV, dB (Mode 1)	27.6	26.0	24.6	22.0	20.1	18.2	16.1
AV, dB (Mode 2 & 3)	24.1	22.4	21.0	18.4	16.6	14.7	12.6

Table 5: External Input Resistor Values Required for Various Voltage Gains

The choice of the voltage gain will strongly influence the loudness and quality of audio sounds. In general, the higher the voltage gain is, the louder the sound is perceived. However an excessive voltage gain may cause audio outputs to be severely compressed or clipped for high-level (loud) audio sounds. On the other hand, an unusually low gain may cause relatively low-level (quite) sounds soft or inaudible. Thus it is crucial to choose a proper voltage gain for well balanced audio quality.

The voltage gain is chosen based upon various system-level considerations including the supply voltage, the dynamic range of audio sources and speaker loads, and the desired sound effects. As a general guideline, the voltage gain can be simply expressed in Equation 2. In the equation, $V_{IN, MAX}$ (in V_{RMS}) is the maximum input level from the audio source, PVDD (in volts) is the supply voltage, and α is the design parameter, which ranges from 0.64 to 2.0. The higher α is, the higher the average output power (louder) is, with some degree of compression for high-level audio sounds.

$$A_V = \frac{\alpha \times PVDD}{V_{IN, MAX}} \quad (2)$$

As an example, Table 6 shows the voltage gain for various input levels with α at about 1.4 when operating in Mode 1. In the table, R_{IN} is the external input resistor in series with the input capacitor.

$V_{IN, MAX}$ (V_{RMS})	A_V (V/V)	A_V (dB)	R_{IN} (kΩ)
0.5	17	25	10
0.7	13	22	20
1.0	10	20	33

Table 6: Typical Voltage Gain Setting for Various Input Levels

Table 7 shows a typical resistor value of RIN and the corresponding voltage gain that can be used for various input levels when operating in Mode 1. In the table, the "VIN, ENTRY" and "VIN, EXIT" refer to the input levels at the entry-point and the exit-point respectively of the ALC range where the device operates in the ALC mode. The "VIN, ENTRY" and "VIN, EXIT", expressed in VRMS, can be calculated by Equation 3 and 4.

$$V_{IN,EXTRY} = \frac{4.0}{A_V} \quad (3)$$

$$V_{IN,EXIT} = \frac{12.0}{A_V} \quad (4)$$

RIN (kΩ)	AV (V/V)	AV (dB)	Audio Inputs in ALC Range		Po, ALC (W) with 4Ω Load
			VIN, ENTRY (VRMS)	VIN, EXIT (VRMS)	
10	17	25	0.24	0.71	3.1
20	13	22	0.30	0.92	3.1
33	10	20	0.40	1.20	3.1

Table 7: Typical Input Resistor Values and Voltage Gain for Various Input Levels

Click-and-Pop Suppression

The ft2830 audio power amplifier features comprehensive click-and-pop suppression. During startup, the click-and-pop suppression circuitry reduces any audible transients internal to the device. When entering into shutdown, the differential audio outputs are pulled to ground through their individual internal resistors (3kΩ) simultaneously.

PSRR Enhancement

Without a dedicated pin for the common-mode voltage bias and an external holding capacitor onto the pin, the ft2830 achieves a high PSRR, 70dB at 1kHz, thanks to a proprietary design technique.

PROTECTION MODES

The ft2830 incorporates various protection functions against possible operating faults for a safe operation. It includes Under-voltage Lockout (UVLO), Over-Current Protection (OCP), and Over-Temperature Shutdown (OTSD).

Under-Voltage Lockout (UVLO)

The ft2830 incorporates circuitry to detect a low supply voltage for safe and reliable operation. When the supply voltage is first applied, the ft2830 will remain inactive until the supply voltage exceeds 2.3V (V_{UVLU}). When the supply voltage is removed and drops below 2.0V (V_{UVLD}), the ft2830 enters into shutdown mode immediately.

Over-Temperature Shutdown (OTSD)

When the die temperature exceeds a preset threshold (160°C), the device enters into the over-temperature shutdown mode, where two differential outputs are pulled to ground through an internal resistor (3kΩ) individually. The device will resume normal operation once the die temperature returns to a lower temperature, which is about 20°C lower than the threshold.

Over-Current Protection (OCP)

During operation, the output of Class-D audio amplifier constantly monitors for any over-current and/or short-circuit conditions. When a short-circuit condition between two differential outputs, differential output to PVDD or ground is detected, the output stage of the amplifier is immediately forced into high impedance state. Once the fault condition persists over a prescribed period, the ft2830 then enters into the shutdown mode and remains in this mode for about 200ms. During the shutdown, the power switches of the charge pump regulator are also turned off, and PVDD is discharged through a resistor to ground.

When the shutdown mode times out, the ft2830 will initiate another startup sequence and then check if the short-circuit condition has been removed. Meanwhile, the charge pump regulator tries to bring PVDD up to the preset voltage again. If the fault condition is still present, the ft2830 will repeat itself for the process of a startup followed by detection, qualification, and shutdown. It is so-called the hiccup mode of operation. Once the fault condition is removed, the ft2830 automatically restores to its normal mode of operation.

Although the output stage of the Class-D audio amplifier can withstand a short between VOP and VON, do not connect either output directly to GND, PVOUT, PVDD, CVDD, or AVDD as this might damage the device permanently specifically when the supply voltage is higher than 4.6V.

CLASS-D AUDIO AMPLIFIER

The Class-D audio amplifier in the ft2830 operates in much the same way as a traditional Class-D amplifier and similarly offers much higher power efficiency than Class-AB amplifiers. The high efficiency of a Class-D operation is achieved by the switching operation of the output stage of the amplifier. The power loss associated with the output stage is limited to the conduction and switching loss of the power MOSFETs, which are much less than the power loss associated with a linear output stage in Class-AB amplifiers.

Fully Differential Amplifier

The ft2830 includes a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the amplifier gain. The common-mode feedback ensures that the common-mode voltage at the output is biased substantially close to an internally-generated voltage reference regardless of the common-mode voltage of the inputs. Although the ft2830 supports for a single-ended input, differential inputs are recommended for the applications, where the environment can be noisy like a wireless handset, in order to ensure maximum SNR.

Low-EMI Filterless Output Stage

Traditional Class-D audio amplifiers require for the use of external LC filters, or shielding, to meet EN55022B electromagnetic-interference (EMI) regulation standards. The ft2830 applies an edge-rate control circuitry to reduce EMI emission, while maintaining high power efficiency. Above 10MHz, the wideband spectrum looks like noise for EMI purposes.

Filterless Design

Traditional Class D amplifiers require an output filter to recover the audio signal from the amplifier's output. The filter adds cost, increases the solution size of the amplifier, and can decrease efficiency and THD+N performance. The traditional PWM scheme uses large differential output swings (twice of supply voltage peak-to-peak) and causes large ripple currents. Any parasitic resistance in the filter components results in loss of power and lowers the efficiency.

The ft2830 does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. By eliminating the output filter, a smaller, less costly, and more efficient solution can be accomplished.

Because the frequency of the ft2830 output is well beyond the bandwidth of most speakers, voice coil movement due to the square-wave frequency is very small. Although this movement is small, a speaker not designed to handle the additional power can be damaged. For optimum results, use a speaker with a series inductance greater than 10uH. Typical 8Ω speakers exhibit series inductances in the range from 20μH to 100uH.

EMI Reduction

The ft2830 does not require an LC output filter for short connections from the amplifier to the speaker. However, additional EMI suppressions can be made by use of a ferrite bead in conjunction with a capacitor, as shown in Figure 41. Choose a ferrite bead with low DC resistance (DCR) and high impedance (100Ω ~ 220Ω) at high

frequencies (>100MHz). The current flowing through the ferrite bead must be also taken into consideration. The effectiveness of ferrites can be greatly aggravated at much lower than the rated current values. Choose a ferrite bead with a rated current value no less than 2A. The capacitor value varies based on the ferrite bead chosen and the actual speaker lead length. Choose a capacitor less than 1nF based on EMI performance

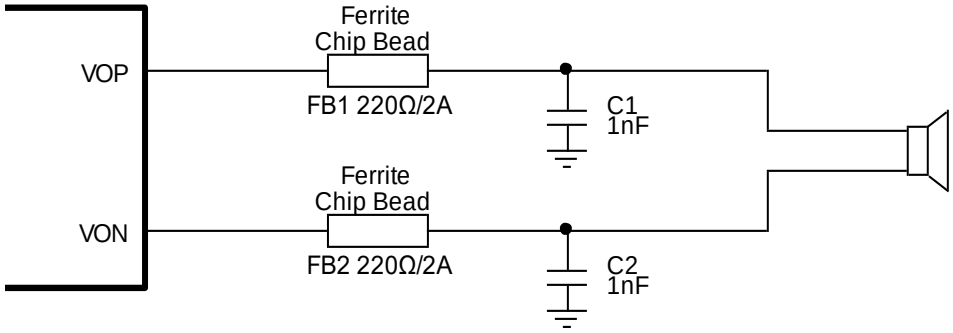


Figure 41: Ferrite Bead Filter to Reduce EMI

Decoupling Capacitor (Cs)

The ft2830 is a high performance Class-D audio amplifier, which requires adequate power supply decoupling to ensure its high efficiency operation with low total harmonic distortion. Sufficient power supply coupling also prevents oscillations for long lead lengths between the amplifier and the speaker.

Place a low equivalent-series-resistance (ESR) ceramic capacitor (X7R or X5R), typically 1μF, as close as possible to the AVDD lead. This choice of capacitor and placement help reject high frequency transients, spikes, or digital hash on the line. Furthermore, placing the decoupling capacitors close to the ft2830 is important for power efficiency, as any parasitic resistance or inductance between the amplifier and the capacitor causes efficiency loss. For best power supply coupling, place an additional 10μF or greater low ESR capacitor close to the CVDD lead. This larger capacitor serves as a charge reservoir for the flying capacitors C_{F1} or C_{F2} of the charge pump regulator each time one of the flying capacitors is charged, thus reducing the amount of voltage ripple seen at CVDD. This will help reduce the amount of EMI passed back along the power trace to other circuitry on the system board.

Input Resistors (R_{IN})

To minimize the number of external components required for the application of ft2830, a set of 24kΩ input resistors are integrated internally at INP and INN pins respectively. The internal input resistors also bring other benefits such as fewer variations on PSRR and minimum turn-on pop noise since on-chip resistors tends to match well. Thus, for typical portable device applications, there is no need for additional input resistors connected to INP or INN pin. However, for applications where additional gain adjustment becomes necessary, a set of external input resistors can be added onto INP and INN pins respectively, as shown in Figure 45. The value of the external input resistors must be included for the calculation of the overall voltage gain (as described in Equation 5) as well as the selection of proper input capacitors (as described in Equation 6). As shown in Equation 5, the external input resistors will attenuate the original overall voltage gain by the ratio of RINTERNAL / (RIN+RINTERNAL).

$$A_V = A_{V0} \times [R_{INTERNAL} / (R_{IN}+R_{INTERNAL})] \quad (5)$$

where A_{V0} = 24 (27.6dB) for Mode 1
A_{V0} = 16 (24dB) for Mode 2 and 3
$R_{INTERNAL}$ = 24kΩ

Input Capacitors (C_{IN})

DC decoupling capacitors for audio inputs are recommended. The audio input DC decoupling capacitors will remove the DC bias from an incoming analog signal. The input capacitors (C_{IN}) and input resistors (R_{IN} plus $R_{INTERNAL}$) form a highpass filter with the corner frequency, fc, as shown in Equation 6.

$$f_C = 1 / [2 \times \pi \times (R_{IN}+R_{INTERNAL}) \times C_{IN}] \quad (6)$$

where $R_{INTERNAL} = 24k\Omega$

Choose C_{IN} such that the f_C is well below the lowest frequency of interest. Setting f_C too high affects the low frequency responses of the amplifier. Consider an example where the specification calls for A_V=25dB and a flat frequency response down to 20Hz. In this example, R_{IN}=10kΩ and C_{IN} is calculated to be 0.23μF; thus 0.22μF or 0.33 μF as a common choice of capacitance, can be chosen for C_{IN}.

Note that any mismatch in resistance or capacitance between two audio inputs will cause a mismatch in the corner frequencies. Severe mismatch may also cause turn-on pop noise, PSRR, CMRR performance. Choose input resistors and capacitors with a tolerance of ±2% or better.

Furthermore, the type of the input capacitor is crucial to audio quality. For best audio quality, use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies.

PRINTED CIRCUIT BOARD (PCB) LAYOUT CONSIDERATIONS

Ground Plane - It is required to use a solid metal plane with sufficiently wide area as a central ground connection (GND) for ft2830. All ground pins (AGND, CGND, and PGND) should be directly connected to the ground plane.

Supply Decoupling capacitors – The supply decoupling capacitors (C_{AVDD} and C_{PVDD}) should be placed as individually close as possible to AVDD and PVDD pins. Also, in tandem with C_{PVDD}, consider adding a small, good quality, low-ESR ceramic capacitor of 0.1μF to PVDD pins for high-frequency supply coupling.

Charge Pump Input Capacitor - Place a 10μF ceramic capacitor C_{CVDD} as close to the CVDD pin as possible.

Charge Pump Flying Capacitors – Place a 2.2μF ceramic capacitor (C_{F1}) as close to CP1 and CN1 pins as possible and another 2.2μF ceramic capacitor (C_{F2}) as close to CP2 and CN2 pins as possible.

Charge Pump Output Capacitors – Place a 10μF ceramic capacitor C_{PVOUT} as close to the PVOUT pin as possible. In tandem, add a bulk tantalum or electrolytic capacitor (220μF or greater) to facilitate higher voltage margin for higher power (greater than 2W) applications. Also, it is required to short PVDD pins to the PVOUT pin by a wide and short metal trace on the system board.

Ferrite Bead EMI Filter – The ferrite bead EMI filters should be placed tightly together and individually close to the audio output pins, VOP and VON respectively, for best EMI performance. Keep the current loop, traversing from each of the audio outputs through the ferrite bead the small filter capacitors and back to PGND, as short as possible.

Power Dissipation - The maximum output power of ft2830 can be severely limited by its thermal dissipation capability. To ensure the device operating properly and reliably at its maximum output power without incurring over-temperature shutdown, the following guidelines are given for optimum thermal dissipation capability:

- Fill both top and bottom layers of the system board with solid GND metal traces.
- Solder the thermal pad directly onto a grounded metal plane.
- Place lots of equally-spaced vias underneath the thermal pad connecting the top and bottom layers of GND. The vias are connected to a solid metal plane on the bottom layer of the board.
- Reserve wide and uninterrupted areas along the thermal flow on the top layer, i.e., no wires cutting through the GND layer and obstructing the thermal flow.
- Place the Input/output capacitors of the charge pump regulator tightly together and on the same layer of the board with ft2830.
- Avoid using vias for traces carrying high current.

TYPICAL APPLICATION CIRCUITS

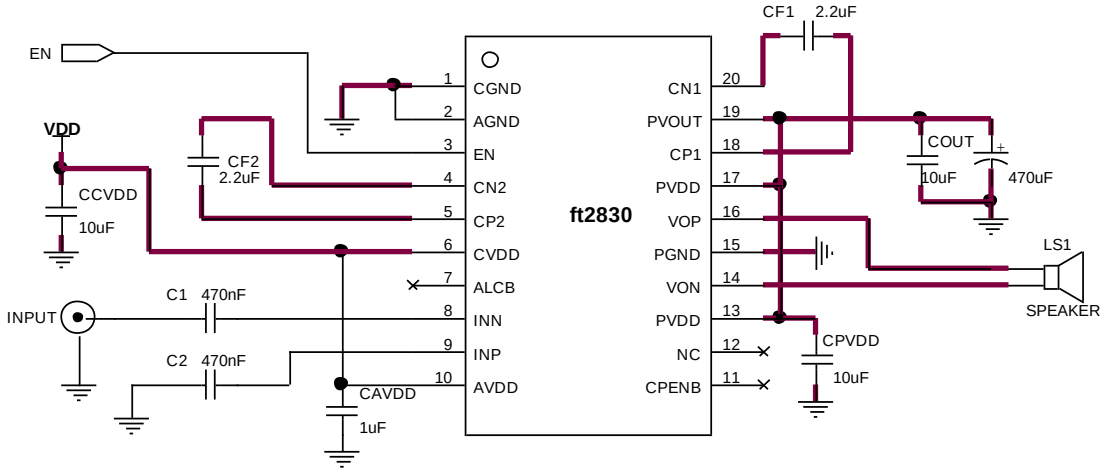


Figure 42: Single-Ended Audio Input in ALC Mode

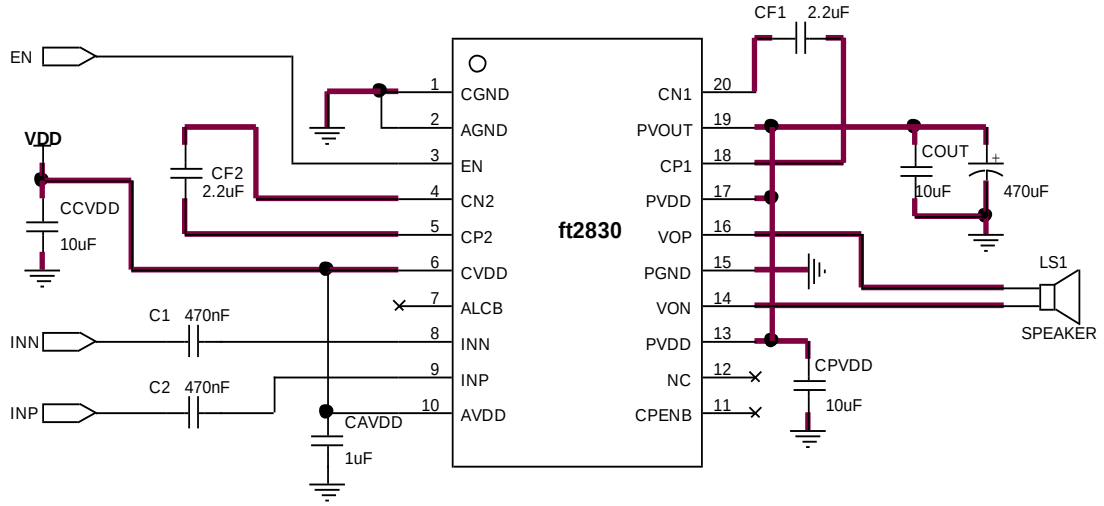


Figure 43: Differential Audio Inputs in ALC Mode

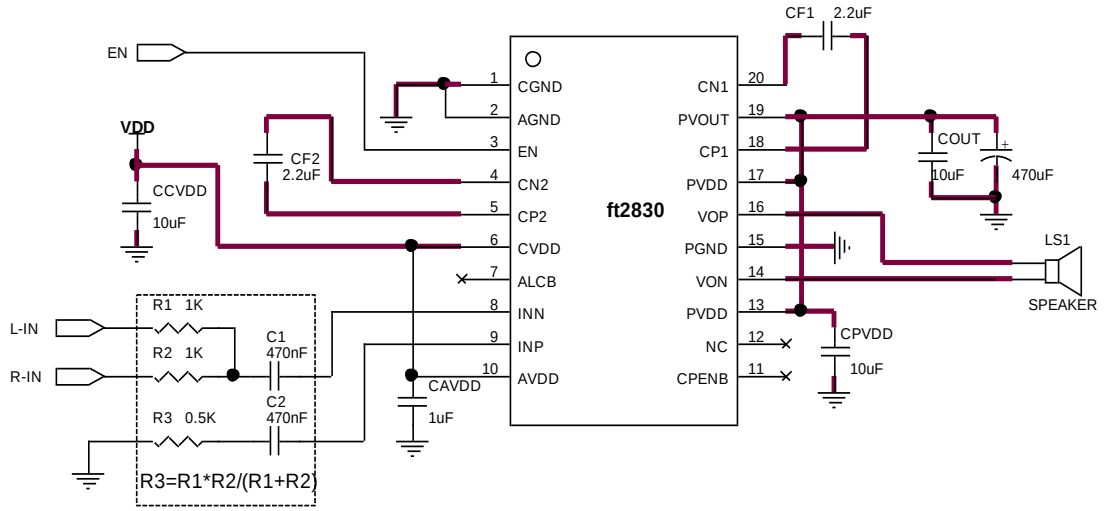


Figure 44: Dual Channel Audio Inputs in ALC Mode

Note: The bold lines indicate high current paths and their respective traces are required to be as wide and short as possible on the system board for high power applications.

TYPICAL APPLICATION CIRCUITS (Cont'd)

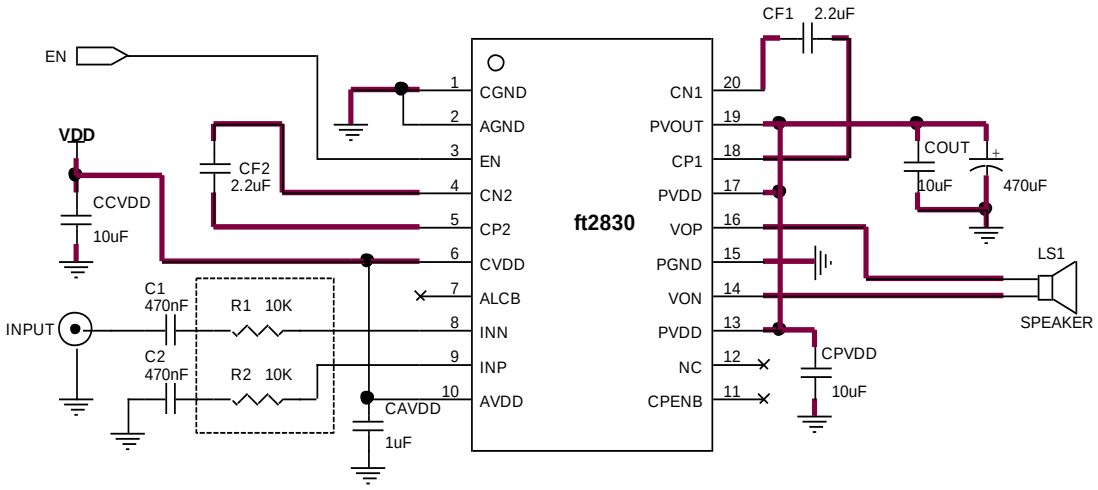


Figure 45: Voltage Gain Adjustment by External Input Resistors

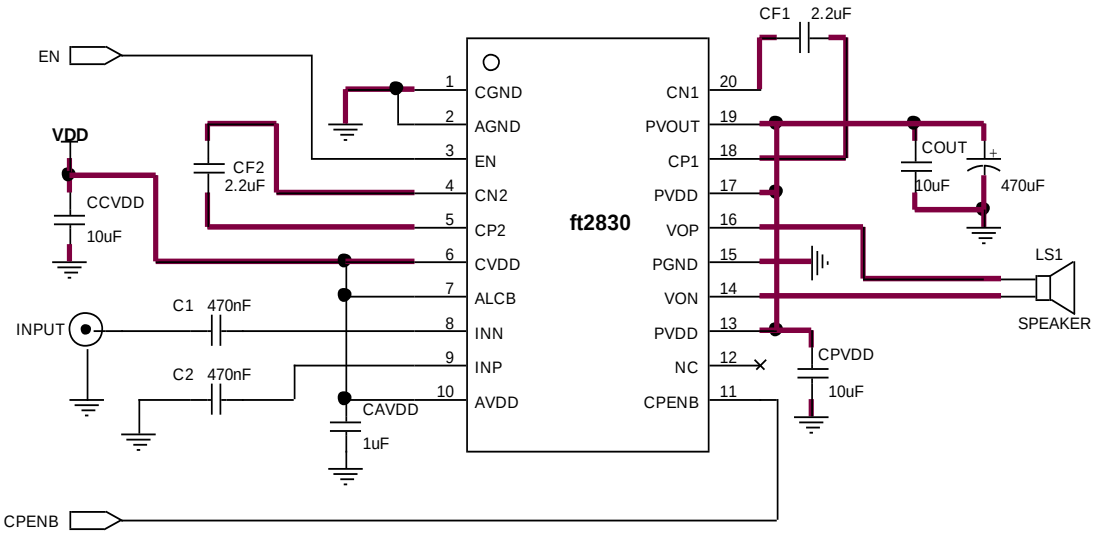
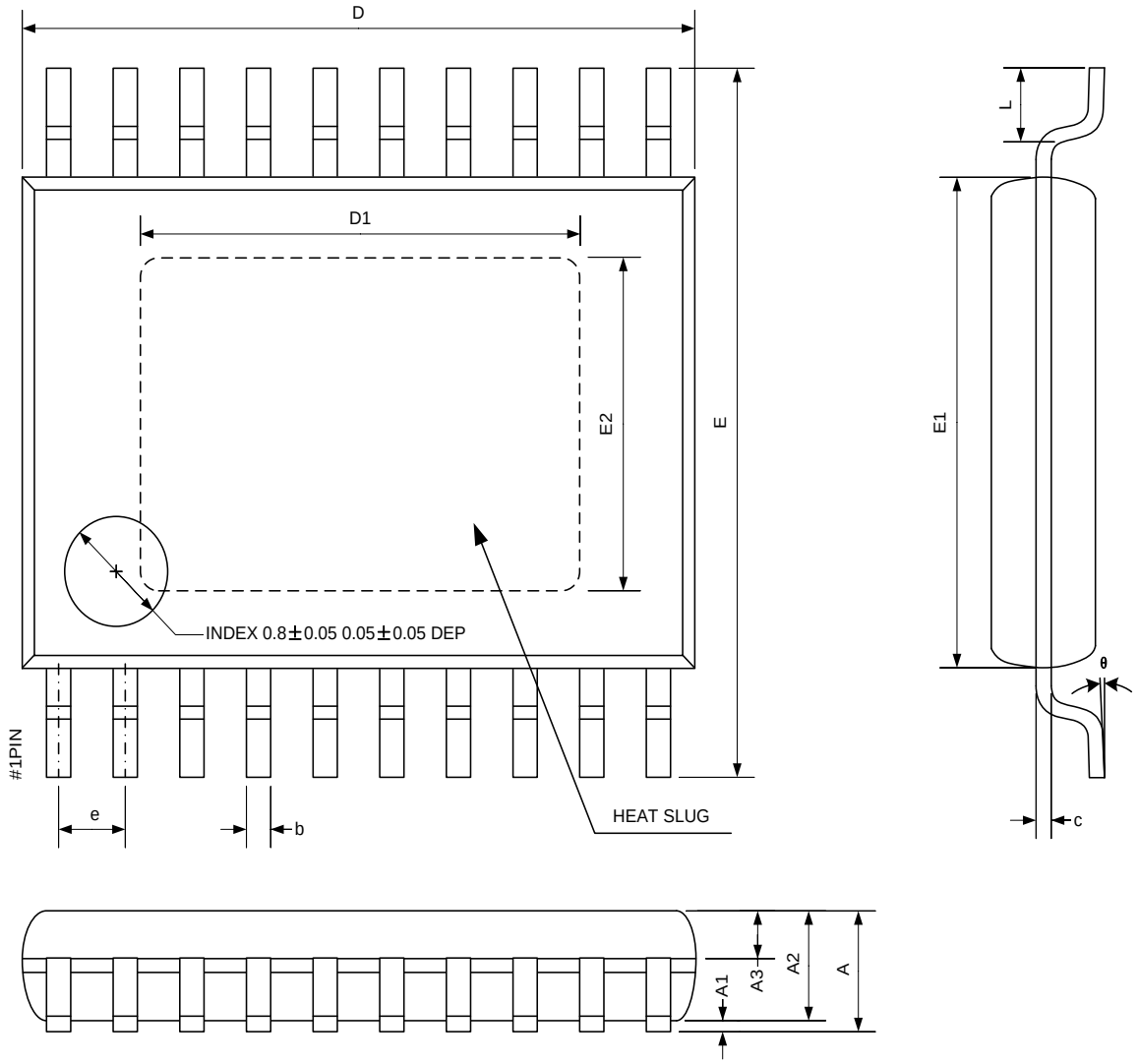


Figure 46: Single-Ended Audio Input in Non-ALC Mode with Charge Pump Control

Note: The bold lines indicate high current paths and their respective traces are required to be as wide and short as possible on the system board for high power applications.

PHYSICAL DIMENSIONS

TSSOP-20L PACKAGE OUTLINE DIMENSIONS



SYMBOL	MIN	NOM	MAX	UNIT
A	-	-	1.20	mm
A1	0.05	-	0.15	mm
A2	0.90	1.00	1.05	mm
A3	0.34	0.44	0.54	mm
b	0.20	-	0.28	mm
c	0.10	-	0.19	mm
D	6.40	6.50	6.60	mm
D1	4.00	4.20	4.40	mm
E	6.20	6.40	6.60	mm
E1	4.30	4.40	4.50	mm
E2	2.80	3.00	3.20	mm
e	0.65BSC			mm
L	0.45	0.60	0.75	mm
θ	0	-	8	°

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