eKT5211

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.2

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial release version	2013/01/14
1.1	Modified some code option information.	2014/07/16
1.2	1. Added User Application Note 2. Modified the Package Type in the Features section 3. Modified Appendix A “Ordering and Manufacturing Information”	2016/03/31

User Application Note

(Before using this chip, take a look at the following description note, it includes important messages.)

We strongly recommend that you have to place external pull-down or pull-high resistor on P77 no matter what the pin function is. The purpose of this is to prevent P77 from floating.

1 General Description

The eKT5211 is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. The device has as an on-chip 4K×15-bit Electrical One Time Programmable Read Only Memory (OTP-ROM) and is equipped with 1-line type touch sensors. The capacitive touchpad sensor uses plastic or glass substrate as cover.

The system controller converts fingertips position on the touchpad into data in accordance with finger positions and human interface context. The ELAN JTAG5200 Simulator is used to develop the user program for this microcontroller and several other ELAN OTP type ICs.

2 Features

■ CPU Configuration:

- 4K×15 bits on-chip ROM
- 304×8 bits on-chip registers (SRAM)
- 8-level stacks for subroutine nesting
- Typical 1.5 µA during Sleep mode
- Three programmable Level Voltage Reset LVR**:** 4.0V, 3.5V, and 2.7V
- Four CPU operating modes**:** Normal, Green, Idle and Sleep

■ I/O Port Configuration:

- Four bi-directional I/O ports
- 13 I/O pins
- Four programmable pin change wake-up ports**:** P5, P6, P7, and P8
- Three programmable pull-down/pull-high/ open-drain I/O ports**:** P5, P6, and P7
- One programmable pull-down I/O port**:** P8
- Four programmable high-sink/drive I/O ports**:** P5, P6, P7, and P8

■ Operating Voltage Range:

- 2.5V~5.5V at -40°C~85°C (Industrial)
- 2.5V~5.5V at 0°C~70°C (Commercial)

■ Operating Frequency Range (base on two clocks):

- Main Oscillator - IRC mode**:**

  8 MHz @ DC 3.0V

  4 MHz @ DC 2.5V

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.5~5.5V)	Process	Total
4 MHz	± 2%	± 1%	± 1%	± 4%
8 MHz	± 2%	± 1%	± 1%	± 4%

- Sub Oscillator

  IRC mode**:** 16K/64kHz @ DC 2.5V

■ Peripheral Configuration:

- 8-bit real time clock (TCC) with selective signal sources (Fm/Fs)
- One 16-bit timer (TMR1) with PWM function
- Power down (Sleep) mode

■ Six Available Interrupts:

- TCC overflow interrupt
- Input-port status changed interrupt
- External interrupt
- One Timer (with PWM function) interrupt

■ Single Instruction Cycle Commands

■ Package Type:

- 16 QFN 3×3×0.8mm : eKT5211QN16
- 16 DIP 300mil : eKT5211D16
- 16 SOP 150mil : eKT5211SO16A

NOTE

These are all Green products which do not contain hazardous substances.

3 Pin Assignment

3.1 Package QFN-16

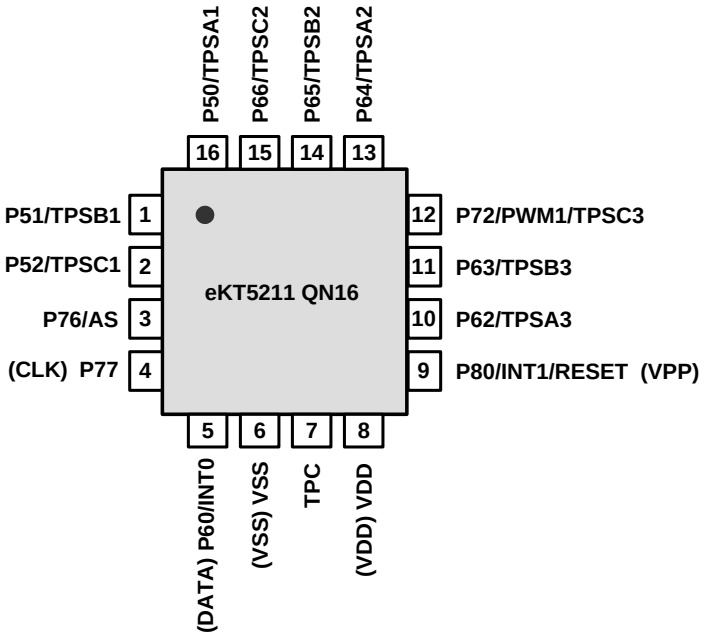


Figure 3-1 eKT5211 QFN-16 Pin Assignment

3.2 Package DIP-16

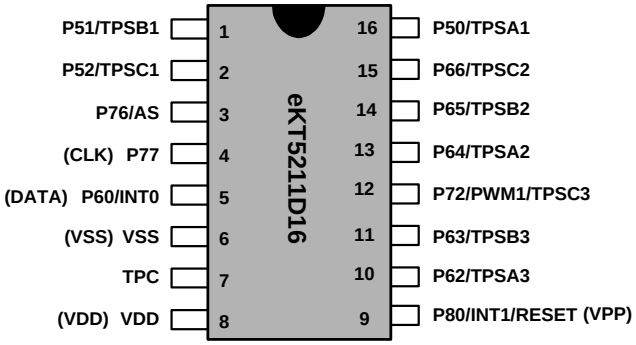


Figure 3-2 eKT5211 DIP-16 Pin Assignment

3.3 Package SOP-16

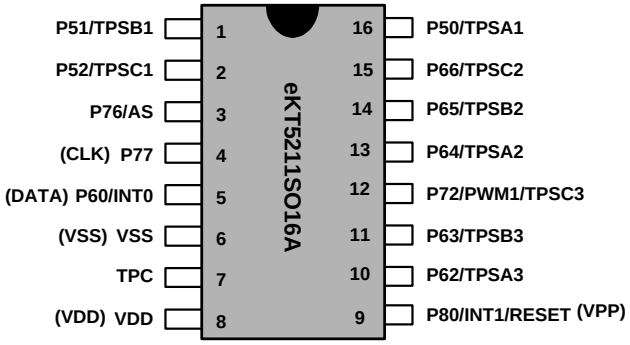


Figure 3-3 eKT5211 SOP-16 Pin Assignment

4 Pin Description

4.1 eKT5211 Kernel Pin

Name	Function	Input Type	Output Type	Description
P50 / TPSA1	P50	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software. They can also be set to open-drain and enable high sink/drive modes by software.
	TPSA1	AN	AN	Touchpad 1-line type sensor pins
P51 / TPSB1	P51	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open drain and enable high sink/drive modes by software.
	TPSB1	AN	AN	Touchpad 1-line type sensor pin
P52 / TPSC1	P52	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open drain and enable high sink/drive modes by software.
	TPSC1	AN	AN	Touchpad 1-line type sensor pin

(Continuation)

Name	Function	Input Type	Output Type	Description
P60 / INT0 / (DATA)	P60	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open drain and enable high sink/drive modes by software.
	INT0	ST	-	External interrupt pin triggered by falling or rising edge (set by EIESCR).
	(DATA)	ST	CMOS	DATA pin for Writer programming
P62 / TPSA3	P62	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open drain and enable high sink/drive modes by software.
	TPSA3	AN	AN	Touchpad 1-line type sensor pin
P63 / TPSB3	P63	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open drain and enable high sink/drive modes by software.
	TPSB3	AN	AN	Touchpad 1-line type sensor pin
P64 / TPSA2	P64	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open drain and enable high sink/drive modes by software.
	TPSA2	AN	AN	Touchpad 1-line type sensor pin
P65 / TPSB2	P65	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open drain and enable high sink/drive modes by software.
	TPSB2	AN	AN	Touchpad 1-line type sensor pin

(Continuation)

Name	Function	Input Type	Output Type	Description
P66 / TPSC2	P66	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open drain and enable high sink/drive modes by software.
	TPSC2	AN	AN	Touchpad 1-line type sensor pin
P72 / PWM1 / TPSC3	P72	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open drain and enable high sink/drive modes by software.
	PWM1	-	CMOS	Pulse Width Modulation 1 output
	TPSC3	AN	AN	Touchpad 1-line type sensor pin
P76 / AS	P76	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open drain and enable high sink/drive modes by software.
	AS	-	AN CMOS	Active shielding pin

(Continuation)

Name	Function	Input Type	Output Type	Description
P77 / (CLK)	P77	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down and pulled-high internally by software control. They can also be set to open drain and enable high sink/drive modes by software.
	(CLK)	ST	CMOS	CLOCK pin for Writer programming
P80 / RESET / INT1 / (VPP)	P80	ST	CMOS	Bidirectional I/O ports. All pins can be pulled-down internally by software control. They can also be set as enable high sink/drive mode by software.
	RESET	ST	-	Schmitt trigger input pin. If this pin remains at logic low, the controller is reset.
	INT1	ST	-	External interrupt pin triggered by falling or rising edge (set by EIESCR).
	(VPP)	AN	-	High voltage input pin for Writer programming
VDD	VDD	Power	-	Power supply pin
VSS	VSS	Power	-	Ground
TPC	TPC	AN	-	Touchpad capacitor*

**TPC external capacitor is 1 µf, stable time is 300 µs*

4.2 Compound Pin Functions Priority

- Priority of Pin P50/TPSA1:

Pin Priority	
1st	2nd
TPSA1	P50

- Priority of Pin P51/TPSB1:

Pin Priority	
1st	2nd
TPSB1	P51

- Priority of Pin P52/TPSC1:

Pin Priority	
1st	2nd
TPSC1	P52

- Priority of Pin P60/INT0:

Pin Priority	
1st	2nd
INT0	P60

- Priority of Pin P62/TPSA3:

Pin Priority	
1st	2nd
TPSA3	P62

- Priority of Pin P63/TPSB3:

Pin Priority	
1st	2nd
TPSB3	P63

- Priority of Pin P64/TPSA2:

Pin Priority	
1st	2nd
TPSA2	P64

- Priority of Pin P65/TPSB2:

Pin Priority	
1st	2nd
TPSB2	P65

- Priority of Pin P66/TPSC2:

Pin Priority	
1st	2nd
TPSC2	P66

- Priority of Pin P72/PWM1/TPSC3:

Pin Priority		
1st	2nd	3rd
TPSC3	PWM1	P72

- Priority of Pin P76/AS:

Pin Priority	
1st	2nd
AS	P76

- Priority of Pin P80/INT1/RESET:

Pin Priority		
1st	2nd	3rd
RESET	INT1	P80

5 Functional Block Diagram

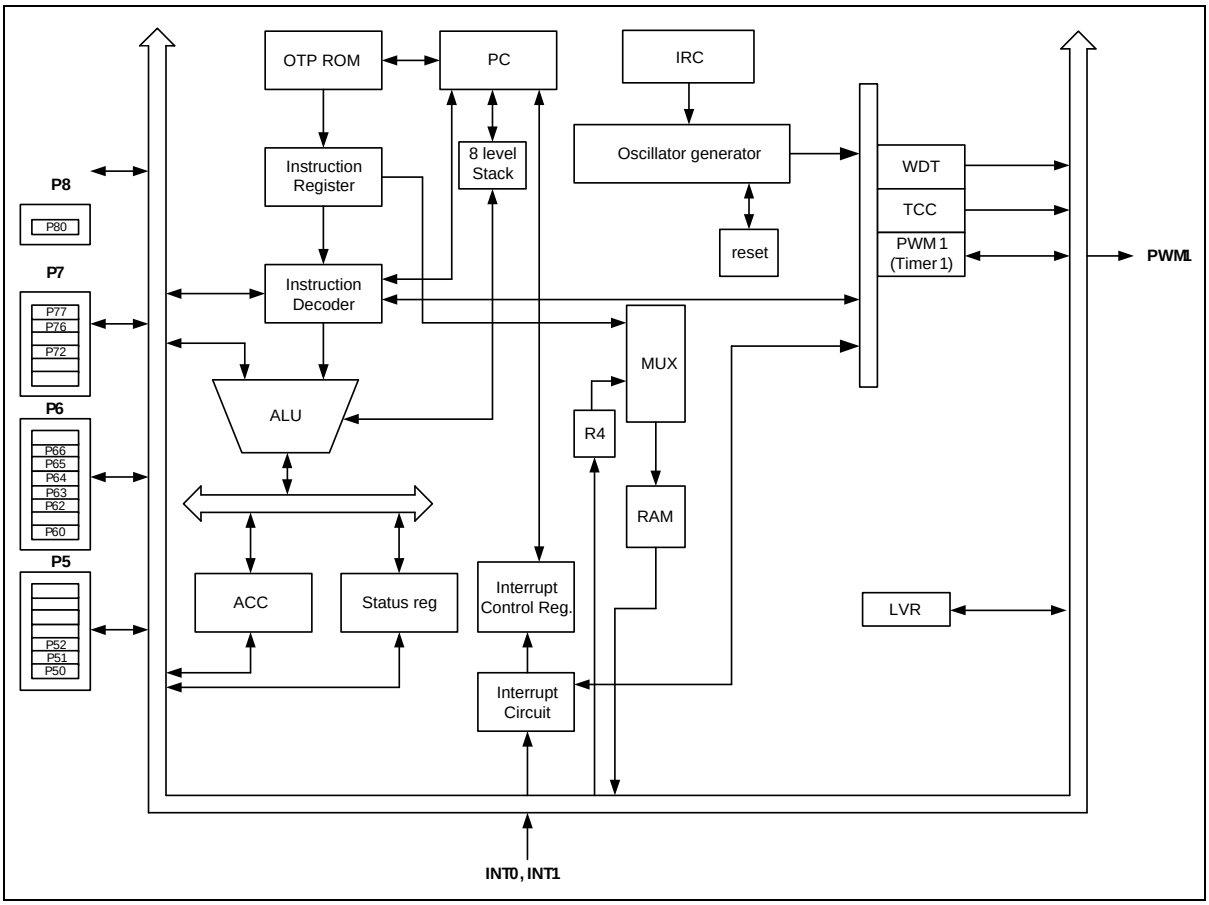


Figure 5-1 eKT5211 Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0: IAR (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1: BSCR (Bank Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	SBS1	SBS0	-	-	-	GBS0
-	-	R/W	R/W	-	-	-	R/W

Bits 7~6: Not used. Set to "**0**" all the time.

Bits 5~4 (SBS1~SBS0): Special register bank select bit. It is used to select Banks 0-/1-/2- of Special Registers **R5~R4F**.

SBS1	SBS0	Special Register Bank
0	**0**	0
0	**1**	1
1	**0**	2
1	**1**	X

Bits 3~1: Not used. Set to "**0**" all the time.

Bit 0 (GBS0): General register bank select bit. It is used to select Banks 0/1 of General Registers **R80~RFF**.

GBS0	RAM Bank
0	0
1	1

6.1.3 R2: PCL (Program Counter Low)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PC7~PC0): The low byte of program counter.

- Depending on the device type, R2 and hardware stack are 15-bits wide. The structure is depicted in Figure 6-1.
- Generating 4K×15 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 4096 words long.
- R2 is set as all "**0**'s" when under RESET condition.
- "JMP" instruction allows direct loading of the lower 12 program counter bits. Thus, "JMP" allows PC to go to any location within a page.
- "CALL" instruction loads the lower 12 bits of the PC, and the present PC value will add **1** and is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "LJMP" instruction allows direct loading of the lower 13 program counter bits. Therefore, "LJMP" allows PC to jump to any location within 8K (2^{13}).
- "LCALL" instruction loads the lower 13 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within 8K (2^{13}).
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and above bits of the PC won't be changed.
- Any instruction, except "ADD R2,A" that is written to R2 (e.g., "MOV R2, A", "BC R2, 6","INC R2", etc.) will cause the ninth bit and the above bits (A8~A12) of the PC to remain unchanged.
- All instructions are single instruction cycle (Fsys/2) except for "LCALL", "CALL", "LJMP", and "JMP" instructions. The "LCALL" and "LJMP" instructions need two instructions cycle.

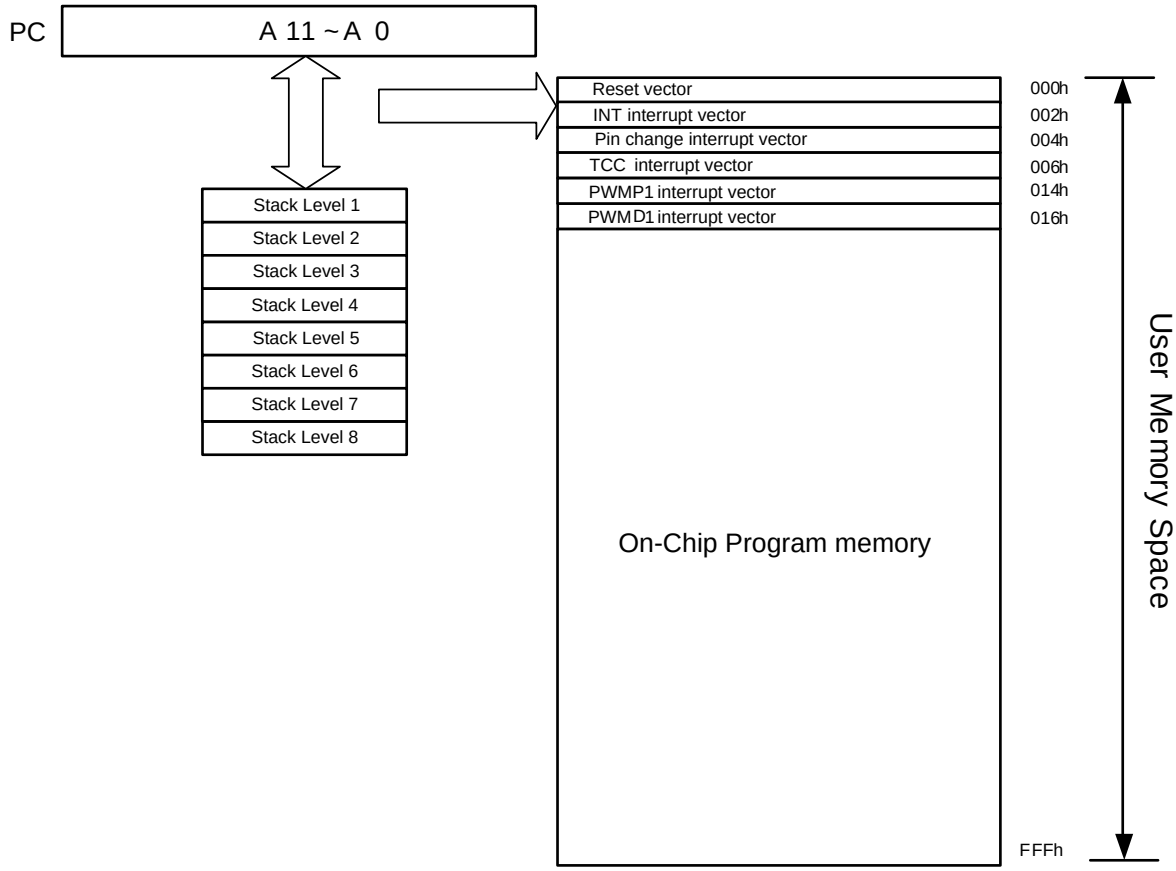


Figure 6-1 eKT5211 Program Counter Organization

■ Data Memory Configuration

Address	Bank 0	Bank 1	Bank 2
0X00	IAR (Indirect Addressing Register)		
0X01	BSR (Bank Select Control Register)		
0X02	PCL (Program Counter Low)		
0X03	SR (Status Register)		
0X04	RSR (RAM Selection Register)		
0X05	Port 5	IOCR8	Unused
0X06	Port 6	Unused	Unused
0X07	Port 7	Unused	Unused
0X08	Port 8	P5PHCR	Unused
0X09	Unused	P6PHCR	Unused
0X0A	Unused	P7PHCR	Unused
0x0B	IOCR5	P5PLCR	Unused
0X0C	IOCR6	P6PLCR	Unused
0X0D	IOCR7	P78PLCR	Unused

(Continuation)

Address	Bank 0	Bank 1	Bank 2
0X0E	OMCR (Operating Mode Control Register)	P5HDSCR	Unused
0X0F	EIESCR (External Interrupt Edge Select Control Register)	P6HDSCR	Unused
0X10	WUCR1	P78HDSCR	Unused
0X11	Unused	P5ODCR	Unused
0X12	WUCR3	P6ODCR	Unused
0X13	Unused	P7ODCR	Unused
0X14	SFR1 (Status Flag Register 1)	Unused	Unused
0X15	Unused	Unused	Unused
0X16	SFR3 (Status Flag Register 3)	PWMSCR	Unused
0X17	SFR4 (Status Flag Register 4)	PWM1CR	Unused
0X18	Unused	PRD1L	Unused
0X19	Unused	PRD1H	Unused
0X1A	Unused	DT1L	Unused
0X1B	IMR1 (Interrupt Mask Register 1)	DT1H	Unused
0X1C	Unused	TMR1L	Unused
0X1D	IMR3 (Interrupt Mask Register 3)	TMR1H	Unused
0X1E	IMR4 (Interrupt Mask Register 4)	Unused	Unused
0X1F	Unused	Unused	Unused
0X20	Unused	Unused	Unused
0X21	WDTCR	Unused	Unused
0X22	TCCCR	Unused	Unused
0X23	TCCD	Unused	Unused
0X24	Unused	Unused	Unused
0X25	Unused	Unused	Unused
0X26	Unused	Unused	Unused
0X27	Unused	Unused	Unused
0X28	Unused	Unused	Unused
0X29	Unused	Unused	Unused
0X2A	Unused	Unused	Unused
0x2B	Unused	Unused	Unused
0X2C	Unused	Unused	Unused
0X2D	Unused	Unused	Unused
0X2E	Unused	Unused	Unused
0X2F	Unused	Unused	Unused

(Continuation)

Address	Bank 0	Bank 1	Bank 2
0X30	Unused	Unused	Unused
0X31	Unused	Unused	Unused
0X32	Unused	Unused	Unused
0X33	Unused	Unused	Unused
0X34	Unused	Unused	Unused
0X35	Unused	Unused	Unused
0X36	Unused	Unused	Unused
0X37	Unused	Unused	Unused
0X38	Unused	Unused	Unused
0X39	Unused	Unused	Unused
0X3A	Unused	Unused	Unused
0x3B	Unused	Unused	Unused
0X3C	Unused	Unused	Unused
0X3D	Unused	Unused	Unused
0X3E	Unused	Unused	Unused
0X3F	Unused	Unused	Unused
0X40	Unused	Unused	Unused
0X41	Unused	Unused	Unused
0X42	Unused	Unused	Unused
0X43	Unused	Unused	Unused
0X44	Unused	Unused	Unused
0X45	Unused	TBPTL	Unused
0X46	Unused	TBPTH	Unused
0X47	Unused	STKMON	Unused
0X48	Unused	PCH	Unused
0X49	Unused	Unused	Unused
0X4A	Unused	COBS1	Unused
0x4B	Unused	Unused	Unused
0X4C	Unused	COBS3	Unused
0X4D	Unused	Unused	Unused
0X4E	Unused	Unused	Unused

(Continuation)

Address	Bank 0	Bank 1	Bank 2
0X4F	Unused	Unused	Unused
0X50	General Purpose Register		
0X51			
:			
:			
0X7F			
0X80	Bank 0	Bank 1	
0X81			
:			
:			
0XFE			
0XFF			

6.1.4 R3: SR (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT	-	-	T	P	Z	DC	C
F	-	-	R/W	R/W	R/W	R/W	R/W

Bit 7 (INT): Interrupt Enable flag

0: Interrupt masked by DISI or hardware interrupt

1: Interrupt enabled by ENI/RETI instructions

NOTE
The INT bit cannot be saved by hardware when interrupt occurs.

Bits 6~5: Not used. Set to "**0**" all the time.

Bit 4 (T): Time-out bit

Set to "**1**" with "SLEP" and "WDTC" commands, or during power up.

Reset to "**0**" by WDT time-out.

Bit 3 (P): Power down bit.

Set to "**1**" during power on or by a "WDTC" command.

Reset to "**0**" by a "SLEP" command.

Bit 2 (Z): Zero flag.

Set to "**1**" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4: RSR (RAM Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (RSR7~RSR0): These bits are used to select registers (Address 00 ~ FF) in indirect addressing mode. For more details, refer to the table on Data Memory Configuration in Section 6.1.3, *R2: PCL (Program Counter Low)*.

6.1.6 Bank 0 R5 ~ R8: (Port 5 ~ Port 8)

R5, R6, R7, and R8 are I/O data registers.

6.1.7 Bank 0 R9 ~ RA: (Reserved)

6.1.8 Bank 0 RB~RD: (IOCR5 ~ IOCR7)

These registers are used to control the I/O port direction. They are both readable and writable.

0: Set the relative I/O pin as output

1: Set the relative I/O pin into high impedance

6.1.9 Bank 0 RE: OMCR (Operating Mode Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPUS	IDLE	-	-	-	-	-	-
R/W	R/W	-	-	-	-	-	-

Bit 7 (CPUS): CPU Oscillator Source Select

0: Fs**:** sub-oscillator

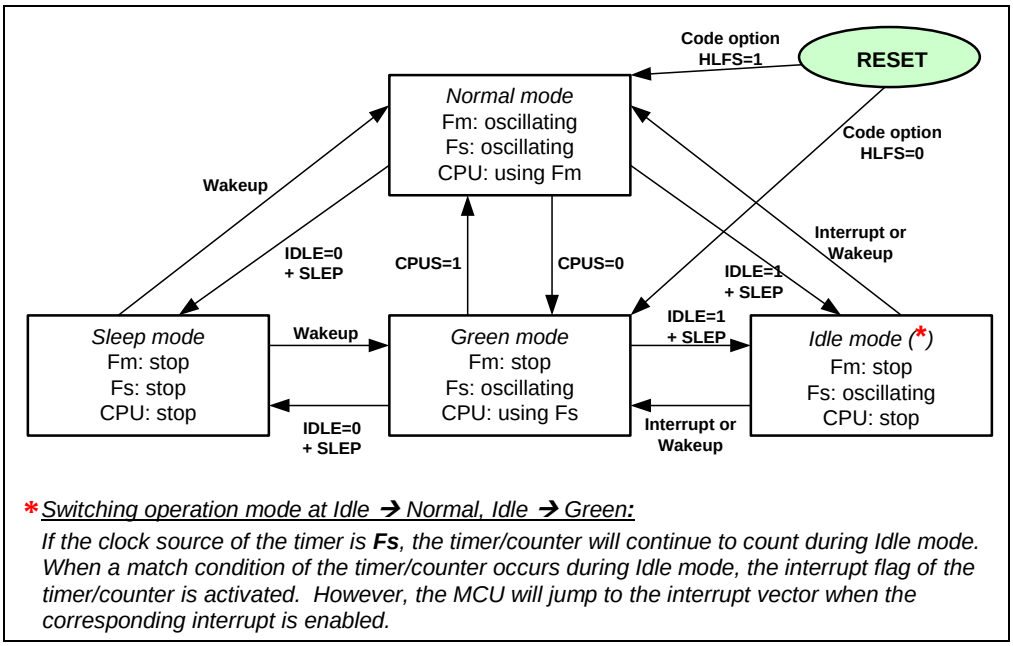
1: Fm**:** main-oscillator (default)

When CPUS = **0**, the CPU oscillator selects the sub-oscillator while the main oscillator is stopped.

Bit 6 (IDLE): Idle Mode Enable Bit. This bit decides which mode (see figure below) to use with the SLEP instruction.

0: "IDLE = **0**" + SLEP instruction → Sleep mode

1: "IDLE = **1**" + SLEP instruction → Idle mode (default)



Switching operation mode at Idle → Normal, Idle → Green:

*If the clock source of the timer is **Fs**, the timer/counter will continue to count during Idle mode. When a match condition of the timer/counter occurs during Idle mode, the interrupt flag of the timer/counter is activated. However, the MCU will jump to the interrupt vector when the corresponding interrupt is enabled.*

Figure 6-2 CPU Operation Mode

■ **Oscillation Characteristics**

CPU Mode Switch	Waiting Time before CPU Resumes Working
Sleep → Normal	WSTO + 8 clocks (main frequency)
Idle → Normal	WSTO + 8 clocks (main frequency)
Green → Normal	WSTO + 8 clocks (main frequency)
Sleep → Green	WSTO + 8 clocks (sub frequency)
Idle → Green	WSTO + 8 clocks (sub frequency)

***WSTO:** Waiting time for Start-to-Oscillation*

Bits 5~0: Not used. Set to "**0**" all the time.

6.1.10 Bank 0 RF: EIESCR (External Interrupt Edge Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	EI1ES	EI0ES	-	-
-	-	-	-	R/W	R/W	-	-

Bits 7~4: Not used. Set to "**0**" all the time.

Bit 3 (EI1ES): External Interrupt 1 edge select bit

0: Falling edge interrupt

1: Rising edge interrupt

Bit 2 (EI0ES): External Interrupt 0 edge select bit

0: Falling edge interrupt

1: Rising edge interrupt

Bits 1~0: Not used. Set to "**0**" all the time.

6.1.11 Bank 0 R10: WUCR1 (Wake-up Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	INTWK1	INTWK0	-	-
-	-	-	-	R/W	R/W	-	-

Bits 7~4: Not used. Set to "**0**" all the time.

Bit 3 (INTWK1): External Interrupt 1(INT1 pin) Wake-up Function Enable Bit

0: Disable External Interrupt 1 wake-up

1: Enable External Interrupt 1 wake-up

When the External Interrupt 1 status change is used to enter interrupt vector or to wake-up IC from Sleep/Idle mode, the INTWK1 bit must be set to “Enable“.

Bit 2 (INTWK0): External Interrupt 0 (INT0 pin) Wake-up Function Enable Bit

0: Disable External Interrupt 0 wake-up

1: Enable External Interrupt 0 wake-up

When the External Interrupt 0 status change is used to enter interrupt vector or to wake-up IC from Sleep/Idle mode, the INTWK0 bit must be set to “Enable“.

Bits 1~0: Not used. Set to "**0**" all the time.

6.1.12 Bank 0 R12: WUCR3 (Wake-up Control Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ICWKP8	ICWKP7	ICWKP6	ICWKP5	-	-	-	-
R/W	R/W	R/W	R/W	-	-	-	-

Bits 7~4 (ICWKP8~ICWKP5): Pin change Wake-up enable for Ports 8/7/6/5.

0: Disable wake-up function

1: Enable wake-up function

Bits 3~0: Not used. Set to "**0**" all the time.

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
Pin Change INT	ICWKPx = 0, PxICIE = 0	Wake-up is invalid				Interrupt is invalid			
	ICWKPx = 0, PxICIE = 1	Wake-up is invalid				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ICWKPx = 1, PxICIE = 0	Wake-up + Next Instruction				Interrupt is invalid			
	ICWKPx = 1, PxICIE = 1	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

NOTE

When the MCU wakes up from Sleep or Idle mode, the ICSF must be equal to 1. If ICSF equals 0, it means the pin status does not change or the pin change ICIE is disabled. Hence the MCU cannot wake-up.

6.1.13 Bank 0 R13: (Reserved)

6.1.14 Bank 0 R14: SFR1 (Status Flag Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	EX1SF	EX0SF	-	TCSF
-	-	-	-	F	F	-	F

Each corresponding status flag is set to "**1**" when interrupt condition is triggered.

Bits 7~4, 1: Not used. Set to "**0**" all the time.

Bit 3 (EX1SF): External Interrupt 1 status flag

Bit 2 (EX0SF): External Interrupt 0 status flag

Bit 0 (TCSF): TCC overflow status flag. Set when TCC overflows. Reset by software.

NOTE

If a function is enabled, the corresponding status flag would be active regardless of whether the interrupt mask is enabled or not.

6.1.15 Bank 0 R15: (Reserved)

6.1.16 Bank 0 R16: SFR3 (Status Flag Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	PWM1PSF	PWM1DSF
-	-	-	-	-	-	F	F

Bits 7~2: Not used. Set to "**0**" all the time.

Bit 1 (PWM1PSF): Status flag of period-matching for PWM1 (Pulse Width Modulation). Set when a selected period is reached. Reset by software.

Bit 0 (PWM1DSF): Status flag of duty-matching for PWM1 (Pulse Width Modulation). Set when a selected duty is reached. Reset by software.

NOTE

If a function is enabled, the corresponding status flag would be active whether the interrupt mask is enabled or not.

6.1.17 Bank 0 R17: SFR4 (Status Flag Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P8ICSF	P7ICSF	P6ICSF	P5ICSF	-	-	-	-
F	F	F	F	-	-	-	-

Bits 7~4 (P8ICSF~P5ICSF): Ports 5~8 input status change status flag. Set when Ports 5~8 input changes. Reset by software.

Bits 3~0: Not used. Set to "**0**" all the time.

NOTE

If a function is enabled, the corresponding status flag will be active regardless of whether the interrupt mask is enabled or not.

6.1.18 Bank 0 R18~R1A: (Reserved)

6.1.19 Bank 0 R1B: IMR1 (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	EX1IE	EX0IE	-	TCIE
-	-	-	-	R/W	R/W	-	R/W

Bits 7~4, 1: Not used. Set to "**0**" all the time.

Bit 3 (EX1IE): EX1SF interrupt enable and **INT1** function enable bit

0: P80/INT1/RESET is P80 pin. EX1SF is always equal **0**.

1: Enable EX1SF Interrupt and P80/INT1/RESET is INT1 pin

Bit 2 (EX0IE): EX0SF interrupt enable and **INT0** function enable bit

0: P60/INT0 is P60 pin. EX0SF is always equal **0**.

1: Enable EX0SF Interrupt and P60/INT0 is INT0 pin

Bit 0 (TCIE): TCSF interrupt enable bit.

0: Disable TCSF interrupt

1: Enable TCSF interrupt

NOTE

If the interrupt mask and instruction "ENI" are enabled, the program counter will jump to the corresponding interrupt vector when the corresponding status flag is set.

6.1.20 Bank 0 R1C: (Reserved)

6.1.21 Bank 0 R1D: IMR3 (Interrupt Mask Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	PWM1PIE	PWM1DIE
-	-	-	-	-	-	R/W	R/W

Bits 7~2: Not used. Set to "**0**" all the time.

Bit 1 (PWM1PIE): PWM1PSF interrupt enable bit

0: Disable period-matching of PWM1 interrupt

1: Enable period-matching of PWM1 interrupt

Bit 0 (PWM1DIE): PWM1DSF interrupt enable bit

0: Disable duty-matching of PWM1 interrupt

1: Enable duty-matching of PWM1 interrupt

NOTE

If the interrupt mask and instruction "ENI" are enabled, the program counter will jump into corresponding interrupt vector when the corresponding status flag is set.

6.1.22 Bank 0 R1E: IMR4 (Interrupt Mask Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P8ICIE	P7ICIE	P6ICIE	P5ICIE	-	-	-	-
R/W	R/W	R/W	R/W	-	-	-	-

Bits 7~4 (P8ICIE~P5ICIE): PxICSF interrupt enable bit

0: Disable PxICSF interrupt

1: Enable PxICSF interrupt

Bits 3~0: Not used. Set to "**0**" all the time.

NOTE

If the interrupt mask and instruction "ENI" are enabled, the program counter will jump into corresponding interrupt vector when the corresponding status flag is set.

6.1.23 Bank 0 R1F~R20: (Reserved)

6.1.24 Bank 0 R21: WDTCR (Watchdog Timer Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	-	-	-	PSWE	WPSR2	WPSR1	WPSR0
R/W	-	-	-	R/W	R/W	R/W	R/W

Bit 7 (WDTE): Watchdog Timer enable bit. WDTE is both readable and writable.

0: Disable WDT

1: Enable WDT

Bits 6~4: Not used. Set to "**0**" all the time.

Bit 3 (PSWE): Prescaler enable bit for WDT

0: Prescaler disable bit. WDT rate is 1:1.

1: Prescaler enable bit. WDT rate is set at bits 2~0.

Bits 2~0 (WPSR2~WPSR0): WDT Prescaler bits

WPSR2	WPSR1	WPSR0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.25 Bank 0 R22: TCCCR (TCC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TCCS	TCCEN	-	PSTE	TPSR2	TPSR1	TPSR0
-	R/W	R/W	-	R/W	R/W	R/W	R/W

Bit 7: Not used. Set to "**0**" all the time.

Bit 6 (TCCS): TCC Clock Source select bit

0: Fs (sub clock)

1: Fm (main clock)

Bit 5 (TCCEN**):** TCC Timer Enable Bit

0: Enable TCC Timer

1: Disable TCC Timer

Bit 4: Not used. Set to "**0**" all the time.

Bit 3 (PSTE): Prescaler enable bit for TCC

0: Prescaler disable bit. TCC rate is 1:1.

1: Prescaler enable bit. TCC rate is set at Bit 2 ~ Bit 0.

Bits 2~0 (TPSR2~TPSR0): TCC Prescaler Bits

TPSR2	TPSR1	TPSR0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.26 Bank 0 R23: TCCD (TCC Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TCC7~TCC0): TCC data

Counter is increased by the internal/external clock. Writable and readable as any other registers.

6.1.27 Bank 0 R24 ~ R2F: (Reserved)

6.1.28 Bank 0 R30 ~ R4F: (Reserved)

6.1.29 Bank 1 R5: IOCR8

These registers are used to control I/O port direction. They are both readable and writable.

1: Put the relative I/O pin into high impedance

0: Put the relative I/O pin as output

6.1.30 Bank 1 R6 ~ R7: (Reserved)

6.1.31 Bank 1 R8: P5PHCR (Port 5 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	PH52	PH51	PH50
-	-	-	-	-	R/W	R/W	R/W

Bits 7~3: Not used. Set to "0" all the time.

Bit 2 (PH52): Control bit used to enable pull-high of P52 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 1 (PH51): Control bit used to enable pull-high of P51 pin

Bit 0 (PH50): Control bit used to enable pull-high of P50 pin

6.1.32 Bank 1 R9: P6PHCR (Port 6 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	PH66	PH65	PH64	PH63	PH62	-	PH60
-	R/W	R/W	R/W	R/W	R/W	-	R/W

Bits 7, 1: Not used. Set to "0" all the time.

Bit 6 (PH66): Control bit used to enable pull-high of P66 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 5 (PH65): Control bit used to enable pull-high of P65 pin

Bit 4 (PH64): Control bit used to enable pull-high of P64 pin

Bit 3 (PH63): Control bit used to enable pull-high of P63 pin

Bit 2 (PH62): Control bit used to enable pull-high of P62 pin

Bit 0 (PH60): Control bit used to enable pull-high of P60 pin

6.1.33 Bank 1 RA: P7PHCR (Port 7 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	P7HPH	P7LPH
-	-	-	-	-	-	R/W	R/W

Bits 7~2: Not used. Set to "**0**" all the time.

Bit 1 (P7HPH): Control bit used to enable pull-high of the Port 7 high nibble pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 0 (P7LPH): Control bit used to enable pull-high of the Port 7 low nibble pin

6.1.34 Bank 1 RB: P5PLCR (Port 5 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	PL52	PL51	PL50
-	-	-	-	-	R/W	R/W	R/W

Bits 7~3: Not used. Set to "**0**" all the time.

Bit 2 (PL52): Control bit used to enable pull low of the P52 pin

0: Enable internal pull-low

1: Disable internal pull-low

Bit 1 (PL51): Control bit used to enable pull low of the P51 pin

Bit 0 (PL50): Control bit used to enable pull low of the P50 pin

6.1.35 Bank 1 RC: P6PLCR (Port 6 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	PL66	PL65	PL64	PL63	PL62	-	PL60
-	R/W	R/W	R/W	R/W	R/W	-	R/W

Bits 7, 1: Not used. Set to "0" all the time.

Bit 6 (PL66): Control bit used to enable pull low of the P66 pin

0: Enable internal pull-low

1: Disable internal pull-low

Bit 5 (PL65): Control bit used to enable pull low of the P65 pin

Bit 4 (PL64): Control bit used to enable pull low of the P64 pin

Bit 3 (PL63): Control bit used to enable pull low of the P63 pin

Bit 2 (PL62): Control bit used to enable pull low of the P62 pin

Bit 0 (PL60): Control bit used to enable pull low of the P60 pin

6.1.36 Bank 1 RD: P78PLCR (Ports 7~8 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	P8LPL	P7HPL	P7LPL
-	-	-	-	-	R/W	R/W	R/W

Bits 7~3: Not used. Set to "**0**" all the time.

Bit 2 (P8LPL): Control bit used to enable pull low of the Port 8 low nibble pin

0: Enable internal pull-low

1: Disable internal pull-low

Bit 1 (P7HPL): Control bit used to enable pull low of the Port 7 high nibble pin

Bit 0 (P7LPL): Control bit used to enable pull low of the Port 7 low nibble pin

6.1.37 Bank 1 RE: P5HDSCR (Port 5 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	H52	H51	H50
-	-	-	-	-	R/W	R/W	R/W

Bits 7~3: Not used. Set to "0" all the time.

Bits 2~0 (H52~H50): P52~P50 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.1.38 Bank 1 RF: P6HDSCR (Port 6 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	H66	H65	H64	H63	H62	-	H60
-	R/W	R/W	R/W	R/W	R/W	-	R/W

Bits 7, 1: Not used. Set to "0" all the time.

Bits 6~2, 0 (H66~H62, H60): P66~P62,P60 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.1.39 Bank 1 R10: P78HDSCR (Ports 7~8 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	P8LHDS	P7HHDS	P7LHDS
-	-	-	-	-	R/W	R/W	R/W

Bits 7~3: Not used. Set to "**0**" all the time.

Bit 2 (P8LHDS): Control bit used to enable high drive/sink of Port 8 low nibble pin

0: Enable high drive/sink

1: Disable high drive/sink

Bit 1 (P7HHDS): Control bit used to enable high drive/sink of Port 7 high nibble pin

Bit 0 (P7LHDS): Control bit used to enable high drive/sink of Port 7 low nibble pin

6.1.40 Bank 1 R11: P5ODCR (Port 5 Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	OD52	OD51	OD50
-	-	-	-	-	R/W	R/W	R/W

Bits 7~3: Not used. Set to "**0**" all the time.

Bits 2~0 (OD52~OD50): Open-Drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.1.41 Bank 1 R12: P6ODCR (Port 6 Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	OD66	OD65	OD64	OD63	OD62	-	OD60
-	R/W	R/W	R/W	R/W	R/W	-	R/W

Bits 7, 1: Not used. Set to "**0**" all the time.

Bits 6~2, 0 (OD66~OD62,OD60): Open-Drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.1.42 Bank 1 R13: P7ODCR (Port 7 Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	P7HOD	P7LOD
-	-	-	-	-	-	R/W	R/W

Bits 7~2: Not used. Set to "**0**" all the time.

Bit 1 (P7HOD): Control bit used to enable open-drain of Port 7 high nibble pin

0: Disable open-drain function

1: Enable open-drain function

Bit 0 (P7LOD): Control bit used to enable open-drain of Port 7 low nibble pin

6.1.43 Bank 1 R14 ~ R15: (Reserved)

6.1.44 Bank 1 R16: PWMSCR (PWM Source Clock Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	PWM1S
-	-	-	-	-	-	-	R/W

Bits 7~1: Not used. Set to "**0**" all the time.

Bit 0 (PWM1S): Clock selection for PWM1 timer

0: Fs (default)

1: Fm

6.1.45 Bank 1 R17: PWM1CR (PWM1 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1E	-	PWM1A	-	T1EN	T1P2	T1P1	T1P0
R/W	-	R/W	-	R/W	R/W	R/W	R/W

Bit 7 (PWM1E): PWM1 enable bit

0: Disable (default)

1: Enable. The compound pin is used as PWM1 pin

Bits 6, 4: Not used. Set to **"0"** all the time.

Bit 5 (PWM1A): Level option of PWM1

0: Duty level is Logic 1 (default)

1: Duty level is Logic 0

Bit 3 (T1EN): TMR1 enable bit. All PWM functions are valid only when this bit is set.

> **NOTE**
> *When the PWM waveform is on, a time delay of 1.5~2.5 PWM clock will occur before PWM output starts.*

0: TMR1 is off (default value)

1: TMR1 is on

PWMXEN	TXEN	Function Description
0	**0**	Not used as PWM function, I/O pin, or as any other pin function.
0	**1**	Timer function, I/O pin, or other pin function
1	**0**	PWM function, the waveform is kept at low level.
1	**1**	PWM function, normal PWM output waveform

Bits 2~0 (T1P2~T1P0):TMR1 clock prescale option bits

T1P2	T1P1	T1P0	Prescale
0	**0**	**0**	1:1 (default)
0	**0**	**1**	1:2
0	**1**	**0**	1:4
0	**1**	**1**	1:8
1	**0**	**0**	1:16
1	**0**	**1**	1:64
1	**1**	**0**	1:128
1	**1**	**1**	1:256

6.1.46 Bank 1 R18: PRD1L (Low Byte of PWM1 Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD1[7]	PRD1[6]	PRD1[5]	PRD1[4]	PRD1[3]	PRD1[2]	PRD1[1]	PRD1[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PRD1[7~0]): The contents of the register are the low byte of the PWM1 period.

NOTE

If the PWM1 duty/period needs to reload, the PRD1L register must be updated.

6.1.47 Bank 1 R19: PRD1H (High Byte of PWM1 Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD1[F]	PRD1[E]	PRD1[D]	PRD1[C]	PRD1[B]	PRD1[A]	PRD1[9]	PRD1[8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PRD1[F~8]): The contents of the register are the high byte of the PWM1 period

6.1.48 Bank 1 R1A: DT1L (Low Byte of PMW1 Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DT1[7]	DT1[6]	DT1[5]	DT1[4]	DT1[3]	DT1[2]	DT1[1]	DT1[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DT1[7~0]): The contents of the register are the low byte of the PWM1 duty.

6.1.49 Bank 1 R1B: DT1H (High Byte of PMW1 Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DT1[F]	DT1[E]	DT1[D]	DT1[C]	DT1[B]	DT1[A]	DT1[9]	DT1[8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DT1[F~8]): The contents of the register are the high byte of the PWM1 duty.

6.1.50 Bank 1 R1C: TMR1L (Low Byte of Timer 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMR1[7]	TMR1[6]	TMR1[5]	TMR1[4]	TMR1[3]	TMR1[2]	TMR1[1]	TMR1[0]
R	R	R	R	R	R	R	R

Bits 7~0 (TMR1[7~0]): The contents of the register are the low byte of the PWM1 timer which is counting. These bits are read-only.

6.1.51 Bank 1 R1D: TMR1H (High Byte of Timer 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMR1[F]	TMR1[E]	TMR1[D]	TMR1[C]	TMR1[B]	TMR1[A]	TMR1[9]	TMR1[8]
R	R	R	R	R	R	R	R

Bits 7~0 (TMR1[F~8]): The contents of the register are the high byte of the PWM1 timer which is counting. These bits are read-only.

6.1.52 Bank 1 R1E ~ R44: (Reserved)

6.1.53 Bank 1 R45: TBPTL (Table Point Low Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TB7~TB0): Table Point Address Bits 7~0.

6.1.54 Bank 1 R46: TBPTH (Table Point High Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLB	-	-	-	TB11	TB10	TB9	TB8
R/W	-	-	-	R/W	R/W	R/W	R/W

Bit 7 (HLB): Obtain MLB or LSB at machine code of ROM.

HLB	Read to Register Data Value Description
0	Read byte value is Bit 7 ~ Bit 0 from machine code.
1	Read byte value is - Highest bit fixed at "**0**" and Bit 14 ~ Bit 8 from machine code.

Bits 6~4: Not used. Set to "**0**" all the time.

Bits 3~0 (TB11~TB8): Table Pointer Address Bits 11~8.

6.1.55 Bank 1 R47: STKMON (Stack Pointer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STOF	-	-	-	STL3	STL2	STL1	STL0
R	-	-	-	R	R	R	R

Bit 7 (STOF): Stack pointer overflow indicator bit. Read only.

0: Stack pointer not overflow

1: Stack pointer overflow

Bits 6~4: Not used. Set to "**0**" all the time.

Bits 3~0 (STL3~0): Stack pointer number. Read only.

6.1.56 Bank 1 R48: PCH (Program Counter High)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	PC11	PC10	PC9	PC8
-	-	-	-	R/W	R/W	R/W	R/W

Bits 7~4: Not used. Set to "**0**" all the time.

Bits 3~0 (PC11~PC8): The high byte of program counter

6.1.57 Bank 1 R49: (Reserved)

6.1.58 Bank 1 R4A: COBS1 (Code Option Bit Select Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLFS	RESETEN	ENWDT	NRHL	NRE	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (HLFS): Mode selection bit after reset occurs

0: CPU is selected as Green mode when a reset occurs.

1: CPU is selected as Normal mode when a reset occurs (default).

Bit 6 (RESETEN): P80//RESET pin selection bit

0: Enable, /RESET pin

1: Disable, P80 pin

Bit 5 (ENWDT): WDT enable bit

0: Enable

1: Disable

Bit 4 (NRHL): Noise rejection high/low pulses defining bit. INT pin is falling edge trigger.

0: Pulses equal to 8/Fsys is regarded as signal

1: Pulses equal to 32/Fsys is regarded as signal

Bit 3 (NRE): Noise Rejection Enable Bit

0: Disable noise rejection

1: Enable noise rejection (note that in Green, Idle, and Sleep modes, the noise rejection circuit is always disabled).

Bits 2~0: Not used. Set to "**0**" all the time.

NOTE

*When the MCU powers on, it latches the code option setting values first. Then, the values in the code option words are determined whether to link them with the corresponding control registers (Bank1 R4A~4C) in accordance with COBS setting (**1** or **0**). If COBS equals "**0**", the initial values in the control registers Bank 1 R4A~4C are the same with the values in the code option words. They can be modified later to any other values.*

6.1.59 Bank 1 R4C: COBS3 (Code Option Bit Selection Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	FSS	-	-	-	-
-	-	-	R/W	-	-	-	-

Bits 7~5: Not used. Set to "**0**" all the time.

Bits 4 (FSS): Sub-oscillator mode selection bits

0: Fs is 64kHz

1: Fs is 16kHz

Bits 3~0: Not used. Set to "**0**" all the time.

NOTE

*When the MCU powers on, it latches the code option setting values first. Then, the values in the code option words are determined whether to link them to the corresponding control registers (Bank1 R4A~4C) in accordance with COBS setting (**1** or **0**). If COBS is equal to "**0**", the initial values in the control registers Bank 1 R4A~4C are the same with the values in the code option words. They can be modified later to any other values.*

6.1.60 Bank 1 R4D ~ R4F: (Reserved)

6.1.61 Bank 2 R21 ~ R4F: (Reserved)

6.1.62 R50~R7F, Banks 0~2 R80~RFF

These are all 8-bit general-purpose registers.

6.2 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The TPSR0~ TPSR2 bits of the TCCCR register (Bank 0 R22) are used to determine the ratio of the prescaler of TCC. Likewise, the WPSR0~WPSR2 bits of the WDTCR register (Bank 0 R21) are used to determine the WDT prescaler. The prescaler counter will be cleared by the instructions each time they are written into TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions. Figure 6-3 depicts the circuit diagram of TCC/WDT.

TCCD (Bank 0 R23) is an 8-bit timer. The clock source of TCC can be internal clock. TCC will increase by 1 at Fc clock (without prescaler).

NOTE

■ *The TCC signal source is from the internal clock, the TCC will stop running when Sleep mode occurs.*

The Watchdog Timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e., in Sleep mode). During Normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during Normal mode by software programming. With no prescaler, the WDT time-out period is approximately 18ms[1] (one oscillator start-up timer period).

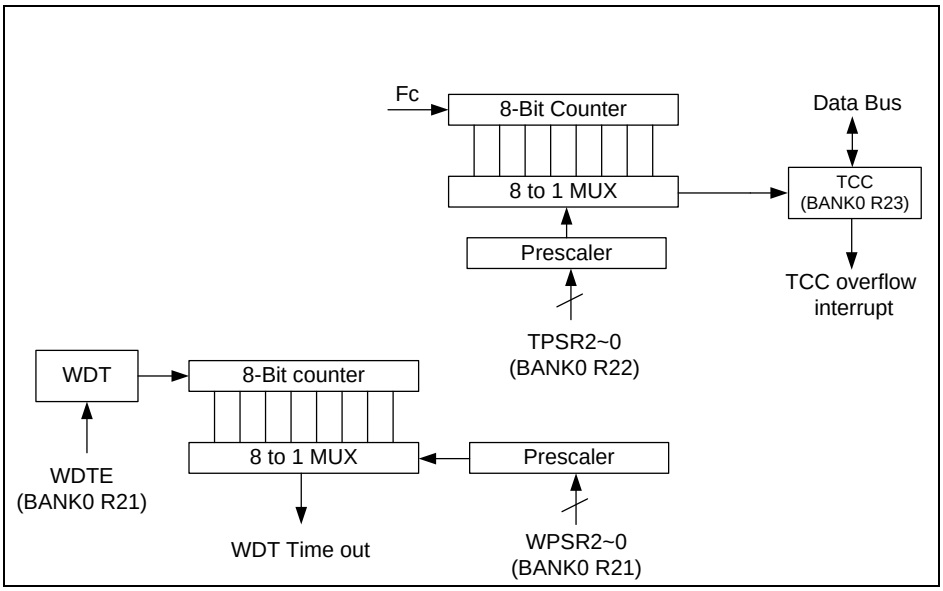


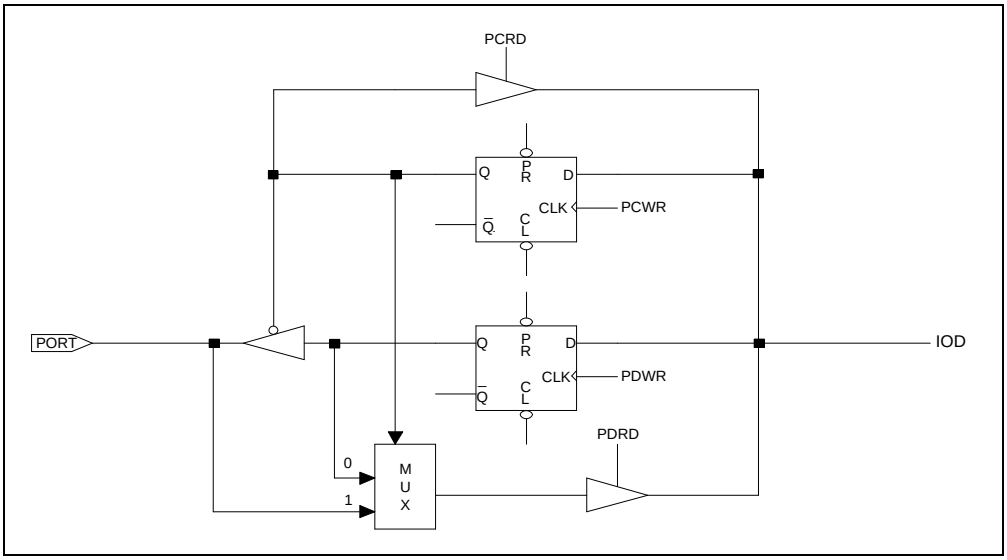
Figure 6-3 TCC and WDT Block Diagram

[1] *VDD=5V, WDT time-out period = 16.5ms ± 30%.*
VDD=3V, WDT time-out period = 18ms ± 30%.

6.3 I/O Ports

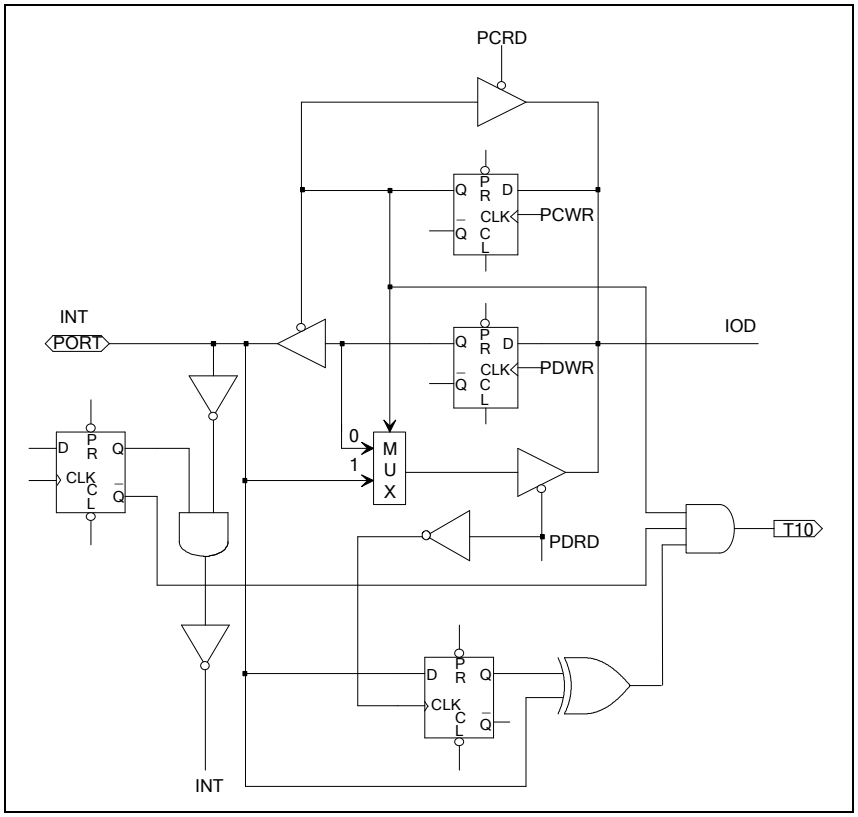
The I/O registers, Port 5~Port 8 are bi-directional tri-state I/O ports. All can be pulled high and pulled low internally by software. Furthermore, they can also be set as open-drain output and high sink/drive by software. Ports 5~8 feature wake-up and interrupt functions as well as input status change interrupt function. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC8).

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 ~ Port 8 are shown in the following Figures 6-4a to 6-4d.



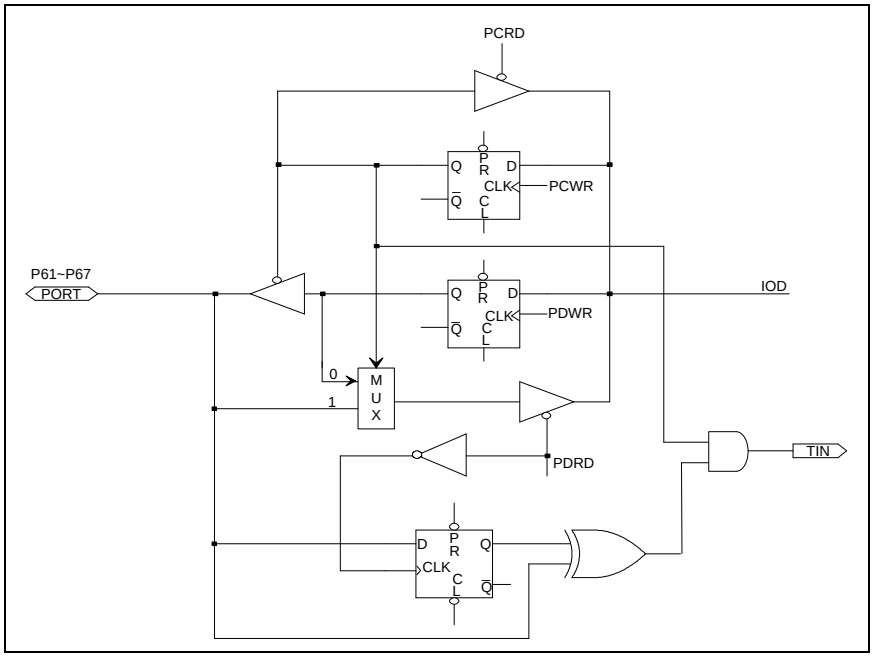
Note: *Pull-down is not shown in the figure.*

Figure 6-4a I/O Port and I/O Control Register for Port 5~8 Circuit Diagram



Note: *Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-4b I/O Port and I/O Control Register for /INT Circuit



Note: *Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-4c I/O Port and I/O Control Register for Ports 5~8 Circuit

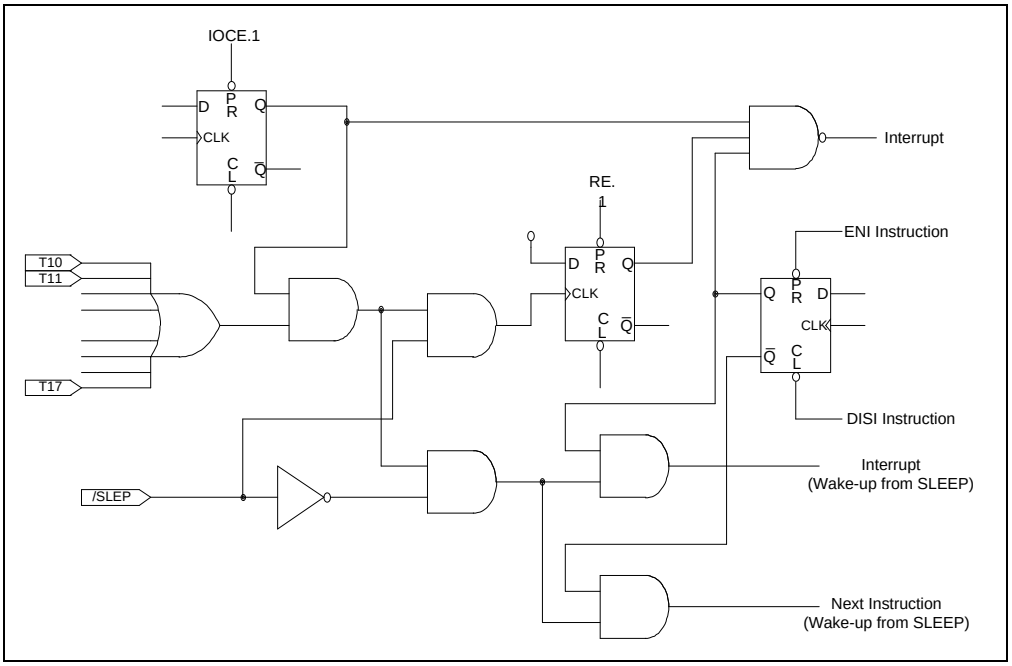


Figure 6-4d I/O Ports 5~8 with Input Change Interrupt/Wake-up Block Diagram

6.3.1 Usage of Ports 5~8 Input Change Wake-up/Interrupt Function

1. Wake-up
a) Before Sleep:
1) Disable WDT
2) Read I/O Port (MOV R6,R6)
3) Execute "ENI" or "DISI"
4) Enable Wake-up bit (Set **ICWKPx** = 1)
5) Execute "SLEP" instruction
b) After Wake-up:
→ Next instruction

2. Wake-up and Interrupt
a) Before SLEEP
1) Disable WDT
2) Read I/O Port (MOV R6,R6)
3) Execute "ENI" or "DISI"
4) Enable Wake-up bit (Set **ICWKPx** = 1)
5) Enable interrupt (Set PxICIE = 1)
6 Execute "SLEP" instruction
b) After Wake-up
1) IF "ENI" → Interrupt vector (0006H)
2) IF "DISI" → Next instruction

6.4 Reset and Wake-up

A Reset is initiated by one of the following events:

1) Power-on reset
2) /RESET pin input "low"
3) WDT time-out (if enabled)
4) LVR (if enabled)

The device is kept under Reset condition for a period of approximately 18ms[2] (one oscillator start-up timer period) after a reset is detected. And if the /Reset pin goes “low” or the WDT time-out is active, a reset is generated. In IRC mode, the reset time is 8/32 clocks. Once a Reset occurs, the following functions are performed (see Figures 6-5):

- The oscillator continuous running, or will be started.
- The Program Counter (R2) is set to all "**0**".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog Timer and prescaler are cleared.
- The control register bits are set as shown in the table under Section 6.4.3, *Summary of Register Initial Values after Reset*.

The Sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering Sleep mode, WDT (if enabled) is cleared but keeps on running. Wake-up is then generated (in IRC mode the wake-up time is 8/32 clocks). The controller can be awakened by any of the following events:

1) External reset input on /RESET pin
2) WDT time-out (if enabled)
3) External (INT1,0) pin changes (if INTWEx is enabled)
4) Port input status changes (if ICWKPx is enabled)
5) TCC Counter mode overflow occur.(if TCIE is enable)

The first two events (1 and 2) will cause the eKT5211 to reset. The T and P flags of R3 are used to determine the source of the reset (Wake-up). Events 3 to 5 are considered as continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following Wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 0x02~0x06 after Wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after Wake-up.

[2] Vdd = 5V, set up time period = 16.8ms ± 30%
Vdd = 3V, set up time period = 18ms ± 30%

Only one of Events 3 to 5 can be enabled before entering into Sleep mode. That is**:**

a) If WDT is enabled before SLEP, the eKT5211 can wake-up only when Event 1 or 2 occurs. Refer to Section 6.5 *Interrupt*, for further details.

b) If External (P80/P60, INT1/INT0) pin change is used to wake-up eKT5211 and INTWEx bit is enabled before SLEP (with WDT disabled). Hence, the eKT5211 can wake-up only when Event 3 occurs.

c) If Port Input Status Change is used to wake-up eKT5211 and the corresponding wake-up setting is enabled before SLEP (with WDT disabled). Hence, the eKT5211 can wake-up only when Event 4 occurs.

d) When TCC Counter mode uses external signal overflow to wake-up eKT5211 and TCIE bit of Bank 0 R1B register is enabled before SLEP, WDT must be disabled by software. Hence, the eKT5211 can wake-up only when Event 5 occurs.

6.4.1 Summary of Wake-up and Interrupt Mode Operation

<table>
<tr><th rowspan="2">Wake-up Signal</th><th rowspan="2">Condition Signal</th><th colspan="2">Sleep Mode</th><th colspan="2">Idle Mode</th><th colspan="2">Green Mode</th><th colspan="2">Normal Mode</th></tr>
<tr><th>DISI</th><th>ENI</th><th>DISI</th><th>ENI</th><th>DISI</th><th>ENI</th><th>DISI</th><th>ENI</th></tr>
<tr><td rowspan="4">External INT</td><td>INTWKx = 0,EXxIE = 0</td><td colspan="8">INT1/INT0 pin Disable</td></tr>
<tr><td>INTWKx = 0,EXxIE = 1</td><td colspan="4">Wake-up is invalid</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td></tr>
<tr><td>INTWKx = 1,EXxIE = 0</td><td colspan="8">INT1/INT0 pin Disable</td></tr>
<tr><td>INTWKx = 1,EXxIE = 1</td><td>Wake up + Next Instruction</td><td>Wake up + Interrupt Vector</td><td>Wake up + Next Instruction</td><td>Wake up + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td></tr>
<tr><td rowspan="2">TCC INT</td><td>TCIE = 0</td><td colspan="4">Wake-up is invalid</td><td colspan="4">Interrupt is invalid</td></tr>
<tr><td>TCIE = 1</td><td>Wake up + Next Instruction (Counter mode)</td><td>Wake up + Interrupt Vector (Counter mode)</td><td>Wake up + Next Instruction</td><td>Wake up + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td></tr>
</table>

(Continuation)

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
PWM1 (When Timer1 Match PRD1)	PWMxPIE=0	Wake-up is invalid				Interrupt is invalid			
	PWMxPIE=1	Wake-up is invalid		Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Pin Change INT	ICWKPx = 0 PxICIE = 0	Wake-up is invalid				Interrupt is invalid			
	ICWKPx = 0 PxICIE = 1	Wake-up is invalid				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ICWKPx = 1 PxICIE = 0	Wake up + Next Instruction				Interrupt is invalid			
	ICWKPx = 1 PxICIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
WDT time out		RESET	RESET	RESET	RESET	RESET	RESET	RESET	RESET

NOTE

After wake up:

1. If interrupt enable → interrupt t + next instruction

2. If interrupt disable → next instruction

6.4.2 The Status of RST, T, and P of Status Register

A Reset condition is initiated by one of the following events:

1) Power-on condition
2) High-low-high pulse on /RESET pin
3) Watchdog timer time-out
4) LVR occurs

The values of T and P, as listed in the following table are used to check how the MCU wakes up. The next table shows the events that may affect the status of T and P.

■ **Values of RST, T and P after Reset:**

Reset Type	T	P
Power-on	1	1
/RESET during Operating mode	P*	P*
/RESET Wake-up during Sleep mode	1	0
WDT during Operating mode	0	P*
WDT Wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

* ***P:*** *Previous status before reset*

■ **Status of T and P when Affected by Events:**

Event	T	P
Power-on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin change during Sleep mode	1	0

* ***P:*** *Previous value before reset*

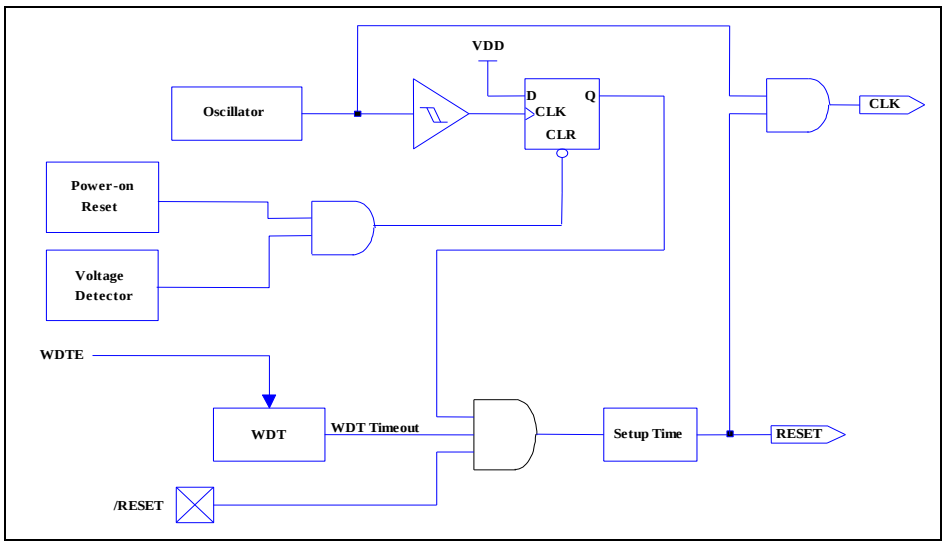


Figure 6-5 Block Diagram of Controller Reset

6.4.3 Summary of Register Initial Values after Reset

Legend: ***U:*** *Unknown or don't care* ***P:*** *Previous value before reset*
C: *Same with Code option* ***t:*** *Check tables under Section 6.4.2*

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x01	R1 (BSCR)	Bit Name	-	-	SBS1	SBS0	-	-	-	GBS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x02	R2 (PCL)	Bit Name	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x03	R3 (SR)	Bit Name	INT	0	0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Sleep/Idle	P	0	0	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X05	Bank 0, R5 (Port 5)	Bit Name	0	0	0	0	0	P52	P51	P50
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	P	P	P
0x06	Bank 0, R6 (Port 6)	Bit Name	0	P66	P65	P64	P63	P62	0	P60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	P	P	P	P	P	0	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x07	Bank 0, R7 (Port 7)	Bit Name	P77	P76	0	0	0	P72	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	0	0	0	P	0	0
0x08	Bank 0, R8 (Port 8)	Bit Name	0	0	0	0	0	0	0	P80
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	0	P
0X0B	Bank 0, RB (IOCR5)	Bit Name	0	0	0	0	0	IOC52	IOC51	IOC50
		Power-on	0	0	0	0	0	1	1	1
		/RESET and WDT	0	0	0	0	0	1	1	1
		Wake-up from Sleep/Idle	0	0	0	0	0	P	P	P
0x0C	Bank 0, RC (IOCR6)	Bit Name	0	IOC66	IOC65	IOC64	IOC63	IOC62	0	IOC60
		Power-on	0	1	1	1	1	1	0	1
		/RESET and WDT	0	1	1	1	1	1	0	1
		Wake-up from Sleep/Idle	0	P	P	P	P	P	0	P
0X0D	Bank 0, RD (IOCR7)	Bit Name	IOC77	IOC76	0	0	0	IOC72	0	0
		Power-on	1	1	0	0	0	1	0	0
		/RESET and WDT	1	1	0	0	0	1	0	0
		Wake-up from Sleep/Idle	P	P	0	0	0	P	0	0
0x0E	Bank 0, RE (OMCR)	Bit Name	CPUS	IDLE	-	-	-	-	-	-
		Power-on	Code option (HLFS)	1	0	0	0	0	0	0
		/RESET and WDT	Code option (HLFS)	1	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0F	Bank 0, RF EIESCR	Bit Name	0	0	0	0	EI1ES	EI0ES	0	0
		Power-on	0	0	0	0	1	1	0	0
		/RESET and WDT	0	0	0	0	1	1	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	0	0

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x10	Bank 0, R10 (WUCR1)	Bit Name	0	0	0	0	INTWK1	INTWK0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	0	0
0x12	Bank 0, R12 WUCR3	Bit Name	ICWKP8	ICWKP7	ICWKP6	ICWKP5	0	0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	0	0	0	0
0X14	Bank 0, R14 SFR1	Bit Name	0	0	0	0	EX1SF	EX0SF	0	TCSF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	0	P
0X16	Bank 0, R16 SFR3	Bit Name	0	0	0	0	0	0	PWM1 PSF	PWM1 DSF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	P	P
0X17	Bank 0, R17 SFR4	Bit Name	P8ICSF	P7ICSF	P6ICSF	P5ICSF	0	0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	0	0	0	0
0X1B	Bank 0, R1B IMR1	Bit Name	0	0	0	0	EX1IE	EX0IE	0	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	0	P
0X1D	Bank 0, R1D IMR3	Bit Name	0	0	0	0	0	0	PWM1PIE	PWM1DIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X1E	Bank 0, R1E IMR4	Bit Name	P8ICIE	P7ICIE	P6ICIE	P5ICIE	0	0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	0	0	0	0
0X21	Bank 0, R21 WDTCR	Bit Name	WDTE	-	-	-	PSWE	WPSR2	WPSR1	WPSR0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X22	Bank 0, R22 TCCCR	Bit Name	-	TCCS	TCCEN	-	PSTE	TPSR2	TPSR1	TPSR0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X23	Bank 0, R23 TCCD	Bit Name	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X05	Bank 1, R5 IOCR8	Bit Name	0	0	0	0	0	0	0	IOC80
		Power-on	0	0	0	0	0	0	0	1
		/RESET and WDT	0	0	0	0	0	0	0	1
		Wake-Up from Sleep/Idle	0	0	0	0	0	0	0	P
0X08	Bank 1, R8 P5PHCR	Bit Name	0	0	0	0	0	PH52	PH51	PH50
		Power-on	0	0	0	0	0	1	1	1
		/RESET and WDT	0	0	0	0	0	1	1	1
		Wake-up from Sleep/Idle	0	0	0	0	0	P	P	P
0X09	Bank 1, R9 P6PHCR	Bit Name	0	PH66	PH65	PH64	PH63	PH62	0	PH60
		Power-on	0	1	1	1	1	1	0	1
		/RESET and WDT	0	1	1	1	1	1	0	1
		Wake-up from Sleep/Idle	0	P	P	P	P	P	0	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0A	Bank 1, RA P7PHCR	Bit Name	0	0	0	0	0	0	P7HPH	P7LPH
		Power-on	0	0	0	0	0	0	1	1
		/RESET and WDT	0	0	0	0	0	0	1	1
		Wake-up from Sleep/Idle	0	0	0	0	0	0	P	P
0X0B	Bank 1, RB P5PLCR	Bit Name	0	0	0	0	0	PL52	PL51	PL50
		Power-on	0	0	0	0	0	1	1	1
		/RESET and WDT	0	0	0	0	0	1	1	1
		Wake-up from Sleep/Idle	0	0	0	0	0	P	P	P
0X0C	Bank 1, RC P6PLCR	Bit Name	0	PL66	PL65	PL64	PL63	PL62	0	PL60
		Power-on	0	1	1	1	1	1	0	1
		/RESET and WDT	0	1	1	1	1	1	0	1
		Wake-up from Sleep/Idle	0	P	P	P	P	P	0	P
0X0D	Bank 1, RD P78PLCR	Bit Name	0	0	0	0	0	P8LPL	P7HPL	P7LPL
		Power-on	0	0	0	0	0	1	1	1
		/RESET and WDT	0	0	0	0	0	1	1	1
		Wake-up from Sleep/Idle	0	0	0	0	0	P	P	P
0X0E	Bank 1, RE P5HDSCR	Bit Name	0	0	0	0	0	H52	H51	H50
		Power-on	0	0	0	0	0	1	1	1
		/RESET and WDT	0	0	0	0	0	1	1	1
		Wake-up from Sleep/Idle	0	0	0	0	0	P	P	P
0X0F	Bank 1, RF P6HDSCR	Bit Name	0	H66	H65	H64	H63	H62	0	H60
		Power-on	0	1	1	1	1	1	0	1
		/RESET and WDT	0	1	1	1	1	1	0	1
		Wake-up from Sleep/Idle	0	P	P	P	P	P	0	P
0X10	Bank 1, R10 P78HDSCR	Bit Name	0	0	0	0	0	P8LHDS	P7HHDS	P7LHDS
		Power-on	0	0	0	0	0	1	1	1
		/RESET and WDT	0	0	0	0	0	1	1	1
		Wake-up from Sleep/Idle	0	0	0	0	0	P	P	P
0X11	Bank 1, R11 P5ODCR	Bit Name	0	0	0	0	0	OD52	OD51	OD50
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X12	Bank 1, R12 P6ODCR	Bit Name	0	OD66	OD65	OD64	OD63	OD62	0	OD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	P	P	P	P	P	0	P
0X13	Bank 1, R13 P7ODCR	Bit Name	0	0	0	0	0	0	P7HOD	P7LOD
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	P	P
0X16	Bank 1, R16 PWMSCR	Bit Name	0	0	0	0	0	0	0	PWM1S
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	0	P
0X17	Bank 1, R17 PWM1CR	Bit Name	PWM1E	-	PWM1A	-	T1EN	T1P2	T1P1	T1P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X18	Bank 1, R18 PRD1L	Bit Name	PRD1[7]	PRD1[6]	PRD1[5]	PRD1[4]	PRD1[3]	PRD1[2]	PRD1[1]	PRD1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X19	Bank 1, R19 PRD1H	Bit Name	PRD1[F]	PRD1[E]	PRD1[D]	PRD1[C]	PRD1[B]	PRD1[A]	PRD1[9]	PRD1[8]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1A	Bank 1, R1A DT1L	Bit Name	DT1[7]	DT1[6]	DT1[5]	DT1[4]	DT1[3]	DT1[2]	DT1[1]	DT1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1B	Bank 1, R1B DT1H	Bit Name	DT1[F]	DT1[E]	DT1[D]	DT1[C]	DT1[B]	DT1[A]	DT1[9]	DT1[8]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X1C	Bank 1, R1C TMR1L	Bit Name	TMR1[7]	TMR1[6]	TMR1[5]	TMR1[4]	TMR1[3]	TMR1[2]	TMR1[1]	TMR1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1D	Bank 1, R1D TMR1H	Bit Name	TMR1[F]	TMR1[E]	TMR1[D]	TMR1[C]	TMR1[B]	TMR1[A]	TMR1[9]	TMR1[8]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X45	Bank 1, R45 TBPTL	Bit Name	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X46	Bank 1, R46 TBPTH	Bit Name	HLB	-	-	-	TB11	TB10	TB9	TB8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X47	Bank 1, R47 STKMON	Bit Name	STOF	0	0	0	STL3	STL2	STL1	STL0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	0	P	P	P	P
0X48	Bank 1, R48 PCH	Bit Name	0	0	0	0	PC11	PC10	PC9	PC8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P
0X4A	Bank 1, R4A COBS1	Bit Name	HLFS	RESET EN	ENWDT	NRHL	NRE	0	0	0
		Power-on	Code Option	Code Option	Code Option	Code Option	Code Option	0	0	0
		/RESET and WDT	P	P	P	P	P	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	0	0	0
0X4C	Bank 1, R4C COBS3	Bit Name	0	0	0	FSS	0	0	0	0
		Power-on	0	0	0	Code Option	0	0	0	0
		/RESET and WDT	0	0	0	Code Option	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	P	0	0	0	0

6.5 Interrupt

The eKT5211 has six interrupts (External, Internal) as listed below**:**

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Interna / External	Reset	-	-	0	High 0
External	INT	ENI + EXIE=1	EXSF	2	1
External	Pin change	ENI +PxICIE=1	ICSF	4	2
Internal	TCC	ENI + TCIE=1	TCSF	6	3
Internal	PWMP1	ENI+PWM1PIE=1	PWM1PSF	14	4
Internal	PWMD1	ENI+PWM1DIE=1	PWM1DSF	16	5

Bank 0 R14~R19 are the interrupt status registers that record the interrupt requests in the relative flags/bits. Bank0 R1B~R20 are the interrupt Mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the enabled interrupts occurs, the next instruction will be fetched from individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICSF bit delete) in the Interrupt Status Register is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

External interrupt is equipped with digital noise rejection circuit (input pulse of less than **4 system clocks time** is eliminated as noise)**.** When an interrupt (Falling edge) is generated by the External interrupt (if enabled), the next instruction will be fetched from Address 002H.

Before the interrupt subroutine is executed, the contents of ACC and the R3 (Bit 0~Bit 4) and R4 registers are saved by hardware. If another interrupt occurs, the ACC, R3 (Bit 0~Bit 4), and R4 will be replaced by the new interrupt. After the interrupt service routine is completed, ACC, R3 (Bit 0~Bit 4), and R4 restored.

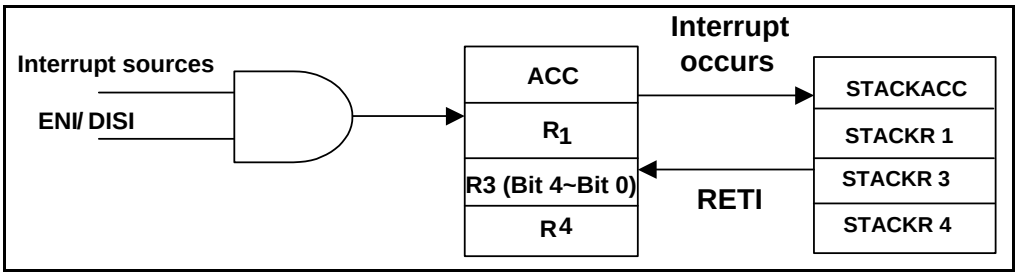


Figure 6-6a Interrupt Backup Diagram

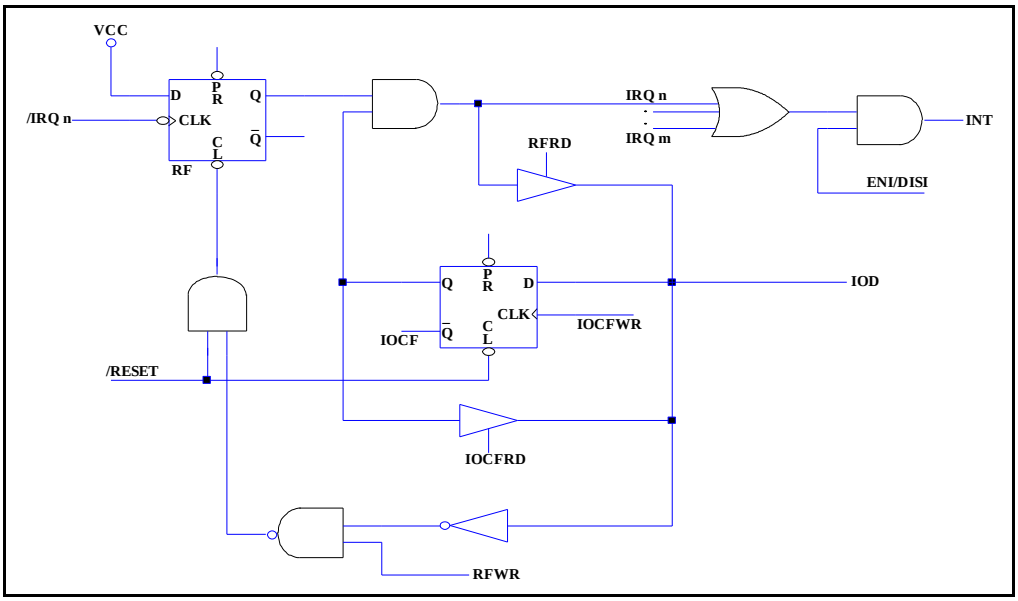


Figure 6-6b Interrupt Input Circuit

6.6 Dual Set of PWM (Pulse Width Modulation)

6.6.1 Overview

Under PWM mode, up to 16-bit resolution PWM output is generated (see. functional block diagram below). A PWM output consists of a time period and a duty cycle, and it keeps the output high. The PWM baud rate is the inverse of the time period.

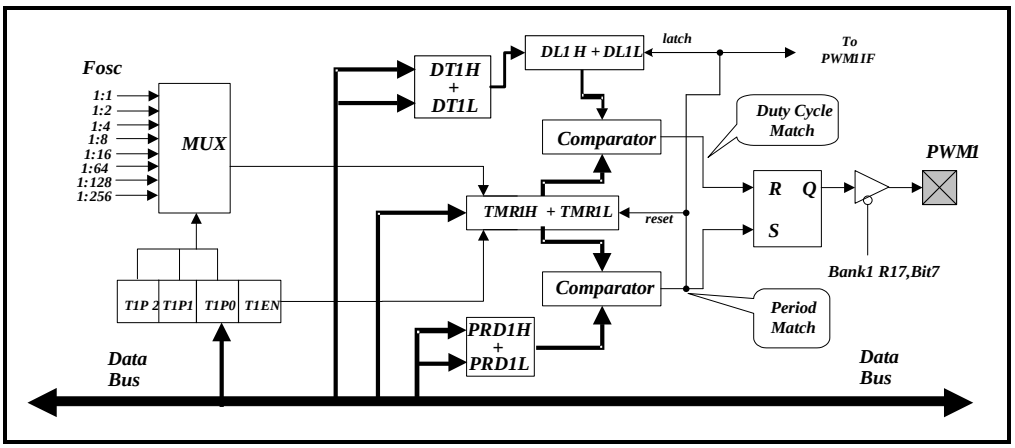


Figure 6-7a Dual PWMs Functional Block Diagram

Figure 6-7b below; *PWM Output Timing*, depicts the relationships between a time period and a duty cycle.

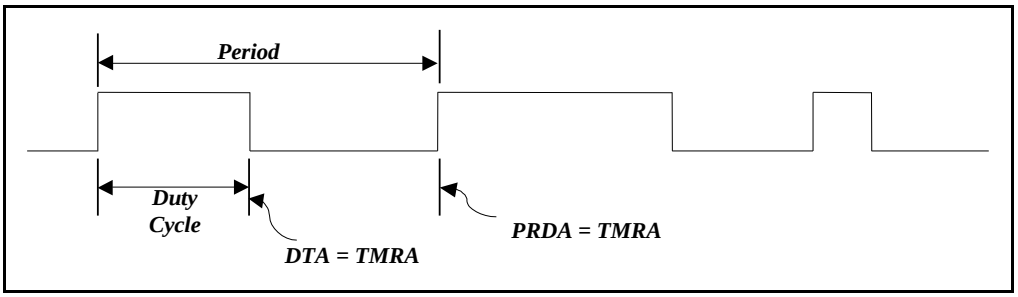


Figure 6-7b PWM Output Timing

6.6.2 Control Register

R_BANK	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x17	SFR3							PWM1PSF	PWM1DS
									F	F
Bank 0	0x1D	IMR3							PWM1PIE	PWM1DIE
									R/W	R/W
Bank 1	0x16	PWMSCR								PWM1S
										R/W
Bank 1	0x17	PWM1CR	PWM1E	-	PWM1A	-	T1EN	T1P2	T1P1	T1P0
			R/W	-	R/W	-	R/W	R/W	R/W	R/W
Bank 1	0x18	PRD1L	PRD1[7]	PRD1[6]	PRD1[5]	PRD1[4]	PRD1[3]	PRD1[2]	PRD1[1]	PRD1[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x19	PRD1H	PRD1[F]	PRD1[E]	PRD1[D]	PRD1[C]	PRD1[B]	PRD1[A]	PRD1[9]	PRD1[8]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1A	DT1L	DT1[7]	DT1[6]	DT1[5]	DT1[4]	DT1[3]	DT1[2]	DT1[1]	DT1[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1B	DT1H	DT1[F]	DT1[E]	DT1[D]	DT1[C]	DT1[B]	DT1[A]	DT1[9]	DT1[8]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1C	TMR1L	TMR1[7]	TMR1[6]	TMR1[5]	TMR1[4]	TMR1[3]	TMR1[2]	TMR1[1]	TMR1[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1D	TMR1H	TMR1[F]	TMR1[E]	TMR1[D]	TMR1[C]	TMR1[B]	TMR1[A]	TMR1[9]	TMR1[8]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.6.3 Increment Timer Counter (TMRX: TMR1H/TMR1L)

TMR1 is 16-bit clock counter with programmable prescaler. It is designed as baud rate clock generators for the PWM module. TMR can be read only. When in use, they can be turned off for power saving by setting the T1EN bit [BANK1-R17 <3>] to "**0**". TMR1 is internal designs and cannot be read.

6.6.4 PWM Time Period (PRDX: PRD1H/PRD1L)

The PWM time period is 16-bit resolution and is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

1) TMRX is cleared

2) The PWMX pin is set to "**1**"

NOTE
*The PWM output cannot be set if the duty cycle is "**0**."*

3) The PWMXIF pin is set to "**1**"

To calculate the PWM time period, use the following formula**:**

$$Period = (PRDX + 1) \times \left(\frac{1}{F_{OSC}}\right) \times (TMRX \ \ prescale\ value)$$

Example:

PRDX = 49; Fosc = 4 MHz; TMRX (0, 0, 0) = 1 : 1,

CLKS bit of the Code Option Register = 0 (two oscillator periods);

Then –

$$Period = (49+1) \times \left(\frac{1}{4M}\right) \times 1 = 12.5\mu s$$

6.6.5 PWM Duty Cycle (DTX: DT1H/DT1L)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded anytime. However, it cannot be latched into DLX until the current value of DLX is equal to TMRX.

The following formula shows how to calculate the PWM duty cycle**:**

$$Duty\ cycle = (DTX) \times \left(\frac{1}{F_{OSC}}\right) \times (TMRX \ \ prescale\ value)$$

Example:

DTX = 10; Fosc = 4 MHz; TMRX (0, 0, 0) = 1 : 1,

CLKS bit of the Code Option Register = 0 (two oscillator periods);

Then –

$$Duty\ cycle = (10) \times \left(\frac{1}{4M}\right) \times 1 = 2.5\mu s$$

6.6.6 PWM Programming Process/Steps

1) Load the PWM duty cycle into DT
2) Load the PWM time period into PRD
3) Enable the interrupt function by writing to Bank 0-R1D, if required
4) Load a desired value for the timer prescaler
5) Enable PWMX function, i.e., enable PWMXE control bit
6) Finally, enable TMRX function, i.e., enable TXEN control bit

If the application needs to change the PWM duty and period cycle at run time, refer to the following programming steps**:**

1) Load new duty cycle (if using dual PWM function) at any time.
2) Load new period cycle. You must take note of the order of loading period cycle. As soon as the low byte of PWM period cycle is assigned with a value, the new PWM cycle is loaded into circuit.
3) The circuit will automatically update the new duty and period cycles to generate new PWM waveform at the next PWM cycle.

6.7 Oscillator

6.7.1 Oscillator Modes

The eKT5211 can be operated in one oscillator mode, i.e., Internal RC oscillator mode (IRC). You need to set the main-oscillator modes, and set sub-oscillator modes by selecting the FSS in the Code Option register to complete the overall oscillator mode setting.

■ **Summary of Maximum Operating Speeds**

Conditions	VDD	Fxt Max. (MHz)
Two cycles with two clocks	2.5	4M
	3.0	8M

6.7.2 Internal RC Oscillator Mode

The eKT5211 offers a versatile internal RC mode with default frequency value of 4 MHz. The Internal RC oscillator mode has other frequencies (8 MHz) that can be set by Code Option**;** RCM1 and RCM0. All these two main frequencies can be calibrated by programming the Writer. The Table below describes a typical drift rate of the calibration.

■ **Internal RC Drift Rate (Ta=25°C, VDD=5.0V±5%, VSS=0V)**

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~+85°C)	Voltage (2.5V~5.5V)	Process	Total
4 MHz	±2%	±1%	±1%	±4%
8 MHz	±2%	±1%	±1%	±4%

NOTE

These are theoretical values intended for reference only. Actual values may vary depending on actual conditions.

6.8 Power-on Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply reaches its steady state. The eKT5211 is equipped with a Power-On Voltage Detector (POVD) with a detection level of 2.2V. It will work well if Vdd rises fast enough (50ms or less). However, in critical applications, extra devices are still required to assist in solving power-up problems.

6.9 External Power-on Reset Circuit

The circuit diagram in Figure 6-11 implements an external RC to generate the reset pulse. The pulse width (time constant) should be kept long enough for VDD to reach minimum operational voltage. Apply this circuit when the power supply has a slow rise time. Since the current leakage from the /RESET pin is about ± 5μA, it is recommended that R should not be greater than 40KΩ in order for the /RESET pin voltage to remain at below 0.2V. The diode (D) functions as a short circuit at the instant of power down. The capacitor (C) will discharge rapidly and fully. The current-limited resistor (Rin) will prevent high current or ESD (electrostatic discharge) from flowing into the /RESET pin.

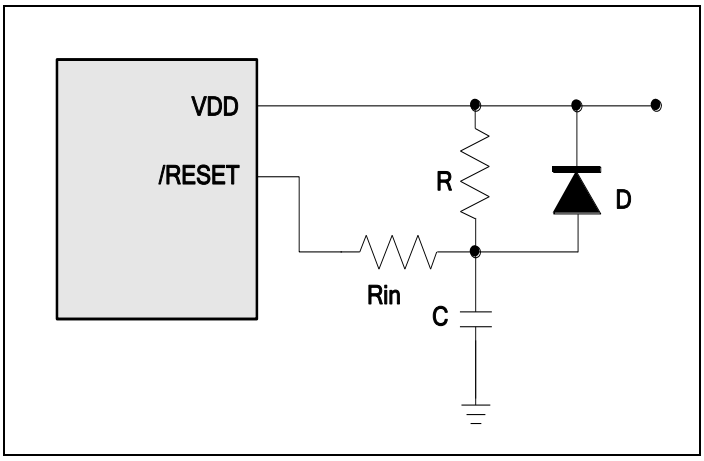


Figure 6-11 External Power-Up Reset Circuit

6.10 Residue-Voltage Protection

When the battery is replaced, device power (VDD) is taken off but residue-voltage remains. The residue-voltage may trips below VDD minimum, but not to zero. This condition may cause a poor power-on reset. The following circuits (Figures 6-12a & 6-12b) show how to accomplish a proper residue-voltage protection circuit.

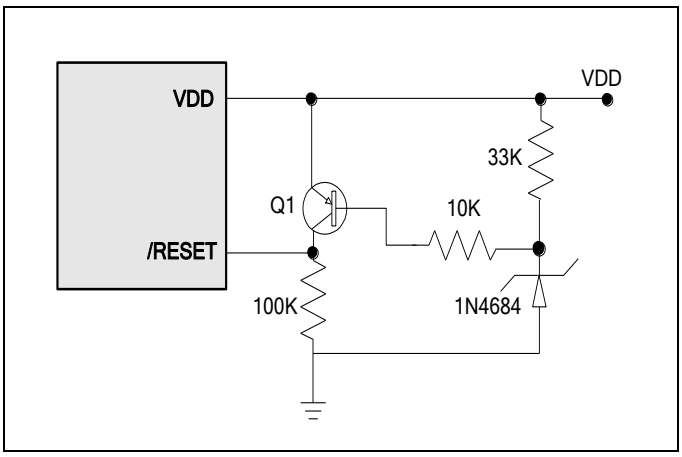


Figure 6-12a Circuit 1 for the Residue Voltage Protection

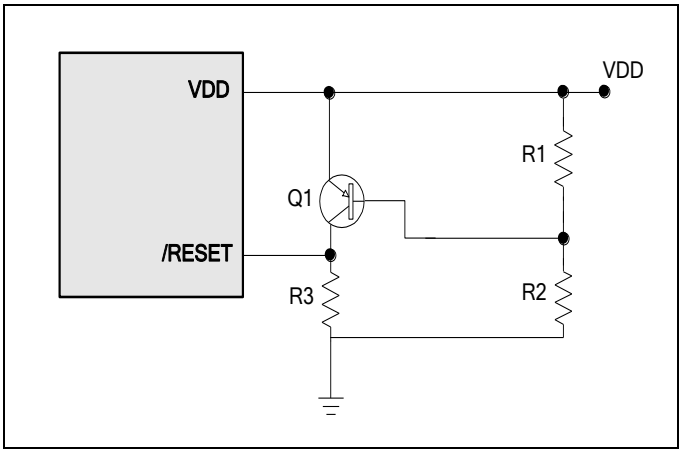


Figure 6-12b Circuit 2 for the Residue Voltage Protection

6.11 Code Option

6.11.1 Code Option Register (Word 0)

Word 0															
Bit	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	**COBS**	**-**	**-**	**-**	**HLFS**	**-**	**LVR1**	**LVR0**	**RESETEN**	**ENWDT**	**NRHL**	**NRE**	**PR2**	**PR1**	**PR0**
1	Code Option	High	High	High	Normal	High	High	High	P80/INT1	Disable	32/fc	Enable	Disable		
0	Register	Low	Low	Low	Green	Low	Low	Low	/RESET	Enable	8/fc	Disable	Enable		
Default	1	1	1	1	1	0	1	1	1	0	1	1	1		

Bit 14 (COBS): Code Option Bit Selection

0: Control bits in Bank 1 R4A, R4B, and R4C are read from the **control register**.

1: Control bits in Bank 1 R4A, R4B, and R4C are read from the **code option register** (default).

NOTE

When the IC powers on, IC latches the code option setting values first. Then, the values in code option words are determined to whether linked them with corresponding Control Registers Bank 1 R4A~4C by setting COBS to "1" or "0". If COBS equals "0", the initial values in the Control Registers Bank 1 R4A~4C are the same with the value in code option words. They can be modified later to any other values as desired.

Bits 13~11: Not used. Set to "**1**" all the time.

Bit 10 (HLFS): Reset to Normal or Green Mode select bit

0: CPU is selected to enter into Green mode when a reset occurs.

1: CPU is selected to enter into Normal mode when a reset occurs (Default)

Bit 9: Not used. Set to "**0**" all the time.

Bits 8~7 (LVR1~LVR0): Low Voltage Reset enable bit

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on reset; default)	
10	2.7V*	2.9V
01	3.5V**	3.7V
00	4.0V***	4.2V

* *If VDD < 2.7V and is kept for about 5 µs, the IC will reset.*

** *If VDD < 3.5V and is kept for about 5 µs, the IC will reset.*

*** *If VDD < 4.0V and is kept for about 5 µs, the IC will reset.*

Bit 6 (RESETEN): P80/INT1/RESET pin select bit

0: Enable /RESET pin

1: Disable P80/INT1 pin (default)

Bit 5 (ENWDT): WDT Enable bit

0: Enable (default)

1: Disable

Bit 4 (NRHL): Noise Rejection High/Low pulse definition bit.

0: Pulses equal to 8/fc [s] is considered as valid signal

1: Pulses equal to 32/fc [s] is considered as valid signal (default)

Bit 3 (NRE): Noise Rejection Enable bit

0: Disable.

1: Enable (default)

NOTE

During Green, Idle, and Sleep modes, the Noise Rejection circuit is always disabled.

Bits 2~0 (PR2 ~ PR0): Protect bit. Each protect status is as follows**:**

PR2	PR1	PR0	Protect
0	**0**	**0**	Enable
1	**1**	**1**	Disable

6.11.2 Code Option Register (Word 1)

Word 1															
Bit	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	**-**	**FSS**	**-**	**-**	**-**	**-**	**-**	**-**	**RCM1**	**RCM0**	**-**	**-**	**-**	**-**	**-**
1	High	16KHz	High	High	High	High	High	High	High	High	High	High	High	High	High
0	Low	64KHz	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low
Default	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1

Bit 14: Not used. Set to "**1**" all the time.

Bit 13 (FSS): Sub-frequency select bit

0: Fs is 64kHz

1: Fs is 16kHz (default)

NOTE

WDT frequency is always 16kHz regardless of the FSS setting.

Bits 12~7: Not used. Set to "**1**" all the time.

Bits 6~5 (RCM1~RCM0): IRC frequency selection

RCM1	RCM0	Frequency (MHz)
0	1	8 (default)
1	1	4

Bits 4~0: Not used. Set to "**1**" all the time.

6.11.3 Code Option Register (Word 2)

Word 2															
Bit	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
1	High	High	High	High	High	High	High	High	High	High	High	High	High	High	High
0	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low
Default	0	1	1	1	1	1	1	0	1	1	1	1	0	1	1

Bit 14: Not used. Set to "**0**" all the time.

Bits 13~12: Not used. Set to "**1**" all the time.

Bits 11~8: Not used. Set to "**1**" all the time.

Bit 7: Not used. Set to "**0**" all the time.

Bits 6~3: Not used. Set to "**1**" all the time.

Bit 2: Not used. Set to "**0**" all the time.

Bits 1~0: Not used. Set to "**1**" all the time.

6.11.4 Code Option Register (Word 3)

Word 3															
Bit	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	-	-	-	-	-	-	-	-	-	ID5	ID4	ID3	ID2	ID1	ID0
1	High	High	High	High	High	High	High	High	High	Customer ID					
0	Low	Low	Low	Low	Low	Low	Low	Low	Low						
Default	1	1	1	1	1	1	1	1	1						

Bit 14: Not used. Set to "**1**" all the time.

Bits 13~8: Not used. Set to "**1**" all the time.

Bits 7~6: Not used. Set to "**1**" all the time.

Bits 5~0 (ID5~ID0): Customer's ID Code

6.12 Instruction Set

Each instruction in the instruction set is a 15-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2, A", "ADD R2, A", or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2, A", "BS(C) R2, 6", "CLR R2", etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows**:**

- “LCALL”, “LJMP”, "JMP", "CALL", "RET", "RETL", "RETI", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Moreover, the instruction set has the following features**:**

1) Every bit of any register can be directly set, cleared, or tested.

2) The I/O register can be considered as general register. That is, the same instruction can operate on the I/O register.

■ Instruction Set Table:

In the following Instruction Set table, the following symbols are used:

*"**R**" represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction.*

*"**b**" represents a bit field designator that selects the value for the bit which is located in the register "**R**", and affects operation.*

*"**k**" represents an 8 or 10-bit constant or literal value.*

Binary Instruction	Mnemonic	Operation	Status Affected
000 0000 0000 0000	NOP	No Operation	None
000 0000 0000 0001	DAA	Decimal Adjust A	C
000 0000 0000 0011	SLEP	0 → WDT, Stop oscillator	T, P
000 0000 0000 0100	WDTC	0 → WDT	T, P
000 0000 0001 0000	ENI	Enable Interrupt	None
000 0000 0001 0001	DISI	Disable Interrupt	None
000 0000 0001 0010	RET	[Top of Stack] → PC	None
000 0000 0001 0011	RETI	[Top of Stack] → PC, Enable Interrupt	None
000 0001 rrrr rrrr	MOV R,A	A → R	None
000 0010 0000 0000	CLRA	0 → A	Z
000 0011 rrrr rrrr	CLR R	0 → R	Z
000 0100 rrrr rrrr	SUB A,R	R-A → A	Z, C, DC
000 0101 rrrr rrrr	SUB R,A	R-A → R	Z, C, DC
000 0110 rrrr rrrr	DECA R	R-1 → A	Z
000 0111 rrrr rrrr	DEC R	R-1 → R	Z
000 1000 rrrr rrrr	OR A,R	A ∨ R → A	Z
000 1001 rrrr rrrr	OR R,A	A ∨ R → R	Z
000 1010 rrrr rrrr	AND A,R	A & R → A	Z
000 1011 rrrr rrrr	AND R,A	A & R → R	Z
000 1100 rrrr rrrr	XOR A,R	A ⊕ R → A	Z
000 1101 rrrr rrrr	XOR R,A	A ⊕ R → R	Z
000 1110 rrrr rrrr	ADD A,R	A + R → A	Z, C, DC
000 1111 rrrr rrrr	ADD R,A	A + R → R	Z, C, DC
001 0000 rrrr rrrr	MOV A,R	R → A	Z
001 0001 rrrr rrrr	MOV R,R	R → R	Z
001 0010 rrrr rrrr	COMA R	/R → A	Z
001 0011 rrrr rrrr	COM R	/R → R	Z
001 0100 rrrr rrrr	INCA R	R+1 → A	Z
001 0101 rrrr rrrr	INC R	R+1 → R	Z
001 0110 rrrr rrrr	DJZA R	R-1 → A, skip if zero	None
001 0111 rrrr rrrr	DJZ R	R-1 → R, skip if zero	None
001 1000 rrrr rrrr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C

(Continuation)

Binary Instruction	Mnemonic	Operation	Status Affected
001 1001 rrrr rrrr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
001 1010 rrrr rrrr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
001 1011 rrrr rrrr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
001 1100 rrrr rrrr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
001 1101 rrrr rrrr	SWAP R	R(0-3) ↔ R(4-7)	None
001 1110 rrrr rrrr	JZA R	R+1 → A, skip if zero	None
001 1111 rrrr rrrr	JZ R	R+1 → R, skip if zero	None
010 0bbb rrrr rrrr	BC R,b	0 → R(b)	None [1]
010 1bbb rrrr rrrr	BS R,b	1 → R(b)	None [2]
011 0bbb rrrr rrrr	JBC R,b	if R(b)=0, skip	None
011 1bbb rrrr rrrr	JBS R,b	if R(b)=1, skip	None
100 kkkk kkkk kkkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
101 kkkk kkkk kkkk	JMP k	(Page, k) → PC	None
110 0000 kkkk kkkk	MOV A,k	k → A	None
110 0100 kkkk kkkk	OR A,k	A ∨ k → A	Z
110 1000 kkkk kkkk	AND A,k	A & k → A	Z
110 1100 kkkk kkkk	XOR A,k	A ⊕ k → A	Z
111 0000 kkkk kkkk	RETL k	k → A, [Top of Stack] → PC	None
111 0100 kkkk kkkk	SUB A,k	k-A → A	Z, C, DC
111 1100 kkkk kkkk	ADD A,k	K+A → A	Z, C, DC
111 1010 0000 kkkk	SBANK k	K->R1(5:4)	None
111 1010 0100 kkkk	GBANK k	K->R1(1:0)	None
111 1010 1000 kkkk kkk kkkk kkkk kkkk	LCALL k	Next instruction: k kkkk kkkk kkkk PC+1→[SP], k→PC	None
111 1010 1100 kkkk kkk kkkk kkkk kkkk	LJMP k	Next instruction: k kkkk kkkk kkkk K→PC	None
111 1011 rrrr rrrr	TBRD R	ROM[(TABPTR)] → R	None

[1] *This instruction is not recommended for interrupt status register operation.*

If user wants to clear Bit 0 for interrupt status register (ex. 0xF), the method recommended is shown below:

MOV A,@0B11111110

AND 0xF,A

[2] *This instruction cannot operate under interrupt status register.*

7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	Vss-0.3V	to	VDD+0.5V
Output voltage	Vss-0.3V	to	VDD+0.5V
Working Voltage	2.5V	to	5.5V
Working Frequency	DC	to	8 MHz

8 DC Electrical Characteristics

■ **(Ta=25°C, VDD=5.0V±5%, VSS=0V)**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fxt	IRC: VDD to 5.0V	4 MHz, 8 MHz	-	F	-	Hz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
IRCE	Internal RC oscillator error per stage	-	-	±1	-	%
IRC1	IRC:VDD to 5.0V	RCM0 : RCM1=1:1	-	4	-	MHz
IRC3	IRC:VDD to 5.0V	RCM0 : RCM1=0:1	-	8	-	MHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIH1	Input High Voltage (Schmitt trigger)	Ports 5, 6, 7, 8	0.7Vdd	-	Vdd+0.3V	V
VIL1	Input Low Voltage (Schmitt trigger)	Ports 5, 6, 7, 8	-0.3V	-	0.3Vdd	V
VIHT1	Input High Threshold Voltage (Schmitt trigger)	/RESET	0.7Vdd	-	Vdd+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	-0.3V	-	0.3Vdd	V
VIHT2	Input High Threshold Voltage (Schmitt trigger)	INT	0.7Vdd	-	Vdd+0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt trigger)	INT	-0.3V	-	0.3Vdd	V
IOH1	Output High Voltage (Ports 5, 6, 7, 8)	VOH = VDD-0.1VDD	-3.0	-5.0		mA
IOH2	Output High Voltage (high drive) (Ports 5, 6, 7, 8)	VOH = VDD-0.1VDD	-6.0	-8.0		mA

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IOL1	Output Low Voltage (Ports 5~8)	VOL = GND+0.1VDD	10	13	-	mA
IOL2	Output Low Voltage (high sink) (Ports 5, 6, 7, 8)	VOL = GND+0.1VDD	20	27	-	mA
IOL3	Output Low Voltage (high sink) (P80)	VOL = GND+0.1VDD	20	30	-	mA
LVR1	Low voltage reset level	Ta=25°C	2.41	2.7	2.99	V
		Ta= -40~85°C	2.15	2.7	3.29	V
LVR2	Low voltage reset level	Ta=25°C	3.1	3.5	3.9	V
		Ta= -40~85°C	2.73	3.5	4.27	V
LVR3	Low voltage reset level	Ta=25°C	3.56	4.0	4.44	V
		Ta= -40~85°C	3.16	4.0	4.82	V
IPH	Pull-high current	Pull-high active, input pin at VSS	-50	-75	-100	μA
IPL	Pull-low current	Pull-low active, input pin at Vdd	30	55	80	μA
ISB1	Power down current (Sleep mode)	/RESET= 'High', Fm and Fs off. All input and I/O pins at VDD, Output pin floating, WDT disabled	-	1.0	2.0	μA
ISB2	Power down current (Sleep mode)	/RESET= 'High', Fm and Fs off. All input and I/O pins at VDD, Output pin floating, WDT enabled	-	5	-	μA
ISB3	Power down current (Idle mode)	/RESET= 'High', Fm off, Fs=64K/16kHz (IRC type), Output pin floating, WDT disabled,	-	5	-	μA
ISB4	Power down current (Idle mode)	/RESET= 'High', Fm off, Fs=64K/16kHz (IRC type), Output pin floating, WDT enabled	-	5	-	μA
ICC1	Operating supply current (Green mode)	/RESET= 'High', Fm off, Fs=64K/16kHz (IRC type), Output pin floating, WDT disabled	-	30	-	μA
ICC2	Operating supply current (Green mode)	/RESET= 'High', Fm off, Fs=64K/16kHz (IRC type), Output pin floating, WDT enabled	-	30	-	μA
ICC3	Operating supply current (Normal mode)	/RESET= 'High', Fm=4MHz (IRC type), Fs on, Output pin floating, WDT enabled	-	2.3	2.9	mA
ICC4	Operating supply current (Normal mode)	/RESET= 'High', Fm=8MHz (IRC type), Fs on, Output pin floating, WDT enabled	-	3.0	3.3	mA

NOTE

- *The above parameters are theoretical values only and have not been tested or verified.*
- *Data under the "Min.", "Typ.", and "Max." columns are based on theoretical results at 25°C. These data are for design guidance only and have not been tested or verified.*

9 AC Electrical Characteristics

■ **(**eKT5211 **-40≦Ta≦85°C, VDD=5.0V, VSS=0V)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	-	45	50	55	%
Tins	Instruction cycle time (CLKS="**0**")	RC type	500	-	DC	ns
Ttcc	TCC input period	-	(Tins+20)/N*	-	-	ns
Tdrh	Device reset hold time	-	11.3	16.2	21.6	ms
Trst	/RESET pulse width	Ta = 25°C	2000	-	-	ns
Twdt	Watchdog timer period	Ta = 25°C	11.3	16.2	21.6	ms
Tset	Input pin setup time	-	-	0		ns
Thold	Input pin hold time	-	15	20	25	ns
Tdelay	Output pin delay time	Cload=20pF	45	50	55	ns

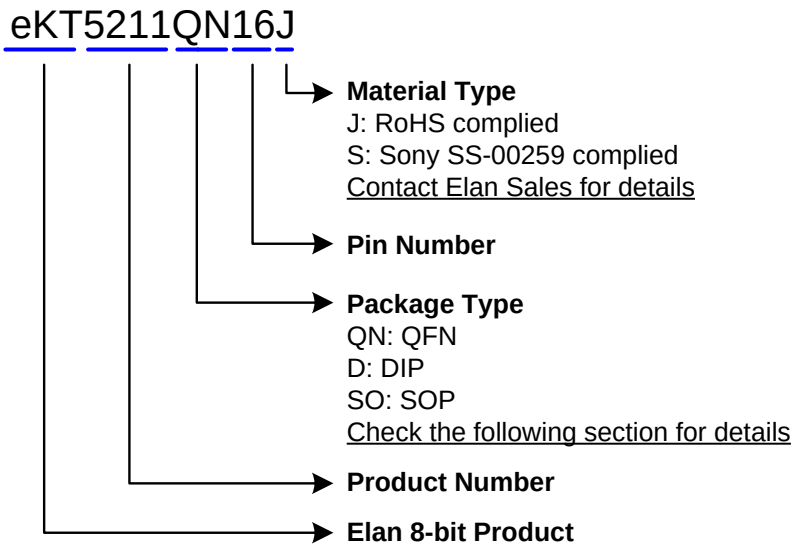
* ***N:*** *Selected prescaler ratio*

NOTE

- *The above parameters are theoretical values only and have not been tested or verified.*
- *Data under the "Min.", "Typ.", and "Max." columns are based on theoretical results at 25°C. These data are for design reference only and have not been tested or verified.*

APPENDIX

A Ordering and Manufacturing Information

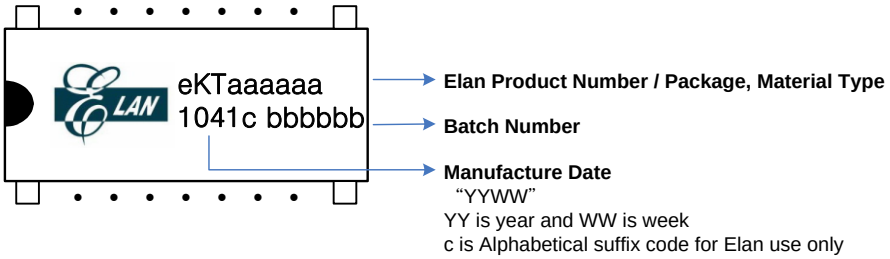


For example:

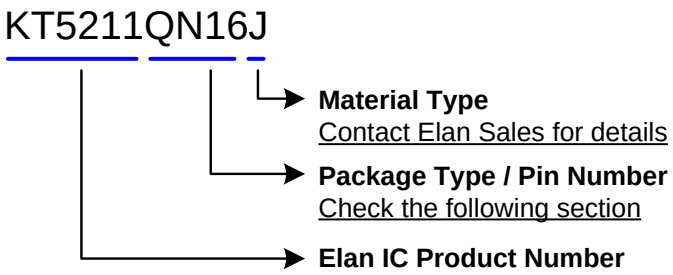
eKT5211D16S

Is eKT5211 with OTP program memory product,
in 16-pin DIP 300mil package with Sony SS-00259 complied

IC Mark



Ordering Code



B Package Type

MCU	Package Type	Pin Count	Package Size
eKT5211QN16	QFN	16 pins	3x3x0.8 mm
eKT5211D16	DIP	16 pins	300 mil
eKT5211SO16A	SOP	16 pins	150 mil

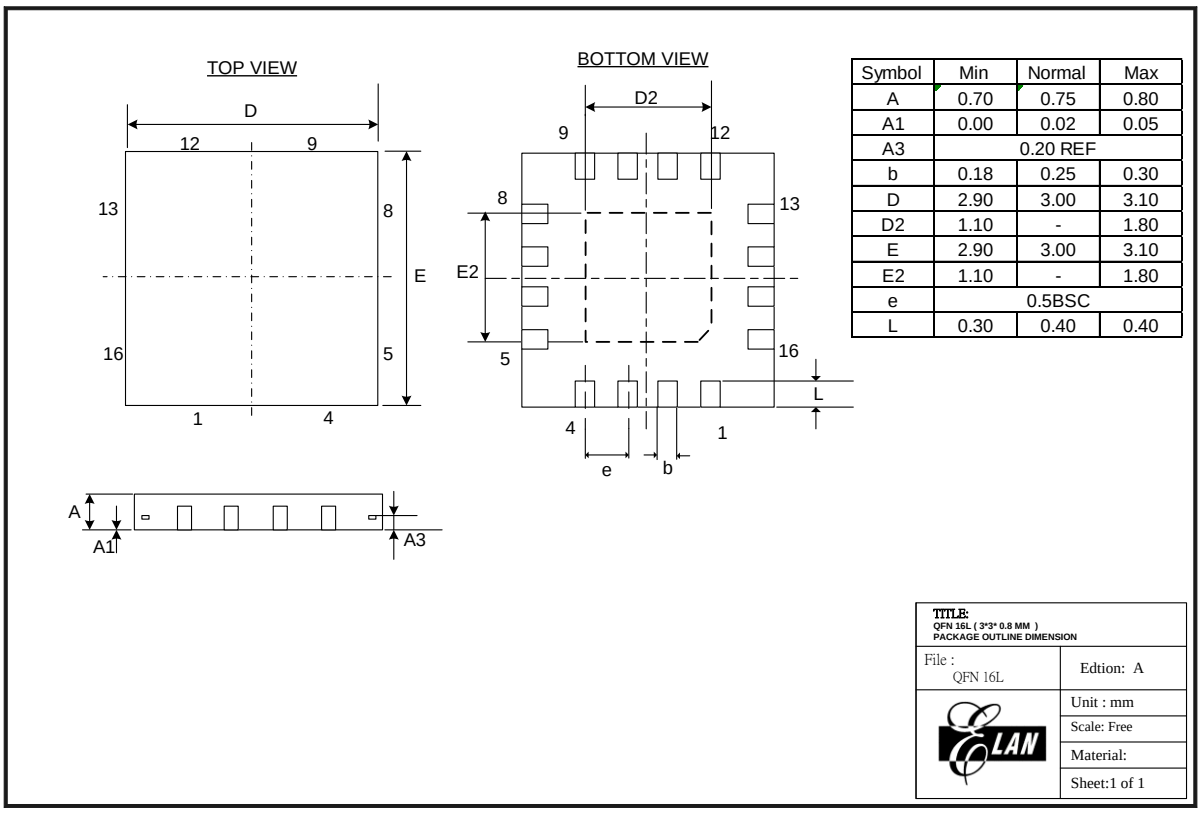
These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

The Pb contents are less 100ppm and comply with Sony specifications.

Part No.	eKT5211J/S
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point (°C)	232°C
Electrical resistivity (μΩ-cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

C Package Information

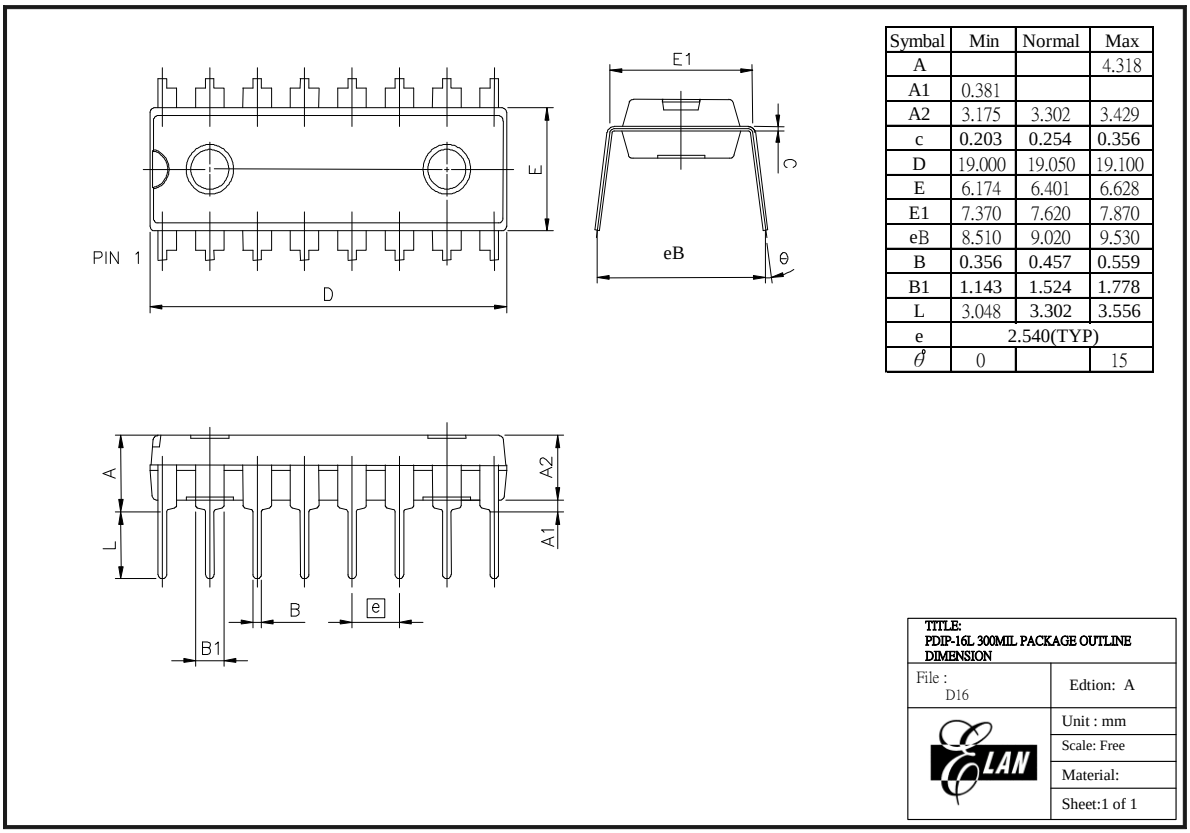
C.1 eKT5211QN16



Symbol	Min	Normal	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D	2.90	3.00	3.10
D2	1.10	-	1.80
E	2.90	3.00	3.10
E2	1.10	-	1.80
e		0.5BSC	
L	0.30	0.40	0.40

Figure C-1 eKT5211 16-pin QFN Package Type

C.2 eKT5211D16

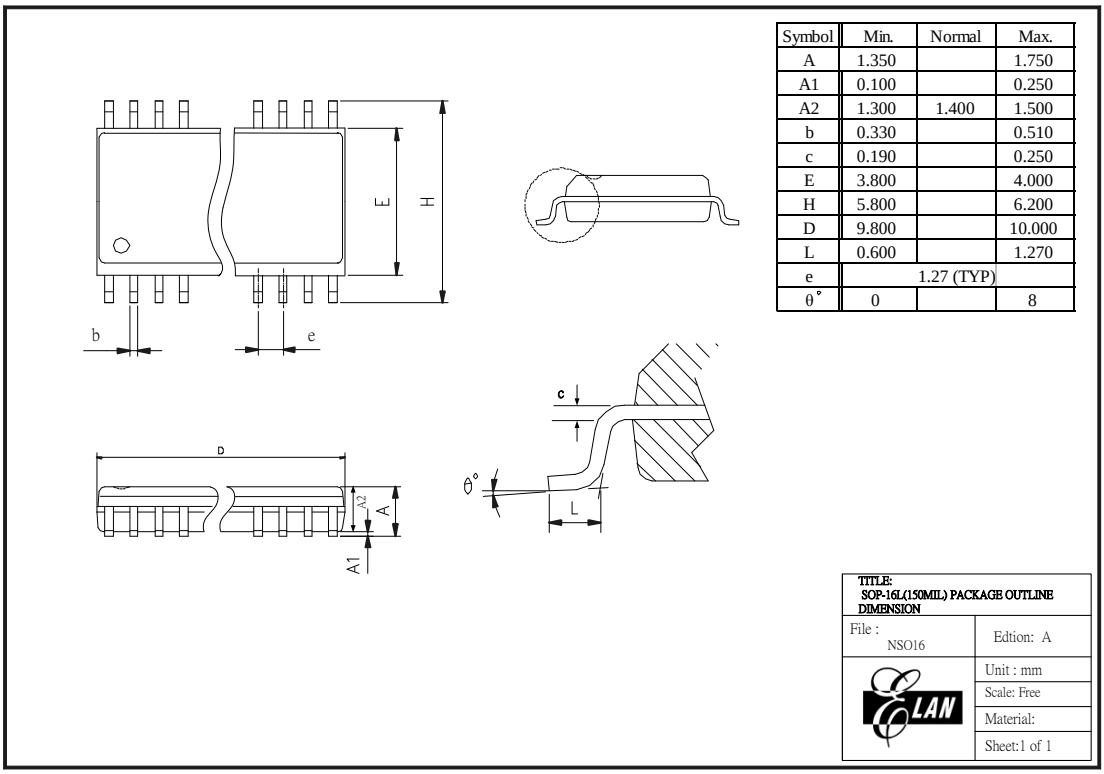


Symbal	Min	Normal	Max
A			4.318
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	19.000	19.050	19.100
E	6.174	6.401	6.628
E1	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

TITLE: PDIP-16L 300MIL PACKAGE OUTLINE DIMENSION	
File : D16	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure C-2 eKT5211 16-pin DIP Package Type

C.3 eKT5211SO16A



Symbol	Min.	Normal	Max.
A	1.350		1.750
A1	0.100		0.250
A2	1.300	1.400	1.500
b	0.330		0.510
c	0.190		0.250
E	3.800		4.000
H	5.800		6.200
D	9.800		10.000
L	0.600		1.270
e	1.27 (TYP)		
θ°	0		8

Figure C-3 eKT5211 16-pin SOP Package Type

D Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245 ± 5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65°C (15 min)~150°C (15 min), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (endurance)=24 hrs	
	Step 3: Soak at 30°C/60%，TD (endurance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5 mm or Pkg volume ≥ 350 mm^3 ----225±5°C) (Pkg thickness ≤ 2.5 mm or Pkg volume ≤ 350 mm^3 ----240 ± 5°C)	
Temperature cycle test	-65°C (15 min)~150°C (15 min), 200 cycles	–
Pressure cooker test	TA =121°C, RH=100%, pressure=2 atm, TD (endurance)= 96 hrs	–
High temperature / High humidity test	TA=85°C , RH=85%，TD (endurance) = 168 , 500 hrs	–
High-temperature storage life	TA=150°C, TD (endurance) = 500, 1000 hrs	–
High-temperature operating life	TA=125°C, VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs	–
Latch-up	TA=25°C, VCC = Max. operating voltage, 150mA/20V	–
ESD (HBM)	TA=25°C, ≥ ｜± 4KV｜	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS (-) mode
ESD (MM)	TA=25°C, ≥ ｜± 400V｜	

D.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.