eAM Series

16 Bits DSP
Sound Processor

Product Specification

DOC. VERSION 1.7

ELAN MICROELECTRONICS CORP.

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Specification Revision History

Doc. Version	Revision Description	Date
1.0	1. Added eAM096, eAM192 and eAM384 2. Modified the Operating Temperature Range in Section 6.2	2006/10/31
1.1	1. Modified the Application Circuits diagram in Section 7 2. Modified the Sampleing Rate Range in Section 4	2007/04/11
1.2	1. Modified the Temperature Range in Section 6.2 2. Modified the Power supply voltage in Section 6.3	2007/08/10
1.3	1. Added package information in Section 4 2. Modified Application Circuit in Section 7	2007/11/10
1.4	1. Modified PWM current in Section 6.3 2. Added PortC DC characteristic in Section 6.3	2008/01/10
1.5	1. Modified Application Circuit diagram in Section 7	2008/10/15
1.6	1. Modified Algorithm-realted information in Section 5	2009/04/15
1.7	1. Modified PC[7:0] pull-up resister in Section 7.3 2. Modified Application Circuit in Section 8	2009/12/1

1 General Description

The ELAN eAM Series IC is a 16-bit DSP Sound Processor with multi-channel speech and instrument playback. It is based on ELAN 16-bit DSP platform. The series has a powerful 16-bit DSP architecture that handles most of the speech and melody functions. Speech and melody can be played back simultaneously. The speech synthesis is implemented by software and supports a wide range of compression bit rates and various volume levels. The ELAN eAM Series provides real instrument waveform to obtain good quality melody. The ELAN eAM peripheral includes ADC, RTC, Timer, WDT, SPI, DAC, PWM, etc.

The ELAN eAM Series IC offer Fast mode, Sleep mode, Green mode, and Slow mode of operation. The use of Green/Slow mode will further reduce the power consumption. Green mode also provides RTC function for wake-up purposes.

The ELAN eAM Series enhanced features make it suitable for versatile voice and sound effect product applications. These enhanced versatile features allow users to create products with a wide variety of new fancy ideas.

The ELAN eAM Series have extreme high performance in melody application based on powerful DSP architecture and good algorithm in audio compression.

2 Features

- MCU
  - 16-bit RISC CPU architecture
  - CPU clock: 20 MHz @ 3.3V
  - Programmable PLL
  - Four CPU operation modes: fast, slow, green, sleep
  - Powerful DSP Instruction Set supports multiplication, division, repeat, loop and soft interrupt instructions
  - Saturation mode is supported for multimedia applications
  - Eight general purpose registers (GPR)
  - 21 interrupt sources with 2-level priority
- Memory
  - 32K-word program memory
  - 2K-word data RAM
  - 096/128/192/256/384/512K-word data ROM
- Peripherals
  - Real Time Clock (RTC) with wake-up function
  - Four 8-bit timers, two general purpose timers, two multiple-function timers
  - 8-bit Watchdog Timer (WDT) with general purpose timer capability

- 40 GPIO + 8 Outputs
- Serial Peripheral Interface (SPI)
- 12-bit Analog to Digital Converter (ADC) with touch panel and MIC inputs

3 Block Diagram

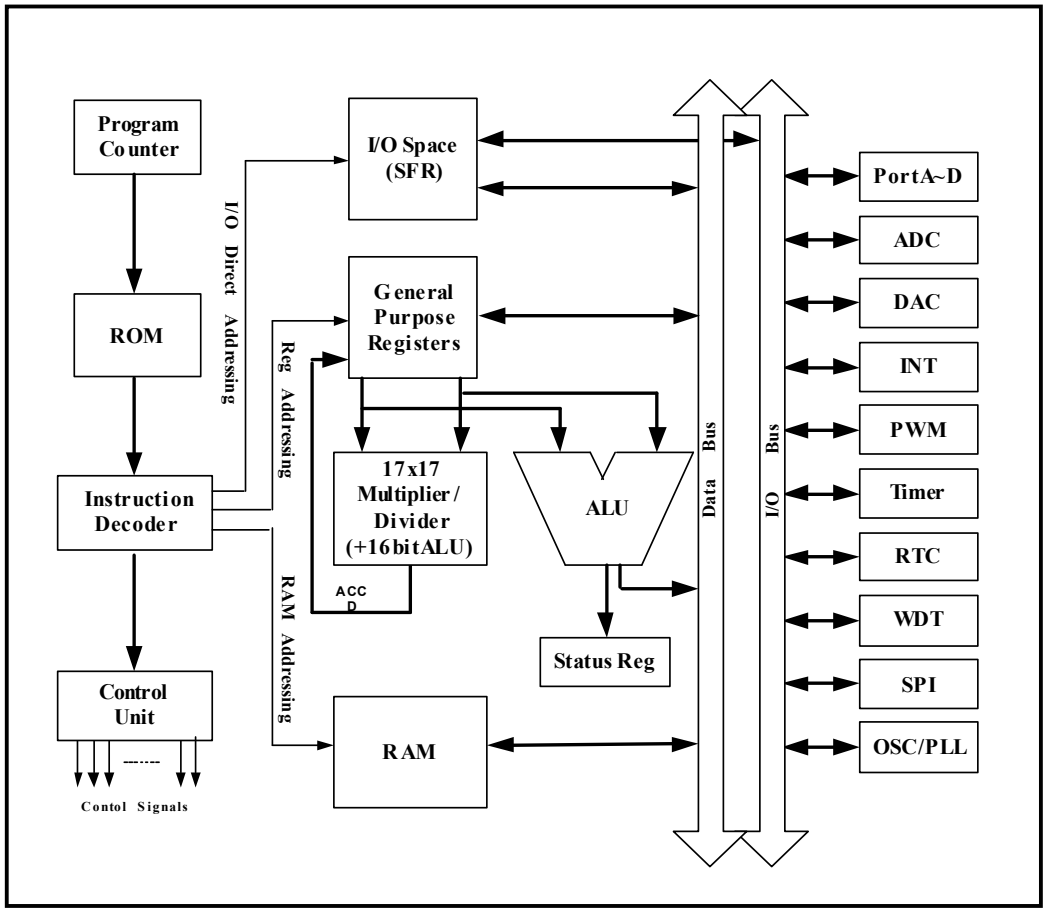


Figure 3-1 ELAN eAM System Block Diagram

4 Selection Table

The ELAN eAM Series integrates an extensive range of features, most of which are common to all devices, except for some distinctive features like Data ROM and Coding Type. For user convenience in the choice of the most suitable product for their application, the following table is provided, which enumerates the main features of each device.

Product No.	eAM096	eAM128	eAM192	eAM256	eAM384	eAM512
Pin Count	81					
Program ROM	32K × 16					
Data RAM	2K ×16					
Data ROM	96K × 16	128K × 16	192K × 16	256K × 16	384K × 16	512K × 16
Timer	4 × 8-bit timers					
Watchdog	Yes					
PWM	10-bit					
A/D Converter	12-bit					
Current D/A	12-bit					
SPI	1 set					
I/O	40 I/O ports + 8 Output ports					

5 Algorithm Selection Table

The ELAN eAM Series algorithm feature

- 12-bit current-steering Digital to Analog Converter (DAC)
- 10-bit resolution Pulse Width Modulation (PWM)
- Multiple flash with volume level option
- Directly controls port output value by waveform (waveform control port)
- Supports mark number in waveform with ROM optimized configuration
- Up to 16-channel melody or 12-channel melody + 4-channel speech

Product No.	eAM096	eAM128	eAM192	eAM256	eAM384	eAM512
Audio*	Up to 16-channel melody or 12-channel melody + 4-channel speech					
Coding Type*	4-bit ADPCM 5-bit ADPCM PCM (96K bps @ 8KHz)					
Sampling Rate Range*	6kHz ~ 48KHz					
Recording	Yes					

* For more detailed information, refer to the Assembler Reference Manual and C Macro Reference Manual.

6 Pin Description

6.1 Power Supply

Name	Type	Supply Voltage	Description
VDD_CPU	P	3V	Positive power supply for CPU, digital peripheral and DRAM
VDD_PM	P	3V	Positive power supply for PROM, DROM and POR
VDD_OSC	P	3V	Positive power supply for Oscillator system and PLL
IOVDD_PWM	P	3V, 5V	Positive power supply for Port D and PWM I/O pad
IOVDD_PB	P	3V, 5V	Positive power supply for Port A.2~15 and Port B I/O pad
IOVDD_PC	P	3V, 5V	Positive power supply for Port C I/O pad
VSS_CPU	P	GND	Negative power supply for CPU, digital peripheral and DRAM
VSS_PM	P	GND	Negative power supply for PROM, DROM and POR
VSS_OSC	P	GND	Negative power supply for Oscillator system and PLL
IOVSS_PWM	P	GND	Negative power supply for Port D and PWM I/O pad
IOVSS_PB	P	GND	Negative power supply for Port A.2~15 and Port B I/O pad
IOVSS_PC	P	GND	Negative power supply for Port C I/O pad
AVDD_AD	P	3V	Positive power supply for A/D and MIC
AVDD_DA	P	3V	Positive power supply for D/A
AVSS_AD	P	GND	Negative power supply for A/D and MIC
AVSS_DA	P	GND	Negative power supply for D/A
VREF	P	3V	External reference voltage input pin for A/D and MIC
RVIN	P	5V	Regulator voltage input
RVOUT	P	3V	Regulator voltage output 3.0V

NOTE

The AVDD_AD, VREF are analog voltage input that need to separate with other digital voltage input to reduce noise issue. For example, you can use on-chip regulator to be the analog voltage source. Or you can refer to development board reference circuit.

6.2 System Control

Name	Type	Description
RSTB	I	RSTB is the low active global reset input *
TEST	I	Test mode select pin (High active). Internal pull down. For chip internal test only, Normally connect to VSS.
OSCI	I	Crystal or RC oscillator connecting pin RC or Crystal selection is by OSCS pin
OSCO	O	Crystal oscillator connecting pin
OSCS	I	RC or Crystal selection: **0** = RC **1** = Crystal
PLLC	I	PLL loop filter capacitor **

* This pin has an internal pull-up 150KΩ resistor, refer to the Application Circuit.

** This pin must connect a 47nF capacitor to ground, please refer to the application circuit.

6.3 DAC Output

Name	Type	Description
DACO	O	Current D/A output pin

6.4 Two-stage Amplifier & Touch Pad Positioning

Name	Type	Description
AMPO	O	Post Amplifier output
MIC	I	Microphone signal input (AC coupling from microphone signal)
AGC	I	Automatic Level Control adjustment pin
Xn	I	Touch Pad positioning for X axis under negative voltage level
Yn	I	Touch Pad positioning for Y axis under negative voltage level
XP/ADIN0	I	Touch Pad positioning for X axis under positive voltage level Analog Input channel 0
YP/ADIN1	I	Touch Pad positioning for Y axis under positive voltage level Analog Input channel 1

6.5 I/O Port

- Port A Attributes and Definitions

Name	Function	Type	Description
PA[0]	GPIO	I/O	General-purpose I/O function
	PWM0	O	PWM Output 0
PA[1]	GPIO	I/O	General-purpose I/O function
	PWM1	O	PWM Output 1
PA[2]	GPIO	I/O	General-purpose I/O function
PA[3]	GPIO	I/O	General-purpose I/O function
PA[4]	GPIO	I/O	General-purpose I/O function
	TEX12	I	External Timer 2 clock input
PA[5]	GPIO	I/O	General-purpose I/O function
	TEX13	I	External Timer 3 clock input
PA [6]	GPIO	I/O	General-purpose I/O function
PA [7]	GPIO	I/O	General-purpose I/O function
PA [8]	GPIO	I/O	General-purpose I/O function
	TCCP2	I/O	Timer 2 capture input or compare output
PA [9]	GPIO	I/O	General-purpose I/O function
	TCCP3	I/O	Timer 3 capture input or compare output
PA [10]	GPIO	I/O	General-purpose I/O function
	EXINT0	I	External Interrupt 0 input
PA [11]	GPIO	I/O	General-purpose I/O function
	EXINT1	I	External Interrupt 1 input
PA [12]	GPIO	I/O	General-purpose I/O function with programmable high current
	/SS	I	SPI function In Slave mode: used as chip select input In Master mode: used as I/O pin with programmable high current
PA [13]	GPIO	I/O	General-purpose I/O function with programmable high current
	MOSI	I/O	SPI function (Master output / Slave input) with programmable high current
PA [14]	GPIO	I/O	General-purpose I/O function with programmable high current
	MISO	I/O	SPI function (Master input / Slave output) with programmable high current
PA [15]	GPIO	I/O	General-purpose I/O function with programmable high current
	SCK	I/O	SPI function with programmable high current In Master mode: used as serial clock output In Slave mode: used as serial clock input

- Port B Attributes and Definitions

Name	Function	Type	Description
PB [7:0]	GPIO	I/O	General-purpose I/O function
		I	Wake-up function with programmable pull-up resistor
PB [15:8]	GPIO	I/O	General-purpose I/O function
		I	Wake-up function with programmable pull-up resistor

- Port C Attributes and Definitions

Name	Function	Type	Description
PC [1:0]	GPIO	I/O	General-purpose I/O function
		I	Input with programmable pull-up resistor
PC [7:2]	GPIO	I/O	General-purpose I/O function
			Input with programmable pull-up resistor
	ADIN2~7	I	Analog Input channels

Note: Port C [7:2] is pin-shared with ADC input. There is no **Schmitt Trigger Input** when input is from Port C [7:2]

- Port D Attributes and Definitions

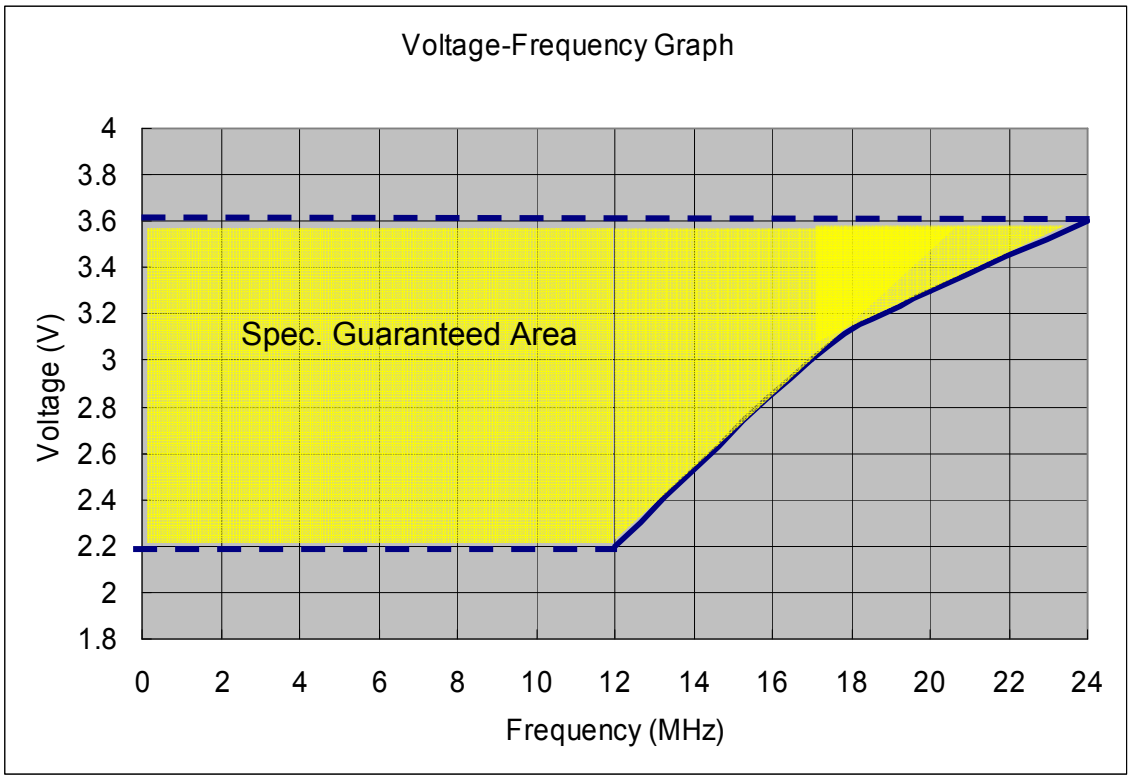
Name	Function	Type	Description
PD [0]	GPO	O	General-purpose output function with high drive current (1 * Tg delay) *
PD [1]	GPO	O	General-purpose output function with high drive current (5 * Tg delay) *
PD [2]	GPO	O	General-purpose output function with high drive current (2 * Tg delay) *
PD [3]	GPO	O	General-purpose output function with high drive current (6 * Tg delay) *
PD [4]	GPO	O	General-purpose output function with high drive current (3 * Tg delay) *
PD [5]	GPO	O	General-purpose output function with high drive current (7 * Tg delay) *
PD [6]	GPO	O	General-purpose output function with high drive current (4 * Tg delay) *
PD [7]	GPO	O	General-purpose output function with high drive current (8 * Tg delay) *

* *Tg = 4 nano-second for low noise design consideration*

7 Electrical Characteristics

7.1 CPU Voltage – Frequency Graph

The speed of a MOS device depends on voltage, temperature, and process variation. Performance analysis is based on a combination of these three factors. The central operating condition is characterized at 3.3V, 25°C, and typical process parameters.



7.2 Absolute Maximum Ratings

Parameter	Pins	Symbol	Condition	Rated Value	Unit
Power supply voltage	VDD	V_{DD}	T_A=25°C	-0.3 to +6.0	V
Input voltage	All Input	V_{IN}	T_A=25°C	-0.3 to VDD+0.3	
Operating temperature range	—	T_A	—	-40 to +85	°C
Storage temperature range	—	T_{STR}	—	-65 to +150	

7.3 DC Characteristics

Standard operation conditions: VDD = 3V, GND=0V, T_A = 25°C

Parameter	Pins	Symbol	Condition	Rated Value			Unit
				Min.	Typ.	Max.	
Power supply voltage	VDD[1]	V_{DD}	2 batteries	2.2	3.0	3.6	V
			3 batteries	3.6	4.5	5.5	
Input voltage	—	V_{IN1}	—	VDD×0.7	—	VDD	
	—	V_{IN2}	—	0	—	VDD×0.3	
Input threshold voltage (Schmitt Trigger)	—	—	—	0.5×VDD	—	0.75×VDD	
	—	—	—	0.2×VDD	—	0.4×VDD	
Pull-up resistor	PC [7:0]	V_{PU0L}	Vin=GND	50	100	150	kΩ
	/RESET	V_{PU1L}	Vin=GND	500	1000	1500	
	/RESET	V_{PU1H}	Vin=2V	80	100	120	
Pull-down resistor	TEST	R_{PD}	Vin=1V	80	100	120	

[1] Refer to the User Manual Voltage Regulator section for details.

Parameter	Pins	Symbol	Condition	Rated Value			Unit
				Min.	Typ.	Max.	
Ports A,B,C output high current	IOH0	IOH0	VDD=3V VOH=2.4V	-2	-3	—	mA
Ports A,B,C output low current	IOL0	IOL0	VDD=3V VOL=0.4V	2	3	—	
Port D output high current	IOH1	IOH1	VDD=3V VOH=2.4V	-7	-10	—	
Port D output low current	IOL1	IOL1	VDD=3V VOL=0.4V	7	10	—	
Port A[12:15] high current (HD enabled)	IOH2	IOH2	VDD=3V VOH=2.4V	-7	-10	—	
Port A[12:15] low current (HD enabled)	IOL2	IOL2	VDD=3V VOL=0.4V	7	10	—	
PWM output high current	PWM0 PWM1	IPWML	VDD=3V VOL=VDD/2 Max volume	-140	-150	—	
PWM output low current	PWM0 PWM1	IPWMH	VDD=3V VOL=VDD/2 Max volume	140	150	—	
DAC output current	DACO	IDAC	VDD=2.2 ~ 3.3V	2.5	3	—	
Regulator output current	RVOUT	IOUT	RVIN=4.5V RVOUT=3.0V Fast, Slow mode	70	—	—	
			RVIN = 4.5V RVOUT = 3.0V Green, Sleep mode	7	—	—	
Fast mode current consumption increment per MHz	—	IFAST	VDD=3V No load DAC off	—	700	800	µA
Slow mode current consumption	—	ISLOW	VDD=3V No load DAC off	—	70	80	
Green mode current consumption	—	IGREEN	VDD=3V	—	8	10	
Sleep mode current consumption	—	ISLEEP	VDD=3V Regulator on	—	1.5	2	
			VDD = 3V Regulator off	—	1	1.2	
CPU operation frequency	—	Fsys	VDD = 3V	14	16	—	MHz

8 Application Circuits

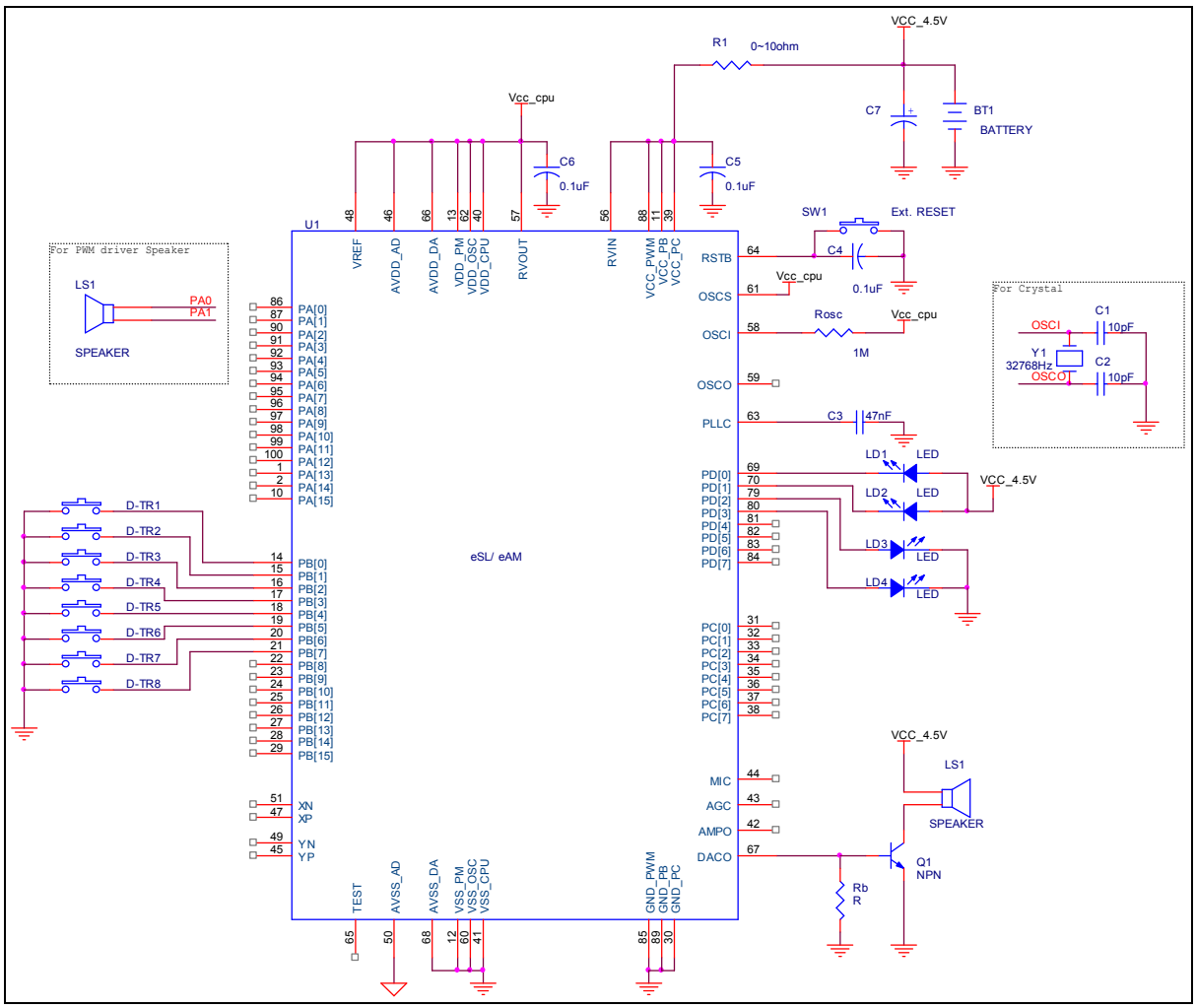


Figure 8-1 ELAN eAM Series with 4.5V No ADC Application Circuit Diagram

NOTE

The AVDD_AD, VREF are analog voltage input that need to separate with other digital voltage input to reduce noise issue. For example, you can use on-chip regulator to be the analog voltage source. Or you can refer to development board reference circuit.

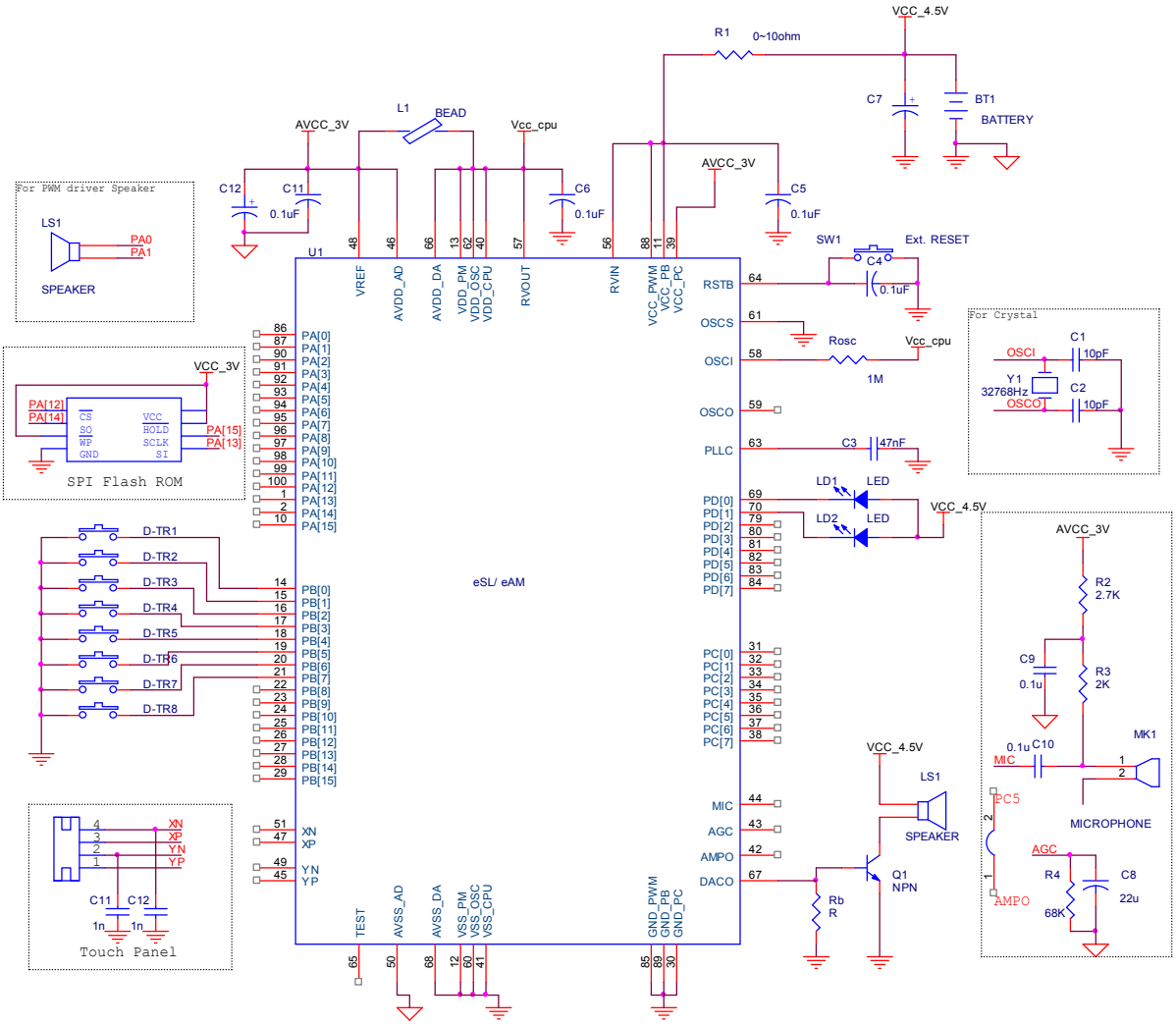


Figure 8-2 ELAN eAM Series Application Circuit Diagram with A/D, D/A using BJT, SPI and PWM for 4.5V Support

NOTE

The AVDD_AD, VREF are analog voltage input that need to separate with other digital voltage input to reduce noise issue. For example, you can use on-chip regulator to be the analog voltage source. Or you can refer to development board reference circuit.

NOTE

For different package type, the system characteristic issue such as power consumption due to IO pad floating must controlled by software. For example, if user don't bonding IO pad, you must set IO pad type is input with pull-up resister or output to prevent power consumption.