apm6998 WiFi 802.11b/g/n Single System Module

DESCRIPTION

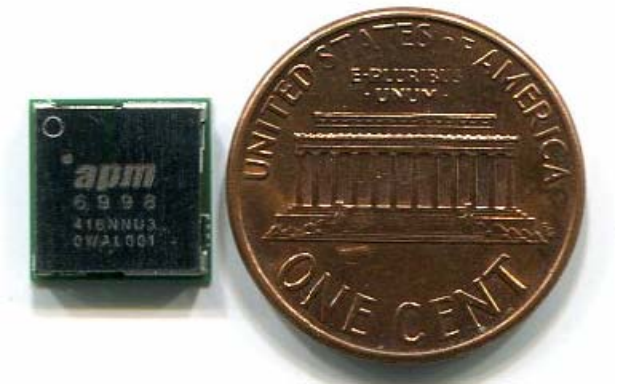
With a small form factor of 9.6×9.6×1.8mm (max.), the apm6998 is a full-featured 802.11b/g/n WiFi single system module that includes support for high linear output power, IEEE 802.11i security, IEEE 802.11e QoS, and hard-wired WiFi-Bluetooth co-existence. By providing SDIO (1-bit, 4-bit, and SPI) host interface combined with support for WinCE and Linux operating systems, the apm6998 enables rapid integration of WiFi technology into a variety of host devices. The pre-tested module eliminates the need to create custom WLAN designs, resulting in greatly reduced development risk, costs and time-to-market.

FEATURES

- Small footprint: 9.6×9.6×1.8mm (max.)
- IEEE 802.11b/g/n compliant
- Frequency band: 2.4 to 2.472GHz (1 to 13 channels)
- 11b data rates: 1, 2, 5.5, 11 Mbps
- 11g data rates: 6, 9, 12, 18, 24, 36, 48, and 54 Mbps
- 11n data rates: CS0-7, 400/800ns 72.2, 65, 58.5, 57.8, 52, 43.3, 39, 28.9, 26, 21.7, 19.5, 14.4, 13, 7.2, 6.5Mbps
- Modulation: DSSS (CCK, DQPSK, DBPSK) and OFDM (BPSK, QPSK, 16QAM, 64QAM)
- Host interface:
  - SDIO: SDIO 1-bit, SDIO 4-bit, SDIO/SPI
- Support for IEEE 802.11e QoS
- Support for IEEE 802.11i advanced security
- Multiple power saving modes to maximize battery
- GSM/GPRS/DCS/PCS/WCDMA/GPS radio non-interference
- Immune from EM interference with metal shielding
- EEPROM, PA, and full RF front end integrated
- Embedded OS supported
- RoHS complaint

APPLICATIONS

- WiFi plug-in modules for non-wireless systems
- Smartphone / PDA / PDA phone / WiFi phone / DSC / DVC with WiFi connectivity
- Printer Server / Multifunctional peripheral with WiFi connectivity



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REVISION HISTORY

Date	Release	Author	Description
28-Mar-14	0.1	Sky	Initial release

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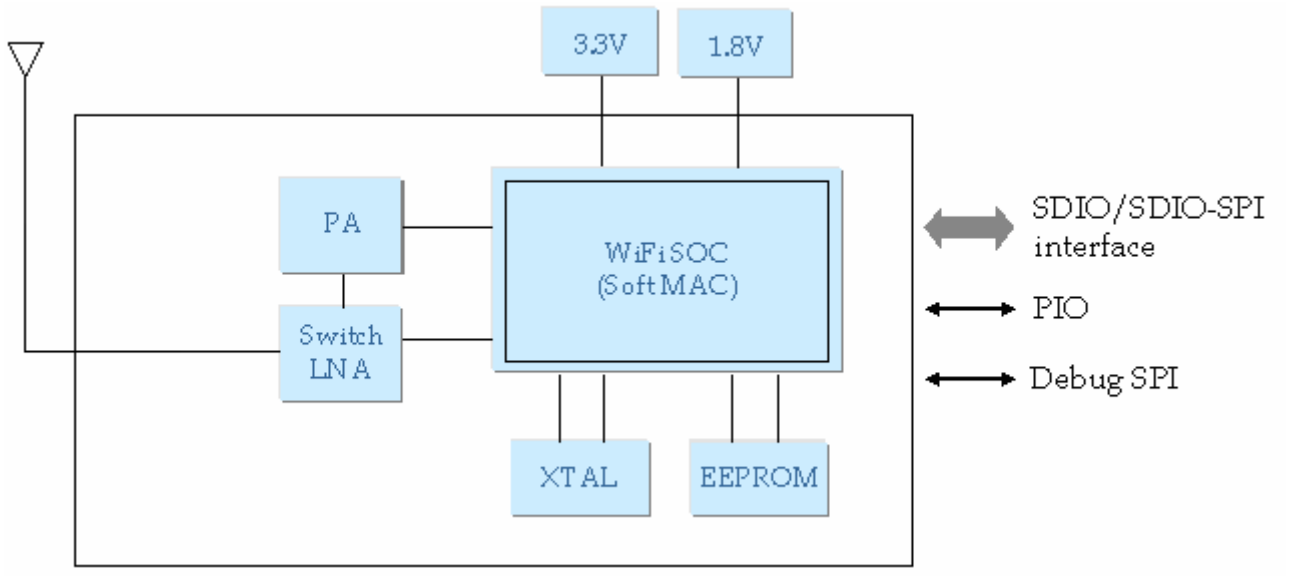
1 Hardware Specification

1-1 General Specification

Network Standard	IEEE 802.11b/g/n Compliant
Host Interface	SDIO v1.0: SDIO 1-bit, SDIO 4-bit, SDIO/SPI
Frequency Band	2400 to 2472MHz (1 to 13 channels)
Data Transfer Mode	OFDM & DSSS
Modulation	64QAM (MCS0-7, 400/800ns 72.2, 65, 58.5, 57.8, 52, 43.3, 39, 28.9, 26, 21.7, 19.5, 14.4, 13, 7.2, 6.5Mbps), 64QAM (54, 48Mbps), 16QAM (36, 24Mbps), QPSK (18, 12Mbps), BPSK (9, 6Mbps); CCK (11, 5.5 Mbps), DQPSK (2 Mbps), DBPSK (1Mbps). STBC reception for MCS0-7
Access Method	Ad hoc mode, Infrastructure mode
Media Access Protocol	CSMA/CA (Carrier Sense Multiple Access with Collision Avoidance)
Antenna	External single antenna support. The output impedance is 50Ω.

1-2 Block Diagram



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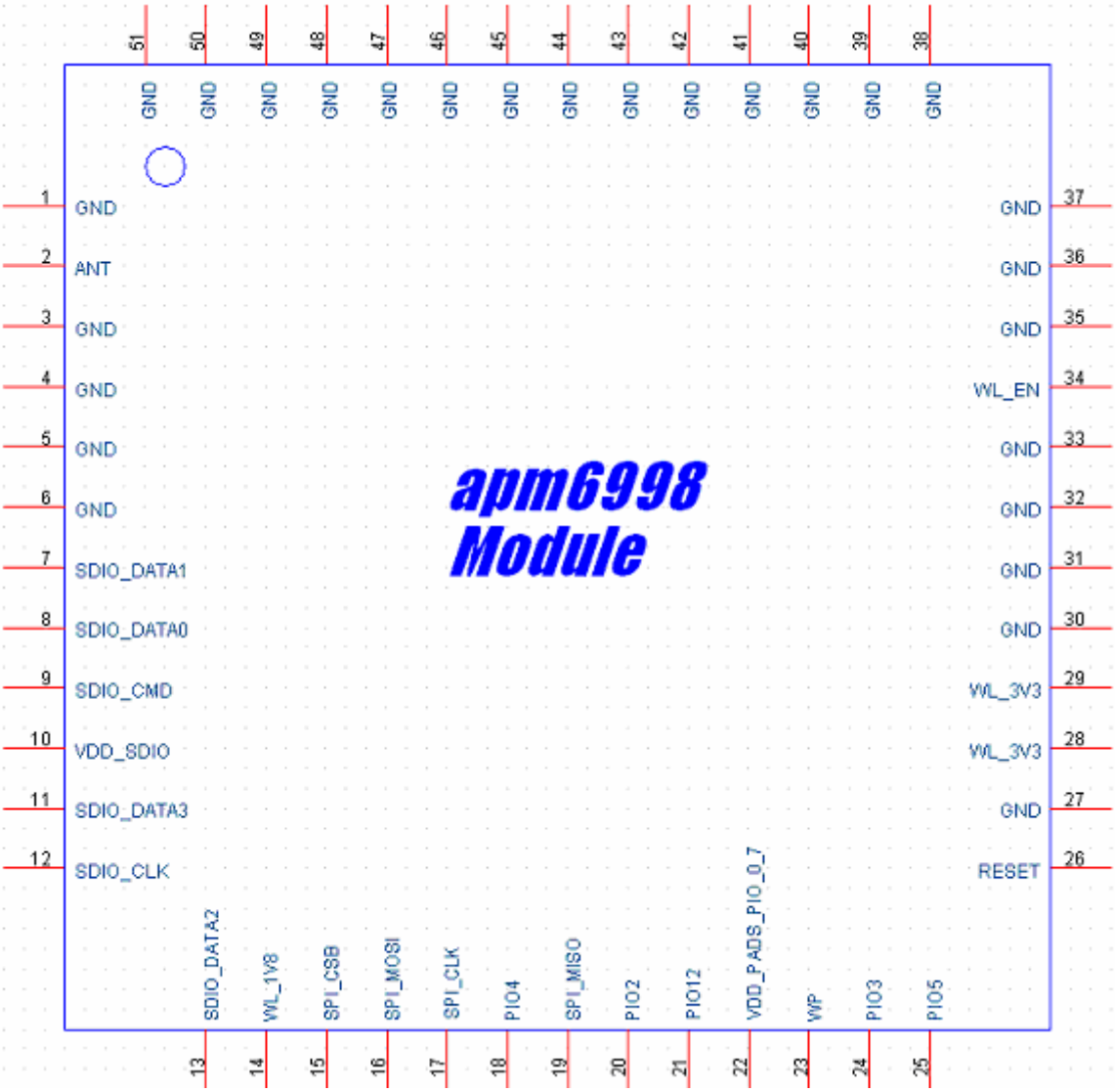
1-3 Pinout

1-3-1 Pin Assignment (Top View)



1-3-2 Pin Description

* I/O: Digital Input/Output, I: Digital Input, O: Digital Output, A: Analog

#	Name	I/O	Description
1	GND	GND	Ground.
2	ANT	A	RF input/output
3	GND	GND	Ground.
4	GND	GND	Ground.

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#	Name	I/O	Description
5	GND	GND	Ground.
6	GND	GND	Ground.
7	SDIO_DATA[1]	I/O	SDIO 4-bit mode: Data line [bit 1] or interrupt. SDIO 1-bit mode: Interrupt. CSPI mode : Intrrupt.
8	SDIO_DATA[0]	I/O	LSB data bit for SDIO interface. SDIO 4-bit mode: Data line [bit 0] SDIO 1-bit mode: Data line. CSPI mode: Data output.
9	SDIO_CMD	I	SDIO 4-bit mode. Command/Response. SDIO 1-bit mode. Command/Response. CSPI mode: Data input.
10	VDD_SDIO	Power	Power supply for SDIO interface level voltage.
11	SDIO_DATA[3]	I/O	SDIO 4-bit mode: Data line [bit 3] SDIO 1-bit mode: Reserved. CSPI mode: Card Select.
12	SDIO_CLK	I	SDIO 4-bit mode: Clock. SDIO 1-bit mode: Clock. CSPI mode : Clock.
13	SDIO_DATA[2]	I/O	SDIO 4-bit mode: Data line [bit 2] or Read wait (optional) SDIO 1-bit mode: Read Wait (optional) SDIO SPI mode: Reserved.
14	WL_1V8	Power	Power supply for analogue/digital voltage regulator.
15	SPI_CSB	I	Debug SPI chip select, active low.
16	SPI_MOSI	I	Debug SPI data input.
17	SPI_CLK	I	Debug SPI clock.
18	PIO[4]	I/O	Programmable input/output.
19	SPI_MISO	O	Debug SPI data output.
20	PIO[2]	I/O	Programmable input/output.
21	PIO[12]	I/O	Programmable input/output (support Host wakeup)
22	VDD_PADS_PIO_0_7	Power	Power supply for SPI, EEPROM, RST# and PIO[0]-PIO[7]
23	WP	I	Write protection for internal EEPROM.
24	PIO[3]	I/O	Programmable input/output.
25	PIO[5]	I/O	Programmable input/output.
26	RESET	I	Reset, active low.

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#	Name	I/O	Description
27	GND	GND	Ground.
28	WL_3V3	Power	Power supply for PIO[12] and PA
29	WL_3V3	Power	Power supply for PIO[12] and PA
30	GND	GND	Ground.
31	GND	GND	Ground.
32	GND	GND	Ground.
33	GND	GND	Ground.
34	WL_EN	Power	Enable for all voltage regulators.
35	GND	GND	Ground.
36	GND	GND	Ground.
37	GND	GND	Ground.
38	GND	GND	Ground.
39	GND	GND	Thermal Ground.
40	GND	GND	Thermal Ground.
41	GND	GND	Thermal Ground.
42	GND	GND	Thermal Ground.
43	GND	GND	Thermal Ground.
44	GND	GND	Thermal Ground.
45	GND	GND	Thermal Ground.
46	GND	GND	Thermal Ground.
47	GND	GND	Thermal Ground.
48	GND	GND	Thermal Ground.
49	GND	GND	Thermal Ground.
50	GND	GND	Thermal Ground.
51	GND	GND	Thermal Ground.

1-4 WiFi Pins

1-4-1 SDIO Pins

apm6998 supports a SDIO device interface that conforms to the industry standard SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access apm6998.

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SDIO Bus Name	Pin #	Pin Name	Description
DAT3	11	SDIO_DAT[3]	SDIO Data 3
DAT2	13	SDIO_DAT[2]	SDIO Data 2
DAT1	7	SDIO_DAT[1]	SDIO Data 1
DAT0	8	SDIO_DAT[0]	SDIO Data 0
CMD	9	SDIO_CMD	SDIO Command
CLK	12	SDIO_CLK	SDIO Clock

1-4-2 CSPI Pins

SDIO port is available on host platform, apm6998 supports a SD-SPI device interface that connects to Synchronous Serial Port (SSP) pins on Marvell PXA platform or the similar interfaces on other host platforms.

The SD-SPI bus has weak internal pull up resistors on chip.

SD-SPI Name	Pin #	Pin Name	Description
CS	11	SDIO_DAT[3]	Card Select
IRQ	7	SDIO_DAT[1]	Interrupt
DO	8	SDIO_DAT[0]	Data output
DI	9	SDIO_CMD	Data input
SCLK	12	SDIO_CLK	Clock

1-4-3 Debug SPI Pins

apm6998 has a SPI interface for test and debugging purposes. The lab tools, such as UniTest and UniPSUtil, can communicate with apm6998 WiFi part using the SPI protocol over a connection to an LPT port.

Debug SPI Name	Pin #	Pin Name	Description
MISO	19	SPI_MISO	Debug SPI data output
MOSI	16	SPI_MOSI	Debug SPI data input
CLK	17	SPI_CLK	Debug SPI clock
CSB	15	SPI_CSB	Debug SPI chip select, active low

1-4-4 PIO Pins

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The PIO pins are used to implement user defined input and output signals to and from the module such as external interrupts and other user-defined I/Os. Each PIO can be independently controlled.

- WL_PIO[12]: Host wakeup.
- WL_PIO[2:3:4:5]: BT Co-existence
- Other PIOs: Reserved

1-4-5 WP Pin

WL_WP is write protection for internal EEPROM. The internal EEPROM stores calibration table, MAC address, etc. for WiFi part. When the pin is pulled high, it protects the EEPROM content. If tied to VSS, normal memory read/write operation is enabled.

The WiFi firmware does not incorporate any support for writing to the EEPROM during normal operation. This significantly reduces the risk of spurious writes corrupting the contents of the EEPROM, and means it is not possible to repair any damage that may occur. Hence, it is suggested that keep the pin, WL_WP, permanently pulled high to minimize the risk of data corruption.

1-5 External Voltage Source

The external supply rails to apm6998 should have less than 10mV rms noise levels between 0 to 10 MHz. Single tone frequencies are also to be avoided. Transient response of external regulators used should be <= 5us.

Supply voltage range	
1.8V	1.8V +/-5% (ripple Vpp<10mV rms)
3.3V	3.3V +/-5% (ripple Vpp<10mV rms)

1-5-1 Reset Pin

WL_RESETn is an active low reset input that is internally filtered using the internal low frequency clock oscillator to avoid spurious resets. A reset occurs after the signal has been asserted for between 250 and 375us. This pin may be tied to WL_3V3 if unused; otherwise it should be asserted for at least 1ms to force a reset.

The power supply supervisor monitors WL_VDD_CORE (internal module voltage) to trigger a power-on-reset. This occurs when the supply falls below 1.05V (typical) in normal operation or 0.825V (typical) in deep sleep, and ends when the supply exceeds 1.10V (typical). Glitches of up to 30mV and 2.5us duration, which could be caused by large load steps, will not trigger a reset.

Each of the internal processors has its own independent watchdog timer to detect and recover from erroneous

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software operation. These are typically configured with a timeout of 1.5s, but this may be increased up to a maximum of 64s for reduced power consumption. The watchdogs are enabled at power-on and continue operating while WiFi is in deep sleep.

During all forms of reset most digital I/O pins (including both bidirectional pins and dedicated inputs or outputs) default to high impedance with weak internal pull-downs. The only exceptions are WL_RESETn and WL_SPI_CS which both have pull-ups, and the SDIO/CSPI bus which is on an independent reset domain. The SDIO/CSPI host interface is only fully reset by the WL_RESETn pin or the power supply supervisor; other forms of reset leave the host interface initialized but simply clear the I/O Enable bit for function 1.

Following a reset, WiFi automatically generates safe clocks for internal use. If an external reference clock is connected to WL_CLK then this is assumed to be at the maximum supported frequency, otherwise the PLL free runs at a nominal frequency. In either case the generated clock will be slower than in normal operation, but this is sufficient for safely booting and configuring the IC.

Power-on Reset	Min	Typ	Max	Units
Reset release on WL_VDD_DIG rising (HI)	1.05	-	1.15	V
Reset assert on WL_VDD_DIG falling (LO)	HI-0.060	-	HI-0.045	V
Reset assert on WL_VDD_DIG falling (Sleep mode)	0.80	0.825	0.85	V

1-6 Electrical Specifications

1-6-1 Absolute Maximum Rating

Symbol	Description	Min.	Max.	Units
T_{ST}	Storage temperature	-40	+85	°C
WL_3V3	Power supply for PIO[12], SDIO and PA	+2.7	+3.6	V
WL_1V8	Power supply for analogue/digital voltage regulator	+1.7	+2.0	V
WL_EN	Enable for all voltage regulators.	+1.7	+2.0	V
VDD_PADS_PIO_0_7	Power supply for SPI, EEPROM, RST# and PIO[2]-PIO[7]	+1.7	+3.6	V

1-6-2 Recommended Operating Conditions

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Symbol	Description	Min.	Typ.	Max.	Units
T_{OP}	Operating temperature	-40	+25	+85	°C
WL_3V3	Power supply for PIO[12], SDIO interface and PA	+3.2	+3.3	+3.6	V
WL_1V8	Power supply for analogue/digital voltage regulator	+1.45	+1.8	+2.0	V
VDD_PADS	Power supply for SPI, EEPROM, RST# and PIO[2]-PIO[7]	+1.7	+1.8/+3.3	+3.3	V

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1-7 RF Specification

1-7-1 Operating frequency

Item	Min	Max	Unit
Support Channel	1	13	Channel Numbers
Center Frequency	2412	2472	MHz

1-7-2 Transmitter and Receiver RF Specification

Conditions: WL_3V3=VDD_PADS_PIO_0_7=+3.3V, WL_1V8=+1.8V, T_{OP}=25°C

Parameter	Test conditions	Min.	Typ.	Max	Units
802.11b Transmit					
Operating frequency range			Ch1 ~ Ch13		-
Transmit output power	1/2/5.5/11Mbps	15.5	17	18.5	dBm
Center frequency tolerance		-	+5	-	ppm
ACPR: 1st side lobe power	Pout=+17.0dBm, 1/2/5.5/11Mbps	-	-42	-	dBc
ACPR: 2nd side lobe power	Pout=+17.0dBm, 1/2/5.5/11Mbps	-	-58	-	dBc
Transmit EVM	11Mbps, Channel 1~13	-	8	-	%
Transmit ramp-up time	10% ~ 90%	-	0.8	-	µs
Transmit ramp-down time	10% ~ 90%	-	1	-	µs
802.11b Receive					
Minimum input level sensitivity	11Mbps CCK, FER<8% at PSDU length of 1024 bytes	-	-88	-	dBm
Maximum input level capability	11Mbps CCK, FER<8% at PSDU length of 1024 bytes	-	+5	-	dBm
802.11g Transmit					
Operating frequency range			Ch1 ~ Ch13		-
Transmit output power	54Mbps OFDM	12.5	14	15.5	dBm
Center frequency tolerance	54Mbps OFDM	-	+5	-	ppm
Symbol clock freq. tolerance	54Mbps OFDM	-	+4	-	ppm
Transmit EVM	54Mbps OFDM, Channel 1~13	-25	-	-	dB
Transmit ramp-up time	10% ~ 90%	-	0.8	-	µs
Transmit ramp-down time	10% ~ 90%	-	1	-	µs

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Parameter	Test conditions	Min.	Typ.	Max	Units
802.11g Receive					
Receive minimum input level sensitivity	54Mbps OFDM, FER<10% at PSDU length of 1024 bytes	-	-72	-	dBm
Receive maximum input level capability	54Mbps OFDM, FER<10% at PSDU length of 1024 bytes	-	-13	-	
802.11n 20MHz Transmit					-
Operating frequency range			Ch1 ~ Ch13		
Transmit output power	MCS7	10.5	12	13.5	dBm
Transmit modulation accuracy	MCS7	-	-	-	ppm
Symbol clock frequency tolerance	MSC7	-	+5	-	ppm
Transmit center frequency tolerance	MCS7	-	+2	-	dBr
Spectrum Mask	f < fc-30, fc+30 <f	-	-49	-	dBr
	fc-30 <f <fc-20, fc+20 <f <fc+30		-42		dBr
	fc-20 <f <fc-11, fc+11 <f <fc+20	-	-31	-	dBr
	fc-11 <f <fc-9, fc+9 <f <fc+11	-	-15	-	
802.11n 20MHz Receive					dBm
Receive minimum input level sensitivity	MCS7 (FER<10% at PSDU length of 1024 bytes)	-	-68	-	dBm
Receive maximum input level capability	MSC7 (FER<10% at PSDU length of 1024 bytes)	-	-17	-	dBm

1-8 Current Consumption

Conditions: WL_1V8= = +1.8V, WL_3V3=VDD_PADS=+3.3V, T_{OP}= 25°C

Parameter	Test conditions	Min.	Typ.	Max.	Units
802.11b Current Consumption					
11Mbps transmit@17 ±1.5dBm	Continuous packet, PSDU length of 1024 Bytes (958us), packet interval 50μs	-	221/ 3V3 120/ 1V8	-	mA
11Mbps receive	-85dBm.Continuous packet, PSDU	-	10/ 3V3	-	mA

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Parameter	Test conditions	Min.	Typ.	Max.	Units
	length of 1024 Bytes, packet interval 50µs		133/ 1V8		
802.11g Current Consumption					
54Mbps transmit@14 ±1.5dBm	Continuous packet, PSDU length of 1024 Bytes (179us), packet interval 117µs	-	123/ 3V3 127/ 1V8	-	mA
54Mbps receive	-70dBm. Continuous packet, PSDU length of 1024 Bytes, packet interval 50µs	-	10/ 3V3 141 /1V8	-	mA
802.11n Current Consumption					
MCS7 transmit@12 ±1.5dBm	Continuous packet, PSDU length of 4096 Bytes	-	120/ 3V3 130/ 1V8	-	mA
MCS7 receive	-68dBm. Continuous packet, PSDU length of 4096 Bytes	-	10/ 3V3 130/ 1V8	-	mA
Listen	Receive but no OFDM/CCK packet in air	-	10/3V3 140/1V8	-	mA
Sleep Current Consumption					
Deep sleep		-	13/3V3 75/1V8	-	uA

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2 Software Specification

2-1 OS Support & Available Drivers

- SDIO 4-bit
  - Linux 2.6.24 to 3.x.x or above
  - Android
  - RTOS

2-2 Security Features Supported

- Support for IEEE 802.11i security enhancements
  - WEP
  - TKIP
  - AES
  - WPA
  - WPA2
  - WAPI

2-3 Other Features

- Support for IEEE 802.11d transmit power control (Regulatory Domain Support for New Countries)
- Support for IEEE 802.11e (Quality of Service): WMM and WMM Power Save
- Host wakeup signaling

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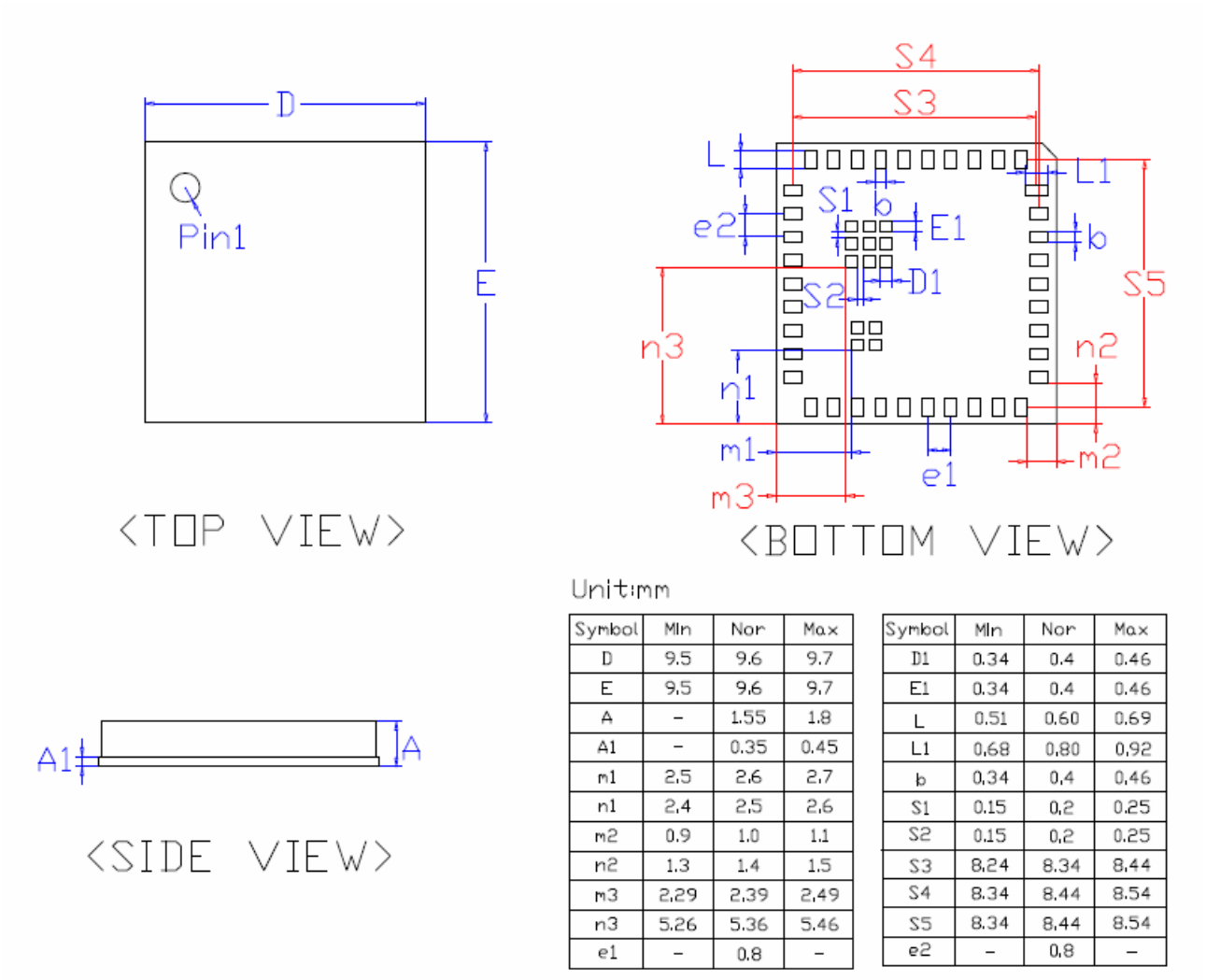
3 Mechanical Specification

Dimension	9.6×9.6×1.8mm. (max. height)
Pinout	51
Weight	TBD
Antenna	External antenna support (Pin 1)

3-1 Package Outline



Unit:mm

Symbol	Min	Nor	Max
D	9.5	9.6	9.7
E	9.5	9.6	9.7
A	-	1.55	1.8
A1	-	0.35	0.45
m1	2.5	2.6	2.7
n1	2.4	2.5	2.6
m2	0.9	1.0	1.1
n2	1.3	1.4	1.5
m3	2.29	2.39	2.49
n3	5.26	5.36	5.46
e1	-	0.8	-

Symbol	Min	Nor	Max
D1	0.34	0.4	0.46
E1	0.34	0.4	0.46
L	0.51	0.60	0.69
L1	0.68	0.80	0.92
b	0.34	0.4	0.46
S1	0.15	0.2	0.25
S2	0.15	0.2	0.25
S3	8.24	8.34	8.44
S4	8.34	8.44	8.54
S5	8.34	8.44	8.54
e2	-	0.8	-

* All detailed specifications including pinouts and electrical specifications may be changed apmcomm without notice.

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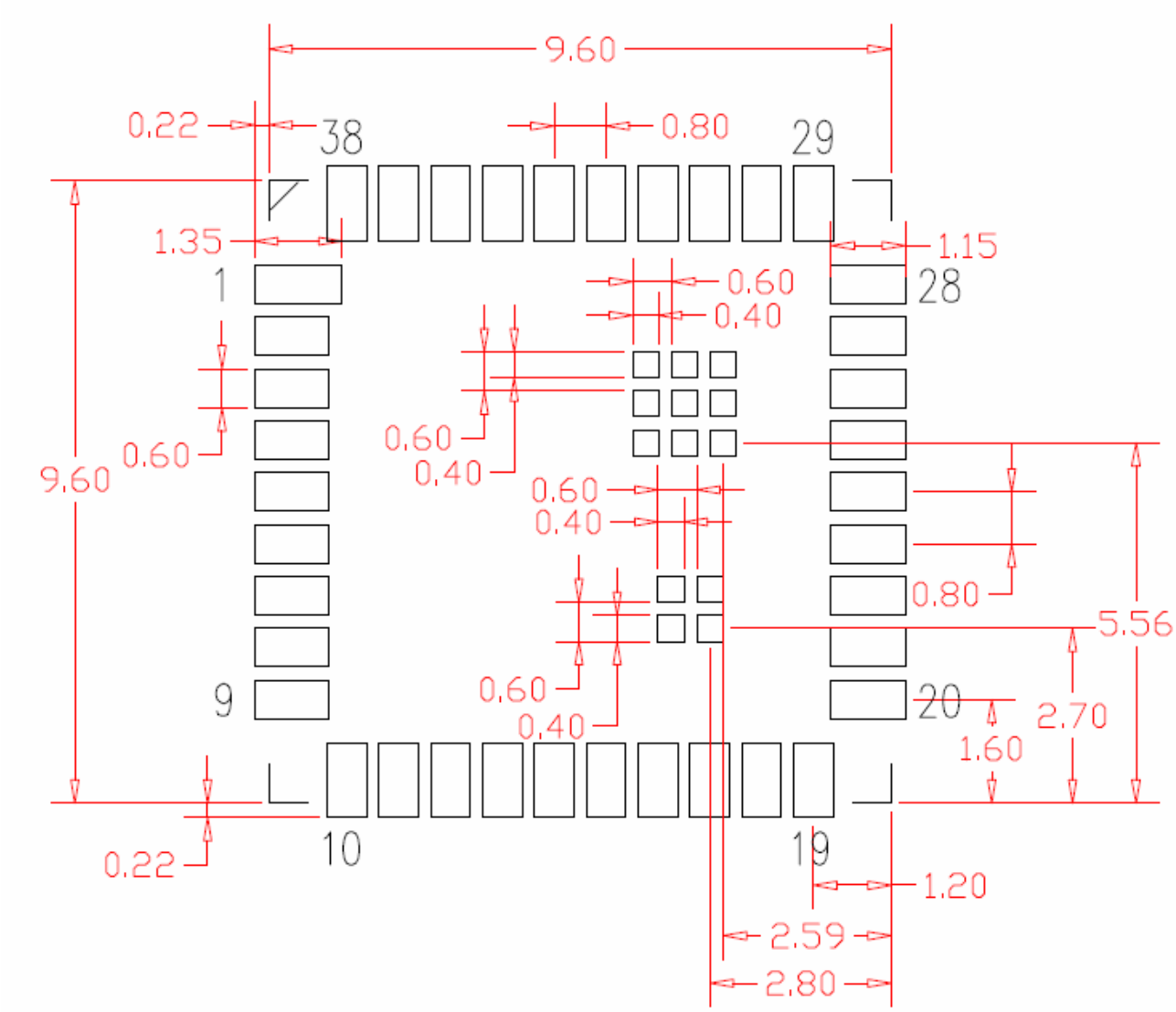
4 Assembly Guideline

4-1 Recommended Mounting Pad Design (Top View)

The following figure illustrates the recommended mounting pad design for apm6998.



TOP VIEW(mm)

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4-2 Baking condition recommendation before IR reflow

Baking condition for apm6998 module:

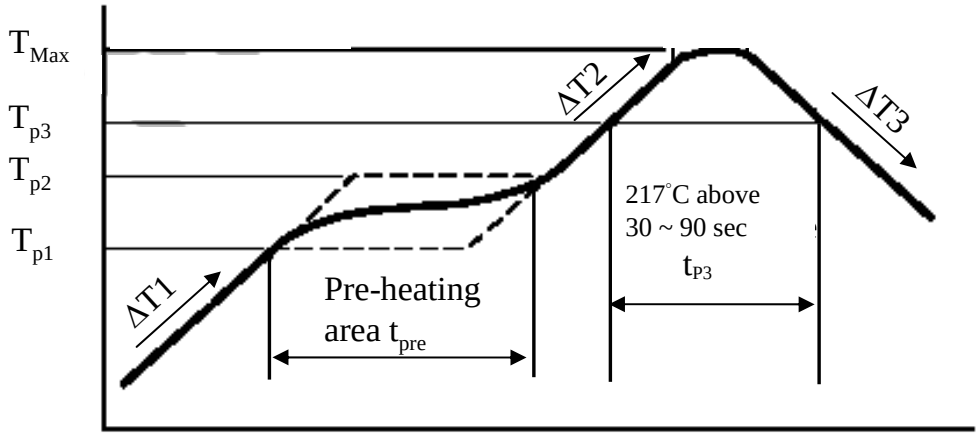
I: 125°C/4 hrs baking is necessary for apm6998 module before SMT process. After baking treatment the modules can be stored in the environment under 30°C and 60% RH for 48 hrs. If the storage time is over 48 hrs, the modules need to be re-baked using the same condition again.

II: In the event that the sealed bag is damaged on receipt of the modules, the baking condition should be changed to 125°C/8 hrs.

4-3 Recommendation for Reflow Profile

Maximum reflow temperature is 250°C.

Preheat ramp-up rate	125°C to 180°C 1 to 3°C /sec.
Peak temperature	250°C max.
Temperature maintained above 217°C	30 ~ 90 sec.
Cooling ramp-down rate	<2°C/sec.
Maximum number of reflow cycles	≤3



Heating/Cooling Speed			Pre-Heating		Heating	
ΔT1	ΔT2	ΔT3	T_{p1}–T_{p2}	t_{pre}	T_{Max}	t_{P3}
1 to 3°C /sec.	1 to 3°C /sec.	< 2°C /sec.	125 ~ 180°C	30 ~ 90 sec.	250°C max.	30 ~ 90 sec.

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