ZY70N65

N-CHANNEL 65V - 70A TO-220 POWER MOSFET

TYPE	Bvdss	Rdson	Id
ZY70N65	65V	10mΩ	70A

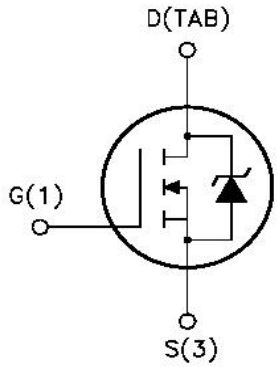
Typical Rdson = 8.5mΩ

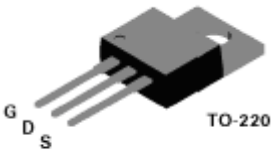
Exceptional dv/dt Capability

100% Avalanche Tested

Application Oriented

Characterization





DESCRIPTION

This Power Mosfet series realized with SZY Corp. DMOS technology trench process has specifically signed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC Converters for Telecom and Computer application. It is also intended for any application with low gate charge drive requirements.

APPLICATIONS

HIGH-EFFICIENCY DC-DC CONVERTERS
DC MOTOR CONTROL
UPS
AUTOMOTIVE ENVIRONMENT

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vds	Drain-Source Voltage (Vgs=0)	65	V
Vdgr	Drain-gate Voltage (R_{GS} = 20 KΩ)	65	V
Vgs	Gate- source Voltage	±20V	V
Id (a)	Drain Current (continuous) at T_C = 25 ℃	70	A
Id	Drain Current (continuous) at T_C = 100 ℃	42	A
IDM (b)	Drain Current (pulsed)	240	A
Ptot	Total Dissipation at T_C = 25 ℃	110	W
	Derating Factor	0.7	W/℃
dv / dt (1)	Peak Diode Recovery voltage slope	4	V/ns
Eas (2)	Single Pulse Avalanche Energy	360	mj
Tstg	Storage Temperature	-55~175	℃
Tj	Max. Operating Junction Temperature		

(a) Current limited by package

(b) Pulse width limited by safe operating area

(1) ISD ≤60A, di/dt ≤400A/us, VDD ≤24V, Tj ≤TJMAX.

(2) Starting Tj = 25 ℃, ID = 30A, VDD = 30V

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	1.36	℃ / W
Rthj-amb	Thermal Resistance Junction-ambient	Max	63	℃ / W
Ti	Maximum Lead Temperature For Soldering Purpose	Typ	300	℃

ELECTRICAL CHARACTERISTICS (T_{case} = 25 ℃ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Bvdss	Drain-source Breakdown Voltage	ID = 250 uA VGS = 0	65			V
Idss	Zero Gate Voltage Drain Current (VGS = 0)	V_{DS} = Max Rating			1	uA
		V_{DS} = Max Rating T_C = 125 ℃			10	uA
Igss	Current (VDS = 0)	V_{GS} = ．20V			±100	nA

ON

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VGS(th)	Gate Threshold Voltage	VDS = VGS ID = 250uA	2	3	4	V
RDS(on)	Static Drain-source On Resistance	VGS = 10V ID=30A		8.5	10	mΩ

DYNAMIC

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Gfs	Forward Tran conductance	VDS = 15V ID=30A		20		S
Ciss	Input Capacitance	VDS = 25V, f = 1 MHz, VGS=0		1810		PF
Coss	Output Capacitance			360		PF
Crss	Reverse Transfer Capacitance			125		PF

ELECTRICAL CHARACTERISTICS

SWITCHING ON

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
td (on)	Turn-on Delay Time	VDD=30V , ID=30A , Rg=4.7Ω		16		ns
tr	Rise Time	VGS=10V (Resistive Load, Figure 3)		108		ns
Qg	Total Gate Charge	VDD = 48V ID = 60 A VGS= 10V		49	66	nc
Qgs	Gate-Source Charge			18		nc
Qgd	Gate-Drain Charge			14		nc

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
td (off)	Turn-off Delay Time	VDD=30V , ID=30A , Rg=4.7Ω		43		ns
tf	Fall Time	VGS=10V (Resistive Load, Figure 3)		20		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
ISD	Source-drain Current				60	A
ISDM (1)	Source-drain Current (pulsed)				240	A
VSD (a)	Forward On Voltage	ISD = 60 A VGS = 0			1.3	V
trr	Reverse Recovery Time	ISD = 60 A VDD = 25 V		73		ns
Qrr	Reverse Recovery Charge	di/dt = 100A/us Tj= 150 ℃		182		nc
IRRM	Reverse Recovery Current	(see test circuit, Figure 5)		5		A

(1) Pulse width limited by safe operating area

(a) Pulsed: Pulse duration = 300 s, duty cycle 1.5 %

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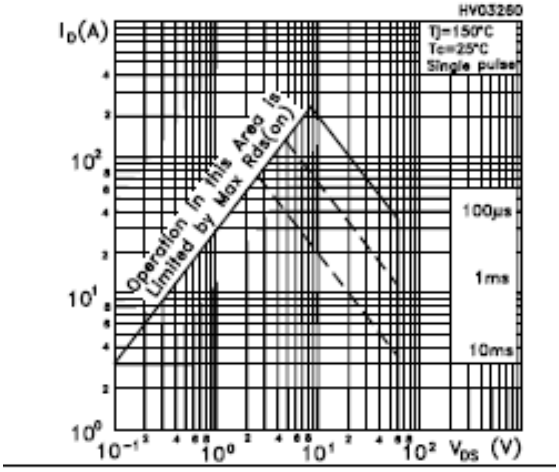
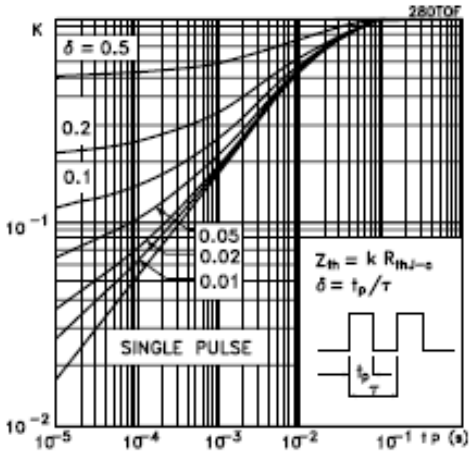
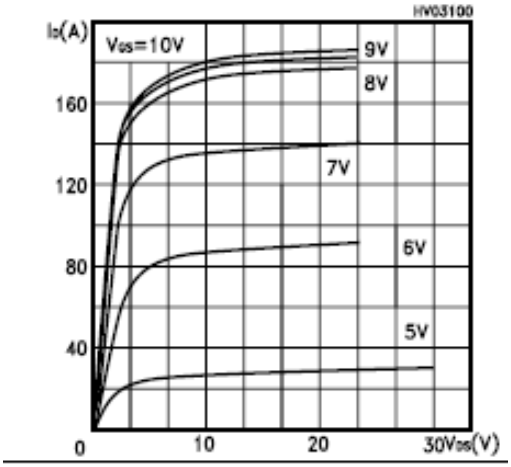
Safe Operating Area



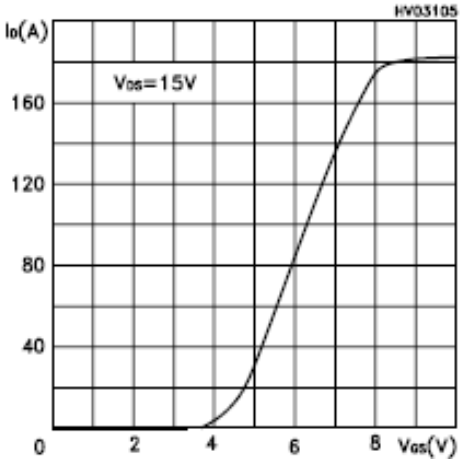
Thermal Impedance



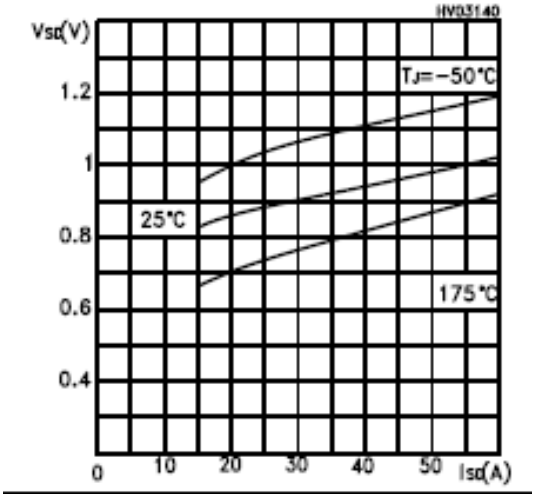
Output Characteristic



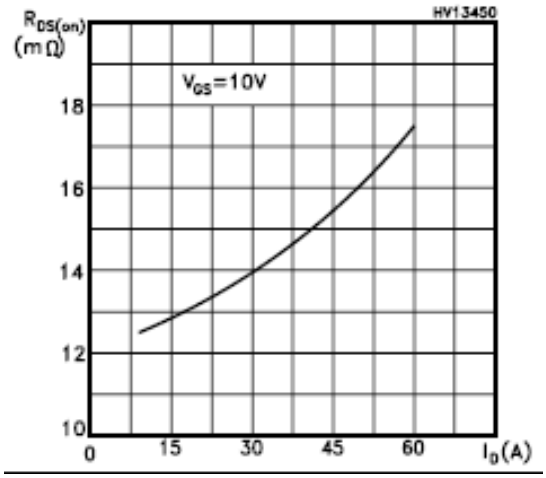
Transfer Characteristics



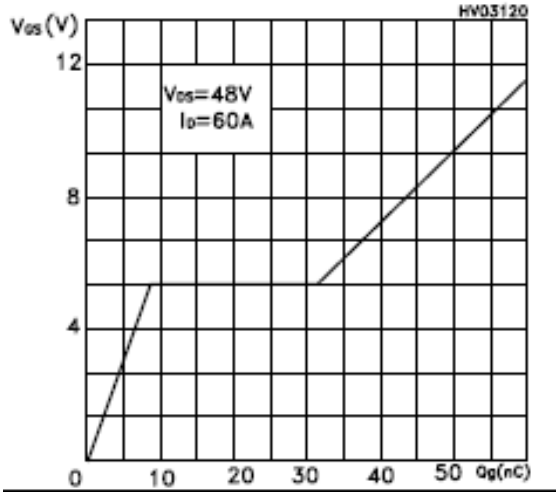
Source-drain diode forward characteristics



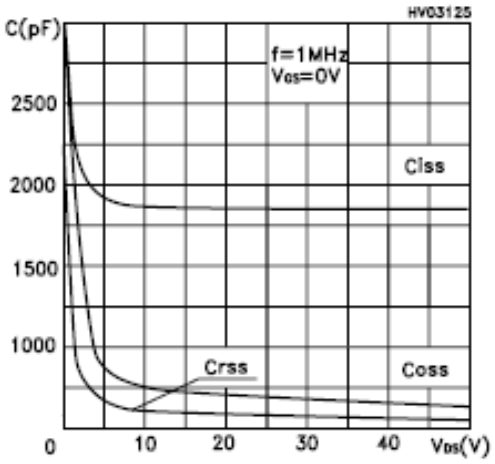
Static Drain-source On Resistanc



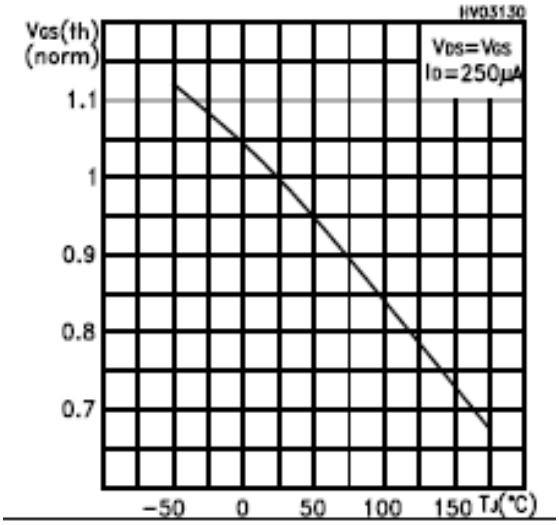
Gate Charge vs Gate-source Voltag



Capacitance Variation



Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature

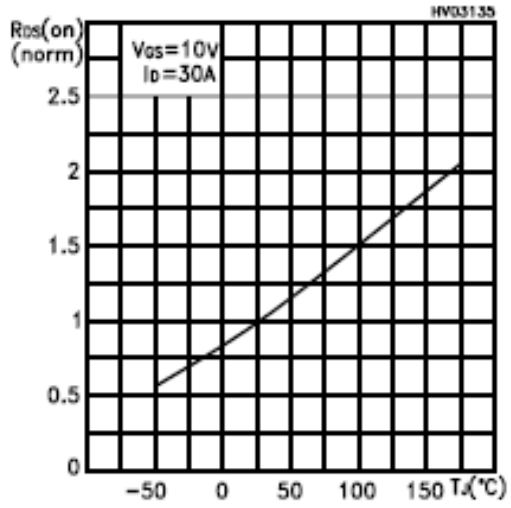


Fig. 1: Unclamped Inductive Load Test Circuit

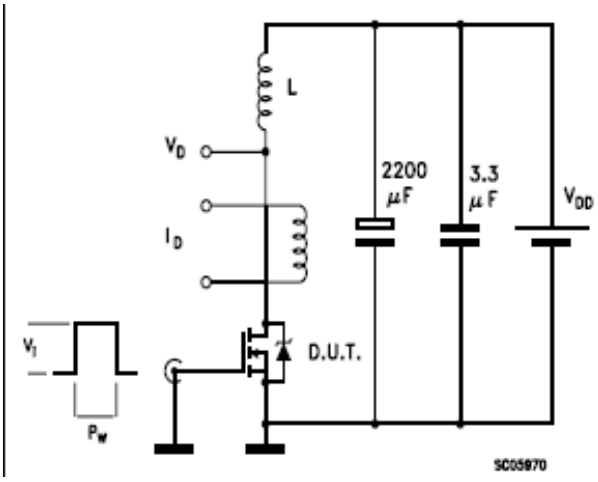


Fig. 2: Unclamped Inductive Waveform

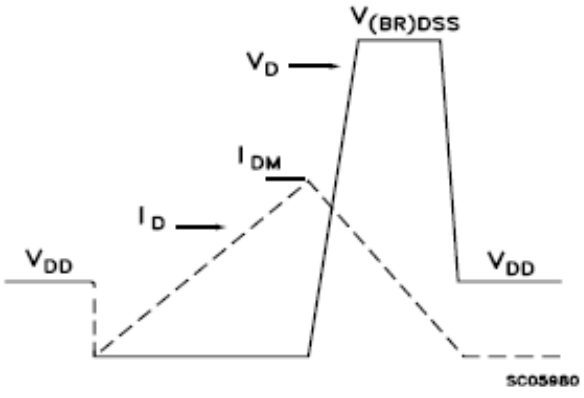


Fig. 3: Switching Times Test Circuits For Resistive Load

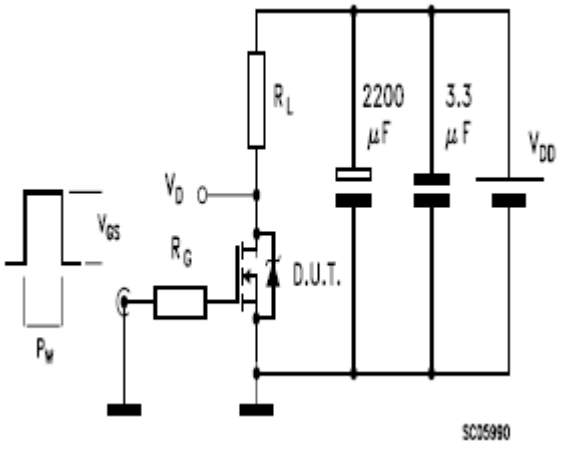


Fig. 4: Gate Charge test Circuit

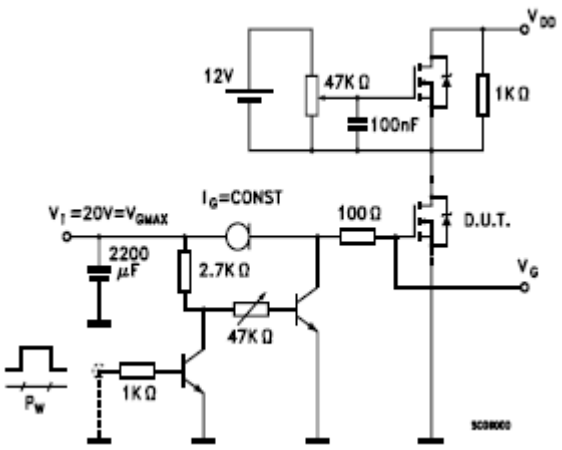
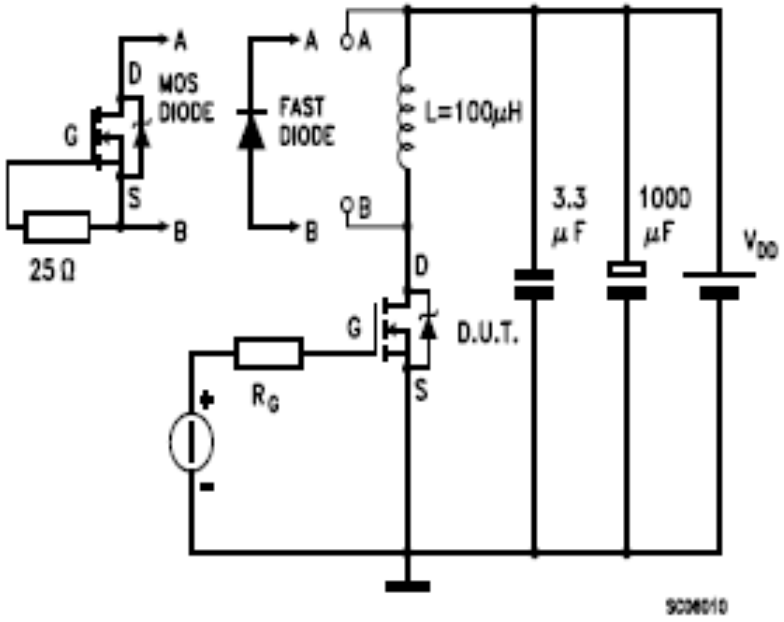


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



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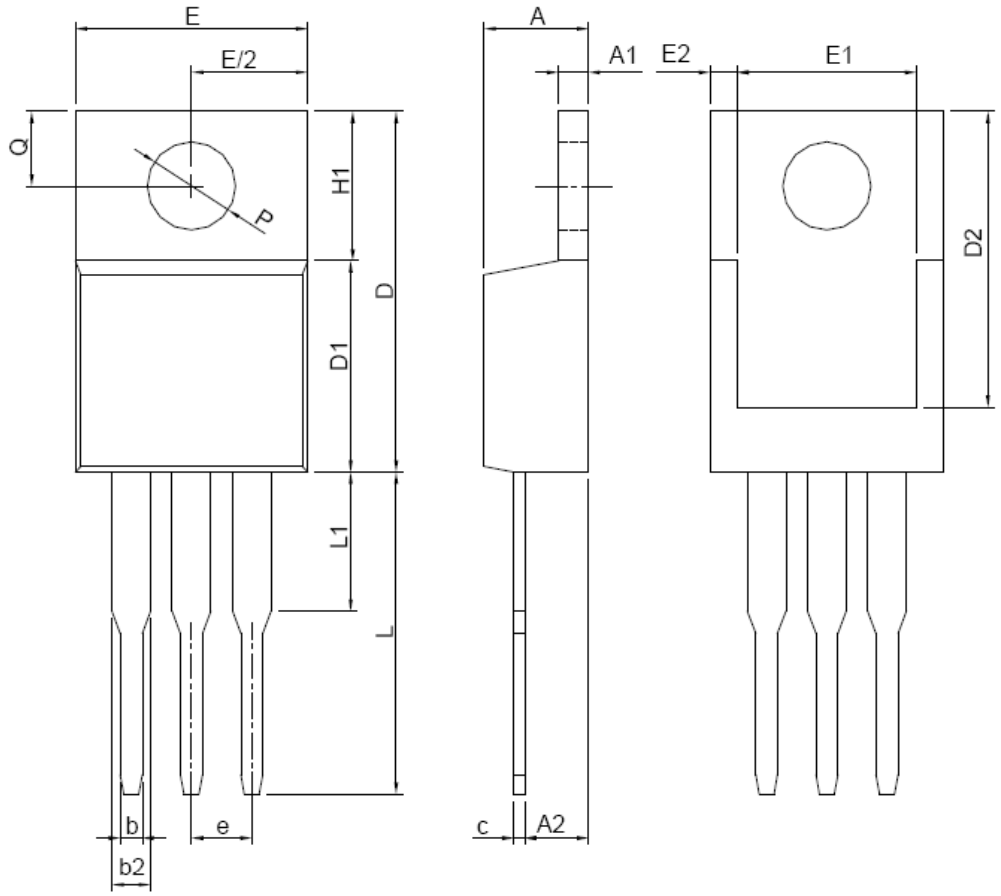
TO-220 POD DATA



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	3.56	4.83	0.140	0.190
A1	0.51	1.40	0.020	0.055
A2	2.03	2.92	0.080	0.115
b	0.38	1.02	0.015	0.040
b2	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.22	16.51	0.560	0.650
D1	8.38	9.02	0.330	0.355
D2	12.19	12.88	0.480	0.507
E	9.65	10.67	0.380	0.420
E1	6.86	8.89	0.270	0.350
E2	-	0.76	-	0.030
e	2.54 BSC		0.100 BSC	
H1	5.84	6.86	0.230	0.270
L	12.70	14.73	0.500	0.580
L1	-	6.35	-	0.250
P	3.53	4.09	0.139	0.161
Q	2.54	3.43	0.100	0.135