

ZXMC3F31DN8 30V SO8 Complementary dual enhancement mode MOSFET

Summary

Device	V _{(BR)DSS} (V)	Q _G (nC)	R _{DS(on)} (Ω)	I _D (A)
Q1	30	12.9	0.024 @ V _{GS} = 10V	7.3
			0.039 @ V _{GS} = 4.5V	5.7
Q2	-30	12.7	0.045 @ V _{GS} = -10V	5.3
			0.080 @ V _{GS} = -4.5V	4



Description

This new generation Trench MOSFET from Zetex has been designed to minimize the on-state resistance $(R_{DS(on)})$ and yet maintain superior switching performance making it ideal for power management and battery charging functions.

Features

- Low on-resistance
- 4.5V gate drive capability
- Low profile SOIC package

Applications

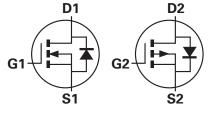
- DC-DC Converters
- SMPS
- Load switching switches
- Motor control
- Backlighting

Ordering information

Device	Reel size	Tape width	Quantity
	(inches)	(mm)	per reel
ZXMC3F31DN8TA	7	12	500

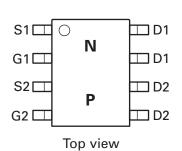
Device marking

ZXMC 3F31



Q1 N-Channel

Q2 P-Channel



Absolute maximum ratings

Parameter	Symbol	N- channel Q1	P- channel Q2	Unit
Drain-Source voltage	V _{DSS}	30	-30	V
Gate-Source voltage	V _{GS}	±20	±20	V
Continuous Drain current @ V_{GS} = 10V; T_A =25°C (b)(d)	Ι _D	7.3 5.9	5.3 4.3	A
@ $V_{GS} = 10V; T_A = 70°C$ @ $V_{GS} = 10V; T_A = 25°C$ (a)(d)		5.7	4.1	
(a)(e) (a)(e) (a)(e) (b)(c) (c)(c) (c)(c) (c)(c) (c)(c) (c)(c) (c)(c) (c)(c) (c)(c) (c)(c) (c)(c)(c) (c)(c)(c)(c) (c)(c)(c)(c)(c)(c)(c)(c)(c)(c)(c)(c)(c)(6.8 7.8	4.9 5.7	
Pulsed Drain current ^(C)	I _{DM}	33	23	А
Continuous Source current (Body diode) ^{(b)(d)}	۱ _S	3.5	3.2	А
Pulsed Source current (Body diode) (c)(d)	I _{SM}	33	23	А
Power dissipation at T _A =25°C ^{(a)(d)} Linear derating factor	P _D		25 0	W mW/°C
Power dissipation at T _A =25°C ^{(a)(e)} Linear derating factor	PD		.8 4	W mW/°C
Power dissipation at T _A =25°C ^{(b)(d)} Linear derating factor	PD		.1 7	W mW/°C
Power dissipation at T _L =25°C ^{(f) (d)} Linear derating factor	PD		35 9	W mW/°C
Operating and storage temperature range	T _j , T _{stg}	-55 t	o 150	°C

Thermal resistance

Parameter	Symbol	Value	Unit
Junction to ambient ^{(a)(d)}	$R_{\theta JA}$	100	°C/W
Junction to ambient (a)(e)	R _{θJA}	70	°C/W
Junction to ambient ^{(b)(d)}	R _{0JA}	60	°C/W
Junction to lead ^(f) (d)	R _{θJL}	53	°C/W

NOTES:

(a) For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 2oz copper, in still air conditions.

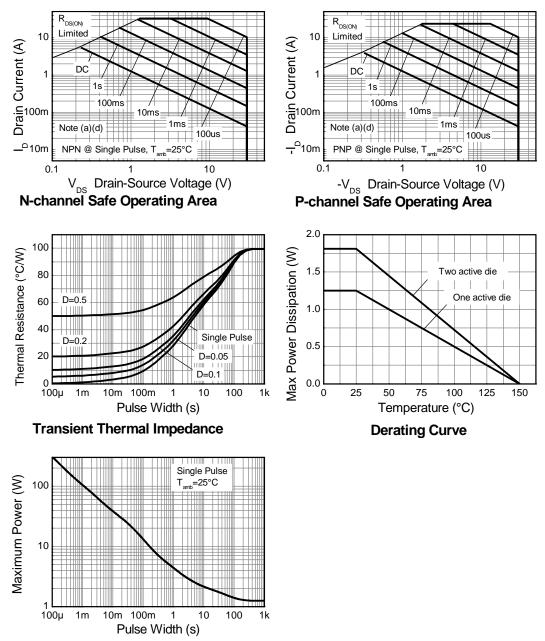
(b) Mounted on FR4 PCB measured at t \leq 10 sec.

(c) Repetitive rating on 25mm x 25mm FR4 PCB, D=0.02, pulse width 300us - pulse width limited by maximum junction temperature.

(d) For a device with one active die.

(e) For a device with two active die running at equal power.(f) Thermal resistance from junction to solder-point (at the end of the drain lead).

Thermal characteristics



Pulse Power Dissipation

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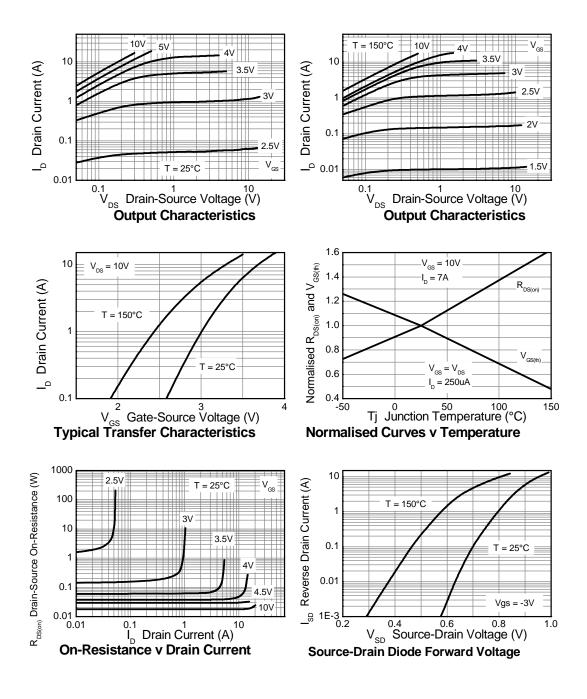
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Static	• •					
Drain-Source breakdown voltage	V _{(BR)DSS}	30			V	$I_D = 250 \mu A, V_{GS} = 0V$
Zero Gate voltage Drain current	I _{DSS}			0.5	μA	V_{DS} =30V, V_{GS} =0V
Gate-Body leakage	I _{GSS}			100	nA	V _{GS} =±20V, V _{DS} =0V
Gate-Source threshold voltage	V _{GS(th)}	1.0		3.0	V	$I_D=250\mu A, V_{DS}=V_{GS}$
Static Drain-Source on-state resistance ^(*)	R _{DS(on)}			0.024 0.039	Ω	V _{GS} = 10V, I _D = 7.0A V _{GS} = 4.5, I _D = 6.0A
Forward Transconductance ^{(*) (†)}	9 _{fs}		16.5		S	V _{DS} = 15V, I _D = 7.0A
Dynamic ^(†)	· ·					
Input capacitance	C _{iss}		608		pF	
Output capacitance	C _{oss}		132		pF	V _{DS} = 15V, V _{GS} =0V
Reverse transfer capacitance	C _{rss}		72		pF	f=1MHz
Switching ^{(‡) (†)}						
Turn-on-delay time	t _{d(on)}		2.9		ns	
Rise time	t _r		3.3		ns	V _{DD} = 15V, V _{GS} =10V
Turn-off delay time	t _{d(off)}		16		ns	I _D = 1A
Fall time	t _f		8		ns	$R_{G}\cong 6.0\Omega,$
Total Gate charge	Qg		12.9		nC	
Gate-Source charge	Q _{gs}		2.5		nC	V _{DS} = 15V, V _{GS} = 10V
Gate-Drain charge	Q _{gd}		2.52		nC	I _D = 7A
Source-Drain diode	<u> </u>					
Diode forward voltage (*)	V _{SD}		0.82	1.2	V	I _S = 1.7A,V _{GS} =0V
Reverse recovery time ^(‡)	t _{rr}		12		ns	I _S = 2.2A,di/dt=100A/μs
Reverse recovery charge ^(‡)	Q _{rr}		4.8		nC	

Q1 N-channel electrical characteristics (at $T_{amb} = 25^{\circ}C$ unless otherwise stated)

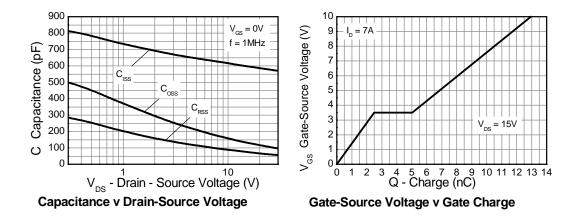
NOTES:

(*) Measured under pulsed conditions. Pulse width $\leq 300 \mu s$; duty cycle $\leq 2\%$. (†)Switching characteristics are independent of operating junction temperature. (‡)For design aid only, not subject to production testing

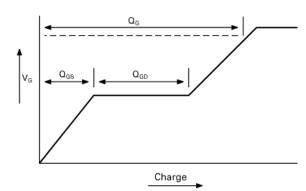
Q1 Typical characteristics



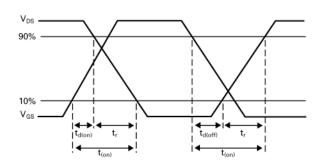
Q1 Typical characteristics -cntd.



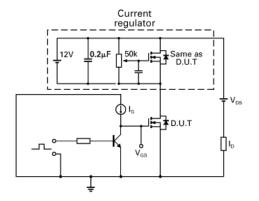
Test circuits



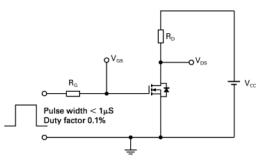
Basic gate charge waveform



Switching time waveforms



Gate charge test circuit





Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Static	· ·					
Drain-Source breakdown voltage	V _{(BR)DSS}	-30			V	I_{D} = -250µA, V_{GS} =0V
Zero Gate voltage Drain current	I _{DSS}			-5.0	μA	V_{DS} =-30V, V_{GS} =0V
Gate-Body leakage	I _{GSS}			-100	nA	V _{GS} =±20V, V _{DS} =0V
Gate-Source threshold voltage	V _{GS(th)}	-1.0		-3.0	V	I_{D} = -250 μ A, V_{DS} = V_{GS}
Static Drain-Source on-state resistance ^(*)	R _{DS(on)}			0.045 0.080	Ω	V _{GS} = -10V, I _D = -5.0A V _{GS} = -4.5V, I _D = -4.0A
Forward Transconductance ^{(*) (†)}	9fs		14		S	V _{DS} = -15V, I _D = -5.0A
Dynamic ^(†)	· · ·					
Input capacitance	C _{iss}		670		pF	
Output capacitance	C _{oss}		126		pF	V _{DS} = -15V, V _{GS} =0V
Reverse transfer capacitance	C _{rss}		70		pF	f=1MHz
Switching ^{(‡) (†)}	•		•	•		
Turn-on-delay time	t _{d(on)}		1.9		ns	
Rise time	t _r		3		ns	V _{DD} = -15V, V _{GS} =-10V
Turn-off delay time	t _{d(off)}		30		ns	I _D = -1A
Fall time	t _f		21		ns	R _G ≅ 6.0Ω,
Total Gate charge	Qg		12.7		nC	
Gate-Source charge	Q _{gs}		2		nC	V _{DS} = -15V, V _{GS} = -10V
Gate-Drain charge	Q _{gd}		2.4		nC	I _D = -5A
Source–Drain diode						
Diode forward voltage (*)	V _{SD}		-0.82	-1.2	V	I _S = -2A,V _{GS} =0V
Reverse recovery time (‡)	t _{rr}		16.5		ns	I _S = -2.1A,di/dt=100A/μs
Reverse recovery charge ^(‡)	Q _{rr}		11.5		nC	13- 2. 1Λ,αι/αι-100Λ/μδ

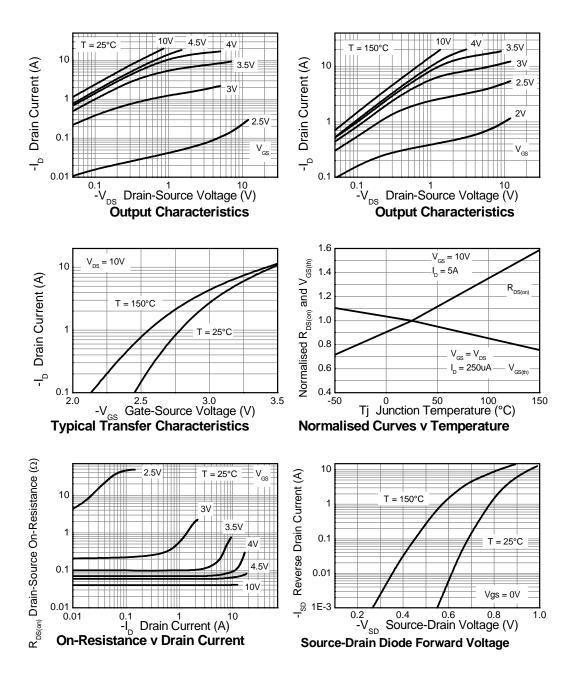
Q2 P-channel electrical characteristics (at $T_{amb} = 25^{\circ}C$ unless otherwise stated)

NOTES:

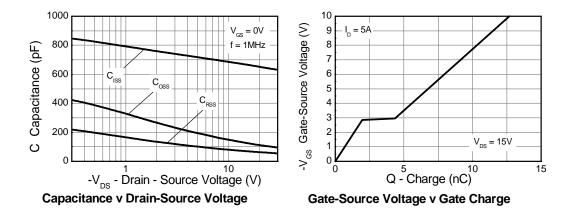
(*) Measured under pulsed conditions. Pulse width \leq 300µs; duty cycle \leq 2%. (†)Switching characteristics are independent of operating junction temperature.

(‡)For design aid only, not subject to production testing

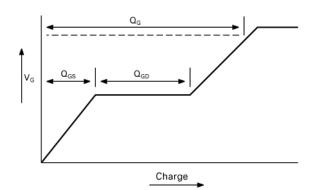
Typical characteristics



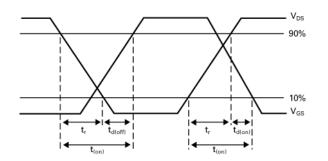
Typical characteristics



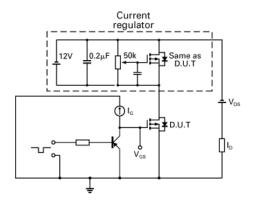
Test circuits



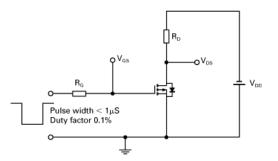
Basic gate charge waveform



Switching time waveforms

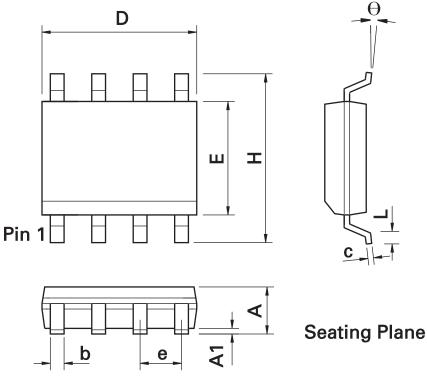


Gate charge test circuit





Package outline SO8



SO8 Package Information

DIM	Inc	hes	Millin	neters	DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
А	0.053	0.069	1.35	1.75	е	0.050 BSC		1.27 BSC	
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	с	0.008	0.010	0.19	0.25
н	0.228	0.244	5.80	6.20	U	0°	8°	0°	8°
E	0.150	0.157	3.80	4.00	h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27	-	-	-	-	-

Note: Controlling dimensions are in inches. Approximate dimensions are provided in millimeters

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"Not recommended for new de		Device is still in production to support existing designs and production							
"Obsolete"	Production has been disconting	nued							
Datasheet status key:									
"Draft version"	This term denotes a very early	y datasheet version and contains	highly provisional						
	information, which may chang	ge in any manner without notice.							
"Provisional version"	This term denotes a pre-relea	This term denotes a pre-release datasheet. It provides a clear indication of anticipated performance.							
	However, changes to the test	conditions and specifications may	occur, at any time and without notice.						
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Fax: (49) 89 45 49 49 49	Fax: (1) 631 360 8222	Fax: (852) 24250 494							

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usa.sales@zetex.com

europe.sales@zetex.com

asia.sales@zetex.com