ZXGD3111N8

200V ACTIVE OR-ING MOSFET CONTROLLER IN SO8

Lead-free Green

Description

ZXGD3111N8 is a 200V Active OR-ing MOSFET controller designed for driving a very low $R_{DS(ON)}$ Power MOSFET as an ideal diode. This replaces the standard rectifier to reduce the forward voltage drop and overall increase the power transfer efficiency.

The ZXGD3111N8 can be used on both high-side and low-side power supply units (PSU) with rails up to ±200V. It enables very low $R_{DS(ON)}$ MOSFETs to operate as ideal diodes as the turn-off threshold is only -3mV with ±2mV tolerance. In the typical 48V configuration, the standby power consumption is <50mW as the low quiescent supply current is <1mA. During PSU fault condition, the OR-ing Controller detects the power reduction and rapidly turns off the MOSFET in <600ns to block reverse current flow and avoid the common bus voltage dropping.

Features

- Active OR-ing MOSFET Controller for High- or Low-Side PSU
- Ideal Diode to Reduce Forward Voltage Drop
- -3mV Typical Turn-Off Threshold with ±2mV Tolerance
- 200V Drain Voltage Rating
- 25V V_{CC} Rating
- <50mW Standby Power with Quiescent Supply Current <1mA
- <600ns Turn-Off Time to Minimize Reverse Current
- **Totally Lead-Free & Fully RoHS compliant (Notes 1 & 2)**
- **Halogen and Antimony free. "Green" Device (Note 3)**

Applications

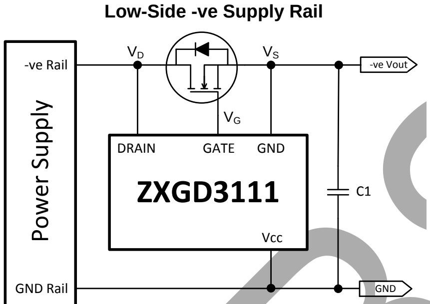
Active OR-ing Controller in:

- (N + 1) Redundant Power Supplies
- Telecom and Networking
- Data Centers and Servers

Mechanical Data

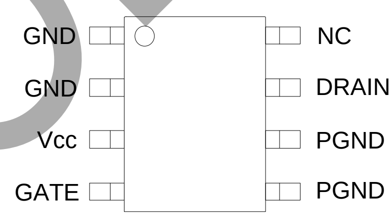
- Case: SO-8
- Case material: Molded Plastic. "Green" Molding Compound UL Flammability Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 (e3)
- Weight: 0.074 grams (Approximate)

Typical Configuration for Low-Side -ve Supply Rail



SO-8

Top View



Top View
Pin-Out

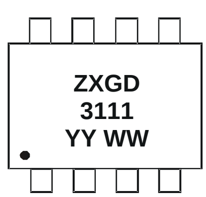
Pin Name	Pin Function
GND	Ground
V_{CC}	Power Supply
GATE	Gate Drive
PGND	Power Ground
DRAIN	Drain Sense
NC	Not Connected Internally

Ordering Information (Note 4)

Product	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXGD3111N8TC	ZXGD 3111	13	12	2,500

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



ZXGD = Product Type Marking Code, Line 1
3111 = Product Type Marking Code, Line 2
YY = Year (ex: 15 = 2015)
WW = Week (01 - 53)

Absolute Maximum Ratings (Voltage relative to GND, @ T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	25	V
Drain Pin Voltage	V_D	-3 to 200	V
Gate Output Voltage	V_G	-3 to V_{CC} + 3	V
Gate Driver Peak Source Current	I_{SOURCE}	2	A
Gate Driver Peak Sink Current	I_{SINK}	5	A

Thermal Characteristics (@ T_A = +25°C, unless otherwise specified.)

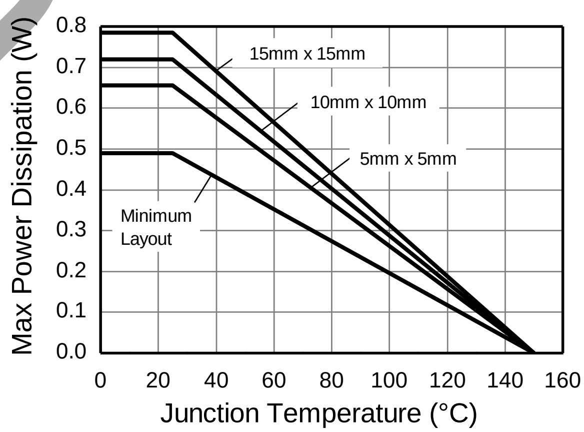
Characteristic		Symbol	Value	Unit
Power Dissipation Linear Derating Factor	(Note 5)	P_D	490 3.92	mW mW/°C
	(Note 6)		655 5.24	
	(Note 7)		720 5.76	
	(Note 8)		785 6.28	
Thermal Resistance, Junction to Ambient	(Note 5)	$R_{θJA}$	255	°C /W
	(Note 6)		191	
	(Note 7)		173	
	(Note 8)		159	
Thermal Resistance, Junction to Lead	(Note 9)	$R_{θJL}$	135	°C /W
Operating and Storage Temperature Range		T_J, T_{STG}	-50 to +150	°C

ESD Ratings (Note 10)

Characteristic	Symbol	Value	Unit	JEDEC Class
Electrostatic Discharge - Human Body Model	ESD HBM	4,000	V	3A
Electrostatic Discharge - Machine Model	ESD MM	400	V	C

Notes:
5. For a device surface mounted on minimum recommended pad layout FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
6. Same as Note 5, except pin 3 (Vcc) and pins 5 & 6 (PGND) are both connected to separate 5mm x 5mm 1oz copper heat-sinks.
7. Same as Note 6, except both heat-sinks are 10mm x 10mm.
8. Same as Note 6, except both heat-sinks are 15mm x 15mm.
9. Thermal resistance from junction to solder-point at the end of each lead on pins 2 & 3 (GND) and pins 5 & 6 (V_{CC}).
10. Refer to JEDEC specification JESD22-A114 and JESD22-A11

Thermal Derating Curve



Derating Curve

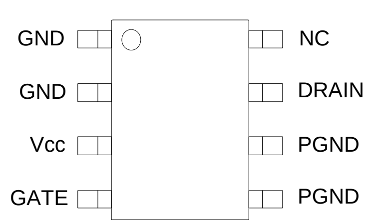
Electrical Characteristics (@ V_{CC} = 12V, T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition	
Input Supply							
Operating Supply Voltage	V_{CC}	4	—	20	V		
Quiescent Current	I_Q	—	200	—	µA	-0.6V ≤ V_{DRAIN} ≤ 200V	
Gate Driver							
Gate Peak Source Current	I_{SOURCE}	—	0.66	—	A	C_L = 47nF	
Gate Peak Sink Current	I_{SINK}	—	3.3	—			
Gate Peak Source Current (Note 11)	I_{SOURCE}	1	—	—	A	V_{GATE} = 5V & V_{DRAIN} = -1V	
Gate Peak Sink Current (Note 11)	I_{SINK}	1.8	—	—	A	V_{GATE} = 5V & V_{DRAIN} = 1V	
Detector under DC condition							
Turn-off Threshold Voltage	V_T	-5	-3	-1	mV	V_G ≤1V	
Gate Output Voltage	$V_{G(off)}$	—	0.1	0.3	V	V_{DRAIN} ≥ 0mV & V_{CC} = 12V	Load: 50nF capacitor connected in parallel with 50kΩ resistor
	V_G	—	9.2	—		V_{DRAIN} = -8mV & V_{CC} = 12V	
	$V_{G(off)}$	—	0.1	0.3		V_{DRAIN} ≥ 0mV & V_{CC} = 4V	
	V_G	—	3.2	—		V_{DRAIN} = -8mV & V_{CC} = 4V	
	$V_{G(off)}$	—	0.1	0.3		V_{DRAIN} ≥ 0mV & V_{CC} = 20V	
	V_G	—	12	—		V_{DRAIN} = -8mV & V_{CC} = 20V	
Switching Performance							
Turn-On Propagation Delay	$t_{d(rise)}$	—	400	—	ns	C_L = 47nF Rise and fall measured 10% to 90% Refer to application test circuit below	
Gate Rise Time	t_r	—	695	—			
Turn-Off Propagation Delay	$t_{d(fall)}$	—	400	—			
Gate Fall Time	t_f	—	131	—			

Note: 11. Measured under pulsed conditions. Pulse width ≤ 300µs. Duty cycle ≤ 2%.

Pin Functions

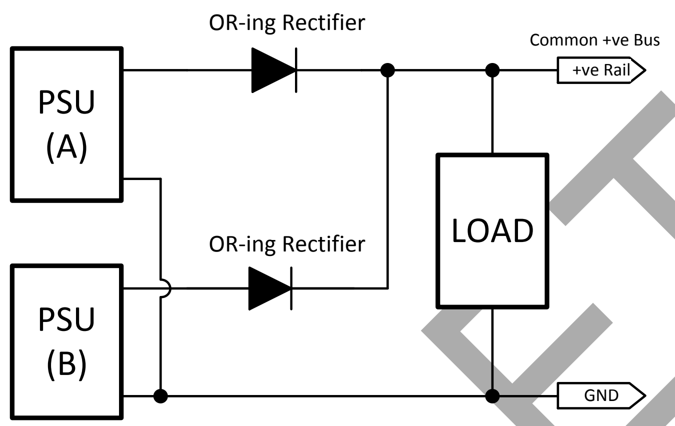
Pin Number	Pin Name	Pin Function and Description
1, 2	**GND**	**Ground** Connect this pin to the MOSFET source terminal and ground reference point.
3	**V_{CC}**	**Power Supply** This supply pin should be closely decoupled to ground with a X7R type capacitor.
4	**GATE**	**Gate drive** This pin sources (I_{SOURCE}) and sinks (I_{SINK}) current into the MOSFET gate. If Vcc > 12V, then the GATE-to-GND will clamp at 12V. The turn on time of the MOSFET can be programmed through an external gate resistor (R_G).
5, 6	**PGND**	**Power Ground** Connect this pin to the MOSFET source terminal and ground reference point.
7	**DRAIN**	**Drain Sense** Connect this pin to the MOSFET drain terminal to detect the change in drain-source voltage.
8	**NC**	**Not Internally Connected**



Layout Considerations

The GATE pin should be close to the MOSFET gate to minimize trace resistance and inductance to maximize switching performance. Whilst the V_{CC} to GND pin needs an X7R type capacitor closely decoupling the supply. Trace widths should be maximized in the high current paths through the MOSFET and ground return in order to minimize the effects of circuit resistance and inductance; also, the ground return loop should be as short as possible. For thermal consideration, the main heat path is from pin 3 (Vcc) and pins 5 & 6 (PGND). For best thermal performance, the copper area connected to pin 3 (Vcc) and pins 5 & 6 (PGND) should be maximized.

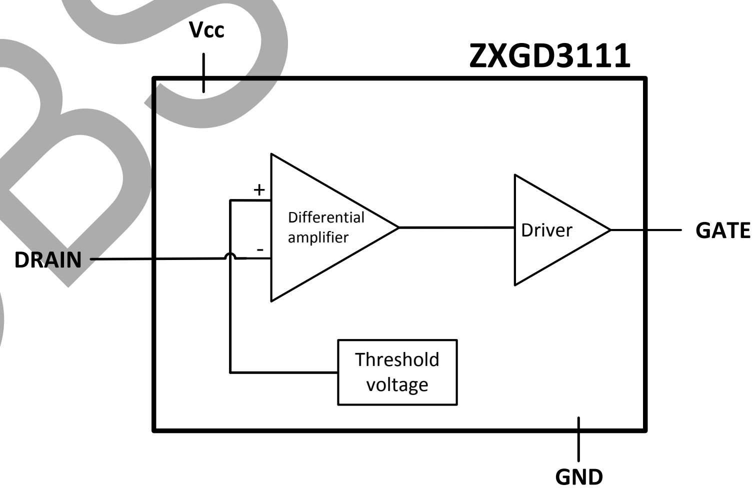
Active OR-ing or (N+1) Redundancy Application



Critical systems require fault-tolerant power supply that can be achieved by paralleling two or more PSUs into (N+1) redundancy configuration. During normal operation, usually all PSUs equally share the load for maximum reliability. If one of the PSU is unplugged or fails, then the other PSUs fully support the load. To avoid the faulty PSU from affecting the common bus, then an OR-ing rectifier blocks the reverse current flow into the faulty PSU. Likewise during hot-swapping, the OR-ing rectifiers isolate a PSU's discharged output capacitors from the common bus.

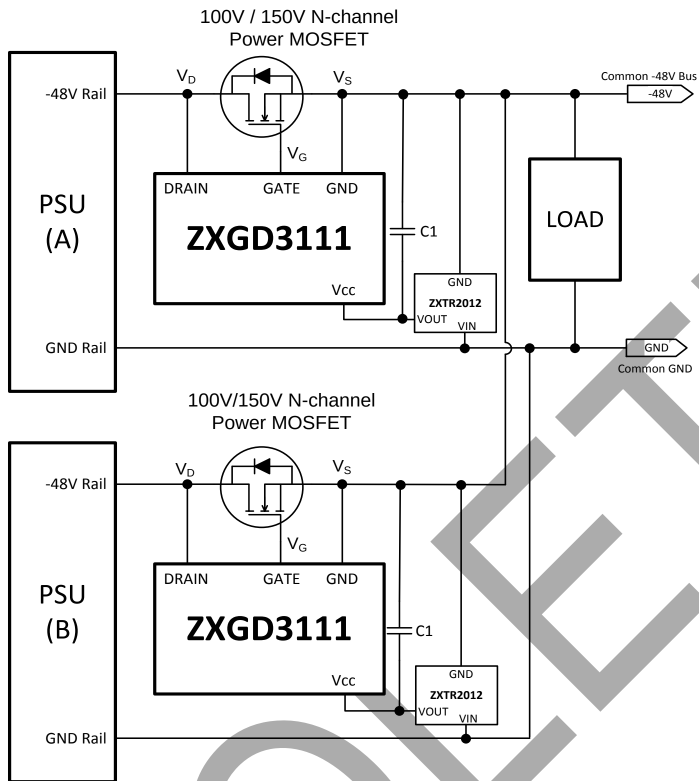
As the load current is in the tens of amps then a standard rectifier has a significant forward voltage drop. This both wastes power and significantly drops the potential on low voltage rails. Hence, very low $R_{DS(ON)}$ Power MOSFETs can replace the standard rectifiers and the ZXGD3111 controls the MOSFET as an ideal diode.

Functional Block Diagram

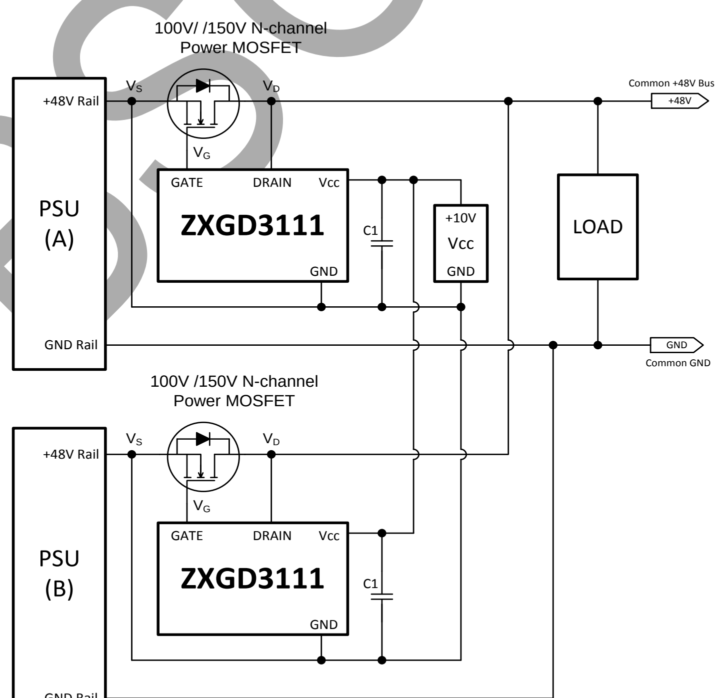


The device is comprised of a differential amplifier and high current driver. The differential amplifier acts as a detector and monitors the DRAIN-to-GND pin voltage difference. When this difference is less than the threshold voltage (V_T) then a positive output voltage approaching Vcc is given on the GATE pin. If Vcc > 12V, then the GATE-to-GND will clamp at 12V. Conversely, when the DRAIN-to-GND pin voltage difference is greater than V_T, then GATE pin voltage is rapidly reduced towards the GND voltage.

Typical Application Circuits



The focus application of the ZXGD3111 OR-ing Controller is for Redundant Low-Side -48V Power Supply Rail. ZXTR2012 (HV input, 12V output regulator) is suggested to power the Vcc of ZXGD3111 from high voltage rail.



Example of the ZXGD3111 OR-ing Controller in a Redundant High-Side +48V Power Supply Rail using an additional Vcc supply.

Operation in Typical Application

The ZXGD3111 operation is described step-by-step with reference to the typical application circuits and the timing diagram below:

1. The ZXGD3111 differential amplifier monitors the MOSFET's drain-source voltage (V_{DS}).

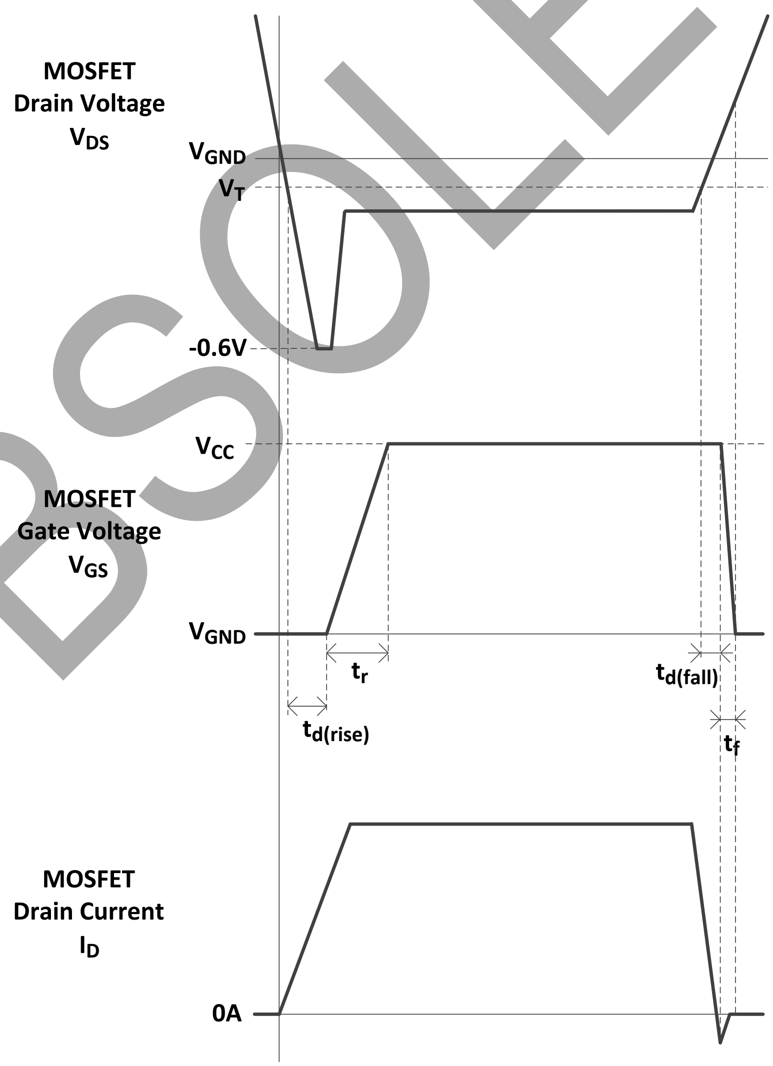
2. At system start up, the MOSFET body diode is forced to conduct current from the input PSU to the load and V_{DS} is approximately -0.6V as measured by the differential amplifier between DRAIN-to-GND pins.

3. As $V_{DS} < V_T$ (threshold voltage), the differential amplifier outputs a positive voltage approaching V_{CC} with respect to GND. This feeds the driver stage from which the GATE pin voltage rises towards V_{CC}. If Vcc > 12V, then the GATE-to-GND will clamp at 12V.

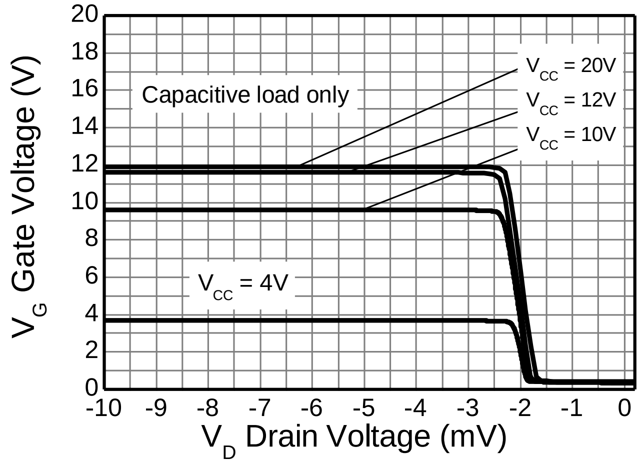
4. The sourcing current out of the GATE pin drives the MOSFET gate to enhance the channel and turn it on.

5. If a short condition occurs on the input PSU, it causes the MOSFET V_{DS} to increase.

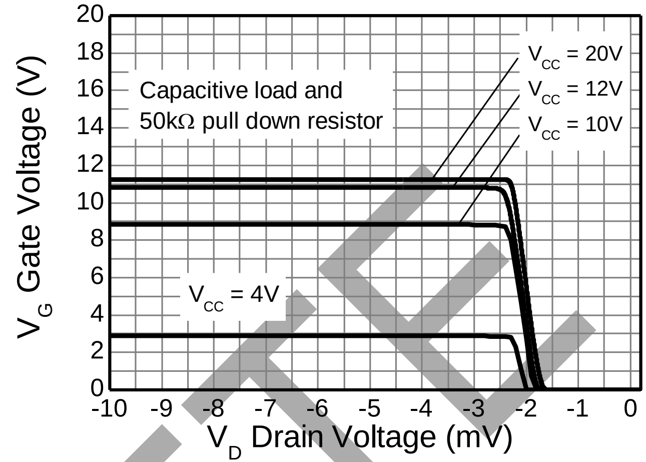
6. When $V_{DS} > V_T$, then the differential amplifier's output goes to GND and the driver stage rapidly pulls the GATE pin voltage to GND, turning off the MOSFET channel. This prevents high reverse current flow from the load to the PSU which could pull down the common bus voltage causing catastrophic system failure.



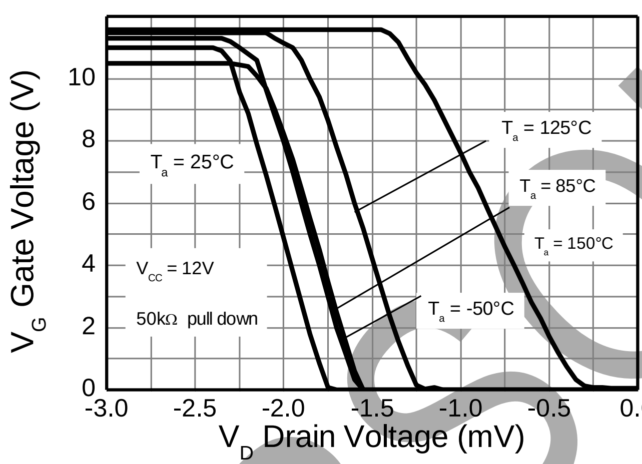
Typical Electrical Characteristics (@ T_A = +25°C, unless otherwise specified.)



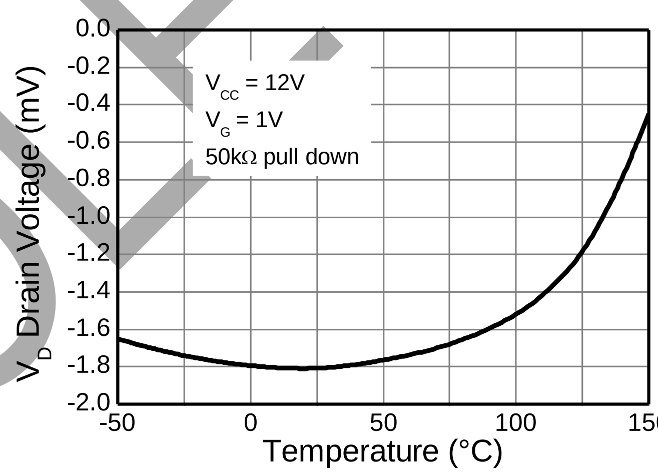
Transfer Characteristic



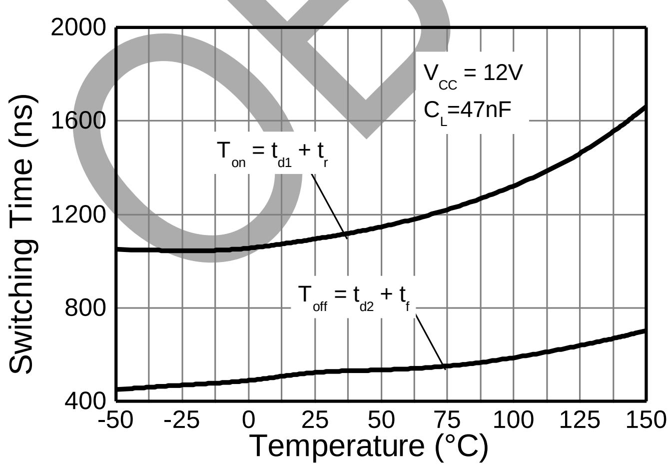
Transfer Characteristic



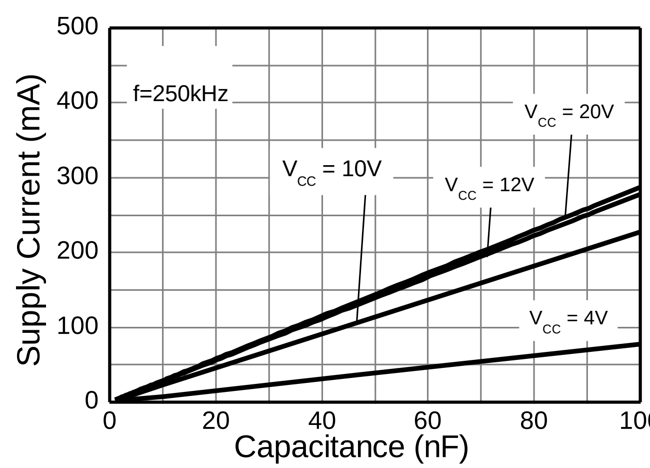
Transfer Characteristic



Drain Sense Voltage vs Temperature

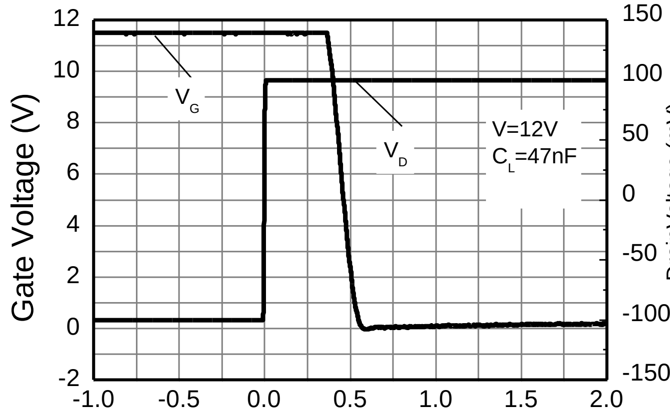


Switching vs Temperature

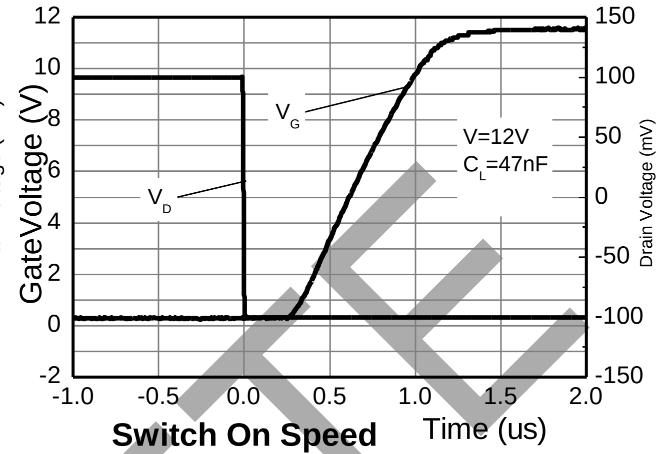


Supply Current vs Capacitive Load

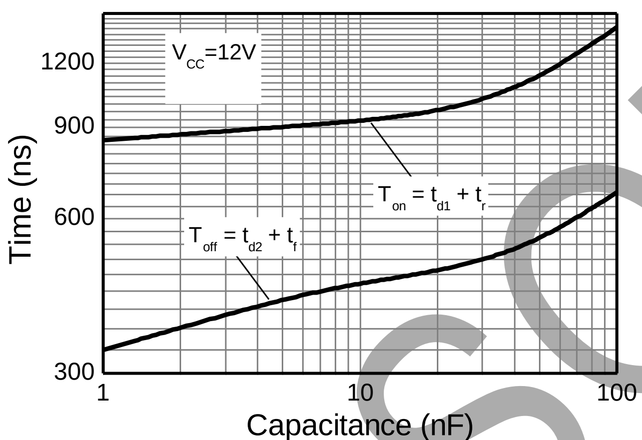
Typical Electrical Characteristics (cont.) (@ T_A = +25°C, unless otherwise specified.)



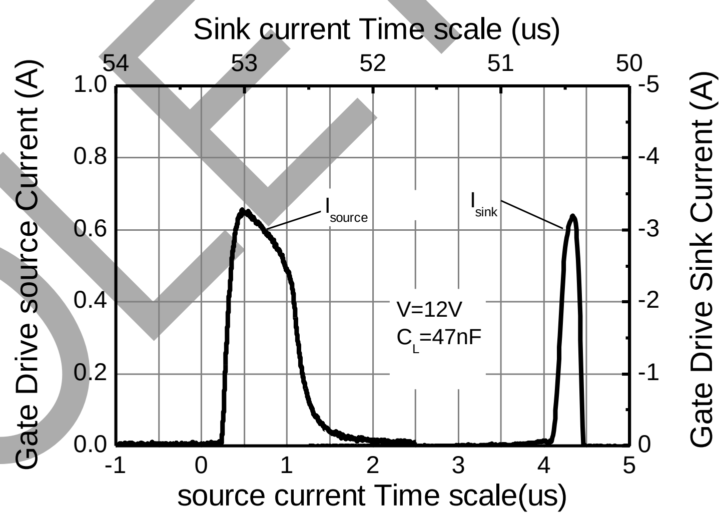
Switch Off Speed



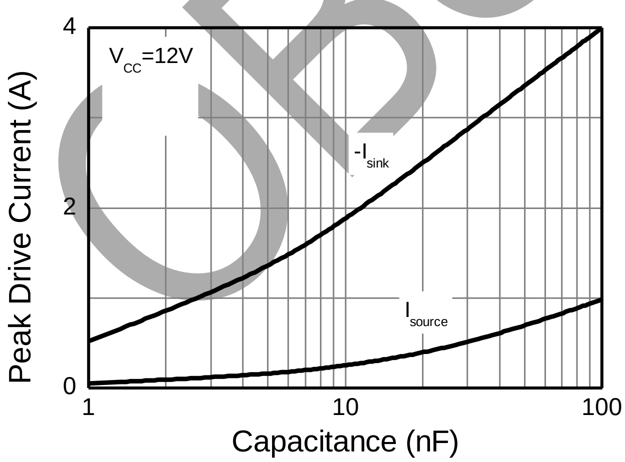
Switch On Speed



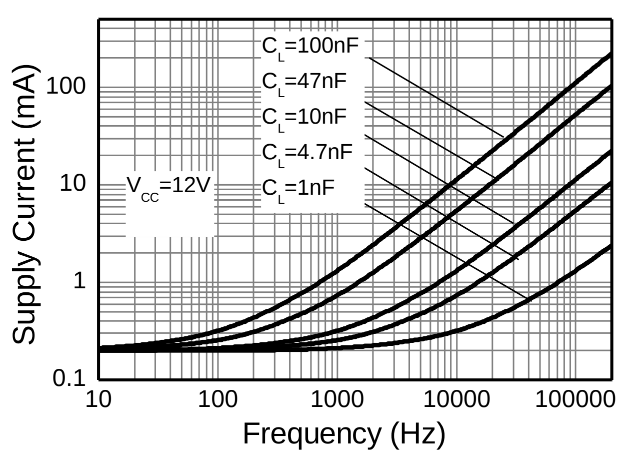
Switching vs Capacitive Load



Gate Drive Current



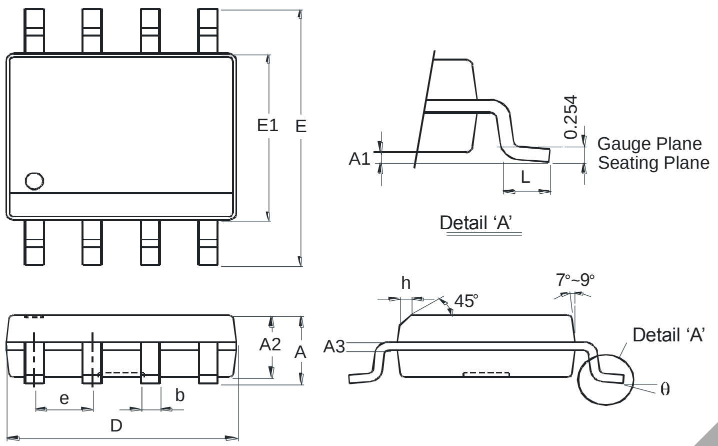
Gate Current vs Capacitive Load



Supply Current vs Frequency

Package Outline Dimensions

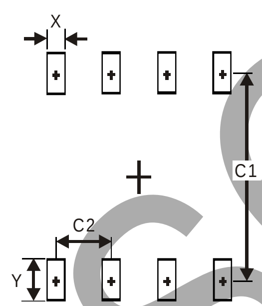
Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



SO-8		
Dim	**Min**	**Max**
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

Note: For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

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