

Data Sheet

ZR36966ELCG-D

DVD SoC

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ZORAN Proprietary

Vaddis 966-D[®] Data sheet

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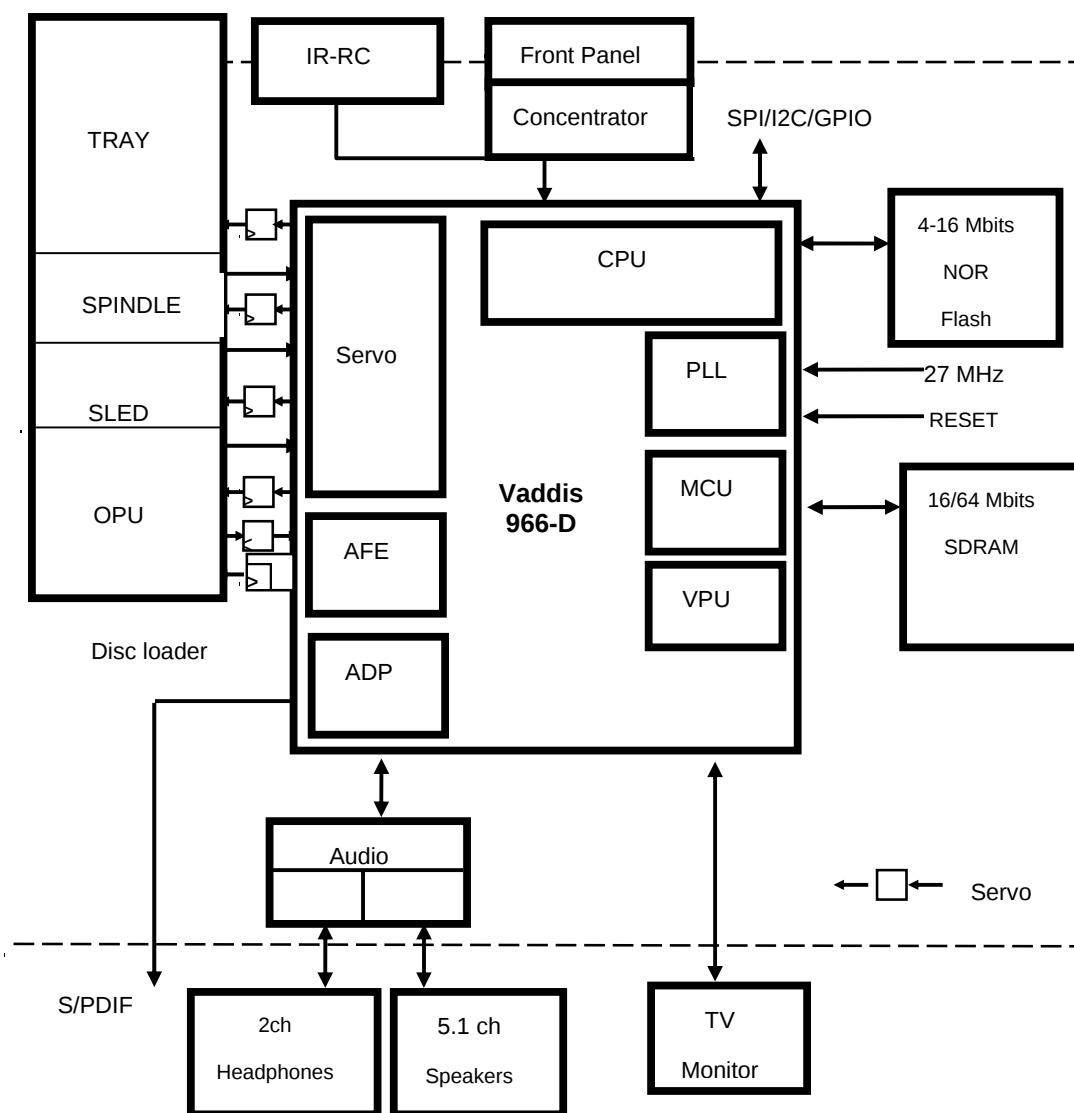
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1 Introduction

The Vaddis 966-D is Zoran's ninth-generation of IC product for entry-level consumer DVD players. This highly-integrated device includes the full front-end disc controller including the RF amplifier stage, back-end decoder functions including MPEG-4, DivX memory cards and integrated audio DACs.

2 Functional Overview



This document describes the technical specification of the **Vaddis 966-D** disc loader controller, flash memory card, and decoder device.

Supported Media: DVD-ROM, DVD-R, DVD+R, DVD-RW, DVD+RW, CD-DA, CD-ROM, CD-ROM (XA) CD-R and CD-RW discs.

Memory Cards: Secure Digital (SD), Memory Stick (MS and MS Pro), Compact Flash (CF Mem and IDE), PCMCIA, XD, SDIO, MultiMedia Card (MMC) and Smart Media (SM).

HDD: The Vaddis 966-D can interface to a Hard Disc, IDE mode.

Video and Audio formats: DVD-Video, CD-DA, VCD (Video-CD), SVCD (Super Video-CD), various formats of MPEG 4 (including DivX), JPEG and compressed audio (MP3, AAC, WMA).

FE – Front End integration

The **Vaddis 966-D** integrates all of the common drive front-end components. It receives data from the disc loader optical pick-up unit OPU, limit switches and other sensors and control the disc loader focus and tracking coils, sled, spindle and tray motors through a servo amplifier external device(s). The **Vaddis 966-D** implements all the signal processing, multi-pass ECC, EDC, track buffer management and servo functions that result in an (error corrected) bitstream.

2.1 Feature List

2.1.1 Disc loader control and bitstream processing

- Single or differential analog RF input from the OPU
- 10 analog inputs for servo errors calculations and RF signals envelope monitoring
- 6 PWM actuators drive or control outputs which can be used e.g. for the tracking and focus coils, for sled and spindle motors, programmed tray motion or external (analog) parameter setting.
- Processing of spindle and sled position read-back devices
- All servo loop closure, closed loop control, jumps, disc identification and error handling.
- Bitstream extraction using AGC, bit clock frequency detection and phase lock loop, adaptive threshold calculations, Viterbi bit decision, defect detection, frame sync detection and EFM/P conversion.
- CD sub-code extraction and processing.
- CD ECC for all CD types. CD EDC for Mode 1 discs
- DVD ECC and EDC.
- Track buffer and re-try management

2.1.2 Decoding

- Single chip solution for playback of DVD-Video Video-CD, Super Video-CD, CD-DA, and MP3, WMA, MPEG 4, DivX or JPEG from flash cards, DVD-ROM, DVD-R, DVD-RW, DVD+R, DVD+RW, CD-ROM, CD-R or CD-R/W discs.
- Decoding and display of JPEG, MPEG-4, DivX, MPEG 1 and MPEG 2 still image sequences.
- Decoding of WMA, Dolby AC-3.
- Decoding of MPEG 1 or MPEG 2 layer II mono, stereo, or multi-channel audio. Decoding of MPEG 1 or MPEG 2 Layer 3 (MP3) mono and stereo audio (including low sampling rate).
- PCM and LPCM audio playback from DVD-Video, Video-CD and CD-DA.
- Decoding and playback of sub-picture (including Highlight), and closed captions ("line 21") data from DVD-Video discs. Decoding and playback of DivX sub-titles
- Interlaced and progressive digital and analog video output.
- PAL playback of NTSC discs and NTSC playback of PAL discs.
- Special modes support like pause, slow motion, fast forward, goto time and reverse.

2.1.3 Post Processing

- Audio down mixing, sample rate conversion, Dolby's Prologic II, Base Management and 3D enhancement.
- Karaoke mixing of decoded audio and two channels of input audio.
- De-jittering filtering of S/PDIF inputs using a high speed PLL and DTO.
- On-chip OSD engine with 256 color (24-bit YUV) palette, up to 8 levels of transparency; and capability of blinking regions and vertical and horizontal scrolling.
- On-screen and off-screen OSD memory regions for animation support.
- 1/4 pixel and 1/4 line pan&scan. Supported
- Horizontal and vertical up- and down-scaling with polyphase two-tap vertical and horizontal interpolation.
- Letterbox and Pan-scan display aspect ratio conversion (16:9 to 4:3).
- Frame rate conversion (e.g., 3/2 pull down) and format conversion (16:9, 4:3, 1:1).
- EIA-608 compatible modulation of line 21 (NTSC) or line 22 (PAL) closed captions data over the video output.

2.1.4 Interfaces

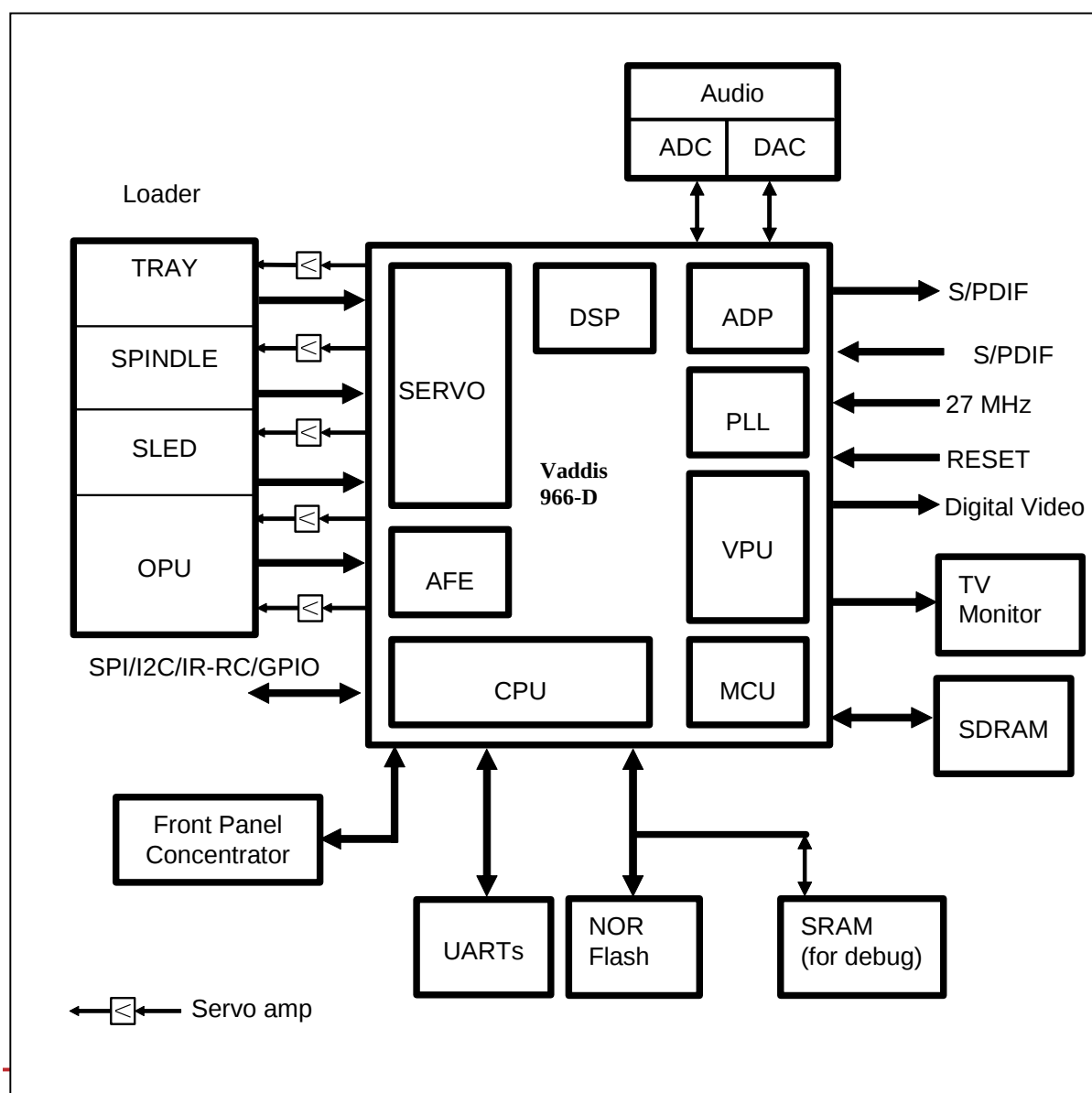
- 8-bit YUV 4:2:2 digital SD interlaced or progressive video output with optional embedded syncs.
- Composite, Y/C, YUV or RGB SD interlaced analog video output or SD component progressive analog video output (using five 14 bits on-chip V.DACs)
- Internally generated SD video sync signals and internally generated audio port clock signals.
- 6/18/20/24-bit I2S or EIAJ serial audio outputs. 16 bit I2S EIAJ serial audio input
- 2 to 8 channels audio output
- 2 channels audio input
- S/PDIF output for compressed audio (including DTS) or reconstructed audio (according to IEC 60958 and IEC 61937).
- Two S/PDIF inputs for compressed or PCM audio (according to IEC 60958 and IEC 61937).
- Single 128 Mbits, single 64-Mbit, single 16-Mbits and dual 16 Mbits SDRAMs (16 bits data) including power-down.
- Direct interface (through servo amplifiers) to several types of disc loaders.
- Direct interface to the following types of serial and parallel flash memory cards: Secure Digital (SD), Memory Stick (MS and MS Pro), Compact Flash (CF Mem and IDE), PCMCIA, XD, SDIO, MultiMedia (MM) and Smart Media (SM).
- 3 line serial general purpose slave interface (SSC)
- 2 UART interfaces for CPU SW debug

3 Unit Description

3.1 External interface

The main external interfaces of the **Vaddis 966-D** are shown in the next figure.

Figure 1. Vaddis 966-D main external interfaces



3.2 CPU - Central Processing Unit

The CPU is the central processing unit of the **Vaddis 966-D**. It is based on a 16 bits Intel 186 instruction set compatible licensed CPU core. The CPU executes from a NOR type Flash memory with 16 bit data bus. Alternately, a compatible EPROM, PROM, OTPROM or masked ROM can be connected.

The CPU core has attached to it 2 KWords instruction/data cache to the flash, 1KWords data/instruction cache to the SDRAM, 6KWords instruction ROM (most of it is dedicated to the DSP) shared with the DSP, 4KWords "scratch pad" data/instruction RAM and peripheral units mentioned below.

The core has internal real-time clock unit, two UART units, GPIO control unit and interrupt handler.

Most of the data transferred over the CPU_Bus are called CPU parameters. The CPU SW always writes and reads 16 bits (or multiple of 16 bits transferred consecutively to/from the same CPU_Bus address) for each parameter. CPU parameters written or read from the same address may or may not have the same name. In the CPU parameters description in the following sections, only "active" bits are mentioned. All "non-active" bits should be written with B'0' or return B'0' when read. It would be prudent for the CPU SW to ignore the values read for of non-active bits. Non-active addresses should not be written to or read from at all.

CPU SW is responsible for user interface and player control, internal units set-up and control, navigation and high level front end functions.

The CPU interfaces with the following external entities using GPIO functions: IR remote control receiver; Audio ADCs and DACs; Serial flash memory; Other player chips and debug aids.

3.3 PDU - Picture Decoding Unit

The PDU unit is mainly responsible for the decoding of MPEG video streams and reconstructing the coded frames. It is made of two main parts: A dedicated programmable processor (DVP) and a dedicated HW called PRU (picture reconstruction unit).

3.4 VPU - Video Processing Unit

The VPU is responsible for all video output processing and timing. It outputs 8 bit (U, Y V, Y interleaved) digital interlaced or progressive SD video with separate syncs and optionally embedded syncs. It can also output interlaced composite, S- or component SD analog video, or progressive components SD analog video.

The VPU units have three operating modes: SD Interlaced when the digital and analog outputs are interlaced, SD Progressive when the digital output is progressive. In this mode, the analog output can be either SD interlaced or progressive. A two fields Deinterlacer can be used (as needed) for the decoded image. The third mode is SD progressive digital output with a mixture of interlaced and progressive SD analog output.

3.5 ADP - Audio Data Processor

The ADP is the audio processing unit of the **Vaddis 966-D**.

All the ADP peripheral units are connected to the ADP core through the AP_Bus (audio peripherals bus). The interrupt handler is also connected directly to the interrupt port of the ADP core.

3.6 Inter-Unit Interfaces

The main inter-unit interfaces are described below.

The CPU is connected to all **BE** units and all **FE** units (apart from the AFE, DRC and SERVO), using the **C_Bus**. The number of data lines used is 16. The C_Bus signals are described in Section **Error! Reference source not found.**

The MCU is connected to the following units: STP, ECC, EDC, DSP, CPU, VPU, ADP, DVP and PDU. For testing and debug, the AFE is also connected to the MCU.

The PLL is generating several processing clocks signals, audio port master clock, and the reset signal, n_reset, that is used by all units.

4 Pin Description

4.1 Pin List

The table below lists the pins, their functions, the direction or nature of each function (according to the legend below). Following is the table legend:

I - standard input-only. **O** - standard active driver, with a 3-state option. **I/O** - bi-directional I/O pin, with a 3-state option. **AI** - Analog input signal. **AO** - Analog output signal. **AI/O** - Analog connection. **ID** - input, not sampled by PCLK. **S** - Power supply or ground.

Pins that are designated AI, S or ID should not be left not connected or floating.

Pins designname with 2 (*PINNAME_2*) marks the 2nd (or 3rd) appearance of this function.

GPIOs designated by a preceding I (IGPIO) means they can be use as interrupts to the CPU.

Table 1 – Pin functions allocation

Pkg	Pin Functions	Dir	Description
			Left wall
1	MEMDA[2]	I/O	PNVM/SRAM bi-directional data bus
	FCUDA[2]	I/O	Flash card interface unit input/output signal FCUIF[4]
2	MEMDA[10]	I/O	PNVM/SRAM bi-directional data bus
	GPIO[0]	I/O	General purpose input/output, monitored/controlled by the CPU – if RS8BIT or RS8BIT16 is active
	FCUDA[10]	I/O	Flash card interface unit input/output signal FCUIF[23]
3	MEMDA[3]	I/O	PNVM/SRAM bi-directional data bus
	FCUDA[3]	I/O	Flash card interface unit input/output signal FCUIF[5]
4	MEMDA[11]	I/O	PNVM/SRAM bi-directional data bus
	FCUDA[11]	I/O	Flash card interface unit input/output signal FCUIF[24]
	GPIO[1]	I/O	General purpose input/output, monitored/controlled by the CPU – if RS8BIT or RS8BIT16 is active
5	MEMDA[4]	I/O	PNVM/SRAM bi-directional data bus
	FCUDA[4]	I/O	Flash card interface unit input/output signal FCUIF[06]
6	MEMDA[12]	I/O	PNVM/SRAM bi-directional data bus
	FCUDA[12]	I/O	Flash card interface unit input/output signal FCUIF[25]
	GPIO[2]	I/O	General purpose input/output, monitored/controlled by the CPU – if RS8BIT or RS8BIT16 is active
7	MEMDA[5]	I/O	PNVM/SRAM bi-directional data bus
	FCUDA[5]	I/O	Flash card interface unit input/output signal FCUIF[07]
8	MEMDA[13]	I/O	PNVM/SRAM bi-directional data bus
	FCUDA[13]	I/O	Flash card interface unit input/output signal FCUIF[26]
	GPIO[3]	I/O	General purpose input/output, monitored/controlled by the CPU – if RS8BIT or RS8BIT16 is active
9	MEMDA[6]	I/O	PNVM/SRAM bi-directional data bus
	FCUDA[6]	I/O	Flash card interface unit input/output signal FCUIF[08]
10	MEMDA[14]	I/O	PNVM/SRAM bi-directional data bus
	FCUDA[14]	I/O	Flash card interface unit input/output signal FCUIF[27]

Table 1 – Pin functions allocation

Pkg	Pin Functions	Dir	Description
	GPIO[4]	I/O	General purpose input/output, monitored/controlled by the CPU – if RS8BIT or RS8BIT16 is active
11	GNDC	S	Digital core ground (of 1.8V and 3.3V supplies)
12	MEMDA[7]	I/O	PNVM/SRAM bi-directional data bus
	FCUDA[7]	I/O	Flash card interface unit input/output signal FCUIF[09]
13	MEMDA[15]	O	PNVM/SRAM address bus outputs
	MEMAD[9]	O	PNVM/SRAM address bus– if RS8BIT is active
	MEMAD_1	O	PNVM/SRAM address bus– if RS8BIT16 is active
	FCUDA[15]	I/O	Flash card interface unit input/output signal FCUIF[42]
14	VDDC	S	1.8 V Digital core power supply
15	VDDP	S	3.3 V Digital peripheral power supply
16	MEMAD[16]	O	PNVM/SRAM address bus outputs
	FCUAD[16]	O	Flash card interface unit output signal FCUIF[43]
	MEMAD[18]	O	PNVM/SRAM address bus– if RS8BIT is active
	GPIO[6]_2	I/O	General purpose input/output, monitored/controlled by the CPU – if RS8BIT is active
17	MEMCS[1]#	O	PNVM/SRAM chip select (active low) output
	MEMLSB	O	PNVM/SRAM l.s. byte select output
	GPIO[5]	I/O	General purpose input/output, monitored/controlled by the CPU
	MEMCS[0]#	O	If BOOTSEL2 == B'1' – swap with MEMCS[1]#
	FCUIF[29]	O	Flash card interface unit output signal
18	MEMAD[15]	O	PNVM/SRAM address bus outputs
	FCUAD[15]	O	Flash card interface unit output signal FCUIF[42]
	MEMAD[19]	O	PNVM/SRAM address bus– if RS8BIT is active
	FGPIO[5]	I/O	General purpose input/output, monitored/controlled by the V8 SW – if RS8BIT is active

Table 1 – Pin functions allocation

Pkg	Pin Functions	Dir	Description
	IGPIO[7]_2	I/O	General purpose input/output, monitored/controlled by the CPU. Can be used as an interrupt for the CPU User only as output (see comment below: <u>Retention limitation on Pin 38</u>) – if RS8BIT is active
19	MEMAD[14]	O	PNVM/SRAM address bus outputs
	FCUAD[14]	O	Flash card interface unit output signal FCUIF[41]
	RS_PLLUBYP	I	PLLu (Level sampled during RESET. In normal operation the pin must be low during RESET
	MEMAD[16]	O	PNVM/SRAM address bus– if RS8BIT is active
20	MEMAD[13]	O	PNVM/SRAM address bus outputs
	FCUAD[13]	O	Flash card interface unit output signal FCUIF[40]
	MEMAD[15]	O	PNVM/SRAM address bus– if RS8BIT is active
21	MEMAD[12]	O	PNVM/SRAM address bus outputs
	FCUAD[12]	I/O	Flash card interface unit output signal FCUIF[39]
	MEMAD[14]	O	PNVM/SRAM address bus– if RS8BIT is active
22	MEMAD[11]	O	PNVM/SRAM address bus outputs
	FCUAD[11]	O	Flash card interface unit output signal FCUIF[38]
	MEMAD[13]	O	PNVM/SRAM address bus– if RS8BIT is active
23	MEMAD[10]	O	PNVM/SRAM address bus outputs
	FCUAD[10]	O	Flash card interface unit output signal FCUIF[20]
	MEMAD[12]	O	PNVM/SRAM address bus– if RS8BIT is active
24	MEMAD[9]	O	PNVM/SRAM address bus outputs
	FCUAD[9]	O	Flash card interface unit output signal FCUIF[19]
	MEMAD[11]	O	PNVM/SRAM address bus– if RS8BIT is active
25	MEMAD[8]	O	PNVM/SRAM address bus outputs
	FCUAD[8]	I/O	Flash card interface unit output signal FCUIF[18]
	RS_DECCFG	I	Dec Config indication input. Level sampled during RESET
	MEMAD[10]	O	PNVM/SRAM address bus– if RS8BIT is active

Table 1 – Pin functions allocation

Pkg	Pin Functions	Dir	Description
26	MEMWR#	O	PNVM/SRAM write enable (active low) output
	FCUIF[0]	O	Flash card interface unit output signal
	MEMAD[8]	O	PNVM/SRAM address bus– if RS8BIT is active
27	MEMAD[18]	O	PNVM/SRAM address bus outputs
	FCUAD[18]	O	Flash card interface unit output signal FCUIF[45]
	GPIO[6]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW – if RS8BIT and RS8BIT16 are <u>not</u> active
	MEMAD[7]	O	PNVM/SRAM address bus– if RS8BIT is active
28	MEMAD[17]	O	PNVM/SRAM address bus outputs
	FCUAD[17]	O	Flash card interface unit output signal FCUIF[44]
	RS8BIT16	I	Reset Selection – 8bit mode in 16bit flash. Level sampled during RESET
	MEMWR#	O	PNVM/SRAM write enable (low) – if RS8BIT is active
29	MEMAD[7]	O	PNVM/SRAM address bus outputs
	FCUAD[7]	O	Flash card interface unit output signal FCUIF[17]
	RS_SYSIND[1]	I	General purpose system configuration indication input. Level sampled during RESET
	MEMAD[17]	O	PNVM/SRAM address bus– if RS8BIT is active
30	MEMAD[6]	O	PNVM/SRAM address bus outputs
	FCUAD[6]	O	Flash card interface unit output signal FCUIF[16]
	RS_ADDRSWAP	I	General purpose system configuration indication input. Level sampled during RESET
31	GNDC	S	Digital core ground (of 1.8V and 3.3V supplies)
32	MEMAD[5]	O	PNVM/SRAM address bus outputs
	FCUAD[5]	O	Flash card interface unit output signal FCUIF[15]

Table 1 – Pin functions allocation

Pkg	Pin Functions	Dir	Description
33	MEMAD[4]	O	PNVM/SRAM address bus outputs
	RS8BIT	I	Reset Selection – 8bit only flash is used. Level sampled during RESET
	FCUAD[4]	I/O	Flash card interface unit input/output signal FCUIF[14]
34	MEMAD[3]	O	PNVM/SRAM address bus outputs
	RS_SYSIND[0]	I	General purpose system configuration indication input. Level sampled during RESET
	FCUAD[3]	I/O	Flash card interface unit input/output signal FCUIF[13]
35	VDDP	S	3.3 V Digital periphery power supply
36	MEMAD[2]	O	PNVM/SRAM address bus outputs
	FCUAD[2]	O	Flash card interface unit output signal FCUIF[12]
	RS_BOOTSEL2	I	CPU SW boot (and execute) source selection. Levels sampled during RESET. If BOOTSEL2 is B'1' – CS#0 and CS#1 are swapped.
37	MEMAD[1]	O	PNVM/SRAM address bus outputs
	FCUAD[1]	O	Flash card interface unit output signal FCUIF[11]
	RS_BOOTSEL1	I	CPU SW boot (and execute) source selection. Levels sampled during RESET.
38	MEMAD[19]	O	PNVM/SRAM address bus outputs
	FCUAD[19]	O	Flash card interface unit output signal FCUIF[46]
	FGPIO[6]	I/O	General purpose input/output, monitored/controlled by the V8 SW – if RS8BIT and RS8BIT16 are both <u>not</u> active. Use as output only.
	IGPIO[7]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. Can be used as an interrupt for the CPU – INT3. – if RS8BIT and RS8BIT16 are both <u>not</u> active. Use as output only. Use only as output (see comment below: Retention limitation on Pin 38)
	MEMAD[0]	O	PNVM/SRAM address bus– if RS8BIT is active
39	VDD	S	3.3 V power supply
40	N/A	I/O	N/A
	GPO[68]	O	General purpose output, controlled by the CPU

Table 1 – Pin functions allocation

Pkg	Pin Functions	Dir	Description
41	<i>N/A</i>	I/O	N/A
	<i>GPO[67]</i>	O	General purpose output, controlled by the CPU
42	<i>GND</i>	S	Ground of 3.3 V supply
43	<i>RAMADD[4]</i>	O	SDRAM address bus output
44	<i>RAMADD[3]</i>	O	SDRAM address bus output
45	<i>RAMADD[5]</i>	O	SDRAM address bus output
46	<i>VDDP</i>	S	3.3 V Digital periphery power supply
47	<i>GNDC</i>	S	Digital core ground (of 1.8V and 3.3V supplies)
48	<i>RAMADD[2]</i>	O	SDRAM address bus output
49	<i>RAMADD[6]</i>	O	SDRAM address bus output
50	<i>RAMADD[1]</i>	O	SDRAM address bus output
51	<i>RAMADD[7]</i>	O	SDRAM address bus output
52	<i>VDDC</i>	S	1.8 V Digital core power supply

Bottom wall

53	<i>RAMADD[0]</i>	O	SDRAM address bus output
54	<i>RAMADD[8]</i>	O	SDRAM address bus output
55	<i>RAMADD[10]</i>	O	SDRAM address bus output
56	<i>VDDP</i>	S	3.3 V Digital periphery power supply
57	<i>GNDC</i>	S	Digital core ground (of 1.8V and 3.3V supplies)
58	<i>RAMADD[9]</i>	O	SDRAM address bus output
59	<i>RAMADD[11]</i>	O	SDRAM address bus output
	<i>GPO[64]</i>	O	General purpose output, controlled by the CPU
60	<i>RAMCS[0]#</i>	O	SDRAM chip select (active low)
	<i>RAMBA[1]</i>	O	SDRAM bank select output
61	<i>RAMBA[0]</i>	O	SDRAM bank select output
62	<i>RAMCS[1]#</i>	O	SDRAM chip select (active low)
	<i>GPO[65]</i>	O	General purpose output, controlled by the CPU
63	<i>RAMRAS#</i>	O	SDRAM row select (active low) output

Table 1 – Pin functions allocation

Pkg	Pin Functions	Dir	Description
64	RAMCAS#	O	SDRAM column select (active low) output
65	VDDP	S	3.3 V Digital periphery power supply
66	GNDC	S	Digital core ground (of 1.8V and 3.3V supplies)
67	RAMWE#	O	SDRAM write enable (active low) output
68	RAMDQM	O	SDRAM data masking (active high) output
69	GNDPCLK	S	Digital ground of filtered 3.3 V supply for PCLK
70	PCLK	O	SDRAM clock output (same as internal processing clock)
71	VDDPCLK	S	3.3 V filtered digital power supply for PCLK
72	RAMDAT[8]	I/O	SDRAM bi-directional data bus
73	RAMDAT[7]	I/O	SDRAM bi-directional data bus
74	RAMDAT[9]	I/O	SDRAM bi-directional data bus
75	RAMDAT[6]	I/O	SDRAM bi-directional data bus
76	VDDP	S	3.3 V Digital periphery power supply
77	GNDC	S	Digital core ground (of 1.8V and 3.3V supplies)
78	RAMDAT[10]	I/O	SDRAM bi-directional data bus
79	RAMDAT[5]	I/O	SDRAM bi-directional data bus
80	RAMDAT[11]	I/O	SDRAM bi-directional data bus
81	RAMDAT[4]	I/O	SDRAM bi-directional data bus
82	RAMDAT[12]	I/O	SDRAM bi-directional data bus
83	RAMDAT[3]	I/O	SDRAM bi-directional data bus
84	VDDP	S	3.3 V Digital periphery power supply
85	GNDC	S	Digital core ground (of 1.8V and 3.3V supplies)
86	RAMDAT[13]	I/O	SDRAM bi-directional data bus
87	RAMDAT[2]	I/O	SDRAM bi-directional data bus
88	VDDC	S	1.8 V Digital core power supply
89	RAMDAT[14]	I/O	SDRAM bi-directional data bus
90	RAMDAT[1]	I/O	SDRAM bi-directional data bus
91	RAMDAT[15]	I/O	SDRAM bi-directional data bus
92	RAMDAT[0]	I/O	SDRAM bi-directional data bus
93	VDDP	S	3.3 V Digital periphery power supply (208 pin only)

Table 1 – Pin functions allocation

Pkg	Pin Functions	Dir	Description
94	RAMDQM2	O	SDRAM data masking (active high) output
	RAMCKE	O	Clock enable signal to the SDRAM (for power down)
	GPO[66]	O	General purpose output, monitored/controlled by the CPU
95	GNDC	S	Digital core ground (of 1.8V and 3.3V supplies)
96	GPIO[10]	I/O	General purpose input/output, monitored/controlled by the CPU
	SDI_PSC	I	Serial Data input for the DDX Core (supply measurement)
	RAMCKE_2	O	Second appearance of RAMCKE
97	GPAIO	I/O	General purpose input/output, to/from the ADP SW
	IGPIO[11]	I/O	General purpose input/output, monitored/controlled by the CPU. Can be used as an interrupt for the CPU – INTO.
98	APWM[7]_P	O	Audio PWM #7 – Positive
	GPIO[12]	I/O	General purpose input/output, monitored/controlled by the CPU
	VID[0]	O	Digital Video Out
99	APWM[7]_N	O	Audio PWM #7 – Negative
	GPIO[13]	I/O	General purpose input/output, monitored/controlled by the CPU
	VID[1]	O	Digital Video Out
100	APWM[6]_P	O	Audio PWM #6 – Positive
	GPIO[14]	I/O	General purpose input/output, monitored/controlled by the CPU
	VID[2]	O	Digital Video Out
101	APWM[7]_P	O	Audio PWM #7 – Positive
	APWM[6]_N	O	Audio PWM #6 – Negative
	GPIO[15]	I/O	General purpose input/output, monitored/controlled by the CPU
	VID[3]	O	Digital Video Out
102	APWM[5]_P	O	Audio PWM #5 – Positive

Table 1 – Pin functions allocation

Pkg	Pin Functions	Dir	Description
	GPIO[16]	I/O	General purpose input/output, monitored/controlled by the CPU
	VID[4]	O	Digital Video Out
103	APWM[5]_N	O	Audio PWM #5 – Negative
	GPIO[17]	I/O	General purpose input/output, monitored/controlled by the CPU.
	VID[5]	O	Digital Video Out
104	AIN[1]	I	Serial input of digital stereo audio
	SPDIFIN[1]	I	S/PDIF receiver input for digital coded or reconstructed audio data
	IGPIO[18]	I/O	General purpose input/output, monitored/controlled by the CPU. Can be used as an interrupt for the CPU – INT1.

Right wall

105	VDDP	S	3.3 V Digital periphery power supply
106	APWM[4]_P	O	Audio PWM #4 – Positive
	PWMCO[5]	O	PWM4 output signal
	VID[6]	O	Digital Video Out
	GPIO[19]	I/O	General purpose input/output, monitored/controlled by the CPU
107	APWM[4]_N	O	Audio PWM #4 – Negative
	VID[7]	O	Digital Video Out
	CLK1	O	CLK1
	APWM[6]_P	O	Audio PWM #6 – Positive
	GPIO[20]	I/O	General purpose input/output, monitored/controlled by the CPU
108	APWM[3]_P	O	Audio PWM #4 – Positive
	APWM[6]_P	O	Audio PWM #6 – Positive
	VSYNC#	O	Digital Video Output - vertical sync output signal
	GPIO[21]	I/O	General purpose input/output, monitored/controlled by the CPU
109	APWM[3]_N	O	Audio PWM #3 – Negative
	APWM[7]_P	O	Audio PWM #7 – Positive
	AOUT[3]	O	Serial output of digital stereo audio

Table 1 – Pin functions allocation

Pkg	Pin Functions	Dir	Description
	HSYNC#	O	Digital Video Output - horizontal sync output signal
	GPIO[22]	I/O	General purpose input/output, monitored/controlled by the CPU
110	GNDC	S	Digital core ground (of 1.8V and 3.3V supplies)
111	APWM[2]_P	O	Audio PWM #2 – Positive
	FGPIO[7]	I/O	General purpose input/output, monitored/controlled by the V8 SW
	IGPIO[23]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. Can be used as an interrupt for the CPU – INT2.
112	APWM[2]_N	O	Audio PWM #2 – Negative
	APWM[2]_N	O	Audio PWM #2 – Negative
	APWM[3]_P	O	Audio PWM #3 – Positive
	AOUT[2]	O	Serial output of digital stereo audio
	VCLKx2	I/O	Digital video clock input/output. 27 MHz (for SD interlaced) or 54 MHz (for SD progressive)
	MEMCS[1]#	O	If BOOTSEL2 == '0' and selected by IOConfig
	MEMCS[0]#	O	If BOOTSEL2 == '1' and selected by IOConfig
	COSYNC	O	Composite sync output. Active only when component analog output is selected
	GPIO[24]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
113	APWM[1]_P	O	Audio PWM #1 – Positive
	GPIO[25]	I/O	General purpose input/output, monitored/controlled by the CPU
114	APWM[1]_N	O	Audio PWM #1 – Negative
	APWM[4]_P	O	Audio PWM #4 – Positive
	AOUT[1]	O	Serial output of digital stereo audio
	GPIO[26]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW

Table 1 – Pin functions allocation

Pkg	Pin Functions	Dir	Description
115	APWM[0]_P	O	Audio PWM #0 – Positive
	GPIO[27]	I/O	General purpose input/output, monitored/controlled by the CPU
116	APWM[0]_N	O	Audio PWM #0 – Negative
	APWM[5]_P	O	Audio PWM #4 – Positive
	AOUT[0]	O	Serial output of digital stereo audio
	GPIO[28]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
117	GNDC-A2	S	Digital core ground (of 1.8V and 3.3V supplies)
118	AMCLK	I/O	Audio Master Clock input/output. 128, 192, 256 or 384 times the sampling frequency (programmable)
	GPIO[29]	I/O	General purpose input/output, monitored/controlled by the CPU
119	VDDP-A2	S	3.3 V filtered digital power supply for AMCLK
120	ALRCLK	O	Digital audio left/right select output for the audio port. Square wave, at the sampling frequency. Programmable polarity
	GPIO[30]	I/O	General purpose input/output, monitored/controlled by the CPU
121	ABCLK	O	Digital audio bit-clock output. Data on AOUT and AIN is output or latched, respectively, with the rising or falling (programmable) edge of this clock
	GPIO[31]	I/O	General purpose input/output, monitored/controlled by the CPU
122	SPDIFOUT	O	S/PDIF transmitter output for digital coded or reconstructed audio data
	GPIO[32]	I/O	General purpose input/output, monitored/controlled by the CPU
	SPDIFIN[2]	I	S/PDIF receiver input for digital coded or reconstructed audio data
123	SPDIFIN[3]	I	S/PDIF receiver input for digital coded or reconstructed audio data
	AIN[2]	I	Serial input of digital stereo audio
	GPIO[33]	I/O	General purpose input/output, monitored/controlled by the CPU
124	GPIO[34]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW

Table 1 – Pin functions allocation

Pkg	Pin Functions	Dir	Description
	<i>SPDIFIN[4]</i>	I	S/PDIF receiver input for digital coded or reconstructed audio data
	<i>RAMCKE_3</i>	O	Clock enable signal to the SDRAM (for power down)
	<i>DVDDAT[7]</i>	I	DVD DSP interface input
125	<i>GPIO[35]</i>	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	<i>DVDDAT[6]</i>	I	DVD DSP interface input
	<i>VID[0]_2</i>	O	Digital Video Out
126	<i>GPIO[36]</i>	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	<i>DVDDAT[5]</i>	I	DVD DSP interface input
	<i>VID[1]_2</i>	O	Digital Video Out
127	<i>IGPIO[37]</i>	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. Can be used as an interrupt for the CPU – INT4.
	<i>FGPIO[4]</i>	I/O	General purpose input/output, monitored/controlled by the V8 SW
	<i>DVDDAT[4]</i>	I	DVD DSP interface input
	<i>VID[2]_2</i>	O	Digital Video Out
	<i>CPUNMI_2</i>	I	CPU non-maskable interrupt input
128	<i>GPIO[38]</i>	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	<i>DVDDAT[3]</i>	I	DVD DSP interface input
	<i>VID[3]_2</i>	O	Digital Video Out
129	<i>GPIO[39]</i>	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	<i>DVDDAT[2]</i>	I	DVD DSP interface input
	<i>VID[4]_2</i>	O	Digital Video Out
130	<i>GPIO[40]</i>	I/O	General purpose input/output, monitored/controlled by the CPU
	<i>DVDDAT[1]</i>	I	DVD DSP interface input

Table 1 – Pin functions allocation

Pkg	Pin Functions	Dir	Description
131	GPIO[41]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	FGPIO[0]	I/O	General purpose input/output, monitored/controlled by the V8 SW
	SSCRXD	I	SSC data input.
	VID[5]_2	O	Digital Video Out
	CPUNMI	I	CPU non-maskable interrupt input
132	GPIO[42]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	FGPIO[1]	I/O	General purpose input/output, monitored/controlled by the V8 SW
	SSCCLK	O	SSC clock output.
	VID[6]_2	O	Digital Video Out
133	GPIO[43]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	FGPIO[2]	I/O	General purpose input/output, monitored/controlled by the V8 SW
	VID[6]_2	O	Digital Video Out
	SSCTXD	O	Serial Interface output
134	IGPIO[44]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. Can be used as an interrupt for the CPU – INT5.
	FGPIO[3]	I/O	General purpose input/output, monitored/controlled by the V8 SW
135	VDDP	S	3.3 V Digital periphery power supply
136	DUPTD0	O	Main debug UART data output
	GPIO[45]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	PWMCO[5]_3	O	PWM5 output signal (for SCART control)
137	DUPRD0	I	Main debug UART data input
	GPIO[46]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
138	DUPTD1	O	Second debug UART data output
	GPIO[47]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
139	DUPRD1	I	Main debug UART data input

Table 1 – Pin functions allocation

Pkg	Pin Functions	Dir	Description
	GPIO[48]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
140	VDDC	S	1.8 V Digital core power supply
141	GNDC	S	Digital core ground (of 1.8V and 3.3V supplies)
142	RESET#	ID	Reset input (active low)
143	GNDA	S	Ground plane of internal PLL circuit
144	VDDA	S	1.8 V Power supply for internal PLL circuit
145	XO	AO	Output to a crystal that is connected to XI . If a crystal is not used at XI , XO must be left not connected
146	XI	ID	27.000MHz clock generator or crystal input for the PLL
147	DAC5	AO	CVBS/C/Y - Analog video output - can be selected to be CVBS, C or Y.
148	GNDDACD	S	Ground for the video DACs 3.3 V analog power supply
149	DAC4	AO	CVBS/G/Y - Analog video output that can be selected to be CVBS, G or Y.
150	VDDDAC	S	3.3 V Analog power supply for the video DACs
151	DAC3	AO	CVBS/C/Y - Analog video output that can be selected to be CVBS, C or Y.
152	DAC2	AO	Y/R/V/C - Analog video output that can be selected to be Y, or R/V or C.
153	VDDDAC	S	3.3 V Analog power supply for the video DACs
154	DAC1	AO	C/B/U - Analog video output that can be selected to be C or B or U.
155	RSET	AI/O	Resistive load for gain adjustment of the DACs
156	GNDDABS2	S	Common Ground for the video and SERVO DACs

Top wall

157	RFINP	AI	RF positive input signal (differential input) // RF input signal (single ended)
158	RFINN	AI	RF negative input signal (differential input) // RF reference input signal
159	VDDAFE	S	Analog AFE 3.3 V supply

Table 1 – Pin functions allocation

Pkg	Pin Functions	Dir	Description
160	<i>ADCIN[A]</i>	AI	ADC input signal (e.g. from OPU)
161	<i>ADCIN[B]</i>	AI	ADC input signal (e.g. from OPU)
162	<i>VDDAFE</i>	S	Analog AFE 3.3 V supply
163	<i>ADCIN[C]</i>	AI	ADC input signal (e.g. from OPU)
164	<i>ADCIN[D]</i>	AI	ADC input signals (e.g. from OPU)
165	<i>ADCIN[J]</i>	AI	ADC input signals (e.g. from OPU)
166	<i>ADCIN[E]</i>	AI	ADC input signals (e.g. from OPU)
167	<i>ADCIN[K]</i>	AI	ADC input signals (e.g. from OPU)
168	<i>ADCIN[F]</i>	AI	ADC input signals (e.g. from OPU)
169	<i>GNDAFE</i>	S	Analog ADC (AFE) ground of 3.3 V supply
170	<i>ADCIN[G]</i>	AI	ADC input signals (e.g. from OPU)
171	<i>ADCIN[H]</i>	AI	ADC input signals (e.g. from OPU)
172	<i>GND1AFE</i>	S	Analog ADC (AFE) ground of 3.3 V supply
173	<i>OPUREF</i>	AO	VC - OPU reference voltage output
174	<i>VREF</i>	AI/ O	Capacitive load for internal band-gap voltage generation
175	<i>RESLOAD</i>	AI/ O	Resistive load for internal reference voltage generation
176	<i>GNDAFER</i>	AI	AFE analog reference voltage ground
177	<i>VDDSAFE</i>	S	Analog AFE 3.3 V supply shield
178	<i>CDMD</i>	AI	CD LASER monitor diode input
179	<i>DVDMD</i>	AI	DVD LASER monitor diode input
180	<i>CDLD</i>	AO	CD LASER diode drive output
181	<i>DVDLD</i>	AO	DVD LASER diode drive output
182	<i>PWMCO[0]</i>	O	PWM output signal – focus PWM
	<i>GPIO[49]</i>	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	<i>DVDDAT[0]</i>	I	DVD DSP interface input
	<i>RFDAT[0]</i>	I	RF channel sample data input for RF by-pass
183	<i>VDDPWMS</i>	S	3.3 V SERVO PWM power supply

Table 1 – Pin functions allocation

Pkg	Pin Functions	Dir	Description
184	PWMCO[1]	O	PWM output signal – track PWM
	GPIO[50]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	DVDSTRB	I	AV bit strobe input. Programmable polarity
	RFDAT[1]	I	RF channel sample data input for RF by-pass
185	GNDPWMS	S	SERVO PWMs ground of 3.3V supply
186	PWMCO[2]	O	PWM output signal – spindle PWM
	GPIO[51]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	DVDVALID	I	AV data valid input for FE by-pass. Programmable polarity
187	PWMCO[3]	O	PWM output signal – sled PWM
	GPIO[52]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	DVDSOS	I	AV start of sector indication input for FE by-pass. Programmable polarity
188	PWMCO[4]	O	PWM output signal
	GPIO[53]	I/O	General purpose input/output, monitored/controlled by the CPU
	DVDERR	I	AV error indication input for FE by-pass. Programmable polarity
	RFDAT[4]	I	RF channel sample data inputs for RF by-pass
189	IGPIO[54]	I/O	General purpose input/output, monitored/controlled by the CPU. Can be used as an interrupt for the CPU – INT6.
	DVDREQ	O	AV data request output for FE by-pass. Programmable polarity
	RFDAT[5]	I	RF channel sample data inputs for RF by-pass
190	VDDC	S	1.8 V Digital core power supply
191	GNDC	S	Digital core ground (of 1.8V and 3.3V supplies)
192	IGPIO[55]	I/O	General purpose input/output, monitored/controlled by the CPU. Can be used as an interrupt for the CPU – INT7.

Table 1 – Pin functions allocation

Pkg	Pin Functions	Dir	Description
	FCUIRQ	I	Card interrupt input
	RFCLK	O	RF channel sampling clock output for RF by-pass
193	GPIO[56]	I/O	General purpose input/output, monitored/controlled by the CPU
	FCURST	O	Card reset output
194	GPIO[57]	I/O	General purpose input/output, monitored/controlled by the CPU
	FCUWAIT#	I	Card wait (not ready) signal input – FCUIF[30]
195	GPIO[58]	I/O	General purpose input/output, monitored/controlled by the CPU
	FCUCS[3]#	O	Flash card interface unit output signal
196	GPIO[59]	I/O	General purpose input/output, monitored/controlled by the CPU
	FCUCS[2]#	O	Flash card interface unit output signal
197	GPIO[60]	I/O	General purpose input/output, monitored/controlled by the CPU
	FCUSCLK	O	Flash card interface unit output signal - FCUIF[34]
198	GPIO[61]	I/O	General purpose input/output, monitored/controlled by the CPU
	FCUIOWR#	O	Flash card interface unit output signal - FCUIF[33]
199	GPIO[62]	I/O	General purpose input/output, monitored/controlled by the CPU
200	MEMCS[2]#	O	PNVM/SRAM chip select (active low) output
	GPIO[63]	I/O	General purpose input/output, monitored/controlled by the CPU
	MEMMSB	O	PNVM/SRAM m.s. byte select output
	FCUAD[20]	O	Flash card interface unit input/output signal FCUIF[50]
201	MEMAD[0]	O	PNVM/SRAM address bus outputs
	MEMAD[-1]	O	PNVM/SRAM address bus outputs – lower address bit (byte select) in case of 8bit flash
	FCUAD[20]	I/O	Flash card interface unit input/output signal FCUIF[50]
202	MEMCS[0]#	O	PNVM/SRAM chip select (active low) output
	FCUCS[0]#	O	Flash card interface unit output signal FCUIF[38]
	MEMCS[1]#	O	If BOOTSEL2 == '1'

Table 1 – Pin functions allocation			
Pkg	Pin Functions	Dir	Description
203	MEMRD#	O	PNVM/SRAM read enable (active low) output
	FCUOE	O	Flash card interface unit output signal
204	MEMDA[0]	I/O	PNVM/SRAM bi-directional data bus
	FCUDA[0]	I/O	Flash card interface unit input/output signal FCUIF[2]
205	MEMDA[8]	I/O	PNVM/SRAM bi-directional data bus
	GPIO[8]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW – only if RS8BIT is active
	MEMDA[1]	I/O	PNVM/SRAM bi-directional data bus (if 160 pin package)
	FCUDA[8]	I/O	Flash card interface unit input/output signal FCUIF[2]
206	MEMDA[1]	I/O	PNVM/SRAM bi-directional data bus
	MEMDA[2]	I/O	PNVM/SRAM bi-directional data bus (if 160 pin package)
	FCUDA[1]	I/O	Flash card interface unit input/output signal FCUIF[2]
207	MEMDA[9]	I/O	PNVM/SRAM bi-directional data bus
	GPIO[9]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW – only if RS8BIT is active
	CLK1_2	O	CLK1_2 – only if RS8BIT is active
	MEMDA[3]	I/O	PNVM/SRAM bi-directional data
	FCUDA[9]	I/O	Flash card interface unit input/output signal FCUIF[2]
208	VDDP	S	3.3 V Digital periphery power supply

Comments:

Retention limitation on Pin 38 it is forbidden to use this pin as input. Both functions on this pin – **FGPIO[6]** and **IGPIO[7]** can be used as outputs without limitation.

5 DC and AC Characteristics

This section does not include specs of the RF amplifier, servo amplifier and loader interface signals which appear in the separate **FE** T-specs document.

5.1 Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
VDDP, VDDP-IP, VDDP-A2, VDDDAC, VDDDACs	-0.5V to + 4.6V
VDDAFERF, VDDAFES, VDDPWMS supply voltage to ground	
VDDC, VDDA supply voltage to ground	-0.5V to + 3.6V
DC voltage applied to digital outputs for high impedance output state (all digital output pins apart from SDRAM, VID[7-0] , VCLKx2 and S/PDIFOUT pins)	-0.5V to +5.5V
DC voltage applied to digital outputs for high impedance output state (SDRAM, VID[7-0] , VCLKx2 and S/PDIFOUT pins), or analog output	-0.5V to +3.6V
DC voltage applied to digital inputs (all digital input pins apart from SDRAM, VID[7-0] , VCLKx2 and S/PDIFOUT and pins)	-0.5V to 5.5V
DC voltage applied to digital inputs (SDRAM, VID[7-0] , VCLKx2 and S/PDIFOUT and pins), or analog inputs)	-0.5V to 3.6 V
DC output current, into output (apart from DACs)	20mA/output (total 200 mA)
DC input current	-10mA to +3.0mA

NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

5.2 Operating Range

Temperature	$0^{\circ}\text{C} < T_A < +70^{\circ}\text{C}$
VDDP, VDDP-IP, VDDP-A2, VDDDAC, VDDDACs	$3.15\text{V} < V_{PP} < 3.45\text{V}$
VDDAFERF, VDDAFES, VDDPWMS Supply Voltage (3.3V supply)	
VDDC, VDDA Supply Voltage (1.8V supply)	$1.7\text{ V} < V_{CC} < 1.9\text{ V}$

5.3 DC Characteristics

Table 2. DC characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
V _{IL}	Digital input low voltage	-0.5	0.8	V	
V _{IH}	Digital input high voltage	2	5.5	V	

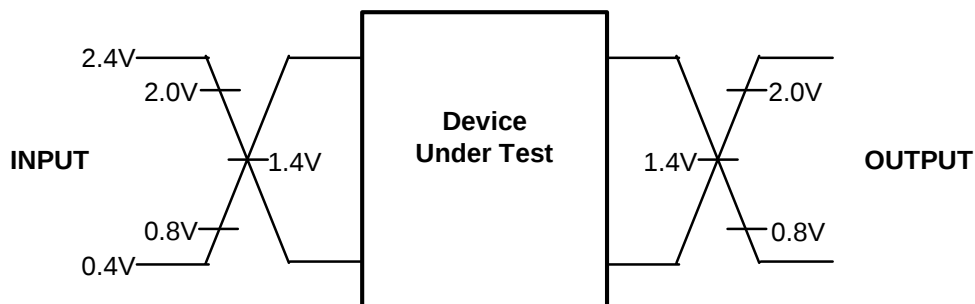
Table 2. DC characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
	(for all input pins, apart from the SDRAM, VID[7-0] , VCLKx2 and S/PDIFOUT)				
V _{IH}	Digital input high voltage (for the SDRAM, VID[7-0] , VCLKx2 and S/PDIFOUT pins)	2	3.6	V	
V _{OL}	Digital output low Voltage	-	0.4	V	I _{OL} = 2 mA
V _{OH}	Digital output high voltage (for driven pins)	2.4	-	V	I _{OH} = 0.4 mA
V _{OHP}	Digital output high voltage (for externally pulled up to 5V pins)	3.5	-	V	1 KOhm pull-up resistor, 50 nSec after pin release
I _{CC18}	Power Supply Current, 1.8V supply	-	270	mA	f = 135 MHz VCC = 1.9V VPP = 3.45V
I _{CC33}	Power Supply Current, 3.3V supply	-	360	mA	f = 135 MHz VPP = 3.45V VCC = 1.9V
I _{LI}	Input Leakage Current	--	10	uA	
I _{LIP}	Input Leakage Current (internally pulled pins)	25	180	uA	Min value indicates the min "strength" of the "pull"
C _{IN}	Input Capacitance	-	10	pF	
C _{IO}	I/O and Output Capacitance	-	10	pF	Garentee by design

5.4 Digital Interface Timing Specifications

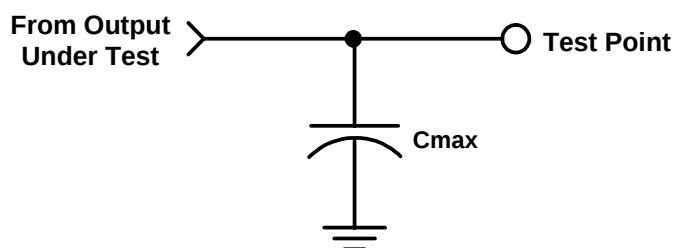
The timing characteristics in this section are given from the external devices stand point.

When the timing depend on the process clock (PCLK), the min or max column is specified for 135 MHz. In these cases, the Comment column indicate the dependency where "P" is one PCLK cycle.



During AC testing, inputs are driven at 0.4V and 2.4V levels. Unless otherwise specified, switching times are measured between the 1.4V, 0.8V or 2.0V levels at the input/output.

Figure 2. AC testing input and output



During AC testing, unless otherwise specified, outputs are loaded as described in this figure. Cmax is given in the following table.

Figure 3. Normal AC test load

Table 3. Max loading capacitance

Pins	Cmax	Comment
<i>ABCLK, ALRCLK</i>	80 pF	
<i>VCLKx2</i>	30 pF	
SDRAM	15 pF	
All other interfaces	50 pF	

Note that the I/O HW of the **Vaddis 966-D** limit all digital outputs, apart from the SDRAM interface and (for I76-H) the digital video port, to 40 MHz.

5.4.1 Digital Video Interface Timing

Table 4. Digital video interface timing

	Description	Min [ns]	Max [ns]	Comment
t_{VCP}	VCLKx2 period	37		For 27 MHz
t_{VCH}	VCLKx2 high time	15		For 27 MHz
t_{VCL}	VCLKx2 low time	15		For 27 MHz
t_{VCP}	VCLKx2 period	18.5		For 54 MHz
t_{VCH}	VCLKx2 high time	5		For 54 MHz
t_{VCL}	VCLKx2 low time	5		For 54 MHz
t_{VCR}	VCLKx2 rise time		4	For 27 or 54 MHz
t_{VCF}	VCLKx2 fall time		4	For 27 or 54 MHz

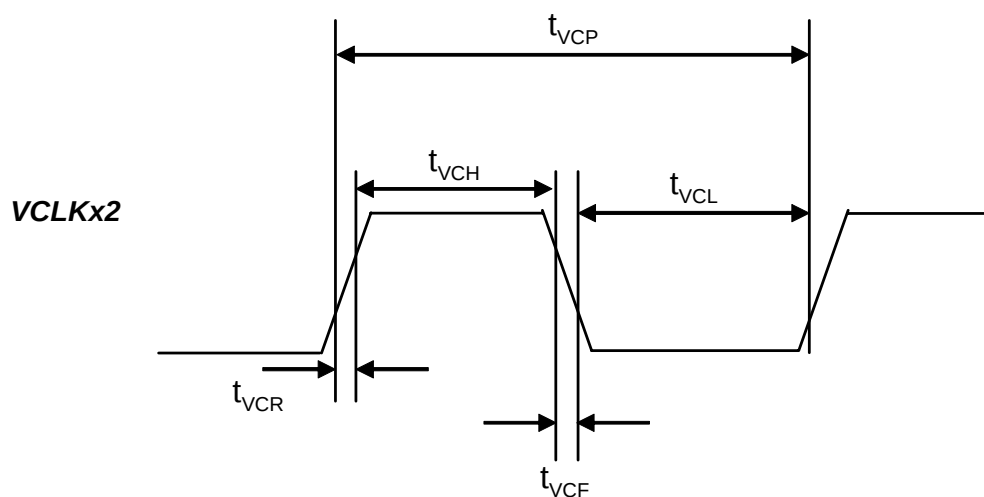


Figure 4. **VCLKx2** Timing

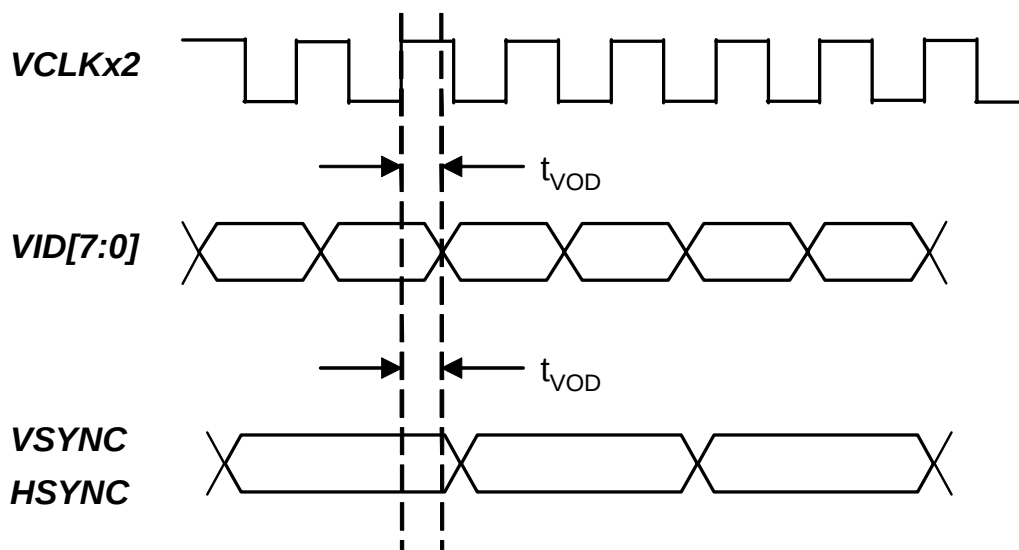


Figure 5. Digital video interface timing

5.4.2 AV Interface Timing

Table 5. AV (parallel port) timing

	Description	Min [ns]	Max [ns]	Comment
t_{DSTRB}	Time between two consecutive DVDSTRB edges	40		4P
t_{DH}, t_{DL}	DVDSTRB signal high and low	12		1.5P
t_{DOD}	DVDREQ output delay after DVDSTRB		15	When synchronized
t_{DIS}	Input set-up time before DVDSTRB	9		
t_{DIH}	Output hold time after DVDSTRB	3		

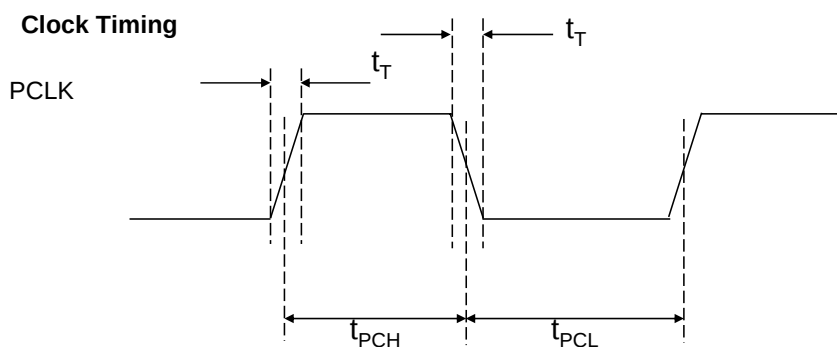


Figure 6. AV Bitstream interface timing

5.4.3 Audio Interface Timing

Table 6. Audio port timing

	Description	Min [ns]	Max [ns]	Comment
t_{AUD0}	AMCLK period	20		
t_{AUD1}	AMCLK high width	45%	55%	Percentage of duty cycle of AMCLK
t_{AUD2}	AMCLK low width	45%	55%	Percentage of duty cycle of AMCLK
t_{AUD3}	ABCLK period	80		
t_{AUD4}	ABCLK high width	45%	55%	Percentage of duty cycle of ABCLK
t_{AUD5}	ABCLK low width	45%	55%	Percentage of duty cycle of ABCLK
t_{AUD6}	AOUT and ALRCLK delay time from ABCLK		25	Measured from selected sampling edge of ABCLK .
t_{AUD7}	AIN set-up time before ABCLK	15		Measured from selected sampling

Table 6. Audio port timing

	Description	Min [ns]	Max [ns]	Comment
				edge of ABCLK .
t_{AUD8}	AIN hold time after ABCLK	15		Measured from selected sampling edge of ABCLK .

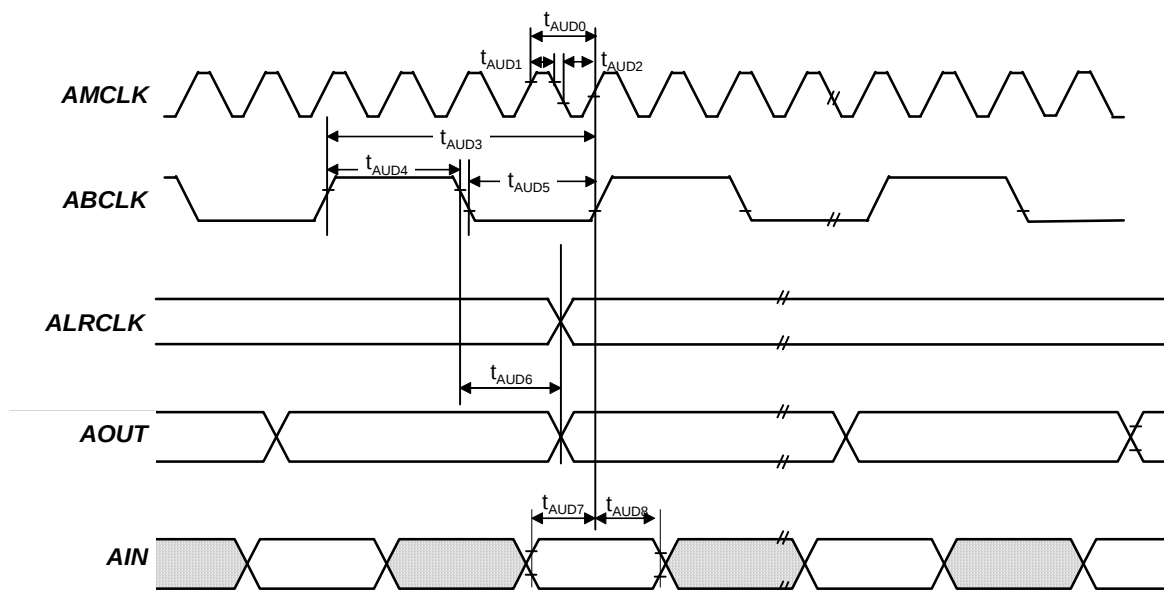


Figure 7. Audio port timing

5.4.4 SDRAM Interface Timing (Update with TRAS -7)

Table 7. SDRAM interface timing for PCLK of 135 MHz

	Description	Min [ns]	Max [ns]	Comment
t_{OD}	Output delay	1	5	
t_{IH}	Input hold	1.5		
t_{IS}	Input set-up	1.4		
t_{TR}	transition time		1	
t_{PCH}	PCLK high	3.9		
t_{PCL}	PCLK low	3.9		

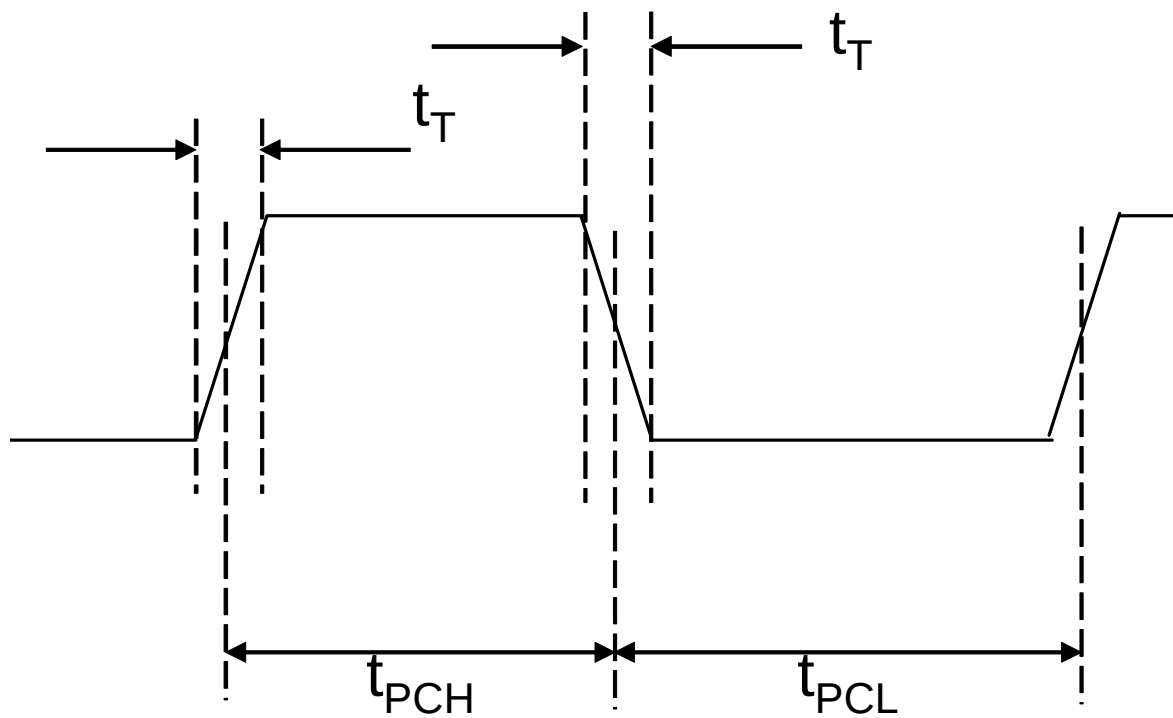


Figure 8. SDRAM clock timing

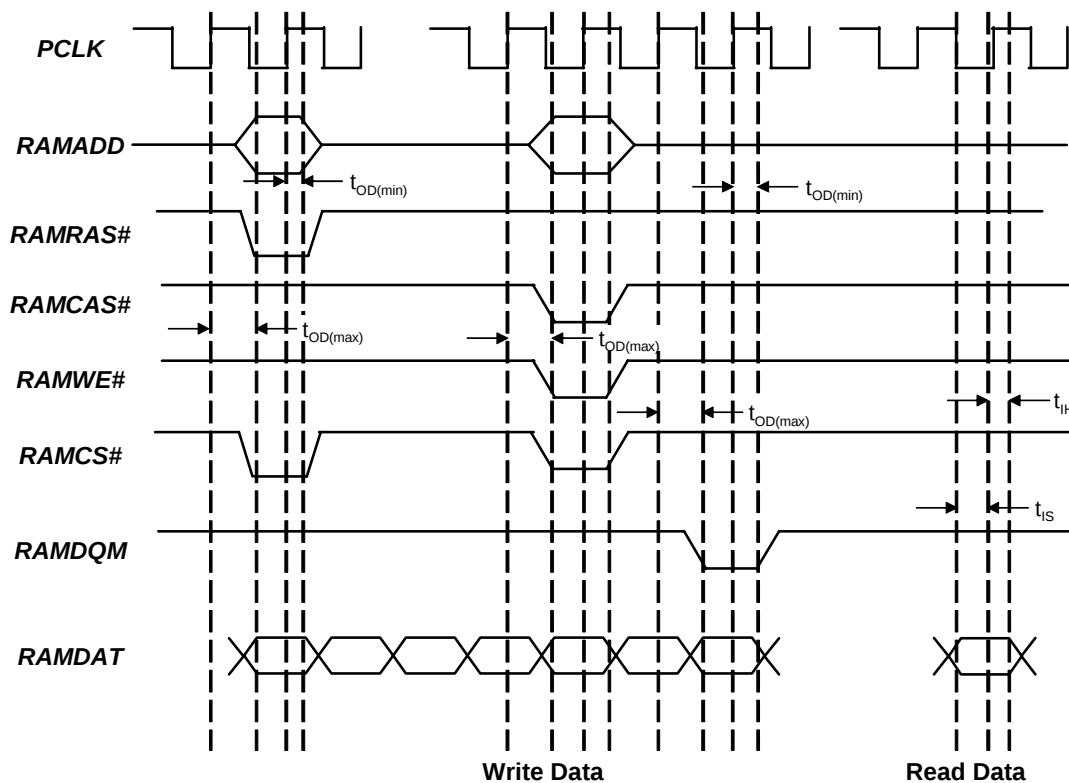
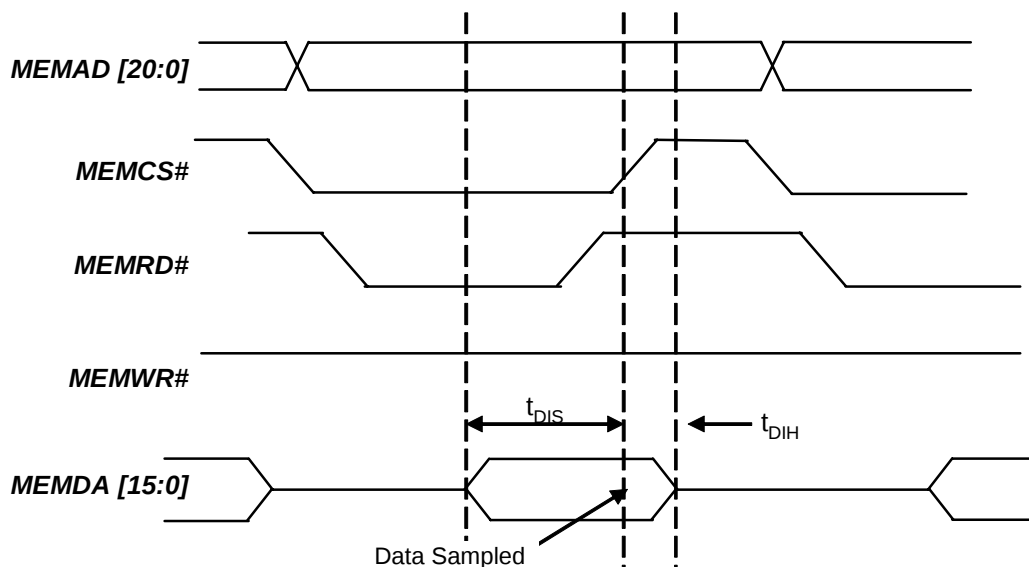
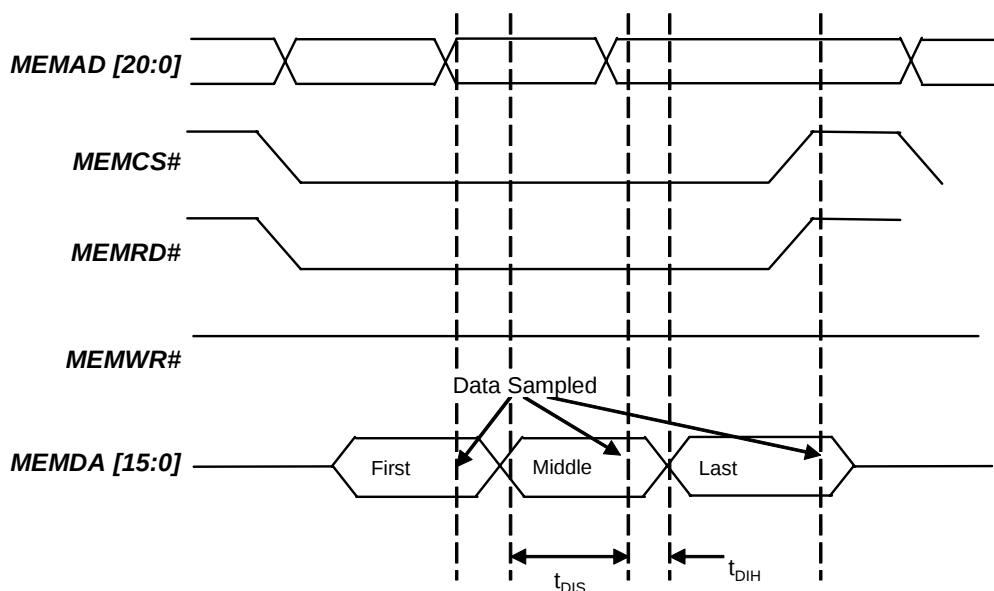


Figure 9. SDRAM interface timing

5.4.5 PNVM (NOR Type Flash, EPROM, OTP ROM and Masked ROM) Interface Timing

Table 8. NOR type Flash, EPROM, OTP ROM and Masked ROM interface timing

	Description	Min [ns]	Max [ns]	Comment
t_{DIS}	MEMDA set-up time before MEMAD change (when <i>XMIFConfig</i> [5]=B'0'), or MEMCS# de-activation (when <i>XMIFConfig</i> [5]=B'1')	25		
t_{DIH}	MEMDA hold time after MEMAD change (when <i>XMIFConfig</i> [5]=B'0'), or MEMCS# de-activation (when <i>XMIFConfig</i> [5]=B'1')	0		

Figure 10. PNV read cycle (when $XMConfig[5]$ equal B'1')Figure 11. PNV read cycle (when $XMConfig[5]$ equal B'0')

5.4.6 SSC Interface Timing

Table 9. SSC serial interface timing

	Description	Min [ns]	Max [ns]	Comment
t_{DIS}	SSCRXD input set-up time before SSCCLK sampling edge	3*P		
t_{DIH}	SSCRXD input hold time after SSCCLK sampling edge	3*P		
t_{DOD}	SSCTXD output delay time after SSCCLK non-sampling edge	0	8*P	
t_{CLP}	SSCCLK period	20*P		
t_{CLD}	First SSCCLK edge after <i>SSCInterface-Busy</i> change from B'0' to B'1'.	8*P		Guarantee by Design

5.4.7 GPIO Interface Timing

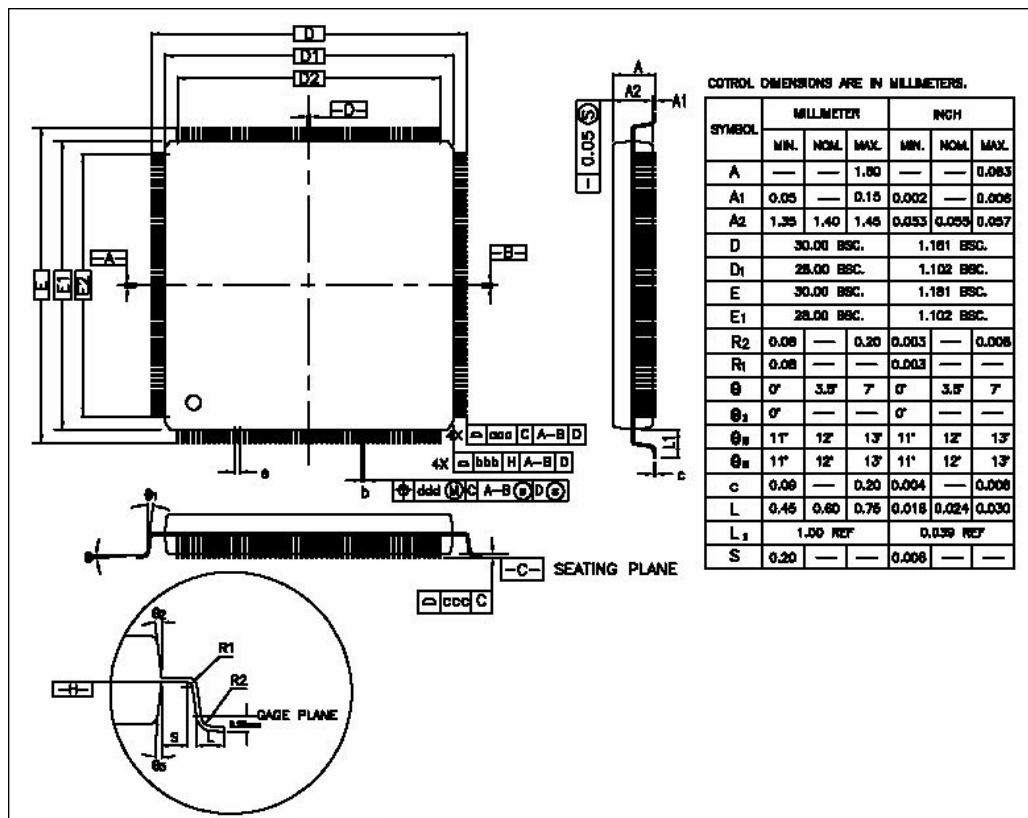
Table 10. GPIO interface timing

	Description	Min [ns]	Max [ns]	Comment
t_{COD}	GPIO output signals delay after <i>GPIONDir</i> or <i>GPIONData</i> CPU parameters write	0	40	
t_{RIS}	GPIO input signals set-up time before <i>GPIONData</i> CPU parameters read	0	30	

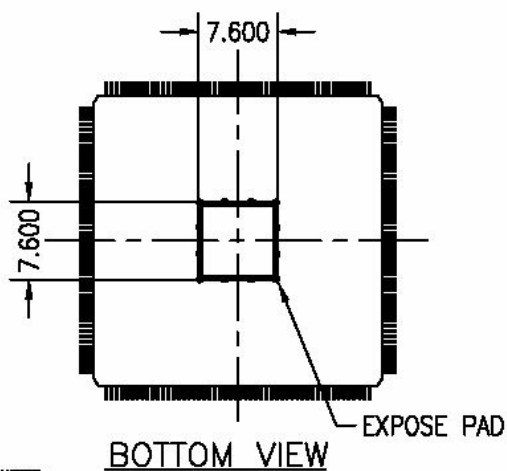
5.5 Analog Interface Specifications

6 Package information

Green package



Proprietary and Confidential Information



SYMBOL	208L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	26.50			1.003		
E2	26.90			1.003		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.