

Features

- 12-channel integrated transimpedance and limiting amplifier operates up to 6.25 Gb/s
- 12 μA_{PP} receiver sensitivity for 10^{-12} BER at 6.25 Gb/s
- Single +3.3 V supply dissipating 140 mW per channel
- Selectable analog multiplexer provides junction temperature, supply voltage, and received signal strength for each channel
- Individual channel signal detect compares input signal strength with adjustable threshold
- Squelch automatically disables output when input signal strength falls below programmable threshold
- 2-wire interface provides access to internal registers
- CML output with selectable pre-emphasis and output amplitude control
- 250-micron channel pitch matches optical ribbon fiber and photodiode arrays
- IC dimensions 2245 x 3870 μm

Applications

- Single data rate (SDR) and double data rate (DDR) XAUI
- Single data rate (SDR) and double data rate (DDR) Infiniband®
- 1G, 2G, 4G Fiber Channel
- Gigabit Ethernet
- PCI Express 1.0 and 2.0
- SNAP12 optical modules
- Proprietary and CWDM parallel optical modules

Description

The growing use of the Internet has created increasingly higher demand for multi-Gb/s I/O performance. The demand for 40 Gb/s bandwidth and beyond fuels the growth of short-reach 10 Gb/s infrastructures within high-end telco and datacom routers, switches, servers and other proprietary chassis-to-chassis links.

The transimpedance amplifier achieves a nominal 5 GHz bandwidth over a wide range of photodiode input capacitance. Excellent channel-to-channel isolation ensures data integrity at the receiver sensitivity limits. An internal circuit provides the photodiode reverse bias voltage supply and senses average photocurrent supplied to the photodiode array.

The transimpedance amplifier is AC-coupled internally to a high-gain, high-bandwidth, differential, limiting amplifier. The limiting amplifier provides a differential back-terminated CML output that can be used to drive 6.25 Gb/s per channel transceivers or other CML compatible clock and data recovery circuits. The CML output provides selectable pre-emphasis control to improve signal quality. The limiting amplifier features a circuit that senses optical modulation amplitude (OMA) to determine a loss of signal.

A selectable analog multiplexer provides junction temperature, supply voltage, and received signal strength for each channel to enable optical module diagnostic features.

Data controlling the Zarlink ZL62089 is loaded by a simple 2-wire serial interface reducing the number of pins required of a microcontroller.

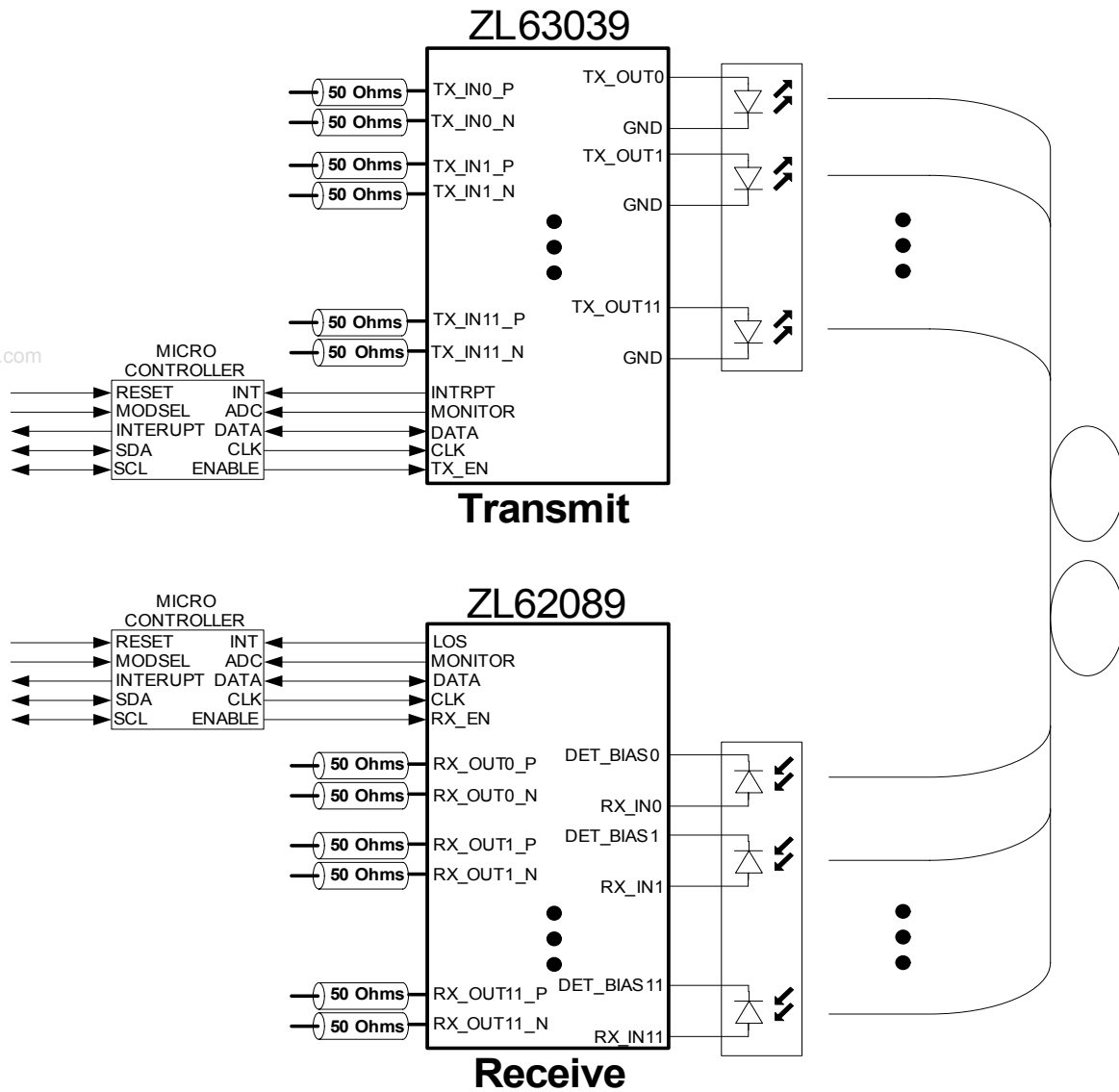


Figure 1: Application Block Diagram Utilizing the ZL63039 VCSEL Driver and the ZL62089 Optical Receiver

Functional Description

The Zarlink ZL62089 receiver is a patented twelve-channel, monolithic SiGe BiCMOS integrated circuit that combines high-sensitivity transimpedance amplifiers with high-gain limiting amplifiers to provide a complete twelve-channel optical networking receiver, as illustrated in Figure 2. Other features include per-channel signal detect, channel enable, and output pre-emphasis independently controllable for each channel.

The transimpedance amplifier is a high-bandwidth, low-noise design that provides 5 GHz bandwidth over a wide range of photodiode input capacitance. This enables cost-effective optical receiver module designs by allowing the use of large aperture photodiodes with simplified optical coupling and alignment requirements. The transimpedance amplifier is insensitive to input capacitance and impedance variations to further enable robust optical receiver designs.

www.DataSheet4U.com

The Zarlink ZL62089 contains a programmable signal detect circuit that compares the input optical modulated amplitude (OMA) against a selectable threshold to determine a valid signal. When the input falls below the selectable threshold the ZL62089 asserts an external interrupt and trips the loss of signal channel register bit. The ZL62089 also has a squelch feature that disables the channel when a loss of signal condition is recognized.

The transimpedance amplifier is DC-coupled internally to a multi-stage differential limiting amplifier. The limiting amplifier features an internal offset control loop to ensure peak receiver sensitivity is maintained for all input signal strengths. The Zarlink ZL62089 CML output is back-terminated and the output common-mode may be adjusted by varying the VPP supply ensuring compatibility with most 50 ohm logic families. The back-terminated output features an adjustable output amplitude control and programmable pre-emphasis circuit for driving lossy transmission lines.

The ZL62089 provides analog diagnostics for received signal strength (RSSI), supply voltage, and junction temperature. Diagnostics are provided by a proportional current or voltage through a single programmable output.

The Zarlink ZL62089 TIA/LA provides a serial digital interface that allows internal registers to be programmed and monitored as seen in Figure 2. The simple 2-wire interface allows commonly available microcontrollers to access registers for device optimization and analog diagnostics.

For ease of manufacturing, the Zarlink ZL62089 features an alignment circuit used to optimize the optical coupling into photo diodes. The alignment circuit is activated when the power supply voltage is set to 2.0 V; under these conditions the MONITOR output sources a current that is proportional to the total detector photocurrent.

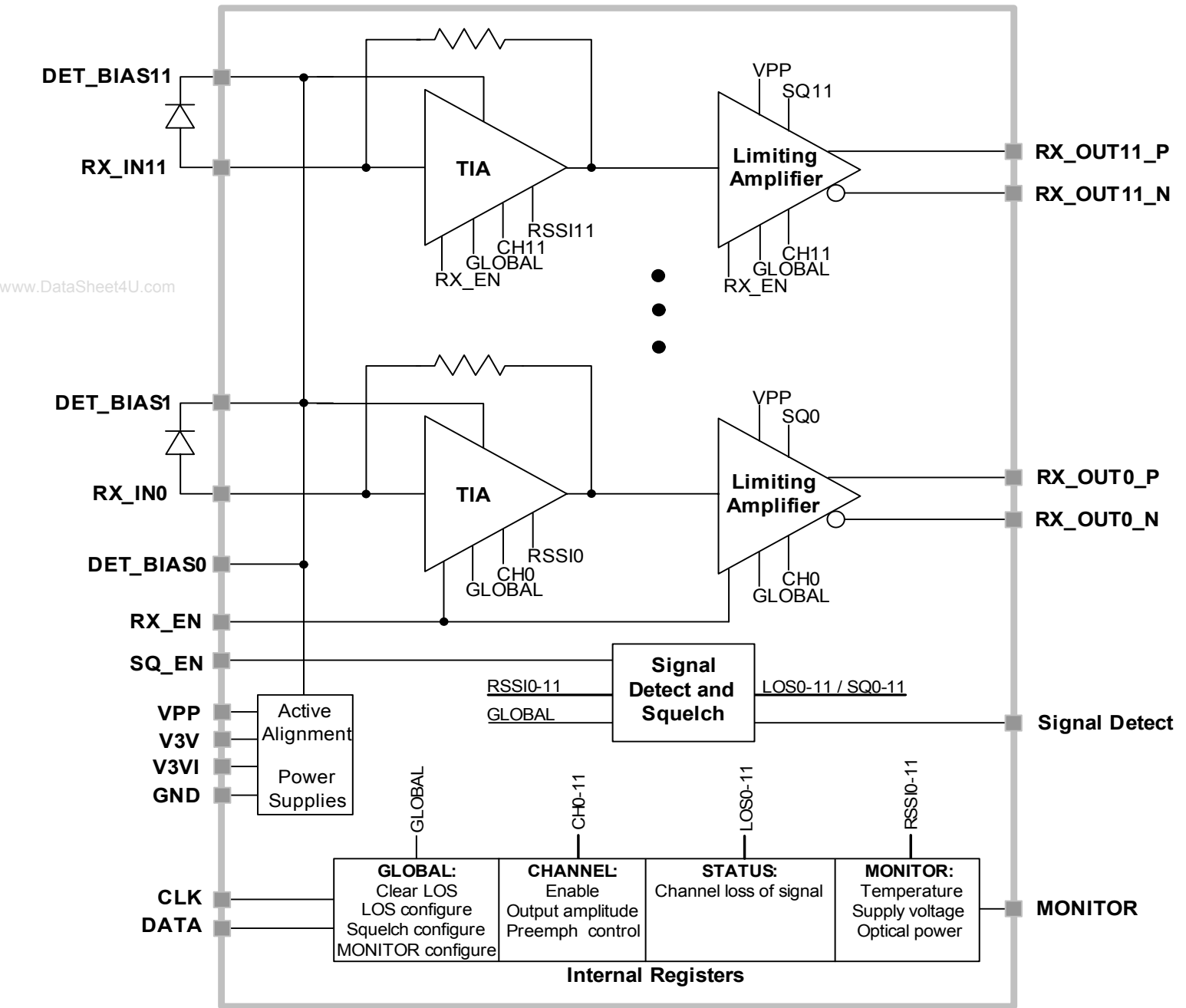


Figure 2: Simplified Block Diagram of the ZL62089

Photonics interface

The ZL62089 provides reverse photodiode bias current through isolated DET_BIAS pads. Each pad is independent of each other. They are located on adjacent sides of each TIA input ensuring compatibility with both isolated aperture and common-cathode photodiode arrays. Any DET_BIAS pad may be used with any adjacent TIA input. Note that the RSSI MONITOR feature requires isolated aperture configurations.

Signal Detect

The ZL62089 has independent signal detect circuits for each channel. The channel signal detect circuits compare the input optical modulation amplitude (OMA) against a programmable threshold to determine a valid signal. The threshold may be adjusted using the SD_TH[1:0] register bits and the hysteresis may be increased with the SD_HYST register bit. When the input signal falls below the programmable threshold, the circuit asserts the external interrupt(s) and asserts the CH_LOS register bit. The external interrupt will remain asserted until the optical input exceeds the loss of signal threshold while the CH_LOS register bit will remain asserted until the clear interrupt sequence is exercised using the 2-wire interface.

The polarity of SD, SD0, and LOS11 pads may be controlled through the GLOBAL register and the output style may be configured as either CMOS or open-drain with the SD_OD register bit.

Squelch

The ZL62089 squelch mode forces the differential outputs of an individual channel to a logic-zero when the signal detect circuit reports a loss of signal. The SQ_EN bit allows the squelch function to be enabled/disabled for each channel. The SQ_SEL register bit forces the outputs of squelch enabled (SQ_EN=1) channels to a logic-zero for test purposes.

Differential Data Outputs

The differential output amplitude for each channel is controlled with the OAC[1:0] register bits. Each increment in OAC provides approximately 10% increase in output amplitude.

The pre-emphasis feature of the ZL62089 provides variable peaking control to optimize the differential output waveform. Three individual control (PRE[2:0]) register bits provide pre-emphasis disable and seven adjustable edge peaking settings. Each channel may be controlled separately.

Power Supplies and Ground

The ZL62089 IC has three power supplies and two separate grounds. The V3VI power supply is for the TIAs, the V3V power supply is for the LAs, and the VPP power supply is for the CML output stages. The GND3VI ground is for the TIAs and the GND3V ground is for both the limiting amplifiers and the CML output stages. Power supply decoupling is recommended.

Active Alignment

For ease of manufacturing, the ZL62089 features an alignment circuit used to optimize the optical coupling into the photo diodes. The alignment circuit is activated when the power supply voltage set to 2.0 V.

Identification Code

The ZL62089 provides revision control with the addressable IDCODE register. The 8 bit register provides a unique value for each Zarlink product and IC revision.

Monitor

The MONITOR[7:0] register bits select the output of the analog multiplexer. The multiplexer output (MONITOR) sources an analog current or voltage that is proportional to the selected diagnostic parameter. Parameters include received signal strength indicator (RSSI), junction temperature, and power supply voltage as defined in Table 1. An external 4k ohm shunt resistor should be connected to MONITOR.

Please note that the RSSI feature requires that each photodiode cathode be separate. The circuit does not support common-cathode photodiode configurations.

Setting	Description
0	DET_BIAS0 photo current
1	DET_BIAS1 photo current
2	DET_BIAS2 photo current
3	DET_BIAS3 photo current
4	DET_BIAS4 photo current
5	DET_BIAS5 photo current
6	DET_BIAS6 photo current
7	DET_BIAS7 photo current
8	DET_BIAS8 photo current
9	DET_BIAS9 photo current
10	DET_BIAS10 photo current
11	DET_BIAS11 photo current
12	DET_BIAS12 photo current
13-23	Reserved
24	Junction temperature (POR state)
25	Power supply voltage monitor ($V_{cc}/2$)
26	Factory test
27-30	Reserved
31	Open circuit state (high impedance)

Table 1: MONITOR Diagnostic Parameters

Description	Equation	Unit
Channel photo current	$I_{pd} = I_{monitor}$	μA
Junction temperature	$T_{junc} = (V_{monitor} - 1.456 V) / (0.005 V/C)$	$^{\circ}C$
Power supply voltage	$V_{CC} = V_{monitor} * 2$	V

Table 2: MONITOR Equations

Digital Control

The Zarlink® ZL62089 TIA/LA provides a serial digital interface that allows internal registers to be programmed and monitored as seen in Figure 3. The simple 2-wire interface allows commonly available microcontrollers to access registers for device optimization and analog diagnostics.

The 2-wire interface is intended for use in a master-slave bus configuration. A microcontroller is the master and the Zarlink IC is the slave. The 2-wire bus consists of a unidirectional clock that is driven by the master and a bidirectional data port that may be driven by either the master or the slave. The data port (DATA) consists of a CMOS input and an open-drain output with an internal pull-up resistor and the clock input (CLK) is CMOS. The bus configuration supports multiple addressable slave devices.

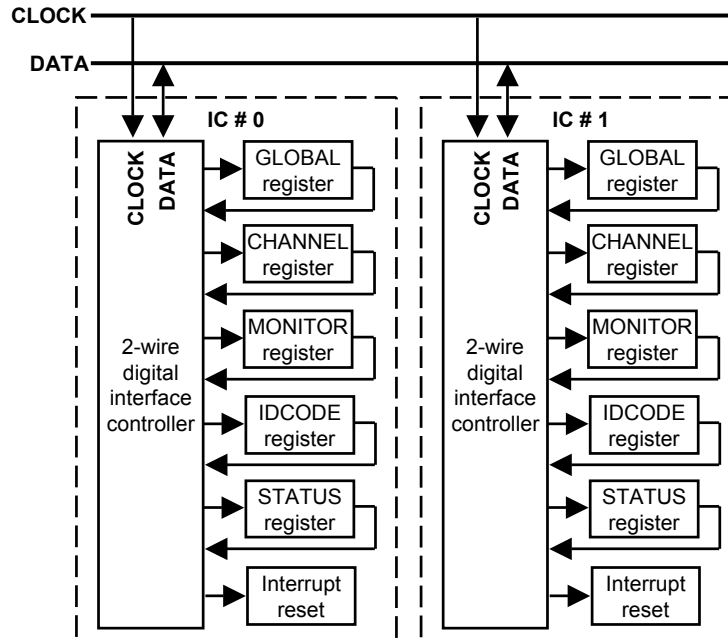


Figure 3: Block Diagram of 2-wire Bus

The ZL62089 has two address inputs (ADRS0 and ADRS1) that may be used to set the physical address of the IC (ADDRESS[3:0]). There are 8 unique addresses available for the ZL63039 and 8 unique addresses for the ZL62089 for up to 16 ICs on a single 2-wire bus. The ADRS0 and ADRS1 tri-level inputs may be connected to VCC, ground, or no connected (NC). The physical IC addresses are shown in Table 3.

ADRS1	ADRS0	ADDRESS[3:0]
NC	NC	1000
NC	GND	1001
NC	VCC	1010
GND	NC	1011
GND	GND	1100
GND	VCC	1101
VCC	NC	1110
VCC	GND	1111
VCC	VCC	1000

Table 3: Physical IC Address Settings

The ZL62089 has five addressable registers as defined in Table 4. Each register can be accessed independently by its specific register address (REGISTER[2:0]). It is necessary for the master to initiate and terminate write or read operations with the exact register length.

Register	Type	Number of bits	Address REGISTER[2:0]
GLOBAL	Read/Write	16	000
MONITOR	Read/Write	8	001
CHANNEL	Read/Write	96	010
IDCODE	Read only	8	011
STATUS	Read only	24	100

Table 4: Register Definitions

Write Sequence

A register write transaction is initiated by the master with a start sequence followed by a physical IC address (ADDRESS[3:0]), a register address (REGISTER[2:0]), write indicator (WR[0]=0) and register payload data. The write transaction is completed by the master with a stop sequence as show in Tables 5 and 6.

START	ADDRESS[3:0]	REGISTER[2:0]	WR[0]=0	Register data (8-96 bits)	STOP
-------	--------------	---------------	---------	---------------------------	------

Table 5: Register Write Sequence

Field	Description
START	Start condition, initiated by the master, and consists of a falling edge on DATA while CLOCK is high
ADDRESS[3:0]	Physical address of slave. Determined by ADRS1 and ADRS0 connections (VCC, NC, or GND)
REGISTER[2:0]	Address for internal registers (GLOBAL, MONITOR, CHANNEL, IDCODE, and STATUS)
WR[0]	Read/write indicator. WR[0]=0 for the write operation
Register data	Register data. Payload must equal to the length of the register (8-96 bits)
STOP	Stop condition, a rising edge on DATA with CLOCK high terminates the 2-wire transaction and resets the digital interface controller

Table 6: Description of Fields in Write Sequence

Figure 4 shows a timing diagram for a register write operation. The binary input is clocked into DATA on the rising edge of CLOCK. It is important to have glitch-free DATA signal while CLK is high to avoid faulty start or stop conditions. The stop condition also serves as the digital reset for the digital interface controller.

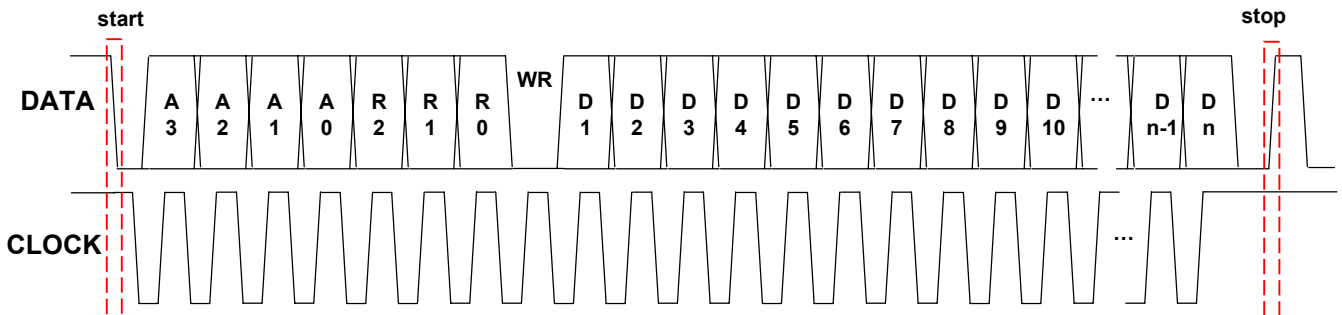


Figure 4: Register Write Timing Diagram

Read Sequence

A register read transaction is initiated by the master with a start sequence followed by a physical IC address (ADDRESS[3:0]), a register address (REGISTER[2:0]), and a write indicator (WR[0]=1) as seen in Table 7. The data payload that follows is always in single byte units. After reading each byte, the master must send an ACK bit to continue reading the contents of a register or a NACK after the complete register has been read. A stop sequence following the NACK will terminate the transaction.

START	ADDRESS[3:0]	REGISTER[2:0]	WR[0]=1	Data (8 bits)	ACK	Data (8 bits)	ACK	...	NACK	STOP
-------	--------------	---------------	---------	------------------	-----	------------------	-----	-----	------	------

Table 7: Register Read Sequence

A timing diagram for a read transaction is shown in Figure 5. The blue-highlighted (byte_1 and byte_n) sections in the DATA waveform indicate that the bidirectional DATA port of the IC is in output mode. The remainder of the time, both CLOCK and DATA of the IC are in input mode.

All registers are set to default values after the IC is powered on. These values are known as power on reset (POR) values and may be seen in the register definition Tables 10-14. The POR register values may be observed by reading a register after a power cycle. Registers may be read repeatedly without disturbing the contents of the register.

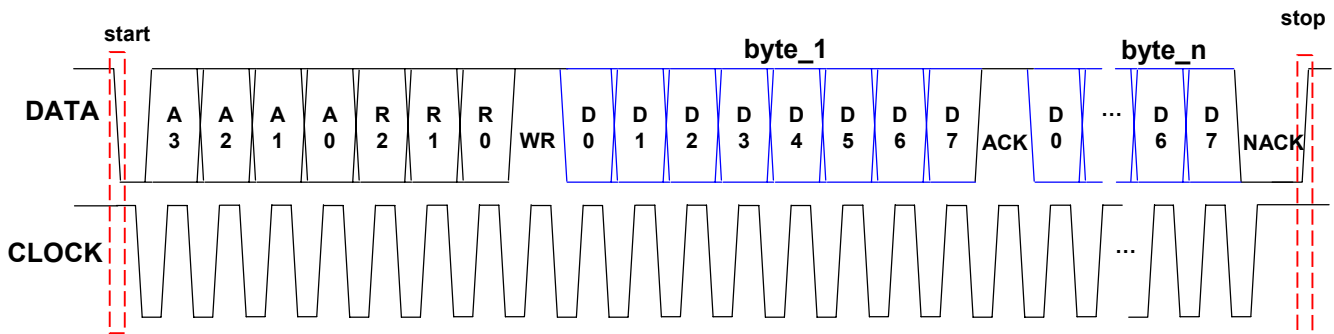


Figure 5: Register Read Timing Diagram

Clear STATUS Register Sequence

In addition to register access, a special 2-wire sequence allows the user to clear the STATUS register. The instruction sequence is shown in Table 8 and the timing diagram is shown in Figure 6.

START	ADDRESS[3:0]	REGISTER[2:0]	WR[0]=0	STOP
-------	--------------	---------------	---------	------

Table 8: Clear STATUS Register Sequence

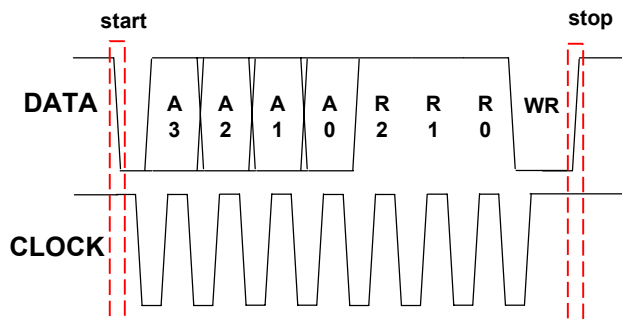


Figure 6: Clear STATUS Register Timing Diagram

Critical Timing

The register read, register write, and clear STATUS register 2-wire transactions share the same timing requirements. Figures 7 and 8 show critical timing relationships and Table 9 provides worst case timing.

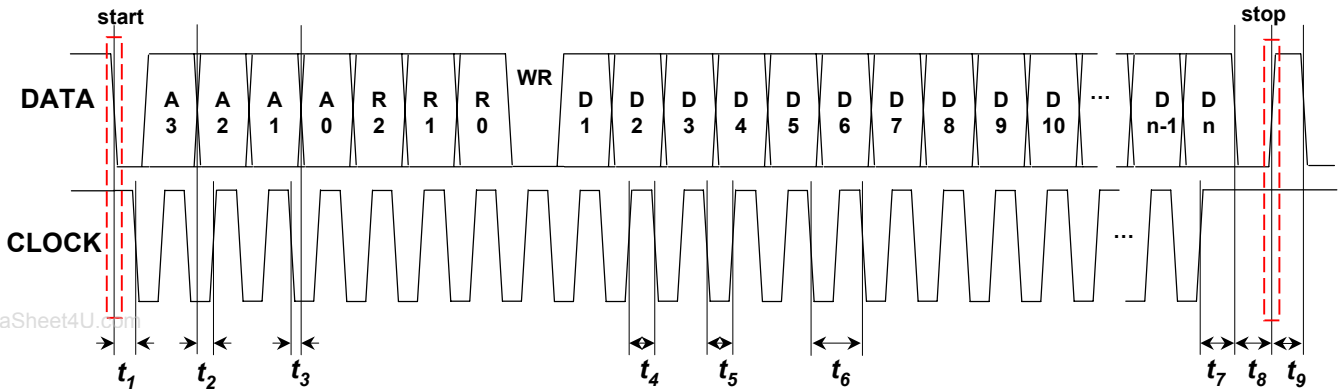


Figure 7: Register Write Sequence with Timing Relationships

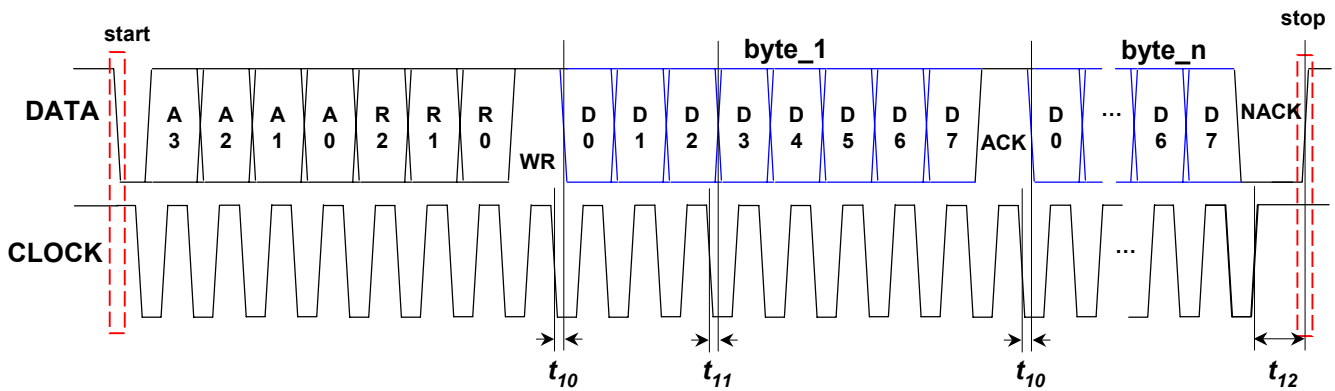


Figure 8: Register Read Sequence with Timing Relationships

Symbol	Description	Worst Case Timing (ns)
t_1	Start condition to first clock transition	0.2
t_2	Write data to clock set time	1.2
t_3	Write data to clock hold time	0.5
t_4	Clock high	17.0
t_5	Clock low	7.0
t_6	Clock period	34.0
t_7	Last clock to last write data transition	6.0
t_8	Data=low before stop condition	0.1
t_9	Between control sequences	22.0
t_{10}	Read data available to clock edge	2.6
t_{11}	Read data delay from clock	2.1
t_{12}	Last clock to stop in read sequence	0.5

Table 9: Worst Case Timing for 2-wire Transactions

Bit	Name	POR	Description, see Note 1
0	SD_TH[1]	1	Signal detect threshold – MSB
1	SD_TH[0]	0	Signal detect threshold
2	SD_HYST[1]	1	Signal detect hysteresis – MSB
3	SD_HYST[0]	0	Signal detect hysteresis
4	SD_INV	0	Changes the polarity of the SD output interrupts
5	LOS11_INV	0	Changes the polarity of the LOS11 output interrupt
6	SD0_INV	0	Changes the polarity of the SD0 output interrupt
7	SD_OD	0	Selects I/O style for all SD/LOS pads. 1 = open-drain, 0 = CMOS
8	SQ_SEL	0	Selects type of squelch, 0 = normal squelch, 1 = forced squelch, gated by CHANNEL SQ_EN register bit
9	TC_DISABLE	0	Disables temperature slope compensation
10	Reserved	1	Reserved for future use, see Note 2
11	Reserved	1	Reserved for future use, see Note 2
12	Reserved	0	Reserved for future use, see Note 2
13	Reserved	1	Reserved for future use, see Note 2
14	Reserved	0	Reserved for future use, see Note 2
15	Reserved	0	Reserved for future use, see Note 2
Note 1: All register bits are asserted by a logic level “1” unless otherwise specified			
Note 2: Reserved bits should always be programmed with POR values during write operations			

Table 10: GLOBAL Register Definition. Register type = Read/Write, address REGISTER[2:0] = 000

Bit	Name	Chan	POR	Description, see Note 1
0	CH_EN	0	1	Channel enable
1	OAC[1]	0	0	Channel output amplitude control – MSB
2	OAC[0]	0	1	Channel output amplitude control
3	PRE[2]	0	0	Pre-emphasis control for differential outputs – MSB
4	PRE[1]	0	0	Pre-emphasis control for differential outputs
5	PRE[0]	0	0	Pre-emphasis control for differential outputs
6	SQ_EN	0	0	Enables squelch circuit or forces squelch condition, see GLOBAL register SQ_SEL bit
7	Reserved	0	0	Reserved for future use, see Note 2
8-15	See bits 0 -7	1	-	See bits 0 -7
16-23	See bits 0 -7	2	-	See bits 0 -7
24-31	See bits 0 -7	3	-	See bits 0 -7
32-39	See bits 0 -7	4	-	See bits 0 -7
40-47	See bits 0 -7	5	-	See bits 0 -7
48-55	See bits 0 -7	6	-	See bits 0 -7
56-63	See bits 0 -7	7	-	See bits 0 -7
64-71	See bits 0 -7	8	-	See bits 0 -7
72-79	See bits 0 -7	9	-	See bits 0 -7
80-87	See bits 0 -7	10	-	See bits 0 -7
88-95	See bits 0 -7	11	-	See bits 0 -7
Note 1: All register bits are asserted by a logic level “1” unless otherwise specified				
Note 2: Reserved bits should always be programmed with POR values during write operations				

Table 11: CHANNEL Register Definition. Register type = Read/Write, address REGISTER[2:0] = 010

Bit	Name	Chan	POR	Description, see Note 1
0	CH_LOS	0	0	Channel loss of signal indicator
1	Reserved	0	0	Reserved for future use
2-3	See bits 0 -1	1	-	See bits 0 -1
4-5	See bits 0 -1	2	-	See bits 0 -1
6-7	See bits 0 -1	3	-	See bits 0 -1
8-9	See bits 0 -1	4	-	See bits 0 -1
10-11	See bits 0 -1	5	-	See bits 0 -1
12-13	See bits 0 -1	6	-	See bits 0 -1
14-15	See bits 0 -1	7	-	See bits 0 -1
16-17	See bits 0 -1	8	-	See bits 0 -1
18-19	See bits 0 -1	9	-	See bits 0 -1
20-21	See bits 0 -1	10	-	See bits 0 -1
22-23	See bits 0 -1	11	-	See bits 0 -1
Note 1: All register bits are asserted as logic level "1" unless otherwise specified				

Table 12: STATUS Register Definition. Register type = Read Only, address REGISTER[2:0] = 100

Bit	Name	POR	Description
0	IDCODE[7]	1	IC identification code – MSB
1	IDCODE[6]	1	IC identification code
2	IDCODE[5]	1	IC identification code
3	IDCODE[4]	1	IC identification code
4	IDCODE[3]	1	IC identification code
5	IDCODE[2]	0	Revision code – MSB
6	IDCODE[1]	0	Revision code
7	IDCODE[0]	0	Revision code

Table 13: IDCODE Register Definition. Register type = Read Only, address REGISTER[2:0] = 011

Bit	Name	POR	Description
0	Reserved	0	Reserved for future use, see Note 1
1	Reserved	0	Reserved for future use, see Note 1
2	Reserved	0	Reserved for future use, see Note 1
3	MONITOR[4]	1	Monitor output control – MSB
4	MONITOR[3]	1	Monitor output control
5	MONITOR[2]	0	Monitor output control
6	MONITOR[1]	0	Monitor output control
7	MONITOR[0]	0	Monitor output control
Note 1: Reserved bits should always be programmed with POR values during write operations			

Table 14: MONITOR Register Definition. Register type = Read/Write, address REGISTER[2:0] = 001

Absolute Maximum Ratings

The IC should be used within the limits specified in Table 15. Exceeding the specified limits may impair the useful life of the component and the device may no longer perform to the specifications within this data sheet. Functionality at or above the values listed is not implied.

Symbol	Description	Min.	Typical	Max	Units	Remarks
V3VI, V3V, VPP	IC supply voltage	-0.5	3.3	+3.63	V	
I _{IN}	Input current			2	mA	
I _{SHORT}	Output short circuit current	-50		50	mA	See Note 1
ESD _{HBM}	ESD tolerance, (HBM)	2			kV	ESD on all pins
T _{ATTACH}	Die attach temperature			260	°C	60 second duration
T _{JUNC}	Junction temperature			125	°C	
T _{STG}	Storage temperature	-65		150	°C	

Table 15: Absolute Maximum Rating

Note 1: To any voltage between 3.3 V and ground

Recommended Operating Conditions

Symbol	Description	Min.	Typical	Max	Units	Remarks
V3VI, V3V	Positive supply range	2.97	3.3	3.63	V	For 2.5/3.3V CML operation
		3.135	3.3	3.465	V	For 1.8V CML operation
VPP	CML output supply range	2.97	3.3	3.63	V	For 3.3V CML operation
		2.25	2.5	2.75	V	For 2.5V CML operation
		1.71	1.8	1.89	V	For 1.8V CML operation
ICC	Supply current		510		mA	V3VI=V3V=VPP=3.3V
				3	mA	All channels disabled
P _{DIS}	Power dissipation		1.68		W	V3VI=V3V=VPP=3.3V
				10	mW	All channels disabled

Table 16: Recommended Operating Conditions

DC Characteristics

(V3VI=V3V=3.3 V +/- 10%, VPP=3.3 V +/- 10%, T_{JUNC}=0-100 °C)

Symbol	Description	Min.	Typical	Max	Units	Remarks
V _{INPUT}	DC voltage present at RX_IN		0.5		V	
C _{DET}	Detector capacitance		600		fF	
Z _{INPUT}	Input impedance		50		ohms	
V _{DET_BIAS}	Detector bias voltage		2.5		V	
I _{DET_BIAS}	Detector current			1	mA	

Table 17: TIA Detector Interface

Symbol	Description	Min.	Typical	Max.	units	Remarks, See Note 1
V_{AMP_DIFF}	Differential output amplitude	500			mV _{pp}	
V_{AMP_SING}	Single-ended output amplitude	250			mV _{pp}	
R_{TERM}	Termination resistance		50		ohms	Terminated to VPP

Table 18: Limiting Amplifier

Note 1: For 1.8V CML operation, the output must be DC-coupled to a CML input

Symbol	Description	Min.	Typical	Max.	units	Remarks
V_{IH}	High-level input voltage	2		$V_{3V}+0.3$	V	$V_{OUT} \geq V_{OH} \text{ (min) or}$ $V_{OUT} \leq V_{OL} \text{ (max)}$
V_{IL}	Low-level input voltage	-0.3		0.8	V	
I_{IN}	Input current			+/-5	μA	$V_{IN} = 0 \text{ V or } V_{IN} = V_{DD}$
V_{OH}	High-level output voltage	$V_{3V}-0.2$			V	$I_{OH} = -100 \text{ μA}$
V_{OL}	Low-level output voltage			0.2	V	$I_{OH} = 100 \text{ μA}$

Table 19: CMOS I/O

AC Characteristics

($V_{3VI}=V_{3V}=3.3 \text{ V} \pm 10\%$, $V_{PP}=3.3 \text{ V} \pm 10\%$, $T_{JUNC}=0-100 \text{ °C}$)

Symbol	Description	Min.	Typical	Max.	units	Remarks
I_{SEN}	Receiver sensitivity		12		μA _{PP}	See Note 1
F_{3dB}	3dB bandwidth		4		GHz	
I_{IN}	Input referred current noise		0.7		μA _{RMS}	See Note 1
I_{SAT}	Input saturation level	1			mA _{PP}	

Table 20: Transimpedance Amplifier

Note 1: $C_{det}=450 \text{ fF}$, 6.25 Gb/s PRBS23 pattern, BER 10^{-12}

Symbol	Description	Min.	Typical	Max.	units	Remarks
F_{CUTOFF}	Low-frequency cutoff		175		kHz	
T_R	Rise time		60		ps	
T_F	Fall time		60		ps	
D_R	Data rate			6.25	Gb/s	

Table 21: Limiting Amplifier

Note 1: Rise and fall times measured 20% to 80%

Signal Pin Definitions

Pad	Pad No.	I/O	Style	Description
GND3V	1	-	Ground	Ground for limiting amplifier and CML output driver
GND3V	2	-	Ground	Ground for limiting amplifier and CML output driver
RX_OUT11_N	3	Output	Digital	Differential output data for channel 11, positive
RX_OUT11_P	4	Output	Digital	Differential output data for channel 11, negative
RX_OUT10_N	5	Output	Digital	Differential output data for channel 10, positive
RX_OUT10_P	6	Output	Digital	Differential output data for channel 10, negative
RX_OUT9_N	7	Output	Digital	Differential output data for channel 9, positive
RX_OUT9_P	8	Output	Digital	Differential output data for channel 9, negative
RX_OUT8_N	9	Output	Digital	Differential output data for channel 8, positive
RX_OUT8_P	10	Output	Digital	Differential output data for channel 8, negative
RX_OUT7_N	11	Output	Digital	Differential output data for channel 7, positive
RX_OUT7_P	12	Output	Digital	Differential output data for channel 7, negative
RX_OUT6_N	13	Output	Digital	Differential output data for channel 6, positive
RX_OUT6_P	14	Output	Digital	Differential output data for channel 6, negative
RX_OUT5_N	15	Output	Digital	Differential output data for channel 5, positive
RX_OUT5_P	16	Output	Digital	Differential output data for channel 5, negative
RX_OUT4_N	17	Output	Digital	Differential output data for channel 4, positive
RX_OUT4_P	18	Output	Digital	Differential output data for channel 4, negative
RX_OUT3_N	19	Output	Digital	Differential output data for channel 3, positive
RX_OUT3_P	20	Output	Digital	Differential output data for channel 3, negative
RX_OUT2_N	21	Output	Digital	Differential output data for channel 2, positive
RX_OUT2_P	22	Output	Digital	Differential output data for channel 2, negative
RX_OUT1_N	23	Output	Digital	Differential output data for channel 1, positive
RX_OUT1_P	24	Output	Digital	Differential output data for channel 1, negative
RX_OUT0_N	25	Output	Digital	Differential output data for channel 0, positive
RX_OUT0_P	26	Output	Digital	Differential output data for channel 0, negative
GND3V	27	-	Ground	Ground for limiting amplifier and CML output driver
MONITOR	28	Output	Analog	Analog multiplexer output. See Note 2
VPP	29	-	Supply	+1.8/2.5/3.3V CML output power supply
VPP	30	-	Supply	+1.8/2.5/3.3V CML output power supply
V3V	31	-	Supply	Limiting amplifier +3.3V power supply
V3V	32	-	Supply	Limiting amplifier +3.3V power supply
GND3V	33	-	Ground	Ground for limiting amplifier and CML output driver
GND3V	34	-	Ground	Ground for limiting amplifier and CML output driver
CLK	35	Input	Digital	Clock input for 2-wire interface. See Notes 1 and 4
ADRS0	36	Input	Tri-level	Sets IC physical address. Connect to +3.3 V, ground or NC

Table 22: Signal Pin Definitions

Pad	Pad No.	I/O	Style	Description
DATA	37	Bi-directional	Input=CMOS Output=open-drain	Data for 2-wire interface, see Notes 1 and 4
SD	38	Output	Digital	Indicates status of all channel signal detect circuits. See Notes 2, 3, and 4
RX_EN	39	Input	Digital	Enables high-speed channels. See Notes 1 and 4
V3VI	40	-	Supply	TIA +3.3V power supply
V3VI	41	-	Supply	TIA +3.3V power supply
GND3VI	42	-	Ground	Ground for TIA
GND3VI	43	-	Ground	Ground for TIA
GND3VI	44	-	Ground	Ground for TIA
DET_BIAS0	45	-	Analog	Photo diode bias
RX_IN0	46	Input	Analog	Channel 0 TIA input
DET_BIAS1	47	-	Analog	Photo diode bias
RX_IN1	48	Input	Analog	Channel 1 TIA input
DET_BIAS2	49	-	Analog	Photo diode bias
RX_IN2	50	Input	Analog	Channel 2 TIA input
DET_BIAS3	51	-	Analog	Photo diode bias
RX_IN3	52	Input	Analog	Channel 3 TIA input
DET_BIAS4	53	-	Analog	Photo diode bias
RX_IN4	54	Input	Analog	Channel 4 TIA input
DET_BIAS5	55	-	Analog	Photo diode bias
RX_IN5	56	Input	Analog	Channel 5 TIA input
DET_BIAS6	57	-	Analog	Photo diode bias
RX_IN6	58	Input	Analog	Channel 6 TIA input
DET_BIAS7	59	-	Analog	Photo diode bias
RX_IN7	60	Input	Analog	Channel 7 TIA input
DET_BIAS8	61	-	Analog	Photo diode bias
RX_IN8	62	Input	Analog	Channel 8 TIA input
DET_BIAS9	63	-	Analog	Photo diode bias
RX_IN9	64	Input	Analog	Channel 9 TIA input
DET_BIAS10	65	-	Analog	Photo diode bias
RX_IN10	66	Input	Analog	Channel 10 TIA input
DET_BIAS11	67	-	Analog	Photo diode bias
RX_IN11	68	Input	Analog	Channel 11 TIA input
DET_BIAS12	69	-	Analog	Photo diode bias
GND3VI	70	-	Ground	Ground for TIA
GND3VI	71	-	Ground	Ground for TIA
GND3VI	72	-	Ground	Ground for TIA
GND3VI	73	-	Ground	Ground for TIA

Table 22: Signal Pin Definitions (continued)

Pad	Pad No.	I/O	Style	Description
V3VI	74	-	Supply	TIA +3.3V power supply
V3VI	75	-	Supply	TIA +3.3V power supply
RX_EN	76	Input	Digital	Enables high-speed channels. See Notes 1 and 4
SQ_EN	77	Input	Digital	Squelch enable. Disables high-speed channels at low input levels. See Note 1
LOS11	78	Output	Digital	Indicates status of channel 11 signal detect circuit. See Note 2 and 3
ADRS1	79	Input	Tri-level	Sets IC physical address. Connect to +3.3V, ground, or NC
SD0	80	Output	Digital	Indicates status of channel 0 signal detect circuit. See Note 2 and 3
GND3V	81	-	Ground	Ground for limiting amplifier and CML output driver
GND3V	82	-	Ground	Ground for limiting amplifier and CML output driver
V3V	83	-	Supply	Limiting amplifier +3.3V supply
V3V	84	-	Supply	Limiting amplifier +3.3V supply
VPP	85	-	Supply	+1.8/2.5/3.3V CML output power supply
VPP	86	-	Supply	+1.8/2.5/3.3V CML output power supply

Table 22: Signal Pin Definitions (continued)

Note 1: Internal 40 k ohm pull-up to VCC

Note 2: Pad functionality programmed through serial interface

Note 3: Selectable CMOS or open-drain output style

Note 4: Two pads on the IC exist with the same name. They are electrically equivalent and only one should be connected.

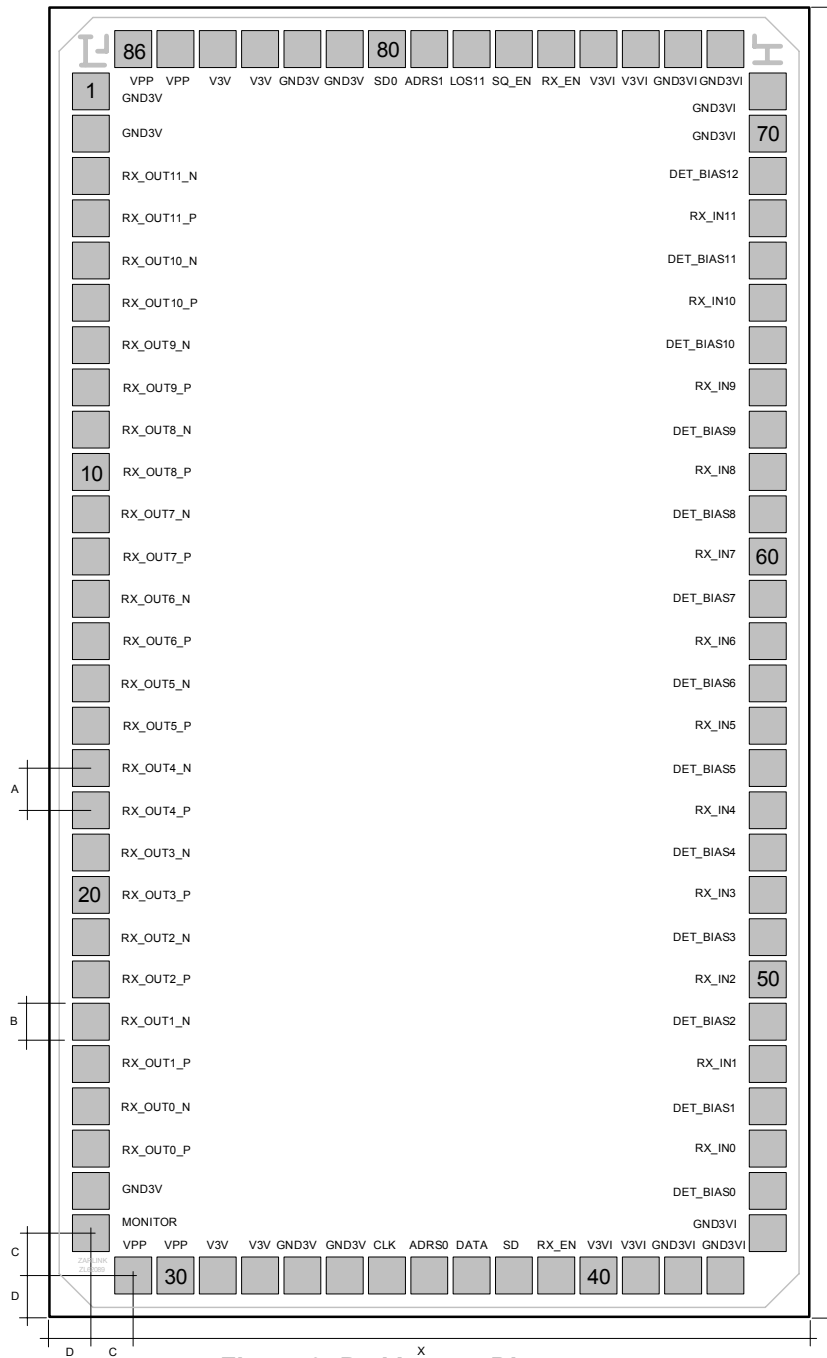


Figure 9: Pad Layout Diagram

Symbol	Description	Length	Unit
A	Pad to pad pitch	125	um
B	Bond pad length/width	114	um
C	Corner pad to corner pad pitch	125	um
D	Pad center to edge of die	122.5	um
X	Overall IC dimensions	2245 +/-25	um
Y	Overall IC dimensions	3870 +/-25	um
Z	Standard die thickness	17	mils

Table 23: Critical Dimensions



**For more information about all Zarlink products
visit our Web Site at
www.zarlink.com**

Information relating to products and services furnished herein by Zarlink Semiconductor Inc. or its subsidiaries (collectively "Zarlink") is believed to be reliable. However, Zarlink assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Zarlink, or non-Zarlink furnished goods or services may infringe patents or other intellectual property rights owned by Zarlink.

This publication is issued to provide information only and (unless agreed by Zarlink in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Zarlink without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Zarlink's conditions of sale which are available on request.

Purchase of Zarlink's I²C components conveys a licence under the Philips I²C Patent rights to use these components in and I²C System, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Zarlink, ZL and the Zarlink Semiconductor logo are trademarks of Zarlink Semiconductor Inc.

Copyright Zarlink Semiconductor Inc. All Rights Reserved.

TECHNICAL DOCUMENTATION - NOT FOR RESALE