ZL40510/14

Dual Output DVD and CD 4 Channel Laser Diode Drivers

Data Sheet

August 2006

Features

- Single 5 V supply (±10%)
- 150 mA low-noise read channel with 100 x current gain
- Three 500 mA write channels with 240 x gain
- Combined channel output 700 mA
- Dual output for DVD/CD laser
- Rise and fall times 1 ns typical
- Oscillator, 500 MHz, 100 mA with external resistor control of frequency and amplitude
- Power Up/Down control
- LVDS control signals
- > 2 kV ESD
- Low R_{th} QFN package
- Contact Zarlink for available Custom Gain and Input Impedance options

Ordering Information

ZL40510LDE	24 Pin QFN	Tubes, Bake & Drypack
ZL40510LDF	24 Pin QFN	Tape & Reel
ZL40510LDG	24 Pin QFN	Trays, Bake & Drypack
ZL40514LDE	24 Pin QFN	Tubes, Bake & Drypack
ZL40514LDF	24 Pin QFN	Tape & Reel
ZL40514LDG	24 Pin QFN	Trays, Bake & Drypack

-40°C to +85°C

Applications

- DVD±RW/RAM
- DVD±R
- CD-RW
- CD-R
- Write optical drives
- Laser Diode current switch
- Supports double density DVD

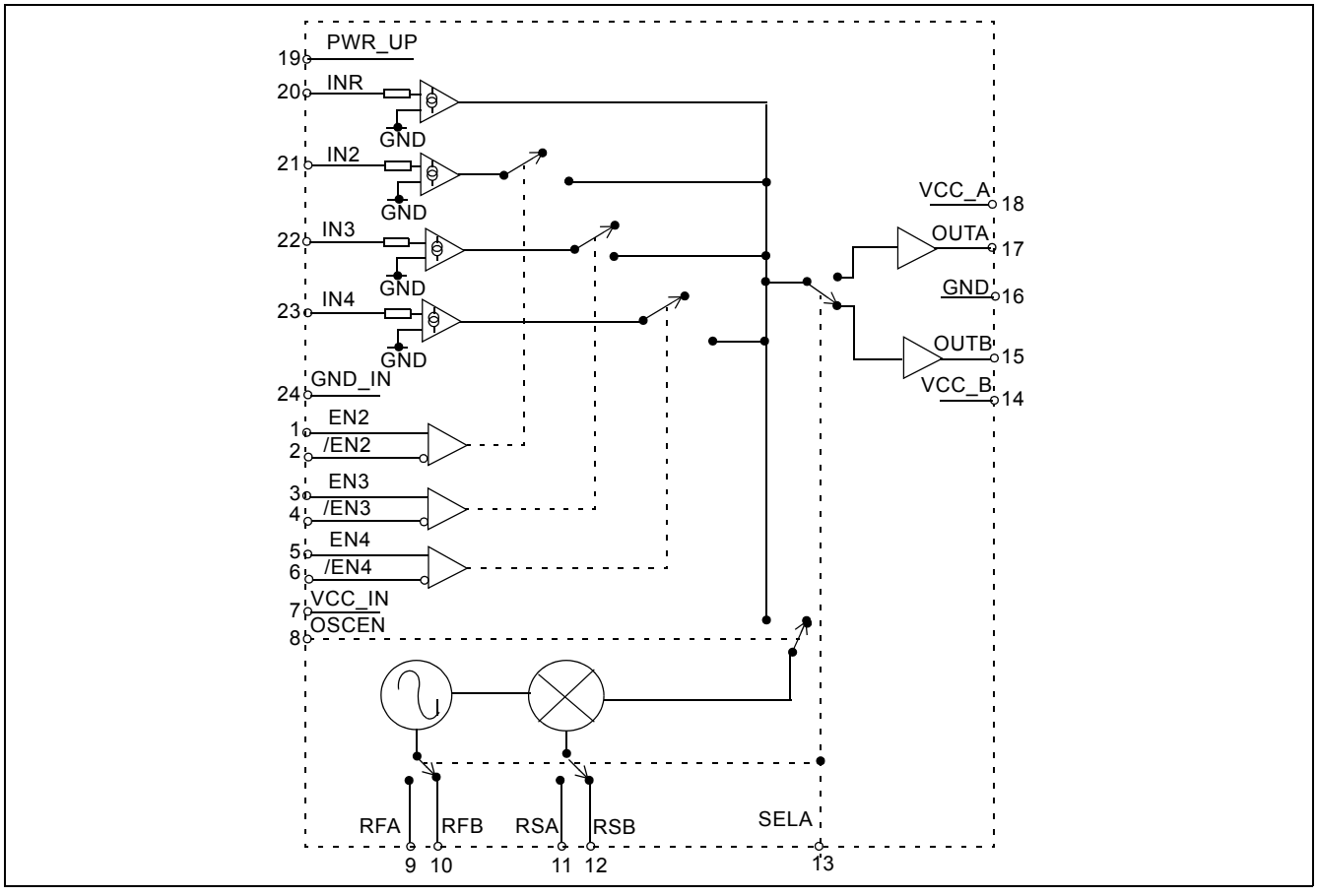

Figure 1 - Functional Block Diagram

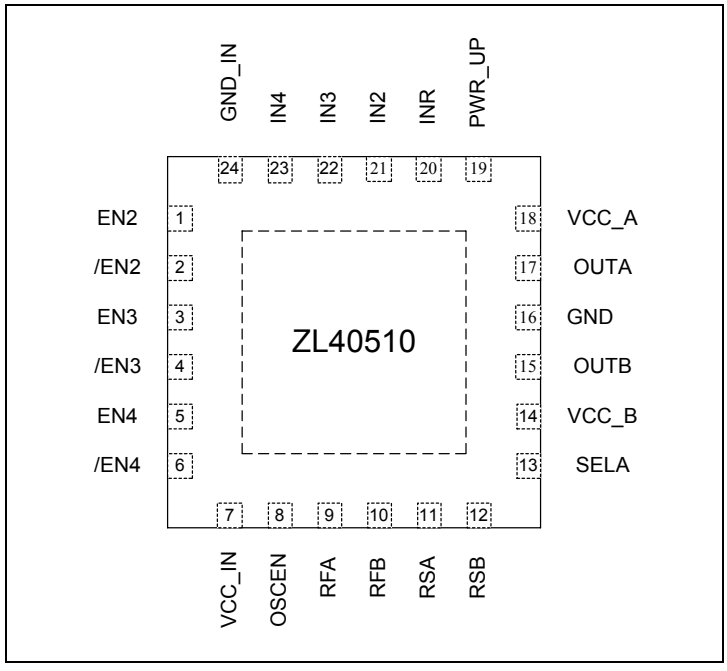

Figure 2 - Pinout of 4x4 mm 24 Pin QFN (top view)

Description

The ZL40510/14 are high performance laser drivers capable of driving two separate cathode grounded laser diodes (e.g., 650 nm and 780 nm laser diodes).

The ZL40510/14 contain a 150 mA low-noise read channel (ChR), and three 500 mA write channels (Ch2, Ch3 and Ch4). The read channel amplifies the positive current supplied at its reference input, INR, by a fixed factor of 100. Write channels amplify the positive currents supplied at its reference inputs IN2, IN3, and IN4 by a fixed factor of 240.

An on-chip RF oscillator is provided for the reduction of laser mode hopping noise.

The ZL40510 offers higher tolerance performance.

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1.0 Application Notes

1.1 Read and Write Channel Operation

The read channel is activated by applying a 'High' signal to the PWR_UP pin. In this mode, the fast write channels can be enabled by applying a 'High' signal to the respective pair of write enable pins (EN2, /EN2), (EN3, /EN3) or (EN4, /EN4). The output currents of the four channels are summed together and output as a composite signal at either OUTA (if SELA select is 'High') or OUTB (if SELA select is 'Low'). This provides the ability to drive two different laser diodes with just one ZL40510/14.

Voltage control of the channel reference inputs (INR, IN2, IN3 and IN4) can be achieved quite easily using an external resistor R_{ref} in series with the reference channel input to convert a given reference potential V_{ref} to an input current, I_{in}:

$$I_{in} = \frac{V_{ref}}{R_{ref} + R_{in}},$$

where R_{in} is the input impedance of the respective reference channel.

1.2 On-chip RF Oscillator

An on-chip RF oscillator is enabled if OSCEN = 'High', and its output signal is added to the appropriate current output (OUTA, if SELA select is 'High', or OUTB, if SELA select is 'Low'). The oscillator amplitude is set by an external resistor from RSA or RSB to GND. Its frequency is set by an external resistor RFA or RFB to GND. RSA and RFA are selected when SELA is ‘High’.

The oscillator signal is summed with the programmed Write and Read levels before amplification to the output. The oscillator signal has zero DC level and +I_pk to –I_pk signal swing. Consequently, if the programmed DC level from the Write and Read Channels is less than the PK level programmed for the Oscillator, the combined signal will be clipped on the negative cycle of the signal. This will increase the harmonic content of the output signal and reduce the pk to pk amplitude output.

1.3 Thermal Considerations

Package thermal resistance is 40°C/W under the EIA/JESD51-3 compliant PCB test board condition.

Users should ensure that the junction temperature does not exceed 150°C. Thermal resistance from junction to case and to ambient is very much dependent on how the IC is mounted onto the board, on the PCB layout and on any heat extraction arrangements.

Power consumption and system ambient operating temperature limits should be noted and careful thermal gradient calculations undertaken to ensure that the junction temperature never exceeds 150°C.

1.4 Electrical and Optical Pulse Response

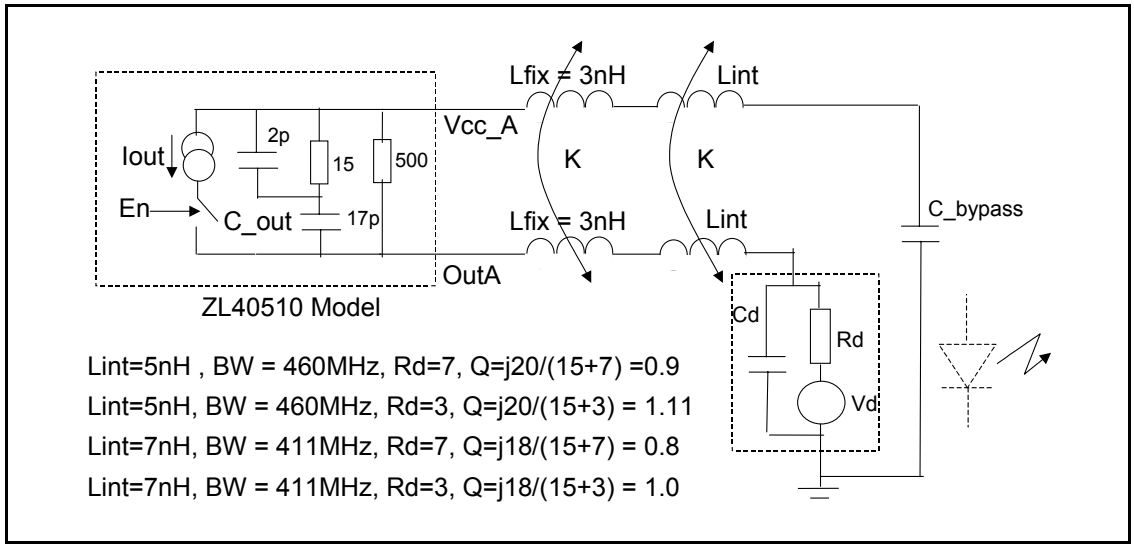


Figure 3 - Pulse Response Model

Figure 3 illustrates a simplified model of the typical ZL40510/14 and the application. The ZL40510/14 consists of an ideal switched current source and an equivalent model of the ZL40510/14 output stage. The Electrical Model for the Laser Diode is a Voltage source Vd (V_on) in series with the On Resistance Rd all in parallel with the Junction Capacitance Cd. This simplified model approximately represents the Laser Diode Electrical load when operated beyond the Laser Threshold. To a first approximation, the Optical output is proportional to the current flow in the Resistor Rd.

The Laser Diode and the ZL40510/14 are connected together by interconnect tracks with the return current passing through the supply decoupling bypass capacitor between ground and output Vcc.

The ZL40510/14 can be approximated to an ideal switched programmed current source with a propagation delay of Iout_on (1.2 nS) and a switch transition time of 400 ps. The final output electrical pulse response parameters, Trise, Tfall, Overshoot and Undershoot are determined by the combined electrical network as illustrated in Figure 3.

For example, the Rise Time and Fall Time for large current steps can be slew rate limited by the combined interconnect and fixed interconnect inductance. The Fixed Inductance represents that associated with packaging and minimum interconnect distance. The Interconnect Inductance is that associated with the additional tracking between Laser Diode and the ZL40510/14 to accommodate application physical limitations.

For example, if a pulse of 360 mA amplitude (40 mA to 400 mA) is to be switched in a time of 1 nS with the Vd = 1.6 V, then the maximum volt drop across the interconnect inductance is approximately 3.5 V (maximum Vpin for 500 mA output) – 1.6 V (Vdiode) = 1.9 V. Consequently, L*di/dt < 1.9 V. Hence, L < 1.9/ (0.36A/1 nS) = 5.3 nH.

Small current step size Rise and Fall time will be determined by the Bandwidth of the combined network. This is dominated by the Interconnect Inductance and the output Capacitance. Similarly, the overshoot and undershoot will be determined by the Q of the network. This is a function of the Source Impedance from the ZL40510/14, the Interconnect inductance and the Load impedance of the Laser Diode. Figure 3 includes example simplified estimates of the Q and BW of the combined Laser Diode, ZL40510/14 and interconnect network for two different interconnect inductance values (5 nH and 7 nH) and two different Diode On resistance (3 Ohm and 7 Ohm). This simple analysis illustrates the change in BW and Q of the network depending on these parameters. This in turn effects the Rise Time and Fall time and the Overshoot and Undershoot performance achieved in the application.

1.5 Specified Electrical Performance with 15 mm Interconnect and Zarlink ZLE40510/14 Evaluation Board

The specified performance in the table are results based on the electrical measurements and simulations across full process corners using the Zarlink Evaluation Board using a 3.9 Ohm resistive load to ground.

The track interconnect between ZL40510/14 and the 3.9 Ohm Resistor is 15 mm long and uses a 2 mm wide track on single sided FR4 board. The return path is via two 2 mm wide tracks spaced 0.25 mm either side of the track between output and the 3.9 Ohm resistor. The combined forward and return path forms a co planar transmission line with a characteristic impedance of approximately 120 Ohms.

The tight coupled return paths carrying the return current reduce the effective series inductance (Leff) which can be approximated to:

$$Leff = 2 * Lint * (1 - K) + 2 * Lfix * (1 - K).$$

The ZLE40510 board has two positions for the Laser Diode at two different distances. (15 and 30 mm).

- The measured value of Leff is 7 nH
- The estimated value of Leff = 2 * 8 (1 – 0.5) = 8 nH

The actual pulse response achieved in an application is thus dependent on the application.

1.6 Application Layout Guide Lines

Minimize interconnect inductance by:

a. Using Short Interconnect Distance

b. Use wide interconnect tracks

c. Keep the return path tightly coupled to the forward path.

1.7 ZLE40510/14 Interconnect

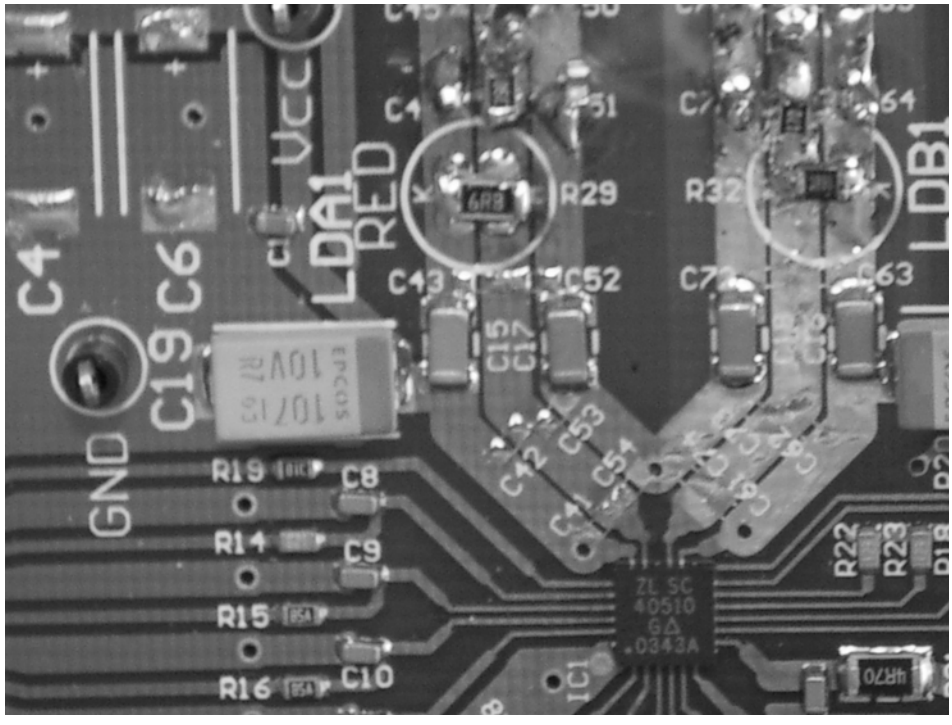


Figure 4 - ZLE40510/14 Application Board Electrical Interconnect

2.0 Application Diagram

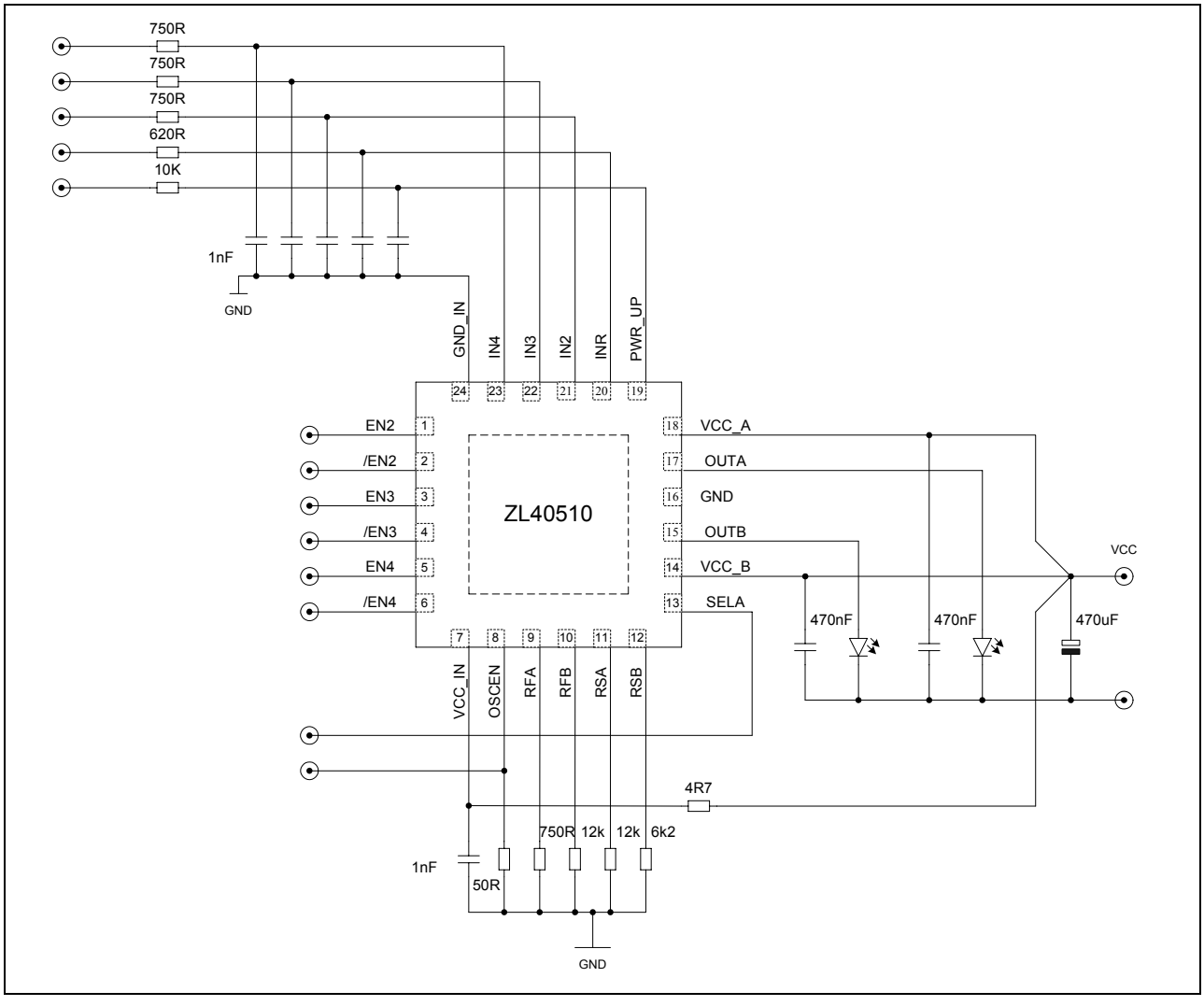


Figure 5 - Application Schematic Diagram

3.0 Evaluation Boards From Zarlink Semiconductor

Zarlink Semiconductor provides an LDD evaluation board. This is primarily for those interested in performing their own assessment of the operation of the LDDs. Figure 5 shows a recommended application configuration. The inputs are connected via side launch SMA connectors.

Please order as ZLE40510.

4.0 Optical Pulse Response

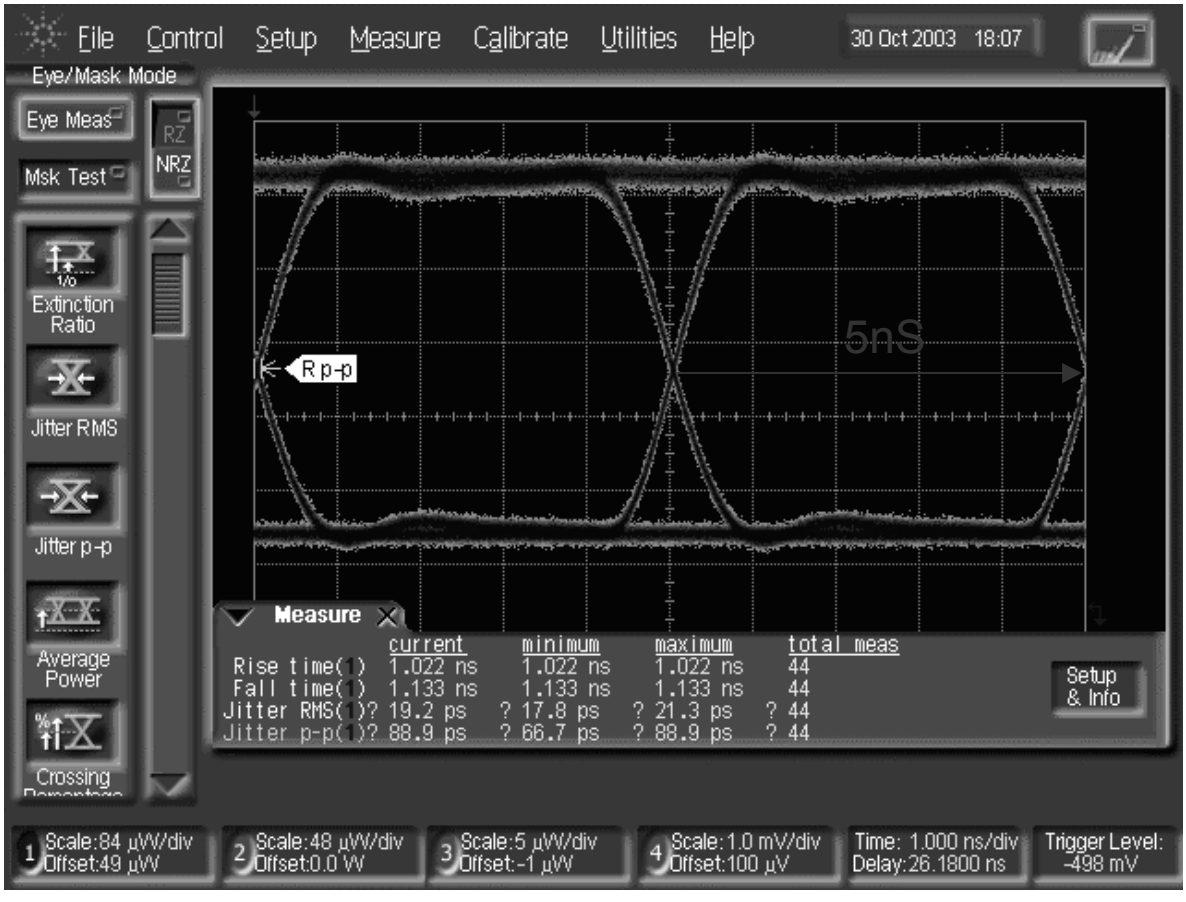


Figure 6 - Typical Optical Eye Diagram Response*

* (Measured using Sanyo DL-7140-201S Infra Red Laser Mounted on ZLE40510 Application Board)
(I read = 50 mA, I write =125 mA, at 15 mm with 200 MHz PRBS Pattern)

Figure 6 illustrates the typical optical response measured with the ZL40510/14 mounted on the ZLE40510/14 application board driving a Sanyo DL-7140-201S Infra Red Laser. The test condition is driving a PRBS pattern at 200 MHz clock rate which is representative of a 16X DVD write pattern using Block Write Strategy with minimum write pulse of 2T duration.

The Sanyo DL-7140-201S Infra Red Laser Diode On resistance is typically 3 Ohms which is representative of the On resistance of the Latest generation 250 mW pulsed High Power Red Laser Diodes that are targeted at 16X and 8X DVD.

The pulse is measured stepping from a low level which is above the laser threshold thus avoiding the laser turn on transient which can distort the measured response.

The ZL40510/14 exhibits excellent pulse response characteristics when used with the optimum interconnect.

5.0 Pin List

Pin No.	Pin name	Type	Function
1	EN2	LVDS	Positive digital control input for channel 2
2	/EN2	LVDS	Negative digital control input for channel 2
3	EN3	LVDS	Positive digital control input for channel 3
4	/EN3	LVDS	Negative digital control input for channel 3
5	EN4	LVDS	Positive digital control input for channel 4
6	/EN4	LVDS	Negative digital control input for channel 4
7	VCC_IN	supply	+5 V Input power supply
8	OSCEN	digital	Oscillator enable control input, high active (TTL)
9	RFA	analog	Resistor to GND sets oscillator frequency when SELA = ’High’
10	RFB	analog	Resistor to GND sets oscillator frequency when SELA = ’Low’
11	RSA	analog	Resistor to GND sets oscillator amplitude when SELA = ’High’
12	RSB	analog	Resistor to GND sets oscillator amplitude when SELA = ’Low’
13	SELA	digital	Output select input; 'High' selects OUTA, 'Low' selects OUTB (TTL)
14	VCC_B	supply	Output B Vcc
15	OUTB	analog	Current output source B
16	GND	supply	Ground
17	OUTA	analog	Current output source A
18	VCC_A	supply	Output A Vcc
19	PWR_UP	digital	Digital chip enable control input, high active (CMOS)
20	INR	analog	Current input, R_{in} = 400 Ohms to GND
21	IN2	analog	Current input, R_{in} = 250 Ohms to GND (Optional 500 Ohms)
22	IN3	analog	Current input, R_{in} = 250 Ohms to GND (Optional 500 Ohms)
23	IN4	analog	Current input, R_{in} = 250 Ohms to GND (Optional 500 Ohms)
24	GND_IN	supply	Ground for input circuit

Absolute Maximum Ratings

Characteristic	Min.	Typ.	Max.	Units	Comments
Supply voltage (VCC, VCC_IN)	-0.5		6.0	V	
Input voltage (INR, IN2, IN3, IN4)	-0.5		6.0	V	
Input voltage (PWR_UP, EN2, /EN2, EN3, /EN3, EN4, /EN4, OSCEN, SELA)	-0.5		(VCC_IN + 0.5)	V	
Output voltage (OUTA, OUTB)	-0.5		Vcc	V	
Junction temperature			150	°C	

Operating Range

Characteristic	Min.	Typ.	Max.	Units	Comments
Supply voltage (VCC, VCC_IN)	4.5		5.5	V	
Input voltage (INR)			0.7	V	
Input voltage (IN2, IN3, IN4)			0.7	V	
Output voltage (OUTA, OUTB)	-0.3		(VCCA, B-0.9)	V	
RF	1			kΩ	External resistor to GND
RS	1			kΩ	External resistor to GND
Operating temperature range, junction	0		150	°C	

Package Thermal Resistance

Package Type	Junction to		Units	Comments
	Case R_{thJC}	ambient R_{thJA}		
24 pin QFN		40	K/W	Exposed paddle soldered to multi-layer PCB

Electrical Characteristics Vcc = 5 V, T_{amb} = 25°C, INR = 400 µA, IN2 = IN3 = IN4 = 160 µA, PWR_UP = High, Ch2, Ch3, Ch4 disabled, OSCEN = Low, unless otherwise specified.

Characteristic	Min.	Typ.	Max.	Units	Comments	Type
Supply Current (into VCC-pin)						
Supply current, power down, I_{ccPD}		80	220	µA	ENABLE = Low	A
Supply current, read mode, oscillator disabled, I_{ccR0}		69	84	mA	INR = 400 µA	A
Supply current, read mode, oscillator enabled, I_{ccR1}		70	85	mA	OSCEN = High, RF = 6.8 kOhm, RS = 8.2 kOhm,	A
Supply current, write mode, I_{ccW}		210	250	mA	Ch2, Ch3, Ch4 enabled	B
Supply current, input off		18		mA	Ch2, Ch3, Ch4 enabled INR = IN2 = IN3 = IN4 = 0	B
SelA & OscEn Digital Inputs						
Logic low voltage			0.8	V		A
Logic high voltage	2.2			V		A
Threshold level		1.68		V	Temperature stabilised	B
Logic low input current	-50			µA	V_{in} = 0 V	B
Logic high input current			50	µA	V_{in} = 3.3 V	B
Power_Up Digital Input						
Logic low voltage			0.5	V	CMOS compatible level	A
Logic high voltage	2.7			V	CMOS compatible level	A
Logic low input current	-50			µA	V_{in} = 0 V	B
Logic high input current			50	µA	V_{in} = 3.3 V	B
LVDS Digital Inputs						
Input voltage range	0		2.4	V		B
Differential input voltage	100		600	mV	V(EN2~/EN2) LVDS Compatible V(EN3~/EN3) LVDS Compatible V(EN4~/EN4) LVDS Compatible	A
Differential Input impedance	87	110	133	Ω		B
Common mode input impedance		10		kΩ	internal resistor to Vcc	B

Note: A = 100% Tested
B = Guaranteed by Characterization and Design
C = Guaranteed by Simulation

Characteristic	Min.	Typ.	Max.	Units	Comments	Type
Current Outputs (OutA & OutB)						
Output current, ChR	150	200		mA	$V_{out} \leq 3.5$ V	B
Output current, Ch2, Ch3, Ch4	500			mA	Channel enabled, INR = 0 μA, $V_{out} \leq$ 3.5 V,Iin = 2.8 mA	A
Total output current	700			mA	Ch2, 3, 4 enabled, $V_{out} \leq 3.5$ V	A
Write Output current, zero input, I_{out0} **(ZL40510)**			12	mA	INR = IN2 = IN3 = IN4 = 0 μA, Ch2, or Ch3 or Ch4 enabled	A
Write Output current, zero input, I_{out0} **(ZL40514)**			15	mA	INR = IN2 = IN3 = IN4 = 0 μA, Ch2, or Ch3 or Ch4 enabled	
Read Output current, zero input, I_{out0}			2.5	mA	INR = IN2 = IN3 = IN4 = 0 μA, Ch2, 3 & 4 disabled	A
Input impedance (INR)	330	400	470	Ω	R_{in} is to GND	B
Input impedance (IN2, IN3, IN4)	205	250	295	Ω	R_{in} is to GND	B
I_{out} supply sensitivity (any channel)	-5		+5	%/V	I_{out} = 40 mA to 300 mA	B
I_{out} temperature sensitivity (any channel)		300		ppm/°C	I_{out} = 40 mA to 300 mA, I_{in} temp coefficient = 0 ppm/°C	B
I_{out} current output noise		3		nA/√Hz	I_{out} = 50 mA InR = 500 uA	B
Current Output OutA & OutB						
Current gain, ChR, best fit	85	100	115	mA/mA	I_{out} = 20 mA to 80 mA †Note 1	A
Current gain, Ch2, best fit	205	240	275	mA/mA	I_{out} = 20 mA to 120 mA † Note 2	A
Current gain, Ch3, best fit	205	240	275	mA/mA	I_{out} = 20 mA to 120 mA † Note 2	A
Current gain, Ch4, best fit	205	240	275	mA/mA	I_{out} = 20 mA to 120 mA † Note 2	A
ZL40510						
Output current offset, ChR, best fit.	-1		8	mA	I_{out} = 20 mA to 80 mA † Note 1	A
Output current offset, Ch2, best fit	-4		12	mA	I_{out} = 20 mA to 120 mA † Note 2	A
Output current offset, Ch3, best fit	-4		12	mA	I_{out} = 20 mA to 120 mA † Note 2	A

Characteristic	Min.	Typ.	Max.	Units	Comments	Type
Output current offset, Ch4, best fit	-4		12	mA	I_{out} = 20 mA to 120 mA † Note 2	A
ZL40514						
Output current offset, ChR, best fit. Note 3	-1		8	mA	I_{out} = 20 mA to 80 mA † Note 1	A
Output current offset, Ch2, best fit. Note 4	-7		15	mA	I_{out} = 20 mA to 120 mA † Note 2	A
Output current offset, Ch3, best fit. Note 4	-7		15	mA	I_{out} = 20 mA to 120 mA † Note 2	A
Output current offset, Ch4, best fit. Note 4	-7		15	mA	I_{out} = 20 mA to 120 mA † Note 2	A
ZL40510 & ZI40514						
Output current linearity (any channel). Note 3	-3.5		1.5	%	I_{out} = 20 mA to 120 mA † Note 2	A
Gain tracking, Ch2 to Ch3 to Ch4	-2.5		+2.5	%	I_{out} = 20 mA to 120 mA † Note 2	A

Note: A = 100% Tested
B = Guaranteed by Characterization and Design
C= Guaranteed by Design

Note 1: Gain, offset and linearity of a channel are derived from a best fit line (linear regression graph) to the following three operating points: Iout = 20mA, 50mA and 80mA.

Note 2: Gain, offset and linearity of a channel are derived from a best fit line (linear regression graph) to the following three operating points: Iout = 20mA, 70mA and 120mA.

Note 3: Best Fit output line through 20mA,50mA,80mA

Note 4: Best Fit output line through 20mA,70mA,120mA

† Electrical measurement into 3.9 Ohm to Gnd

Characteristic	Min.	Typ.	Max.	Units	Comments	Type
Timing						
Current Output OutA & OutB						
Channel rise time, (10% to 90%), t_{r2}		0.9	1.2	ns	40 to 375 mA, Ch2, 3 or 4 pulsed † ‡	B
Channel fall time, (10% to 90%), t_{f2}		1.1	1.4	ns	40 to 375 mA, Ch2, 3 or 4 pulsed † ‡	B
Output current overshoot (any write channel)			13	%	40 to 375 mA Ch2 3, 4 pulsed †	B
Output current undershoot (any write channel)			13	%	40 to 375 mA Ch2 3, 4 pulsed †	B
Channel to Channel Enable Skew Tr		50		ps		B
Channel to Channel Enable Skew Tf		25		ps		B
I_{out} ON propagation delay, t_{onCh}		1.4	1.8	ns	50% En High-Low to 50% I_{out}, any write channel	B
I_{out} OFF propagation delay, t_{offCh}		1.2	1.6	ns	50% En Low-High to 50% I_{out}, any write channel	B
Amplifier -3dB bandwidth (ChR)	23	43	68	MHz	INR = 400 μA	C
Amplifier -3dB bandwidth (Ch2, 3, 4)	6	11	16	MHz	IN2, IN3, IN4 = 400 μA	C
Power_Up & SelA						
Power_Up time, t_{on}		1.5	3.5	μs	50% Enable Low-High to 50% I_{out}	C
Power_Up time, t_{off}		20	33	ns	50% Enable High-Low to 50% I_{out}	C
Output A select delay		5	8	ns	50% DVD/CD select Low-High to 50% I_{OUTA}	C
Output A deselect delay		5	8	ns	50% DVD/CD select High-Low to 50% I_{OUTA}	C

Note: A = 100% Tested
B = Guaranteed by Characterization and Design
C= Guaranteed by Design

† (EN2, /EN2), (EN3, /EN3), (EN4, /EN4) input pulse rise and fall time = 0.4 ns.

‡ Parameter is measured Electrical Pulse Response using 3.9 Ohm load to gnd and Zarlink Application Board. Pulse response performance parameters Trise, Tfall, Overshoot and Undershoot can be limited by interconnect inductance. Optical Response is influenced by Laser Diode response. See Application Notes.

Electrical Dynamic Characteristics Vcc = 5 V, T_{amb} = 25°C, INR = 400 uA, IN2 = IN3 = IN4 = 160 µA, PWR_UP = High, Ch2, Ch3, Ch4 disabled, OSCEN = Low, unless otherwise specified.

Characteristic	Min.	Typ.	Max.	Units	Comments	Type
Oscillator						
Frequency adjust range Low			250	MHz	RF = 16 kΩ, OSCEN = High	B
Frequency adjust range High	575			MHz	RF = 2 kΩ, OSCEN = High	B
Frequency tolerance **(ZL40510)**	338	375	412	MHz	RF = 7.5 kΩ, OSCEN = High	A
Frequency tolerance **(ZL40514)**	322	375	428	MHz	RF = 7.5 kΩ, OSCEN = High	A
Frequency temperature coefficient		200		ppm/ °C	RF = 7.5 kΩ, OSCEN = High	C
Amplitude adjust range Low (RS=11KΩ)			36	mA pk to pk	RS = 11 kΩ, OSCEN = High RF=9 K (350 MHz) InR = 1 mA	B
Amplitude adjust range High (RS=1KΩ)	100			mA pk to pk	RS = 1 kΩ, OSCEN = High RF = 9 K (330 MHz) InR = 1 mA	B
Third Harmonic		-30		dBC	RS = 10 kΩ to 2 kΩ, OSCEN = High RF = 9 K (330 MHz) InR = 400 uA	C
Second Harmonic		-20		dBC	RS = 10 kΩ to 2 kΩ, OSCEN = High RF = 9 K (330 MHz) InR = 400 uA	C
Amplitude tolerance	-20	0	20	%	Fosc= 250 MHz to 450 MHz, OSCEN = High, RS 1%	C
Amplitude (RS = 7.5 K)		42		mA pk to pk	f = 375 MHz, RS = 7.5 kΩ, OSCEN = High	C
Amplitude flatness		4		dB	RS = 7.5 kΩ, RF = 9 kΩ to 4 kΩ	B
Amplitude temperature coefficient		800		ppm/ °C	RF = 5.6 kΩ, OSCEN = High	C
Oscillator enable time, t_{onOsc}			2	ns	50% OSCEN High-Low to 50% I_{out}	B
Oscillator disable time, t_{offOsc}			3	ns	50% OSCEN Low-High to 50% I_{out}	B

Note: A = 100% Tested
B = Guaranteed by Characterization and Design
C= Guaranteed by Design
† (EN2, /EN2), (EN3, /EN3), (EN4, /EN4) pulse rise and fall time = 0.4 ns.

6.0 Characteristic Curves

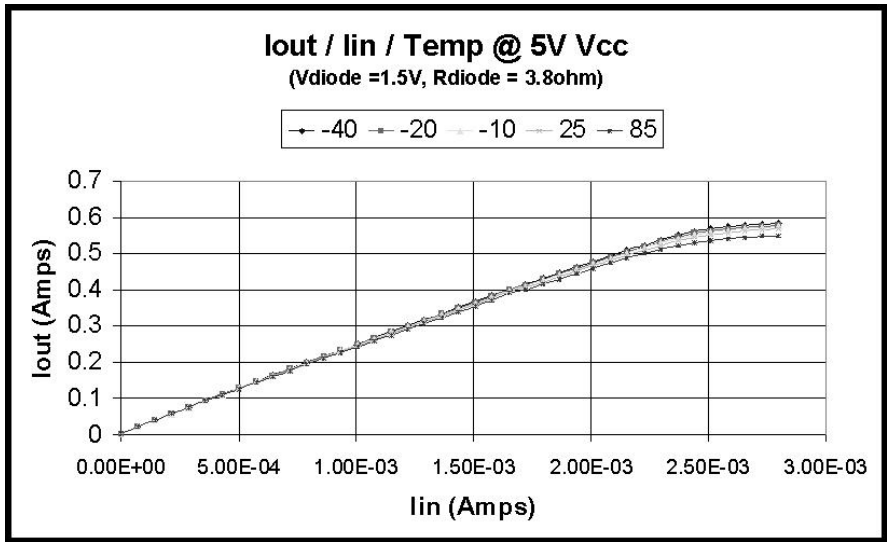


Figure 7 - Write Channel 2, 3 and 4 IP/OP Transfer Characteristic/Temp

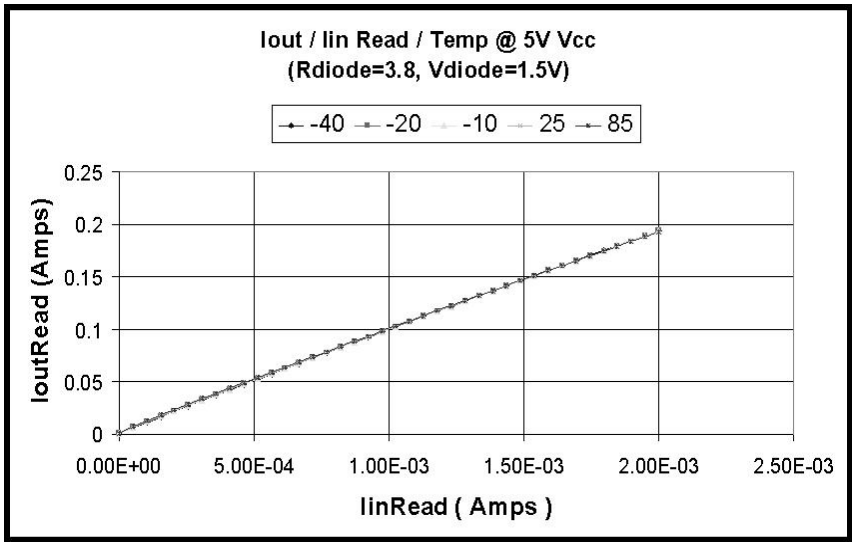


Figure 8 - Read Channel IP/OP Transfer Characteristic/Temp

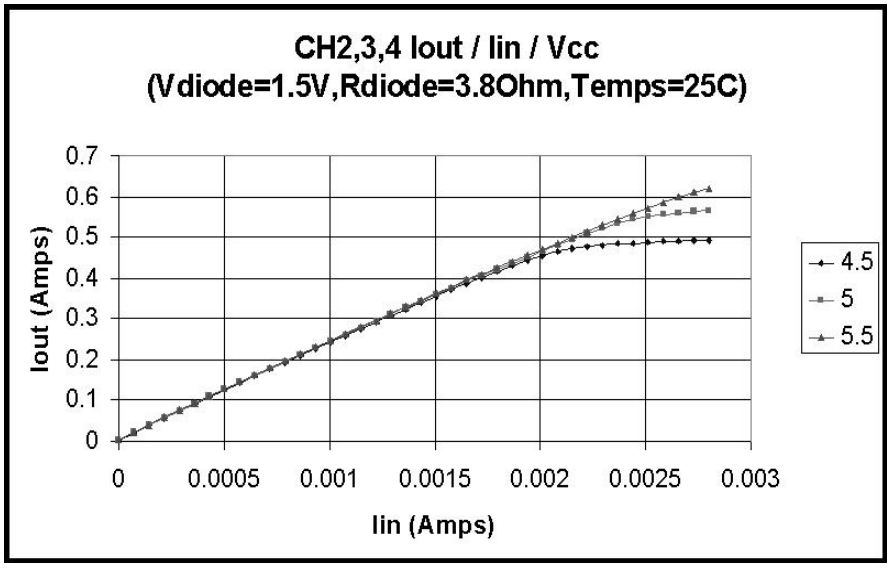


Figure 9 - Write Channel 2, 3 or 4 IP/OP Transfer Characteristic/Vcc

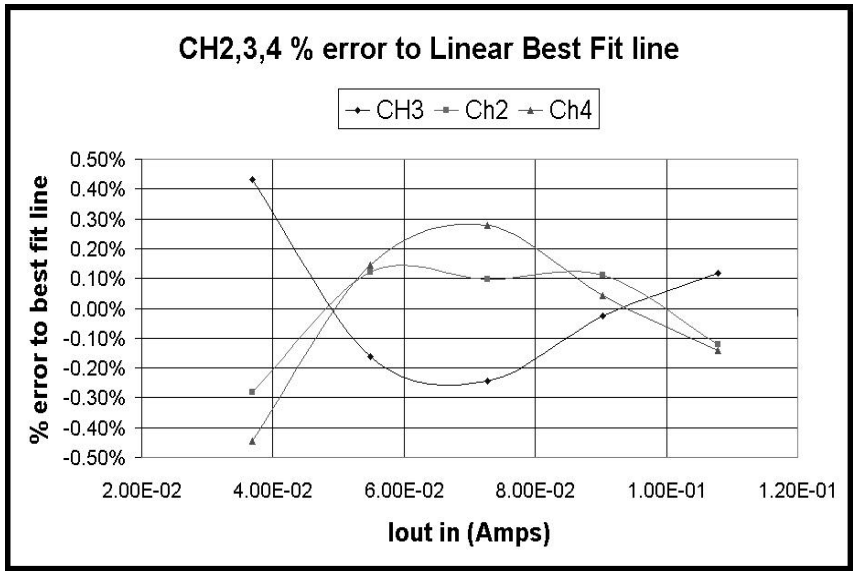


Figure 10 - Write Channel 2, 3 or 4 IP/OP Best Fit Line% Error

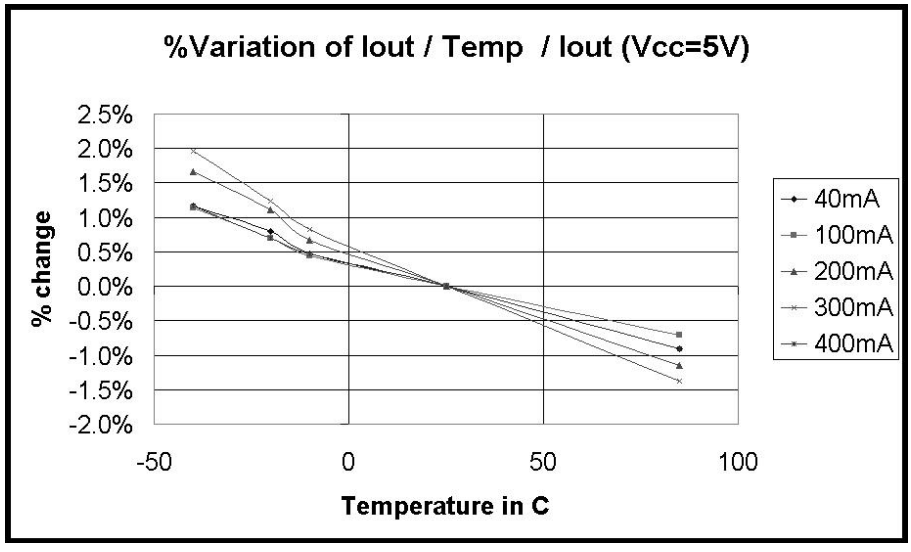


Figure 11 - Write Channel 2, 3 or 4 ∆ Iout% Variation with Temperature

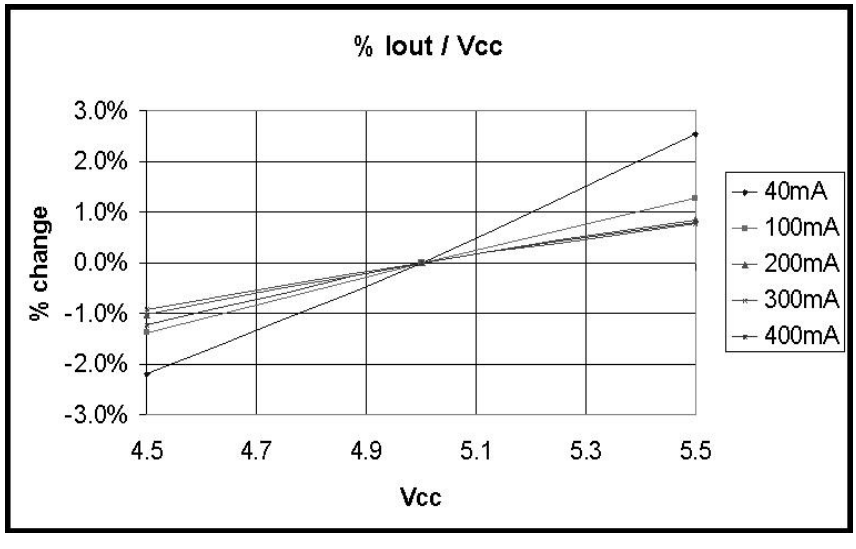


Figure 12 - Write Channel 2, 3 or 4 ∆ Iout% Variation with Vcc

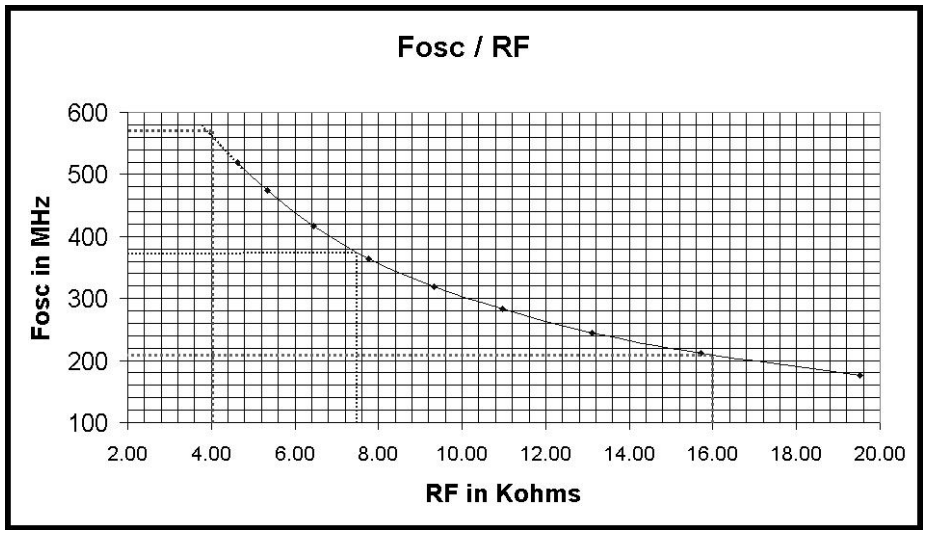


Figure 13 - Oscillator Frequency/RF
Vcc = 5 V, Temp = 25°C

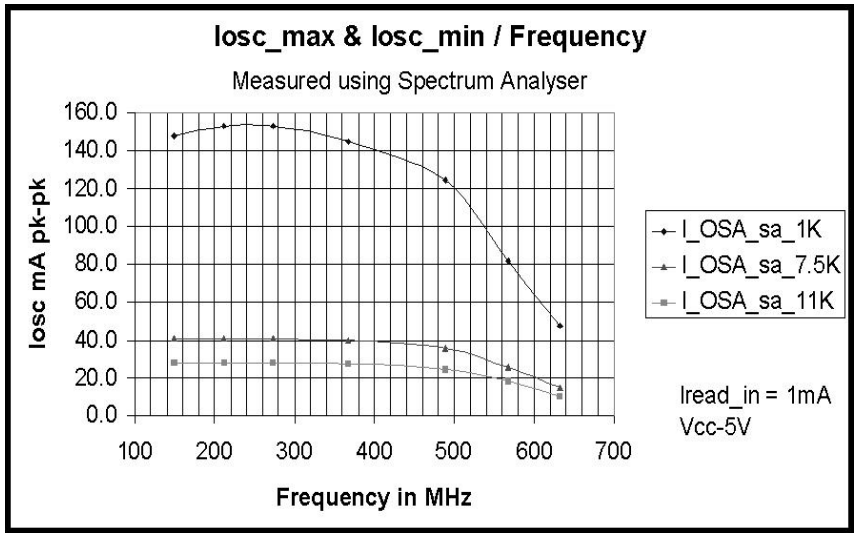


Figure 14 - Iosc Out/Frequency/
RS = 1 K, 7.5 K, 11 K, Vcc = 5 V, Temp = 25°C

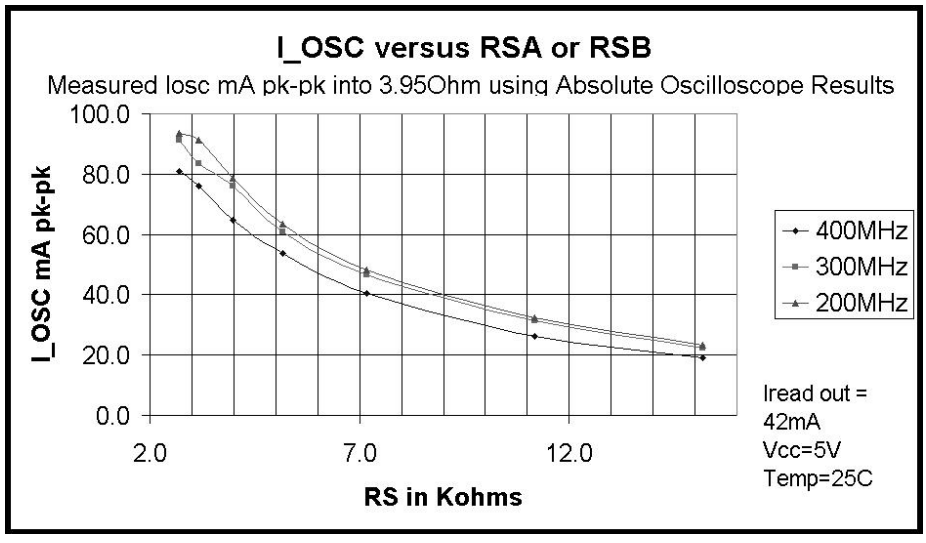


Figure 15 - Iosc Amplitude mA pk-pk/RSA or RSB
Vcc = 5 V, Temp = 25°C

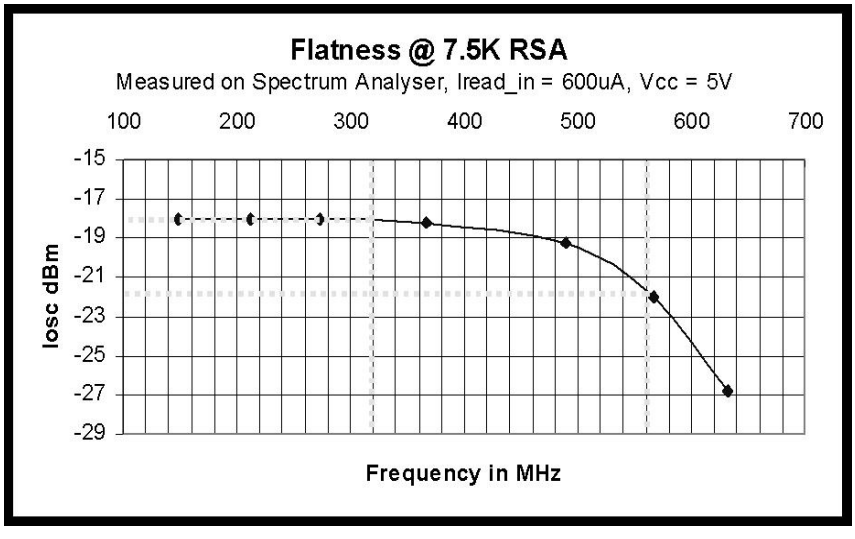


Figure 16 - Iosc/Frequency
RS = 7.5 K, Vcc = 5 V, Temp = 25°C

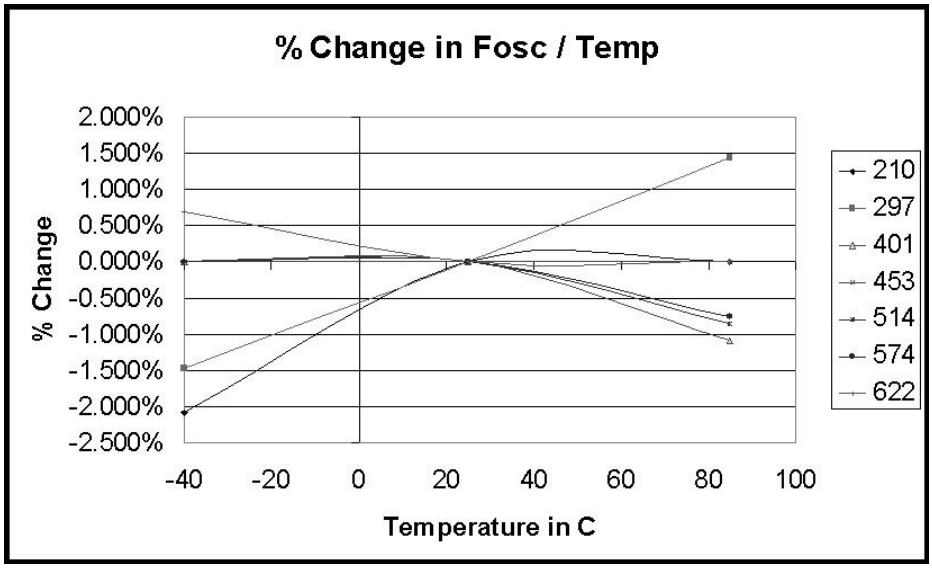


Figure 17 - ∆ Freq% Variation with Temperature

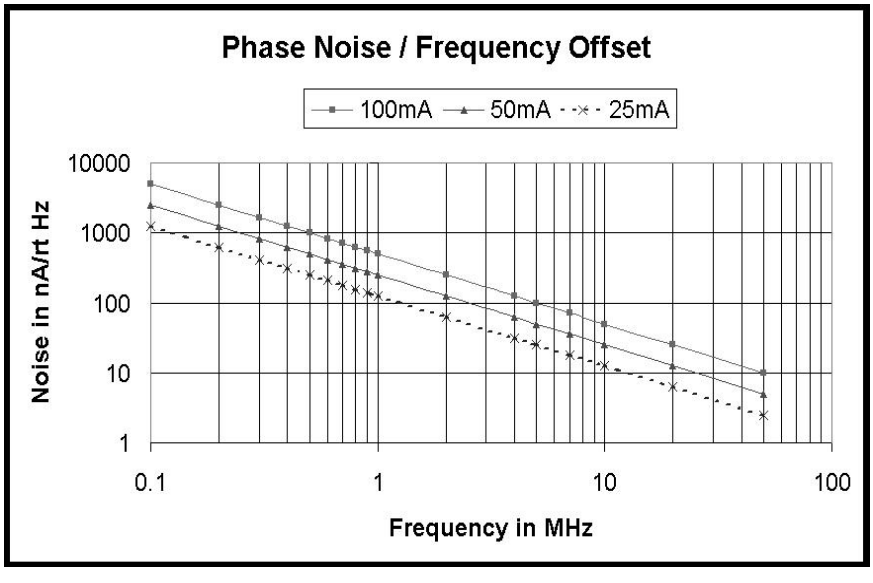


Figure 18 - Oscillator Noise Spectral Density
Vcc = 5 V, Temp = 25°C

7.0 I/O Diagrams

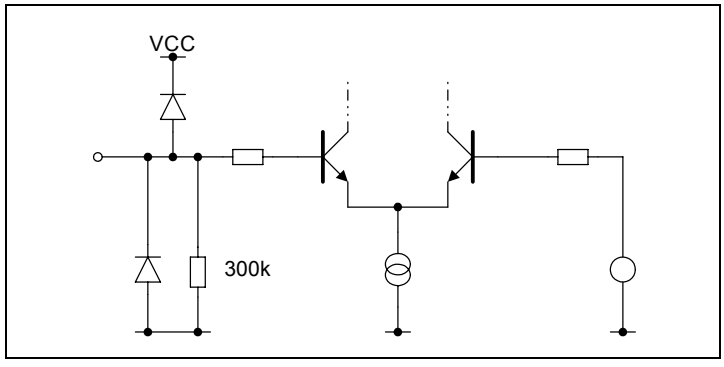


Figure 19 - CMOS/LVTTL Input (PWR_UP, OSCEN)

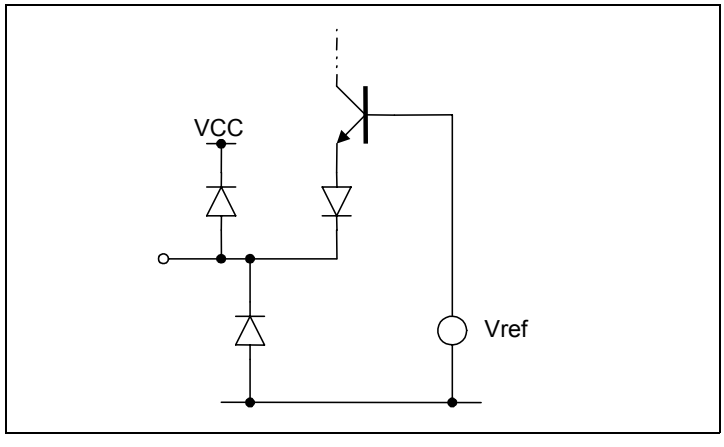


Figure 20 - Oscillator Resistors (RF, RS)

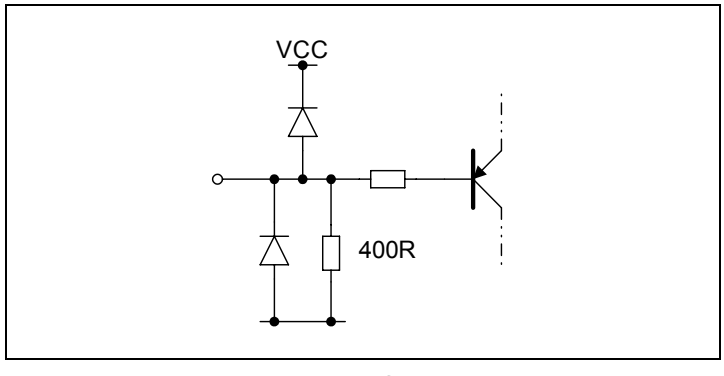


Figure 21 - Read Current Input (INR)

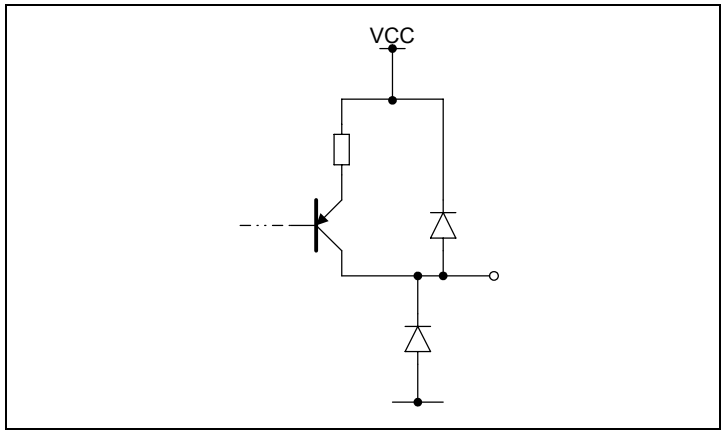


Figure 22 - Output (OUTA, OUTB)

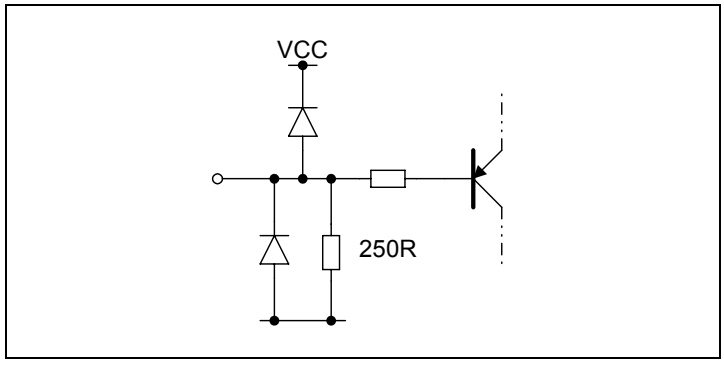


Figure 23 - Write Current Input (IN2, IN3, IN4)

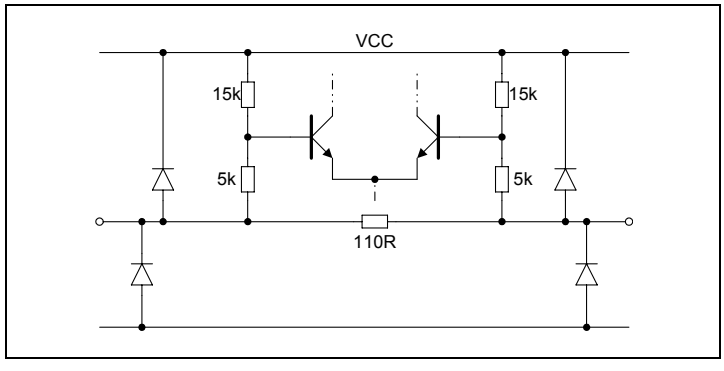


Figure 24 - LVDS Input (EN2, /EN2), (EN3, /EN3), (EN4, /EN4)

8.0 Timing Waveforms

Applying logic levels to the inputs, as shown in Table 1, gives the output waveform shown in Figure 26.

PWR_UP	EN2	EN3	EN4	OUTPUT
0	X	X	X	OFF
1	0	0	0	READ
1	1	0	0	LEVEL 2
1	1	1	0	LEVEL 3
1	1	1	1	LEVEL 4
Note: 1 = logic high, 0 = logic low and X = "don’t care"				

Table 1 - Output Function for Set Logic Inputs

9.0 Timing Diagrams

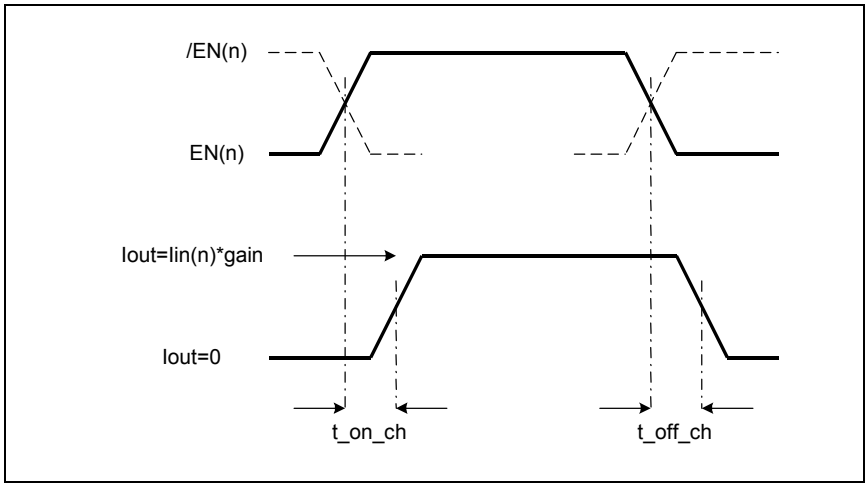


Figure 25 - Timing of Read or Write Channels

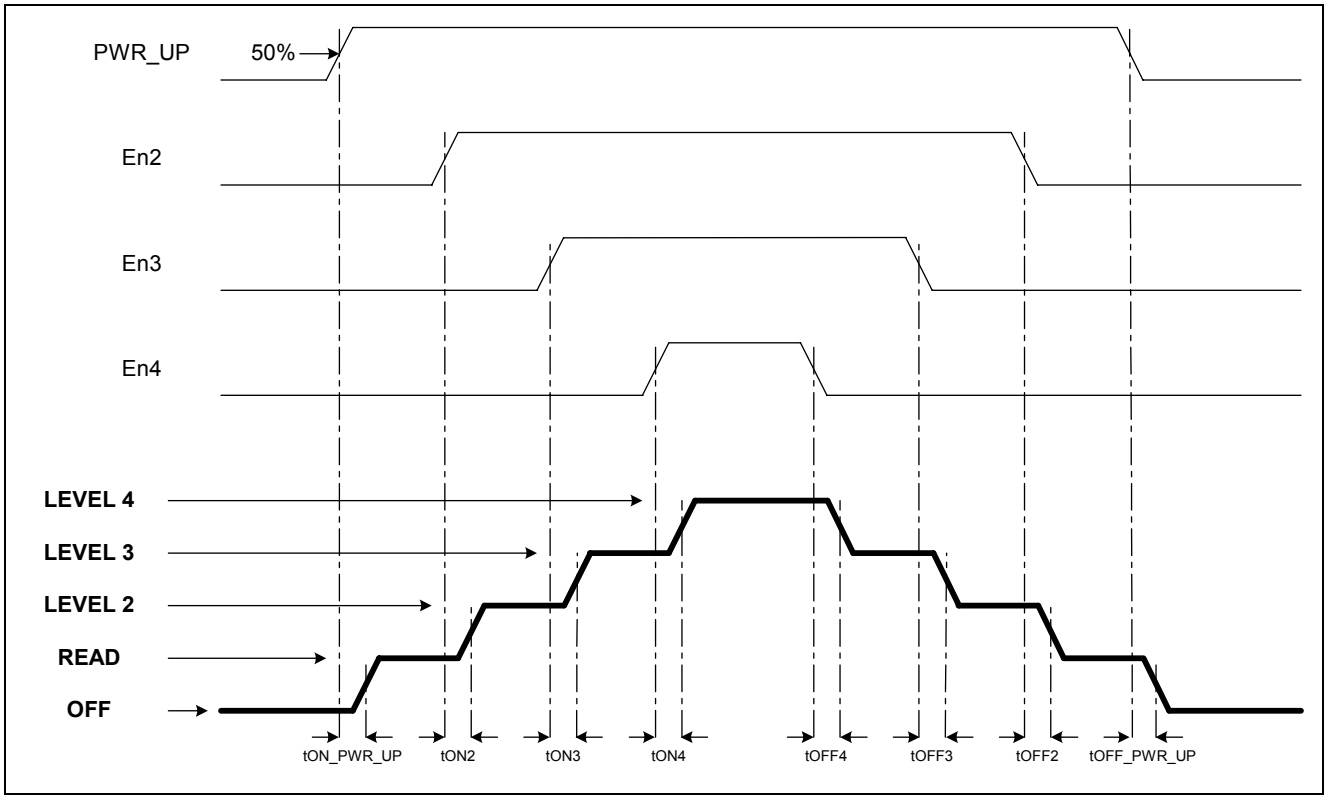


Figure 26 - Output Waveform Showing Addition of Read and Write Levels

10.0 Example Waveforms

10.1 Write Waveform

The Write output waveform may be produced as shown in example 1, Figure 27. The Erase level is set by switching off both the Bias level and the Write level. The Write switching waveform is produced by switching off the Erase level and Switching on the Bias level and then modulating that with the Write level. The peak of the Write waveform is the sum of the Bias and the Write levels.

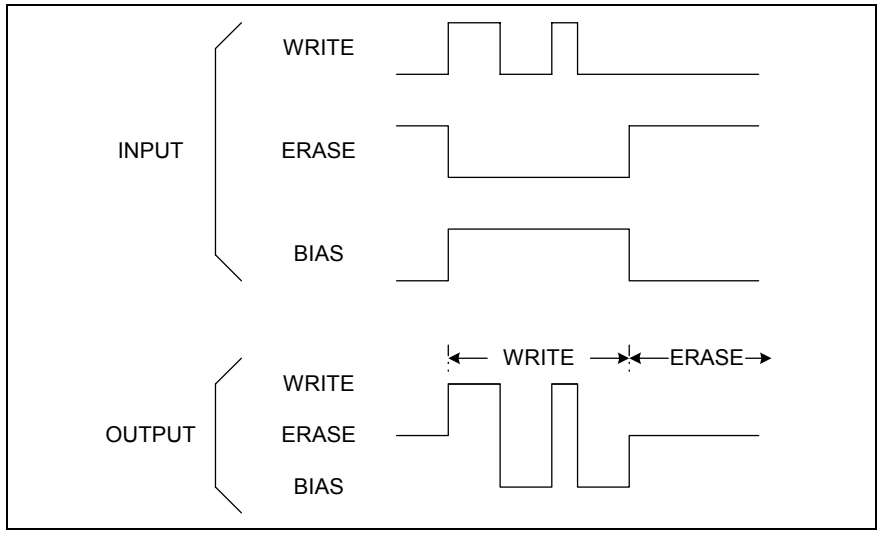


Figure 27 - Example of Write Waveform

NOTES:

1. Only the Write signal changes to modulate the output during the Write pulse.
2. Each of the Write Channels can provide up to 500 mA. It is not necessary to add together the output of more than one Write Channel to achieve 500 mA.

10.2 Oscillator Waveform

The Oscillator may be enabled independently and is summed with the selected level.

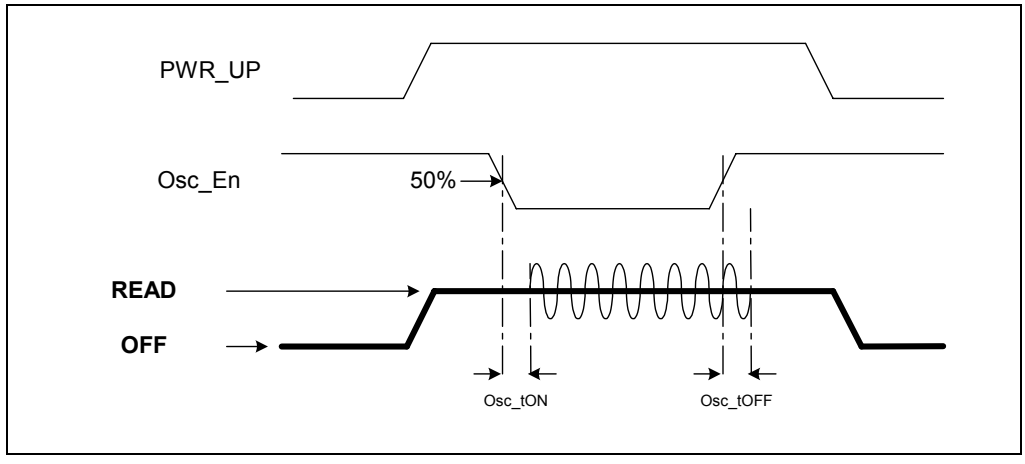
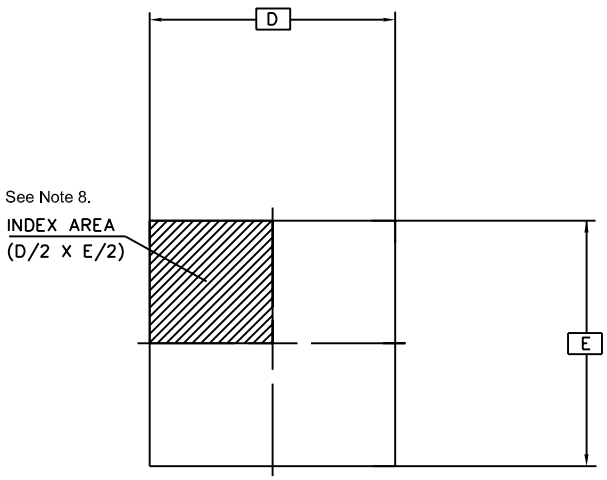
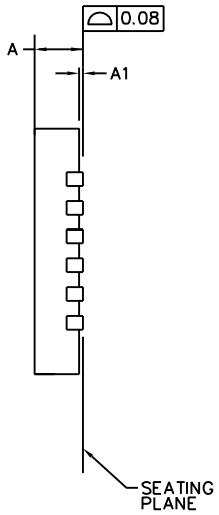


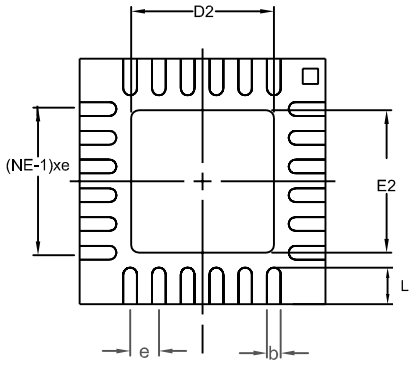
Figure 28 - Example of Oscillator Waveform Superimposed on the Read Waveform

NOTE: The amplitude of the Oscillator must be less than the programmed DC output level to avoid clipping and subsequent increase in harmonic distortion.



TOP VIEW





BOTTOM VIEW

SYMBOL	COMMON DIMENSIONS	
	MIN.	MAX.
A	0.80	1.00
A1	0.00	0.05
b	0.18	0.30
D	4.00 BSC	
D2	2.00	2.25
E	4.00 BSC	
E2	2.00	2.25
N	24	
Nd	6	
Ne	6	
e	0.50 BSC	
L	0.30	0.50

Conforms to JEDEC MO-220

NOTES:
1. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd & Ne ARE THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED
   BETWEEN 0.25 AND 0.30mm FROM TERMINAL.
4. ALL DIMENSIONS ARE IN MILLIMETERS.
5. LEAD COUNT IS 24 .
6. PACKAGE WARPAGE MAX 0.08mm.
7. NOT TO SCALE.
8. TERMINAL #1 IDENTIFIER MUST BE LOCATED WITHIN THE ZONE INDICATED AND MAY BE EITHER A MOULD OR MARKED FEATURE.

ISSUE	1	2		
ACN	CDCA	CDCA		
DATE	11Aug03	5Sep03		
APPRD.				

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