ZARLINK SEMICONDUCTOR

ZL10312
Satellite Demodulator
Data Sheet

November 2004

Features

- Conforms to EBU specification for DVB-S and DirecTV specification for DSS
- On-chip digital filtering supports 1 - 45 MSps symbol rates
- On-chip 60 or 90 MHz dual-ADC
- High speed scanning mode for blind symbol rate/code rate acquisition
- Automatic spectral inversion resolution
- High level software interface for minimum development time
- Up to ±22 MHz LNB frequency tracking
- DiSEqC™ v2.2: receive/transmit for full control of LNB, dish and other components
- Compact 64 pin LQFP package (7 x 7 mm)
- Sleep pin gives ~1,000 fold reduction in power to help products meet ENERGY STAR® requirements

Applications

- DVB 1 - 45 MSps compliant satellite receiver
- DSS 20 MSps compliant satellite receivers
- SMATV trans-modulators. (Single Master Antenna TV)
- Satellite PC applications

Ordering Information

ZL10312QCG	64 Pin LQFP	Trays, Bake & Drypack
ZL10312QCF	64 Pin LQFP	Tape & Reel
ZL10312QCG1	64 Pin LQFP*	Trays, Bake & Drypack
ZL10312UBH	Die supplied in wafer form**	

*Pb Free Matte Tin
**Please contact Sales for further details

0°C to +70°C

Description

The ZL10312 is a QPSK/BPSK 1 - 45 MSps demodulator and channel decoder for digital satellite television transmissions to the European Broadcast Union ETS 300 421 specification. It receives analogue I and Q signals from the tuner, digitises and digitally demodulates this signal, and implements the complete DVB/DSS FEC (Forward Error Correction), and de-scrambling function. The output is in the form of MPEG2 or DSS transport stream data packets. The ZL10312 also provides automatic gain control to the RF front-end device.

The ZL10312 has a serial 2-wire bus interface to the control microprocessor. Minimal software is required to control the ZL10312 because of the built in automatic search and decode control functions.

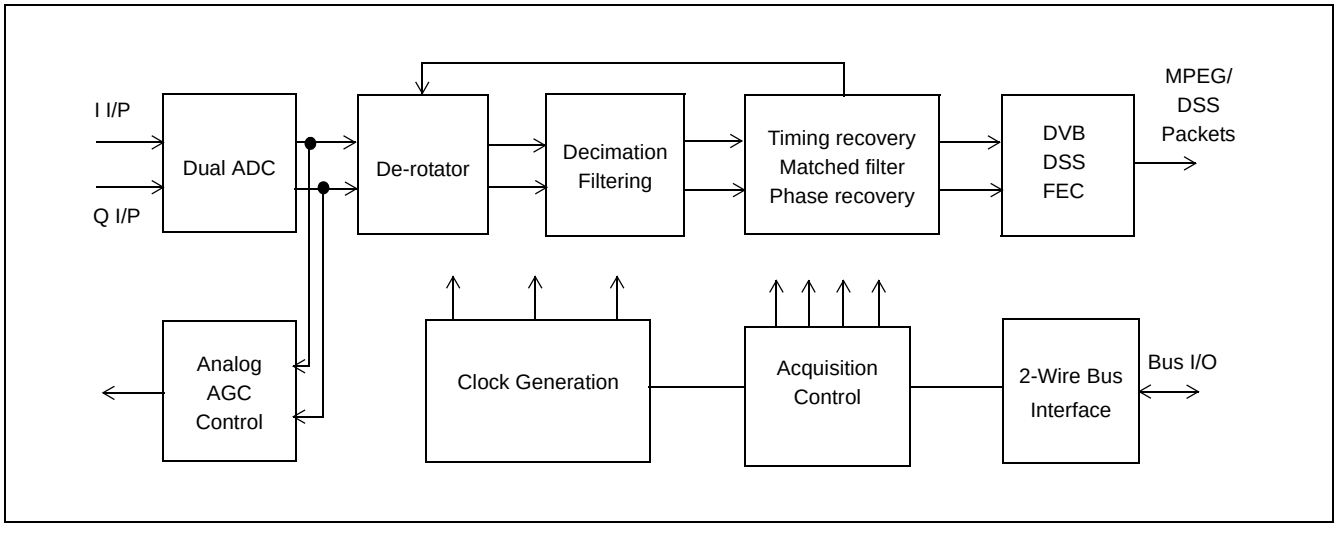


Figure 1 - Functional Block Diagram

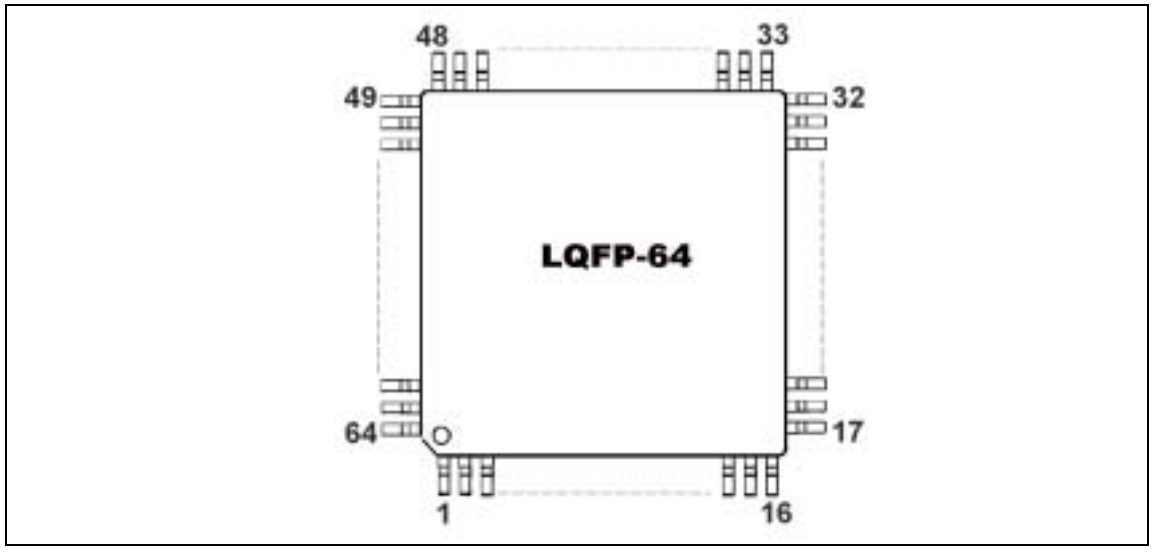


Figure 2 - ZL10312 Pin Allocation

Pin Table

No.	Name	No.	Name	No.	Name	No.	Name
1	$\overline{\text{Reset}}$	17	CVdd	33	Gnd	49	MDO[1]
2	DiSEqC[2]	18	Gnd	34	CVdd	50	CVdd
3	DiSEqC[1]	19	$\overline{\text{XTI}}$	35	Addr[1]	51	Gnd
4	DiSEqC[0]	20	XTO	36	Addr[2]	52	MDO[2]
5	Vdd	21	Gnd	37	Addr[3]	53	MDO[3]
6	Gnd	22	CVdd	38	Addr[4]	54	Gnd
7	CVdd	23	Gnd	39	Vdd	55	Vdd
8	Gnd	24	Iin	40	Gnd	56	MDO[4]
9	Sleep	25	$\overline{\text{Iin}}$	41	AGC	57	MDO[5]
10	CLK1	26	Gnd	42	Test	58	Gnd
11	DATA1	27	Vdd	43	$\overline{\text{IRQ}}$	59	CVdd
12	CVdd	28	Gnd	44	CVdd	60	MDO[6]
13	Gnd	29	$\overline{\text{Qin}}$	45	Gnd	61	MDO[7]
14	DATA2	30	Qin	46	MOSTRT	62	MOCLK
15	CLK2	31	Gnd	47	MOVAL	63	$\overline{\text{BKERR}}$
16	OscMode	32	CVdd	48	MDO[0]	64	Status

Note: All supply pins **must** be connected as they are not all commoned internally.

Table of Contents

Overview

The ZL10312 is a QPSK/BPSK 1 - 45 MSps demodulator and channel decoder for digital satellite television transmissions compliant to both DVB-S and DSS standards and other systems.

A Command Driven Control (CDC) system is provided making the ZL10312 very simple to program. After the tuner has been programmed to the required frequency to acquire a DVB transmission, the ZL10312 requires a minimum of five registers to be written.

The ZL10312 provides a monitor of Bit Error Rate after the QPSK module and also after the Viterbi module. For receiver installation, a high speed scan or 'blind search' mode is available. This allows all signals from a given satellite to be evaluated for frequency, symbol rate and convolutional coding scheme. The phase of the IQ signals can be automatically determined.

Full DiSEqC v2.x is provided for both writing and reading DiSEqC messages. Storage in registers for up to eight data bytes sent and eight data bytes received is provided.

Additional Features

- 2-wire bus microprocessor interface with separate interface to tuner
- All digital clock and carrier recovery
- On-chip PLL clock generation using low cost 10 to 16 MHz crystal
- Low power operation, with stand-by and sleep modes
- 3.3 V operation with 1.8 V for core logic
- 7 x 7mm 64 pin LQFP package
- Low external component count
- Commercial temperature range 0 to 70°C

Demodulator

- BPSK or QPSK programmable
- Optional fast acquisition mode for low symbol rates

Viterbi

- Programmable decoder rates 1/2, 2/3, 3/4, 5/6, 6/7, 7/8
- Automatic spectral inversion resolution
- Constraint length k=7
- Trace back depth 128
- Extensive SNR and BER monitors

De-Interleaver

- Compliant with DVB and DSS standards

Reed Solomon

- (204, 188) for DVB and (146,130) for DSS
- Reed Solomon bit-error-rate monitor to indicate Viterbi performance

De-Scrambler

- EBU specification de-scrambler for DVB mode

Outputs

- MPEG transport parallel & serial output
- Integrated MPEG2 TEI bit processing for DVB only

Application Support

- Design Manual
- Channel decoder system evaluation board
- Windows based evaluation software
- ANSI-C generic software

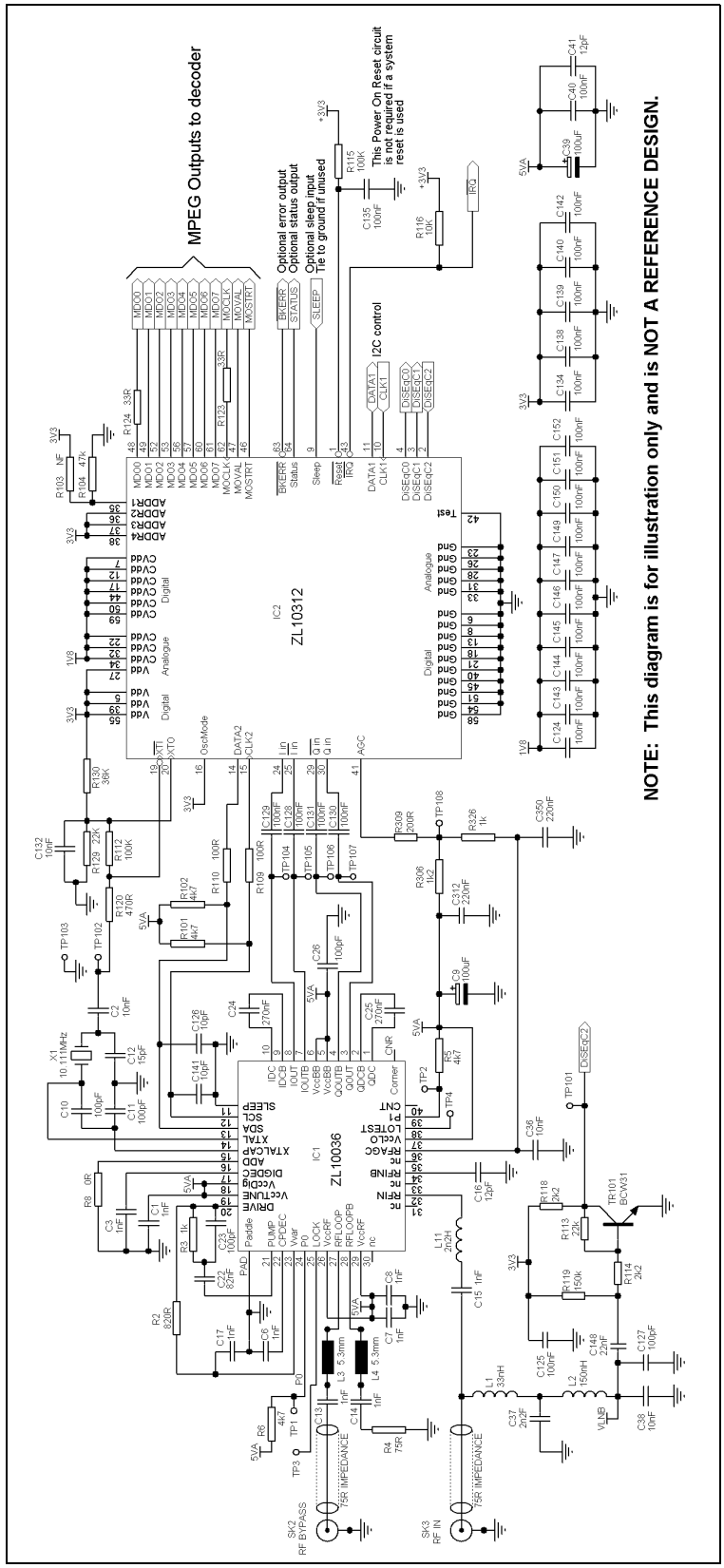


Figure 3 - Typical Application Schematic

1.0 Functional Overview

1.1 Introduction

ZL10312 is a single-chip variable rate digital QPSK/BPSK satellite demodulator and channel decoder. The ZL10312 accepts base-band in-phase and quadrature analogue signals and delivers an MPEG or DSS packet data stream. Digital filtering in ZL10312 removes the need for programmable external anti-alias filtering for all symbol rates from 1 - 45 MSps. Frequency, timing and carrier phase recovery are all digital and the only feed-back to the analogue front-end is for automatic gain control. The digital phase recovery loop enables very fine bandwidth control that is needed to overcome performance degradation due to phase and thermal noise.

All acquisition algorithms are built into the ZL10312 controller. The ZL10312 can be operated in a Command Driven Control (CDC) mode by specifying the symbol rate and Viterbi code rate. There is also a provision for a search for unknown symbol rates and Viterbi code rates.

1.2 Analogue-to-Digital Converter and PLL

The A/D converters sample single-ended or differential analogue inputs and consist of a dual ADC and circuitry to provide improved SiNaD (Signal-Noise and Distortion) and channel matching.

The fixed rate sampling clock is provided on-chip using a programmable PLL needing only a low cost 10 to 16 MHz crystal. Different crystal frequencies can be combined with different PLL ratios, depending on the maximum symbol rate, allowing a very flexible approach to clock generation. An external clock signal in the range 4 to 16 MHz can also be used as the master clock.

1.3 QPSK Demodulator

The demodulator in the ZL10312 consists of signal amplitude offset compensation, frequency offset compensation, decimation filtering, carrier recovery, symbol recovery and matched filtering. The decimation filters give continuous operation from 2Mbits/s to 90Mbits/s allowing one receiver to cover the needs of the consumer market as well as the single carrier per channel (SCPC) market with the same components without compromising performance, that is, the channel reception is within 0.5dB of theoretical. For a given symbol rate, control algorithms on the chip detect the number of decimation stages needed and switch them in automatically.

The frequency offset compensation circuitry is capable of tracking out up to ±22.5 MHz frequency offset. This allows the system to cope with relatively large frequency uncertainties introduced by the Low Noise Block (LNB). Full control of the LNB is provided by the DiSEqC outputs from the ZL10312. Horizontal/vertical polarisation and an instruction modulated 22kHz signal are available under register control. All DiSEqC v2.x functions are implemented on the ZL10312. An internal state machine that handles all the demodulator functions controls the signal acquisition and tracking. Various pre-set modes are available as well as blind acquisition where the receiver has no prior knowledge of the received signal. Fast acquisition algorithms have been provided for low symbol rate applications. Full interactive control of the acquisition function is possible for debug purposes. In the event of a signal fade or a cycle slip, the QPSK demodulator allows sufficient time for the FEC to re-acquire lock, for example, via a phase rotation in the Viterbi decoder. This is to minimise the loss of signal due to the signal fade. Only if the FEC fails to re-acquire lock for a long period (which is programmable) would QPSK try to re-acquire the signal.

The matched filter is a root-raised-cosine filter with either 0.20 or 0.35 roll-off, compliant with DSS and DVB standards. Although not a part of the DVB standard, ZL10312 allows a roll-off of 0.20 to be used with other DVB parameters. An AGC signal is provided to control the signal levels in the tuner section of the receiver and ensure the signal level fed to the ZL10312 is set at an optimal value under all reception conditions.

The ZL10312 provides comprehensive information on the input signal and the state of the various parts of the device. This information includes signal to noise ratio (SNR), signal level, AGC lock, timing and carrier lock signals. A maskable interrupt output is available to inform the host controller when events occur.

1.4 Forward Error Correction

The ZL10312 contains FEC blocks to enable error correction for DVB-S and DSS transmissions. The Viterbi decoder block can decode the convolutional code with rates 1/2, 2/3, 3/4, 5/6, 6/7 or 7/8. The block features automatic synchronisation, automatic spectral inversion resolution and automatic code rate detection. The trace back depth of 128 provides better performance at high code rates and the built-in synchronisation algorithm allows the Viterbi decoder to lock onto signals with very poor signal-to-noise ratios. A Viterbi bit error rate monitor provides an indication of the error rate at the QPSK output.

The 24-bit error count register in the Viterbi decoder allows the bit error rate at the output of the QPSK demodulator to be monitored. The 24-bit bit error count register in the Reed-Solomon decoder allows the Viterbi output bit error rate to be monitored. The 16-bit uncorrectable packet counter yields information about the output packet error rate. These three monitors and the QPSK SNR register allow the performance of the device and its individual components, such as the QPSK demodulator and the Viterbi decoder, to be monitored extensively by the external microprocessor. The frame/byte align block features a sophisticated synchronisation algorithm to ensure reliable recovery of DVB and DSS framed data streams under worst case signal conditions. The de-interleaver uses on-chip RAM and is compatible with the DVB and DSS algorithms. The Reed-Solomon decoder is a truncated version of the (255, 239) code. The code block size is 204 for DVB and 146 for DSS. The decoder provides a count of the number of uncorrectable blocks as well as the number of bit errors corrected. The latter gives an indication of the bit error rate at the output of the Viterbi decoder. In DVB mode, spectrum de-scrambling is performed compatible with the DVB specification. The final output is a parallel or serial transport data stream; packet sync; data clock; and a block error signal. The data clock may be inverted under software control.

2.0 Electrical Characteristics

2.1 Recommended Operating Condition

Parameter	Symbol	Min.	Typ.	Max.	Units
Core power supply voltage	CVdd	1.71	1.8	1.89	V
Periphery power supply voltage	Vdd	3.13	3.3	3.47	V
Input clock frequency (note [1])	Fxt1	3.99		16.01	MHz
Crystal oscillator frequency	Fxt2	9.99		16.01	MHz
CLK1 clock frequency [2] (with 10 MHz or above)	Fclk1			400	kHz
Ambient operating temperature		0		70	°C

1. When not using a crystal, $\overline{XTI}$ may be driven from an external source over the frequency range shown.
2. The maximum serial clock speed on the primary 2-wire bus is related to the input clock frequency and is limited to 100 kHz with a 4.0 MHz clock.

2.2 Absolute Maximum Ratings

Maximum Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Power supply	Vdd	-0.3	+4.5	V
Power supply	CVdd	-0.3	2.3	V
Voltage on input pins (5 V rated)	Vi	-0.3	6.5	V
Voltage on input pins (3.3 V rated)	Vi	-0.3	Vdd + 0.5	V
Voltage on input pins (1.8 V rated, i.e. $\overline{XTI}$)	Vi	-0.3	CVdd + 0.5	V
Voltage on output pins (5 V rated)	Vo	-0.3	5.5	V
Voltage on output pins (3.3 V rated)	Vo	-0.3	Vdd + 0.5	V
Voltage on output pins (1.8 V rated, i.e., XTO)	Vo	-0.3	CVdd + 0.5	V
Storage temperature	Tstg	-55	150	°C
Operating ambient temperature	Top	0	70	°C
Junction temperature	Tj		125	°C
ESD protection (human body model)		4		kV

Note 1: Stresses exceeding these listed under 'Absolute Ratings' may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

2.3 Primary 2-Wire Bus Timing

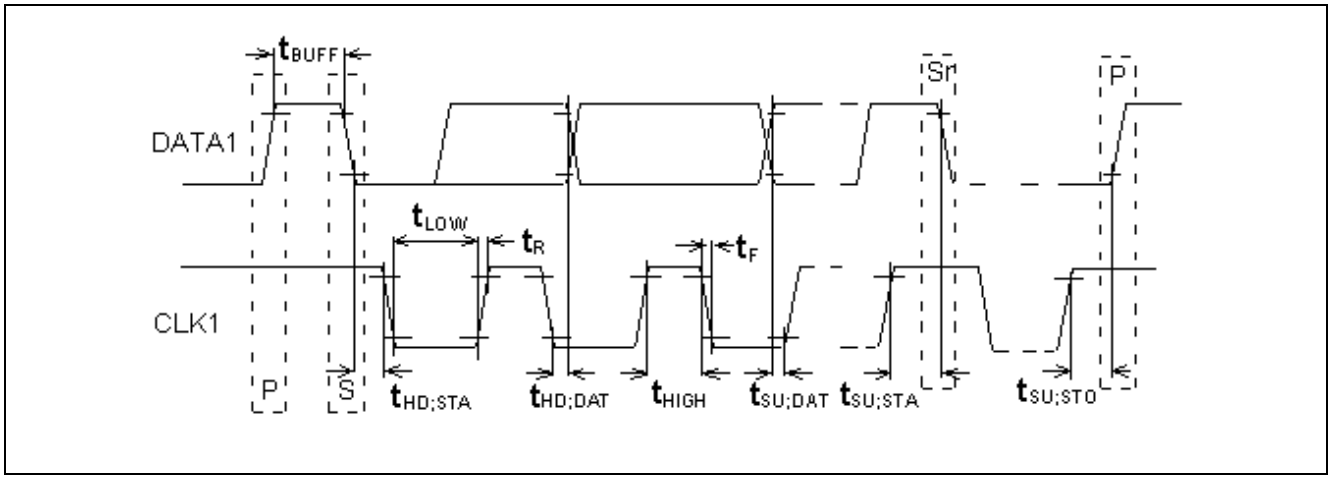


Figure 4 - Primary 2-Wire Bus Timing

Where: S = Start
Sr = Restart, i.e. Start without stopping first.
P = Stop.

Parameter: Primary 2-wire bus only	Symbol	Value		Unit
		Min.	Max.	
CLK1 clock frequency (for $\overline{XTI}$ ≥10 MHz)	fCLK	0	400	kHz
Bus free time between a STOP and START condition.	to	1300		ns
Hold time (repeated) START condition.	tHD;STA	600		ns
LOW period of CLK1 clock.	tLOW	1300		ns
HIGH period of CLK1 clock.	tHIGH	600		ns
Set-up time for a repeated START condition.	tSU;STA	600		ns
Data hold time (when input).	tHD;DAT	0		ns
Data set-up time	tSU;DAT	100		ns
Rise time of both CLK1 and DATA1 signals.	tR	20+0.1Cb[1]	Note[2]	ns
Fall time of both CLK1 and DATA1 signals, (100pF to ground)	tF	20+0.1Cb[1]	300	ns
Set-up time for a STOP condition.	tSU;STO	600		ns

Table 1 - Primary 2-wire Bus Timing

1. Cb = the total capacitance on either clock or data line in pF.
2. The rise time depends on the external bus pull up resistor and bus capacitance.

2.4 Crystal Specification

Parallel resonant fundamental frequency (preferred) 9.99 to 16.00 MHz.

Tolerance over operating temperature range ±25 ppm.

Tolerance overall ±50 ppm.

Nominal load capacitance 30 pF.

Equivalent series resistance <75 Ω

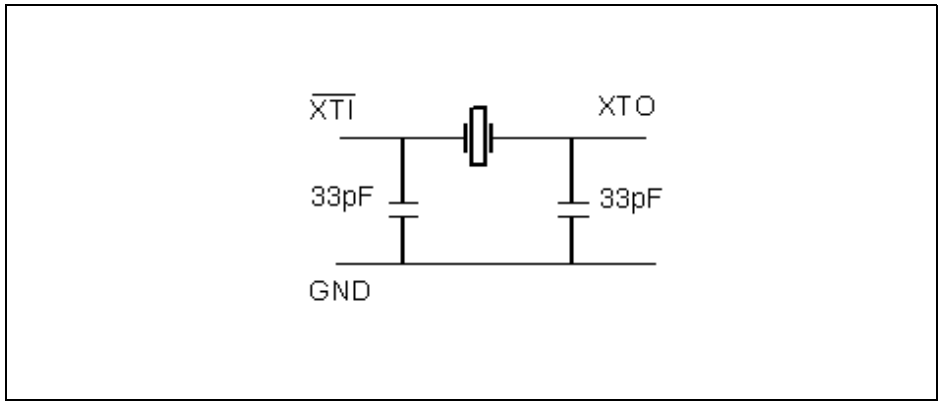


Figure 5 - Crystal Oscillator Circuit

Note: The crystal frequency should be chosen to ensure that the system clock would marginally exceed the maximum symbol rate required, e.g. 10.111 MHz with a multiplier of x9 will give a 91 MHz system clock to guarantee 45 MSps operation.

2.5 Electrical Characteristics

DC Electrical Characteristics

Parameter	Conditions/Pin	Symbol	Min.	Typ.	Max.	Unit
Core voltage		CVdd	1.71	1.8	1.89	V
Peripheral voltage		Vdd	3.13	3.3	3.47	V
Core current	45 MSps CR 7/8 91 MHz system clock	CIdd		160	216	mA
Peripheral current		Idd		10	11.25	mA
Total power (91 MHz system clock)		Ptot1		320	450	mW
Total power (stand-by)	See Note 1	Ptot2		2.2	3.3	mW
Total power (sleep)	Pin 9 = logic ‘1’. See Note 1	Ptot3		0.35	0.525	mW
Output low level	2, 6 or 12 mA per output (see section 2.6, ZL10312 Pinout Description)	Vol			0.4	V
Output high level	2, 6 or 12 mA per output	Voh	2.4			V
Output leakage	Tri-state when off or open-drain when high				±1	µA
Output capacitance	All outputs except XTO, CLK1 & open-drain types. Excludes packaging contribution (~0.35 pF)			2.7		pF
	Open-drain outputs. Excludes packaging contribution (~0.35 pF)			3.3		pF
Input low level		Vil			0.8	V
Input high level		Vih	2.0			V
Input leakage	Vin = 0 or Vdd				±1	µA
Input capacitance	Excludes packaging contribution (~0.35 pF)			1.5		pF

Note 1: To minimize the power comsumption the MPEG outputs should be tristated and the ADC turned off.

AC Electrical Characteristics

Parameter	Conditions/Pin	Min.	Typ.	Max.	Unit
ADC Full-scale input single range (single-ended or differential)	Differential source is recommended		0.5	1.0	Vpp
ADC analog input resistance	Per input pin	10			kΩ
ADC input common mode voltage level		0.7		1.7	V
ADC input impedance	Typically 12 K in parallel with 2 pF				

2.6 ZL10312 Pinout Description

Pin Description Table

Pin	Name	Description	I/O	Note	V	mA
1	$\overline{\text{Reset}}$	Active low reset input	I	CMOS[1]	5	
2	DiSEqC[2]	DiSEqC input for level 2 control. Also usable as GPP2 (general purpose port pin) for other purposes.	I/O	Open drain[1]	5	6
3	DiSEqC[1]	Horizontal/vertical LNB control (acts as input only in production test modes)	I/O	CMOS	3.3	2
4	DiSEqC[0]	22 kHz output to LNB (acts as input only in production test modes)	I/O	CMOS	3.3	2
9	Sleep	Stops oscillator and sets minimum power levels to entire device (except ADCs - register controlled power-down)	I	CMOS	3.3	
10	CLK1	Primary 2-wire serial bus clock	I	CMOS[1]	5	
11	DATA1	Primary 2-wire serial bus data	I/O	Open drain[1]	5	6
14	DATA2	Secondary 2-wire bus data to tuner front end. Also usable as GPP1 (general purpose port pin) for other purposes.	I/O	Open drain[1]	5	6
15	CLK2	Secondary 2-wire bus clock to tuner front end. Also usable as GPP0 (general purpose port pin) for other purposes.	I/O	Open drain[1]	5	6
16	OscMode	Controls oscillator mode to suit crystal or external signal	I	CMOS	3.3	
19	$\overline{\text{XTI}}$	Crystal input or external reference clock input	I	CMOS	1.8	
20	XTO	Crystal output, includes internal feedback resistor to $\overline{\text{XTI}}$	I/O	CMOS	1.8	
24	Iin	I channel input	I	analog		
25	$\overline{\text{Iin}}$	I channel negative input	I	analog		
29	$\overline{\text{Qin}}$	Q channel negative input	I	analog		
30	Qin	Q channel input	I	analog		
35,36,37 38	ADDR[1:4]	Primary 2-wire bus address defining pins	I	CMOS	3.3	
41	AGC	AGC sigma-delta output (acts as input only in production test modes)	I/O	Open drain[1]	5	6
42	Test	For normal operation, this pin must be held at 0V.	I	CMOS	3.3	
43	$\overline{\text{IRQ}}$	Active low interrupt output. Reading all active interrupt registers resets this pin (acts as input only in production test modes)	I/O	Open drain[1]	5	6
46	MOSTRT	MPEG output start signal. High during the first byte of a packet.	O	CMOS Tri-state	3.3	2

Pin Description Table (continued)

Pin	Name	Description	I/O	Note	V	mA
47	MOVAL	MPEG data output valid. High during the MOCLK cycles when valid data bytes are being output.	O	CMOS Tri-state	3.3	2
48,49,52, 53,56, 57,60,61	MDO[0:7]	MPEG transport packet data output bus. Can be tri-stated under control of a register bit.	O	CMOS Tri-state	3.3	2
62	MOCLK	MPEG clock output at the data byte rate.	O	CMOS Tri-state	3.3	12
63	$\overline{\text{BKERR}}$	Active low uncorrectable block indicator or no-signal indicator. Mode selected by ERR_IND bit (#7) of the QPSK_DIAG_CTL register (add. 0x67). Can also be inverted.	O	CMOS Tri-state	3.3	2
64	STATUS	Status output. Register defined function including audio frequency proportional to BER (acts as input only in production test modes)	I/O	CMOS	3.3	2
5, 39, 55	Vdd	Peripheral supply pins. All pins **must** be connected.			3.3	
27	Vdd	Peripheral supply pin used for the ADC.			3.3	
7, 12, 44, 50, 59	CVdd	Core supply pins. All pins **must** be connected.			1.8	
17, 22, 32, 34	CVdd	PLL/ADC supply pins. All pins **must** be connected.			1.8	
6, 8, 13, 40, 45 51, 54, 58	Gnd	Ground supply pins. All pins **must** be connected.			0	
18, 21, 23 26, 28, 31, 33	Gnd	PLL/ADC ground supply pins. All pins **must** be connected.			0	

Note 1: 5 V tolerant pins with thresholds related to 3.3 V.

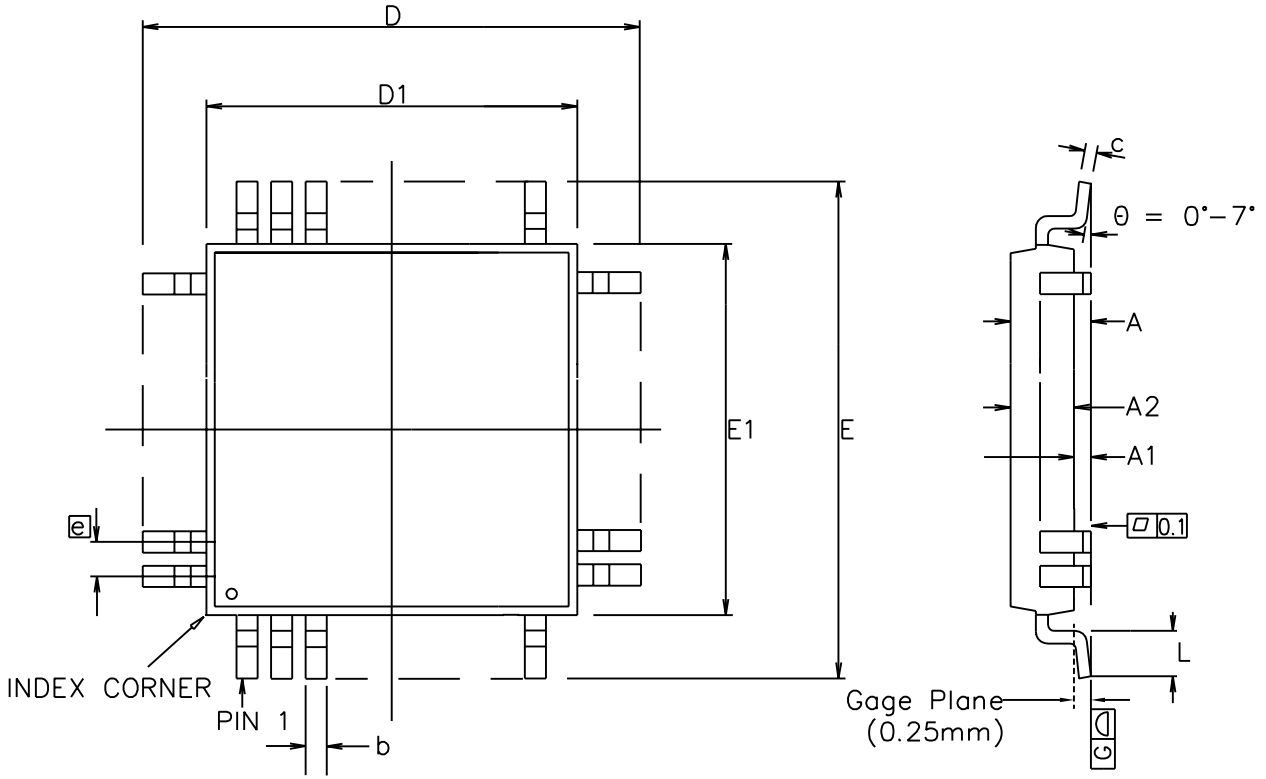
2.7 Alphabetical Listing of Pin-Out

Name	No.	Name	No.	Name	No.	Name	No.
Addr[1]	35	CVdd	59	Gnd	40	MOCLK	62
Addr[2]	36	DATA1	11	Gnd	45	MOSTRT	46
Addr[3]	37	DATA2	14	Gnd	51	MOVAL	47
Addr[4]	38	DiSEqC[0]	4	Gnd	54	OscMode	16
AGC	41	DiSEqC[1]	3	Gnd	58	Qin	29
BKERR	63	DiSEqC[2]	2	Iin	24	Qin	30
CLK1	10	Gnd	6	Iin	25	Reset	1
CLK2	15	Gnd	8	IRQ	43	Sleep	9
CVdd	7	Gnd	13	MDO[0]	48	Status	64
CVdd	12	Gnd	18	MDO[1]	49	Test	42
CVdd	17	Gnd	21	MDO[2]	52	Vdd	5
CVdd	22	Gnd	23	MDO[3]	53	Vdd	27
CVdd	32	Gnd	26	MDO[4]	56	Vdd	39
CVdd	34	Gnd	28	MDO[5]	57	Vdd	55
CVdd	44	Gnd	31	MDO[6]	60	XTI	19
CVdd	50	Gnd	33	MDO[7]	61	XTO	20

3.0 Trademarks

DiSEqC™ is a trademark of EUTELSAT.

ENERGY STAR® is a registered trademark of the United States Environmental Protection Agency (EPA).



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	– – –	1.60		– – –	0.063
A1	0.05	0.15		0.002	0.006
A2	1.35	1.45		0.053	0.057
D	9.00 BSC			0.354 BSC	
D1	7.00 BSC			0.276 BSC	
E	9.00 BSC			0.354 BSC	
E1	7.00 BSC			0.276 BSC	
L	0.45	0.75		0.018	0.030
e	0.40 BSC			0.016 BSC	
b	0.13	0.23		0.005	0.009
c	0.09	0.20		0.004	0.008
	Pin features				
N	64				
ND	16				
NE	16				
NOTE	SQUARE				

Conforms to JEDEC MS-026 BBD Iss. C

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.08 mm max.

This drawing supersedes 418/ED/51210/031 (Swindon)

ISSUE	1	2	3	
ACN	201370	207115	212445	
DATE	29Oct96	9Jul99	26Mar02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

GP / B

Package Code QC

Package Outline for 64 lead LQFP (7 x 7 x 1.4mm) 2mm Footprint

GPD00250

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