ZENIC
CUSTOM IC DESIGN

PROGRAMMABLE UNIVERSAL COUNTER

Description

ZENIC ZEN2041F is a programmable universal counter LSI.

THE ZEN2041F counts phase-shifted signals and up/down pulse signals, generated from rotary encoders or linear scales.

Since the counter response speed is as high as 20MHz(MAX),the ZEN2041F is used in a variety of high speed services including digital servo control and precision measurement.

THE ZEN2041F is provided with a function which monitors the input signals and detects any abnormal input accompanied with noise or other disturbances, so that the reliability of counted values are secured.

1. Features

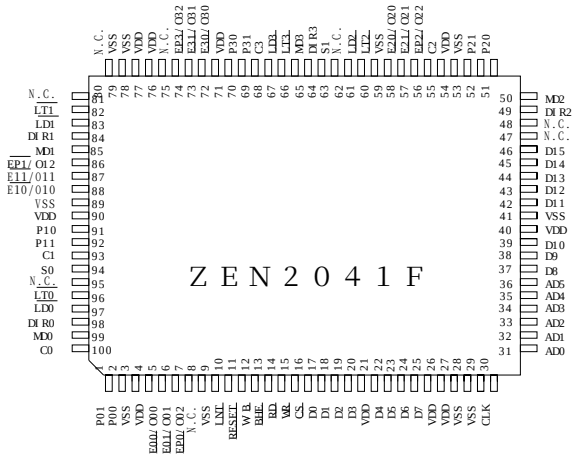
Selectable count resolution and channels.
16bit Λ4ch. or 32bit Λ2ch. or
16bit Λ2ch. + 32bit Λ1ch.
Count response speed:
20Mcps.(MAX.) (CLK f_0 = 20MHz at 50% duty)
Input frequency of count pulse.
Phase-shifted signal input:
A/B phase input DC~ 5MHz.
(less than f_0 Λ1/4)
Up/down pulse signal input:
Up/down input DC~ 10MHz
(less than f_0 Λ1/2)
CLK frequency DC~ 20MHz.
(MAX.:duty ratio 50%)
Direction recognition for up/down counting
Abnormal input detection circuit.
Preload register for the up/down counter.
Latch register for the up/down counter.
Reference value - count value coincidence detection function.
On-chip status register.
Counter operation mode.
Edge evaluation selection : 1/2/4 .
(only for phase-shifted signal input)
Count direction selection.
Counter clear control:synchronous/ asynchronous clear.
Selectable 16/8 bit data bus.
Low power CMOS technology.
TTL compatible.
Single 5V power supply.
100 pin QFP.

Typical Applications

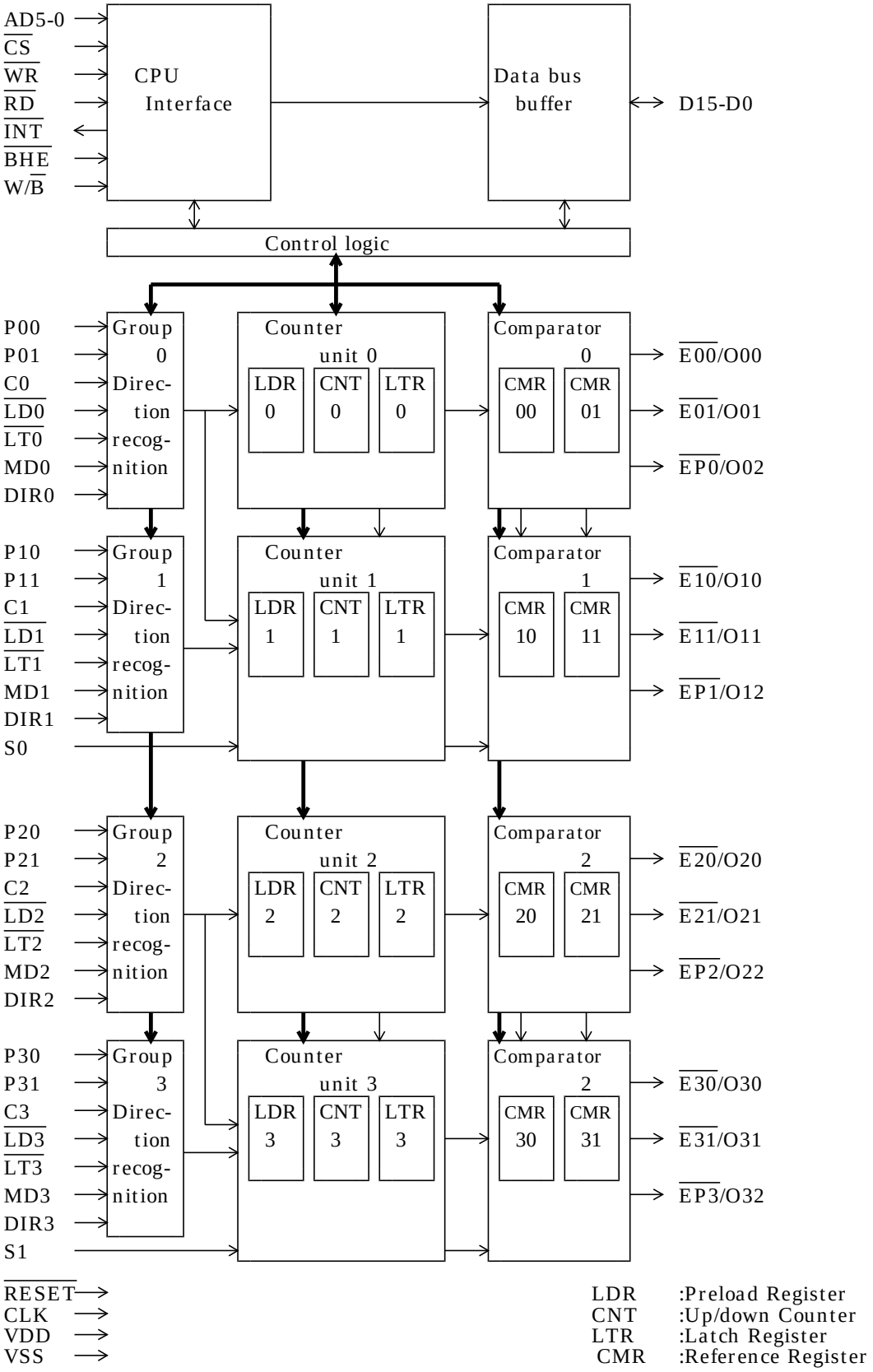
For Multi channel
NC machine tools
Precision positioners
Robot arm controllers
Speed controllers for rotating machines
Electronic gauges
Frequency counters

Pin configuration

(Top View)



2. Block diagram (Figure.2)



3. Block Description (refer to Figure.2)

1) CPU Interface

It is interface to write data into register or read data from register.

It outputs the $\overline{INT}$ signal by interrupt from direction recognition logic and comparator.

Refer to [5.Basic Operations] and [6.Internal Register Mapping].

2) Control logic

It operates to write data into register or read data from register.

It transmits interrupt signal to CPU interface from direction recognition logic and comparator.

3) Data Bus Buffer

It is 16 or 8bit bidirectional, and interface between CPU and ZEN2041F.

4) Direction Recognition

It outputs the UP, DOWN, Data Load and Data Latch signal to the counter upon the external signal, mode register, command register.

If interrupt enable, it indicates CPU interface to make $\overline{INT}$="L".

The input signals can be monitored by the monitor register, therefore the input signals(*) not inputed to the counter can be used for universal inputs.

5) Counter unit

It is composed of the load register, up/down counter and command register.

It operates by the UP, DOWN, CLEAR, DATA LOAD, DATA LATCH, and Carry, Borrow.

The counter connection S0 and S1 determine the direction recognition group and the pre-stage counter.

S0	Connection	Counter unit	Direction Recognition	Pre-stage Counter unit
0	Independent	0	Group 0	-
		1	1	-
1	Cascade	0	0	-
		1	0	0

S1	Connection	Counter unit	Direction Recognition	Pre-stage Counter unit
0	Independent	2	Group 2	-
		3	3	-
1	Cascade	2	2	-
		3	2	2

Cascade connection (32bit counter)

Counter unit 0 and 2 are lower word(16bit).

And, counter unit 1 and 3 are upper word(16bit).

6) Comparator

It is composed of two reference registers.

It compares the counter value with the reference register. If the coincidence is detected, comparator outputs the status, the interrupt, the coincidence and the window, according to the setting condition.

Refer to [9.Coincidence Detection Function].

*)Input signals to the group 1 and 3 when cascade connected.

4. Pin Definitions and Functions

Table.1

Pin	Symbol	I/O	Functions
36	AD5		Address0-5
35	AD4		These are used for selection internal register with W/$\overline{B}$ and $\overline{BHE}$.
34	AD3	I	Refer to [5.Basic Operations] and [6.Internal Register Mapping].
33	AD2		
32	AD1		
31	AD0		
16	$\overline{CS}$	I	CHIP SELECT
14	$\overline{RD}$	I	READ
15	$\overline{WR}$	I	WRITE
10	$\overline{INT}$	O	INERRUPT REQUEST
12	W/$\overline{B}$	I	WORD/BYTE : Word transfer is "H". Byte transfer is "L".
13	$\overline{BHE}$	I	BUS HIGH ENABLE
46	D15		DATA BUS
45	D14		
44	D13		Enable bits are selected by $\overline{BHE}$ and AD0.
43	D12		Refer to [5.Basic Operations.].
42	D11		
39	D10		
38	D9		
37	D8	I/O	
25	D7		
24	D6		
23	D5		
22	D4		
20	D3		
19	D2		
18	D1		
17	D0		
11	$\overline{RESET}$	I	RESET:initialize internal registers.
30	CLK	I	CLOCK:is used for synchronizing internal signals and counting.
2	P00		PULSE INPUTS 00-31
1	P01		Refer to [8. Counter Operation and Timing.].
91	P10		
92	P11	I	
51	P20		
52	P21		
70	P30		
69	P31		
100	C0		CLEAR0-3 : clear each counter value.
93	C1	I	About clear conditions, refer to [7.5) Mode Register.].
55	C2		
68	C3		
97	$\overline{LD0}$		DATA LOAD : After the falling edge is detected, the value of load
83	$\overline{LD1}$	I	register is stored to each counter.
61	$\overline{LD2}$		
67	$\overline{LD3}$		
96	$\overline{LT0}$		DATA LATCH : After the falling edge is detected, the value of counter
82	$\overline{LT1}$	I	is stored to each latch register.
60	$\overline{LT2}$		
66	$\overline{LT3}$		

Pin	Symbol	I/O	Functions
99 85 50 65	MD0 MD1 MD2 MD3	I	MODE SELECTION : O : Phase-shifted pulse 1 : Up/Down pulse
98 84 49 64	DIR0 DIR1 DIR2 DIR3	I	COUNTING DIRECTION Refer to [8. Counting Operation and Timing.].
94 63	S0 S1	I	COUNTER CONNECTION Refer to [3.5) Counter unit].
5 6 58 57 88 87 72 73	$\overline{E00}$/O00 $\overline{E01}$/O01 $\overline{E20}$/O20 $\overline{E21}$/O21 $\overline{E10}$/O10 $\overline{E11}$/O11 $\overline{E30}$/O30 $\overline{E31}$/O31	O	COINCIDENCE DETECTION 00-31 / UNIVERSAL OUTPUT 00-31 Refer to [9. Coincidence Detection Function.].
7 86 56 74	$\overline{EP0}$/O02 $\overline{EP1}$/O12 $\overline{EP2}$/O22 $\overline{EP3}$/O32	O	WINDOW OUTPUT 0-3 / UNIVERSAL OUTPUT 02-32 Refer to [9. Coincidence Detection Function.].
4 21 26 27 40 54 71 76 77 90	VDD	-	Supply voltage +5V
3 9 28 29 41 53 59 78 79 89	VSS	-	Ground 0V

5. Basic Operation

Table.2

$\overline{CS}$	W/$\overline{B}$	$\overline{BHE}$	AD0	$\overline{RD}$	$\overline{WR}$	D15-D8	D7-D0	Basic Operation
1	*		*	*	*	High-impedance	High-impedance	Disable
0	1	1	1	*	*			
0	1	0	0	1	0	Input	Input	Write word data
0	1	0	0	0	1	Output	Output	Read word data
0	1	1	0	1	0	High-impedance	Input	Write lower byte data
0	1	1	0	0	1	High-impedance	Output	Read lower byte data
0	1	0	1	1	0	Input	High-impedance	Write upper byte data
0	1	0	1	0	1	Output	High-impedance	Read upper byte data
0	0	1	0	1	0	High-impedance	Input	Write lower byte data
0	0	1	0	0	1	High-impedance	Output	Read lower byte data
0	0	1	1	1	0	High-impedance	Input	Write upper byte data
0	0	1	1	0	1	High-impedance	Output	Read upper byte data
0	0	0	*	*	*	-	-	Inhibit
0	*	*	*	0	0			

6. Internal Register Mapping

Table.3

$\overline{RD}$	$\overline{WR}$	AD5	AD4	AD3	AD2	AD1	AD0	Selected register and Operation
1	0	0	0	0	0	0	0	Load register 0, Write
1	0	0	0	0	0	1	0	Reference register 00, Write
1	0	0	0	0	1	0	0	Reference register 01, Write
1	0	0	0	0	1	1	0	Mode register 0, Write
1	0	0	0	1	0	0	0	Load register 1, Write
1	0	0	0	1	0	1	0	Reference register 10, Write
1	0	0	0	1	1	0	0	Reference resister 11, Write
1	0	0	0	1	1	1	0	Mode register 1, Write
1	0	0	1	0	0	0	0	Load register 2, Write
1	0	0	1	0	0	1	0	Reference register 20, Write
1	0	0	1	0	1	0	0	Reference register 21, Write
1	0	0	1	0	1	1	0	Mode register 2, Write
1	0	0	1	1	0	0	0	Load register 3, Write
1	0	0	1	1	0	1	0	Reference register 30, Write
1	0	0	1	1	1	0	0	Reference register 31, Write
1	0	0	1	1	1	1	0	Mode register 3, Write
1	0	1	0	0	0	0	0	Command register 0, Write
1	0	1	0	0	0	1	0	Command register 1, Write
1	0	1	0	0	1	0	0	Command register 2, Write
1	0	1	0	0	1	1	0	Command register 3, Write
1	0	1	0	1	0	0	0	Global command register,Write
0	1	0	0	0	0	0	0	Latch register 0, Read
0	1	0	0	0	1	1	0	Monitor register 0, Read
0	1	0	0	1	0	0	0	Latch register 1, Read
0	1	0	0	1	1	1	0	Monitor register 1, Read
0	1	0	1	0	0	0	0	Latch register 2, Read
0	1	0	1	0	1	1	0	Monitor register 2, Read
0	1	0	1	1	0	0	0	Latch register 3, Read
0	1	0	1	1	1	1	0	Monitor register 3, Read
0	1	1	0	0	0	0	0	Status register 0, Read
0	1	1	0	0	0	1	0	Status register 1, Read
0	1	1	0	0	1	0	0	Status register 2, Read
0	1	1	0	0	1	1	0	Status register 3, Read

7. Registers

1) Load register

The value of this register is stored in the up/down counter at the falling edge of $\overline{LDn}$ or executing data load(D9) of the command register.

2) Reference register n0

The lower value of window comparison is stored in it.

3) Reference register n1

The upper value of window comparison is stored in it.

4) Latch register

The value of the up/down counter is stored in this register at the rising edge of $\overline{LTn}$ or executing data latch(D8) of the command register.

These registers

Digit 0(D0) : LSB

Digit 15(D15) : MSB

5) Mode register : Subscript n is 0 to 3.

Table.5

Bit	Symbol	Description
D15	ILDn	Interrupt control($\overline{LDn}$) 0 : inhibit 1 : enable when the D9 of mode register is "1".
D14	ILTn	Interrupt control($\overline{LTn}$) 0 : inhibit 1 : enable when the D8 of mode register is "1".
D13	IAIn	Interrupt control (by an abnormal input) 0 : inhibit 1 : enable
D12	ICn	Interrupt control (by Cn) 0 : inhibit 1 : enable when ZEn1="1"
D11	IEn1	Interrupt control (by coincidence detection) 0 : inhibit 1 : enable when $\overline{En1}$="L"
D10	IEn0	Interrupt control (by coincidence detection) 0 : inhibit 1 : enable when $\overline{En0}$="L"
D9	ELDn	Enable $\overline{LDn}$ 0 : disable 1 : enable
D8	ELTn	Enable $\overline{LTn}$ 0 : disable 1 : enable
D7	OCn2	Output control 2 0 : $\overline{EPn}$/On2 = universal output 1 : = coincidence output
D6	OCn1	Output control 1 0 : $\overline{En1}$/On1 = universal output 1 : = coincidence output

Bit	Symbol	Description
D5	OCn0	Output control 0 0 : $\overline{En0}$/On0 = universal output 1 : = coincidence output
D4	ZMDn	Clear mode 0 : asynchronous clear 1 : synchronous clear for phese-shifted pulse input
D3 D2	ZEn1 ZEn0	Clear count ZEn1 ZEn0 0 0 no operation 0 1 Disable clear 1 0 only 1 time 1 1 every times
D1 D0	Xn1 Xn0	Edge evaluation for phase-shifted pulse input Xn1 Xn0 Edge evaluation 0 0 Single 0 1 Double 1 1 Quad

6) Command register : Subscript n is 0 to 3.

Table.6

Bit	Symbol	Description
D15	RLDn	Reset interrupt by $\overline{LDn}$ 0 : no operation 1 : Reset
D14	RLTn	Reset interrupt by $\overline{LTn}$ 0 : no operation 1 : Reset
D13	RAIn	Reset interrupt by abnormal input 0 : no operation 1 : Reset
D12	RCn	Reset interrupt by Cn 0 : no operation 1 : Reset
D11	REn1	Reset interrupt by coincidence detection 0 : no operation (D11 of mode register) 1 : Reset
D10	REn0	Reset interrupt by coincidence detection 0 : no operation (D10 of mode register) 1 : Reset
D9	LDn	Data $\overline{load}$ When $\overline{LDn}$=1, the value of load register is stored into the up/down counter.
D8	LTn	Data $\overline{latch}$ When $\overline{LTn}$=1, the value of up/down counter is stored into the latch register.
D7	OTn2	Control universal output 2 : when OCn2(D7)=0 (command register) 0 : On2="L" 1 : ="H"
D6	OTn1	Control universal output 1 : when OCn1(D6)=0 (command register) 0 : On1="L" 1 : ="H"

Bit	Symbol	Description
D5	OTn0	Control universal output 0 : when OCn0(D5)=0 (command register) 0 : On0="L" 1 : ="H"
D4	-	0
D3	ZEn1	equal to D3 of mode register
D2	ZEn0	equal to D2 of mode register
D1	-	0
D0	-	0

7) Global command register

Table.7

Bit	Symbol	Description	
D15	LD3	Equal to D9 (command register 3)	
D14	LD2	D9	2
D13	LD1	D9	1
D12	LD0	D9	0
D11	LT3	D8	3
D10	LT2	D8	2
D9	LT1	D8	1
D8	LT0	D8	0
D7-D0		0	

8) Monitor register : monitor all input signals. Subscript n is 0 to 3.

Table.8 : Format of the monitor register n

Bit	Symbol	Description
D15	Pn0M	Monitor Pn0 signal 0 : Pn0="L" 1 : ="H"
D14	Pn1M	Monitor Pn1 signal 0 : Pn1="L" 1 : ="H"
D13	CnM	Monitor Cn signal 0 : Cn="L" 1 : ="H"
D12	LDnM	Monitor $\overline{\text{LDn}}$ signal 0 : LDn="L" 1 : ="H"
D11	LTnM	Monitor $\overline{\text{LTn}}$ signal 0 : LTn="L" 1 : ="H"
D10	MDnM	Monitor MDn signal 0 : MDn="L" 1 : ="H"
D9	DIRnM	Monitor DIRn signal 0 : DIRn="L" 1 : ="H"
D8	SmM	Monitor Sm signal : is enable for the status register 00 and 20. 0 : Sm="L" 1 : ="H"
D7-D0		fixed '0'

9) Status register : Subscript n is 0 to 3.

Table.9

Bit	Symbol	Description
D15	SILDn	Done interrupt by $\overline{LDn}$. Reset by RLDn(D15)=1 of the command register n. 0 : not done 1 : Done
D14	SILTn	Done interrupt by $\overline{LTn}$. Reset by RLTn(D14)=1 of the command register n. 0 : not done 1 : Done
D13	SAIn	Done interrupt by abnormal input. Reset by RAIn(D13)=1 of the command register n. 0 : not done 1 : Done
D12	SCn	Done interrupt by Cn. Reset by ICn(D12)=1 of the command register n. 0 : not done 1 : Done
D11	SEn1	Done interrupt by coincidence detection. Reset by REn1(D11)=1 of the command 0 : not done register n. 1 : Done
D10	SEn0	Done interrupt by coincidence detection. Reset by REn0(D10)=1 of the command 0 : not done register n. 1 : Done
D9	SLDn	Completed loading data 0 : reset after reading out. 1 : is set with completion of storing the load resister value into the counter.
D8	SLTn	Completed latching data 0 : reset after reading out. 1 : is set with completion of storing the counter value into the latch register
D7	EPnM	Monitor $\overline{EPn}$: equal to $\overline{EPn}$
D6	En1M	Monitor $\overline{En1}$: equal to $\overline{En1}$
D5	En0M	Monitor $\overline{En0}$: equal to $\overline{En0}$
D4	-	0
D3 D2 D1 D0	ISR3 ISR2 ISR1 ISR0	Indicate to done interrupt 0 : Not done 1 : Done

8. Counter operation and Timing

These signals are sampled by CLK.
RESET, Pulse input(P00-P31), Clear(C0-C3), Load data($\overline{LD0}$-$\overline{LD3}$), Latch data($\overline{LT0}$-$\overline{LT3}$)

1) Counting operation

Table.10 Counting direction

Phase-shifted pulse (MDn="L")

DIRn	Phase	Counting direction
1	Pn0 phase 90 advance	Count up
	Pn1 phase 90 advance	Count down
0	Pn0 phase 90 advance	Count down
	Pn1 phase 90 advance	Count up

Up/down pulse (MDn="H")

DIRn	Rising edge	Counting direction
1	Pn0	Count up
	Pn1	Count down
0	Pn0	Count down
	Pn1	Count up

2) Count timing (Refer to Figure.3-1)

Phase-shifted pulse
Counting condition is depend on the edge evaluation.

Edge evaluation	Counting condition
single	Change of Pn0 when Pn1="L"
double	Change of Pn0
quad	Change of Pn0 or Pn1

Up/down pulse
When it is sampled the rising edge of pulse input, count up or down depend on DIRn.
Don't change the other input.

3) Abnormal input

Phase-shifted pulse
The definition of abnormal input is the simultaneously changing Pn0 with Pn1.
Causes of abnormal input
* It cannot be sampled because the changing time of input is too short.
* the transition state is abnormal because the noise is sampled.

Up/down pulse
No definition

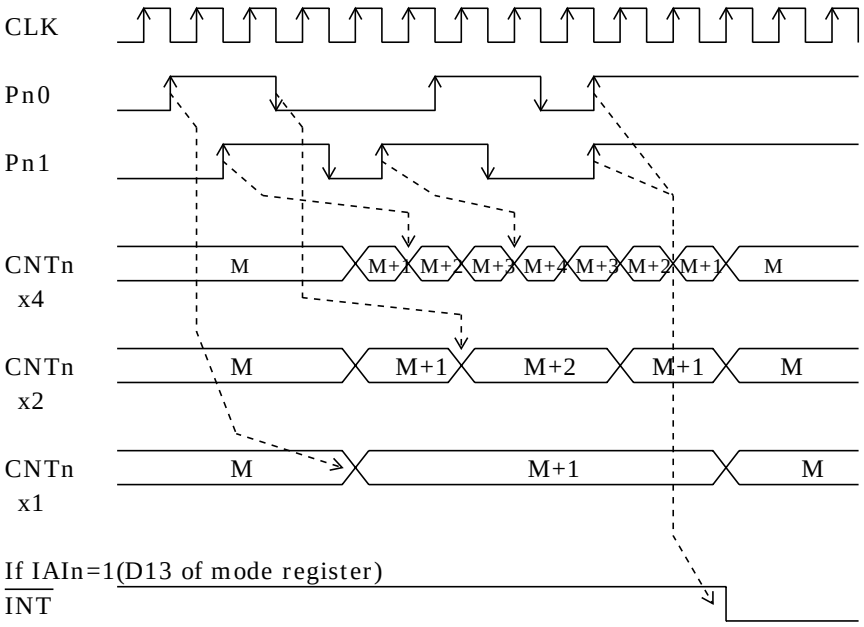
4) Clear operation : Refer to Figure.3-2.

* Asynchronous clear
  After the rising edge of Cn is detected, the counter is cleared.
* Synchronous clear
  After Cn="H",Pn1="L",and change of Pn0 are detected, the counter is cleared.

5) Loading data, Latching data operation : Refer to Figure.3-3.

Figure.3-1 : Counting operation

Phase-shifted pulse input (DIRn="H")



Up/down pulse input (DIRn="H")

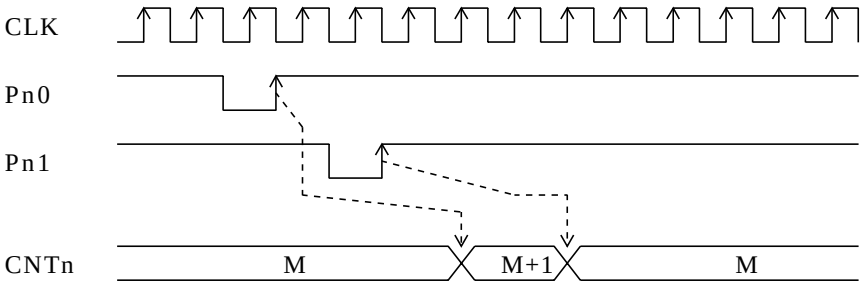
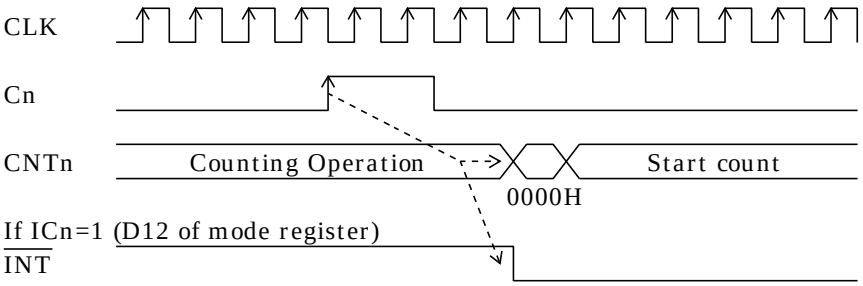


Figure.3-2 : Clearing Operation

* Asynchronous clearing



* Synchronous clearing (only for phase-shifted pulse input)

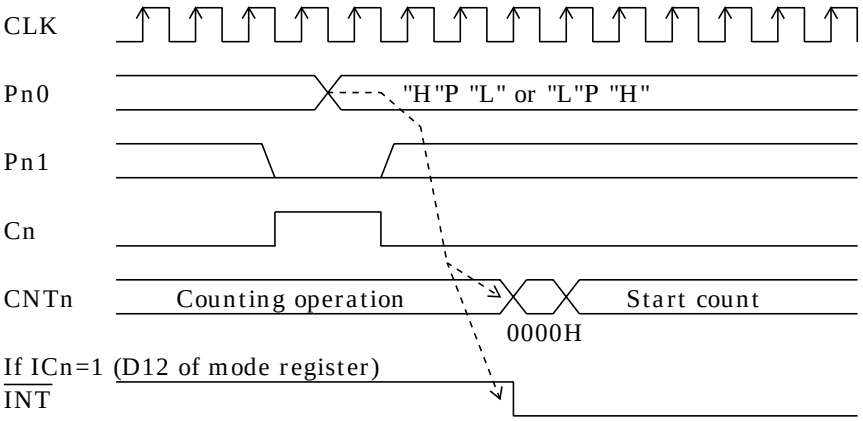
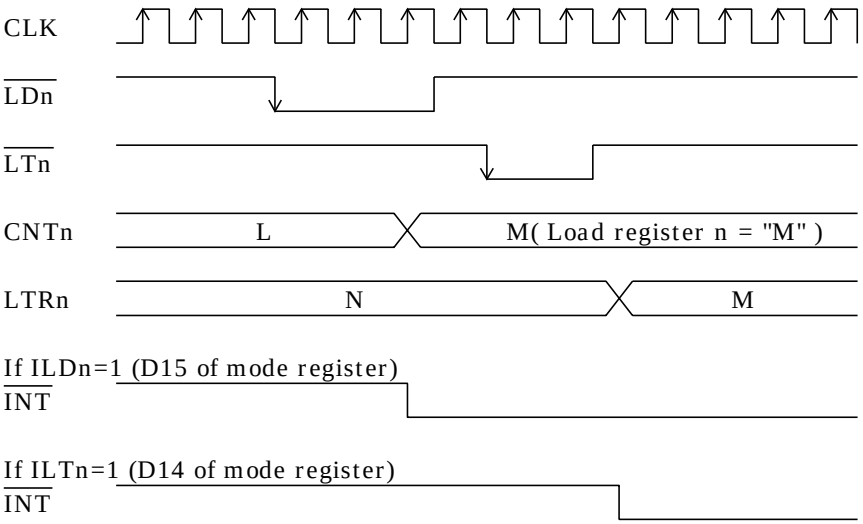


Figure.3-3 : Loading data, Latching data



9. Coincidence Detection

There are two reference registers for every counter. They are used for storing data to window comparison. And it outputs a coincidence signal a reference register with count value.

1) Independent (S0,S1="L")

Table.12

Up/down Counter	Lower value register	Upper value register	Coincidence signal	Window output
CNT0	CMR00		$\overline{E00}$	$\overline{EP0}$
		CMR01	$\overline{E01}$	
CNT1	CMR10		$\overline{E10}$	$\overline{EP1}$
		CMR11	$\overline{E11}$	
CNT2	CMR20		$\overline{E20}$	$\overline{EP2}$
		CMR21	$\overline{E21}$	
CNT3	CMR30		$\overline{E30}$	$\overline{EP3}$
		CMR31	$\overline{E31}$	

Coincidence signal is "L" during count value=reference register.

Window output is "L"
Condition 1 : lower value register < upper value register,
During : lower value register < count value < upper value register
Condition 2 : lower value register = upper value register,
During : count value = lower value register
Condition 3 : lower value register > upper value register,
During : count value = lower value register or upper value register

2) Cascade connect (S0,S1="H")

Table.13

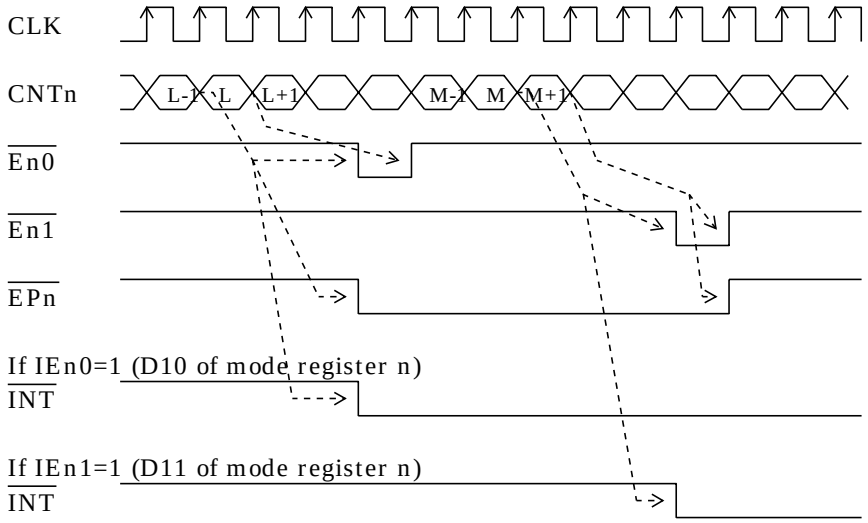
counter		lower value register		upper value register		coincidence	window
lower word	upper word	lower word	upper word	lower word	upper word	signal	output
CNT0	CNT1	CMR00	CMR10			$\overline{E10}$	$\overline{EP1}$
				CMR01	CMR11	$\overline{E11}$	
CNT2	CNT3	CMR20	CMR30			$\overline{E30}$	$\overline{EP3}$
				CMR21	CMR31	$\overline{E31}$	

count value = (counter upper word)*10000(H) + (counter lower word)
lower value register = (upper word register)*10000(H) + (lower word register)
upper value register = (upper word register)*10000(H) + (lower word register)

Note
If enable interrupt, while counter value equal to reference register, interrupt output is "Low".

Example of interrupt process.
1, unable interrupt or modify reference register.
2, reset interrupt.
3, interrupt process.
4, exit interrupt routine.
5, if counter value unequal to reference register, enable interrupt.

Figure.4 : Coincidence detection and window output
When a reference register n0 = "L" and a reference register n1 = "M"



10. Electrical specification

1) Absolute maximum rating

Rating	Symbol	Min.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}-0.5	V_{SS}+7.0	V
Input voltage	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output voltage	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Input current	I_I	-20	+20	mA
Storage temperature	T_{STG}	-50	+125	C

2) Recommended operating conditions

V_{SS}=0V

Rating	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	4.50	5.00	5.50	V
Operating temperature	T_{OP}	-40	25	+70	C

3) DC characteristics (at the recommended operating conditions)

Rating		Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage	"H" level	V_{IH}	TTL input	2.2	-	-	V
	"L"	V_{IL}	TTL input	-	-	0.8	V
Output voltage	"H"	V_{OH}	I_{OH}=-4mA	V_{DD}-1.0	-	-	V
	"L"	V_{OL}	I_{OL}=4mA	-	-	V_{SS}+0.4	V
Input leakage current		I_L	V_I=V_{DD}/V_{SS}	-10	-	+10	µA
Standby current		I_{DDS}	V_{IH}= V_{DD},V_{IL}= V_{SS}			100	µA

4) AC characteristics-1 (at the recommended operating conditions)

NO.	Symbol	Rating	Min.	Max.	Unit
1	Φ_R	Rising up time of CLK		5	ns
2	Φ_F	Falling down time of CLK		5	ns

5) AC characteristics-2 (n=0~ 3, at the recommended operating conditions)

NO.	Symbol	Rating	Min.	Max.	Unit
1	Φ_{CY}	CLK Cycle time	50		ns
2	Φ_{H}	CLK Pulse width("High")	25		ns
3	Φ_{L}	CLK Pulse width("Low")	25		ns
4	T_{WAS}	Setting up time of address for $\overline{WR}$ Π	5		ns
5	T_{WAH}	Holding time of address for $\overline{WR}$–	5		ns
6	T_{WRL}	$\overline{WR}$ pulse width ("Low")	100		ns
7	T_{WRH}	Recovering time after rising up $\overline{WR}$(note.3)	$5\Phi_{CY}$		ns
8	T_{DS}	Setting up time of input data for $\overline{WR}$–	40		ns
9	T_{DH}	Holding time of input data for $\overline{WR}$–	0		ns
10	T_{RAS}	Setting up time of address for $\overline{RD}$ Π	5		ns
11	T_{RAH}	Holding time of address for $\overline{RD}$–	5		ns
12	T_{RDL}	$\overline{RD}$ pulse width ("Low")	100		ns
13	T_{RDH}	Recovering time after rising up $\overline{RD}$(note.3)	$4\Phi_{CY}$		ns
14	T_{ZV}	Deley time from $\overline{RD}$ Πto fixed data		70	ns
15	T_{DZ}	Deley time from $\overline{RD}$– to float output		70	ns
16	T_{10}	Setting up time of Pn0 for Pn1	Φ_{CY}+ 25		ns
17	T_{01}	Setting up time of Pn1 for Pn0	Φ_{CY}+ 25		ns
18	T_{S10}	Setting up time of Pn0 for Pn1–	Φ_{CY}+ 25		ns
19	T_{H10}	Holding time of Pn0 for Pn1–	Φ_{CY}+ 25		ns
20	T_{S01}	Setting up time of Pn1 for Pn0–	Φ_{CY}+ 25		ns
21	T_{H01}	Holding time of Pn1 for Pn0–	Φ_{CY}+ 25		ns
22	T_{PW}	Pulse width of input (Pn0,Pn1)	Φ_{CY}+ 25		ns
23	T_{CW}	Pulse width of Cn	Φ_{CY}+ 25		ns
24	T_{LW}	Pulse width of $\overline{LDn}$,$\overline{LTn}$	Φ_{CY}+ 25		ns
25	T_{RL}	Pulse width of $\overline{RESET}$	$5\Phi_{CY}$		ns
26	T_{RH}	Recovering time after rising up $\overline{RESET}$	$5\Phi_{CY}$		ns
27	T_{I}	Delay time from CLK– to $\overline{INT}$ output		65	ns
28	T_{E}	Delay time from CLK– to coincidence output		40	ns

note.3) Inhibit time to read or write.

Measuring condition for AC characteristics-2

Rating	Symbol	Standard value	Unit
Input driving level	V_{IH}	2.4 (3.0)	V
	V_{IL}	0.45(0.4)	V
Test point of timing	V_{OH}	2.0	V
(input,output)	V_{OL}	0.8	V
Loading capacity	C_{L}	50	pF
Loading current	I_{OH}	-4	mA
	I_{OL}	4	mA

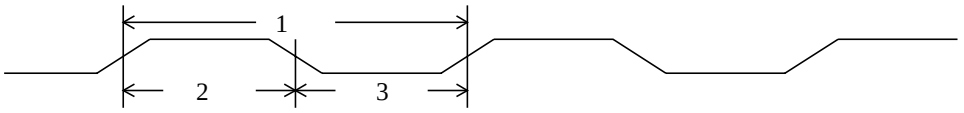
The value in parentheses is for CLK input.

Operation current

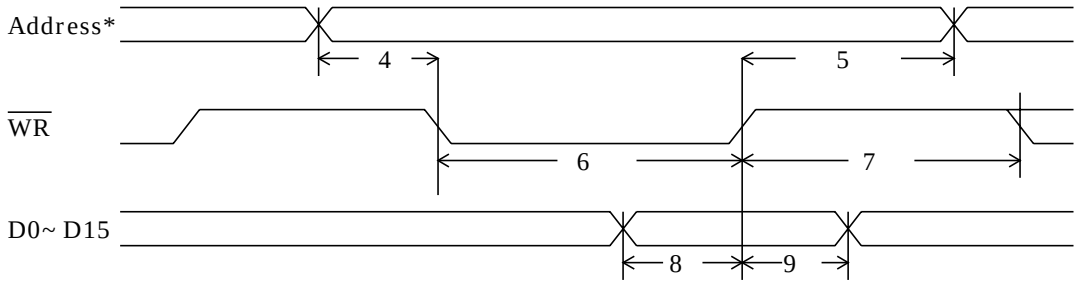
Rating	Symbol	Measuring condition	Max	Unit
Operation current	I_{DDO}	Output is open CLK = 20MHz	90	mA

Timing diagram

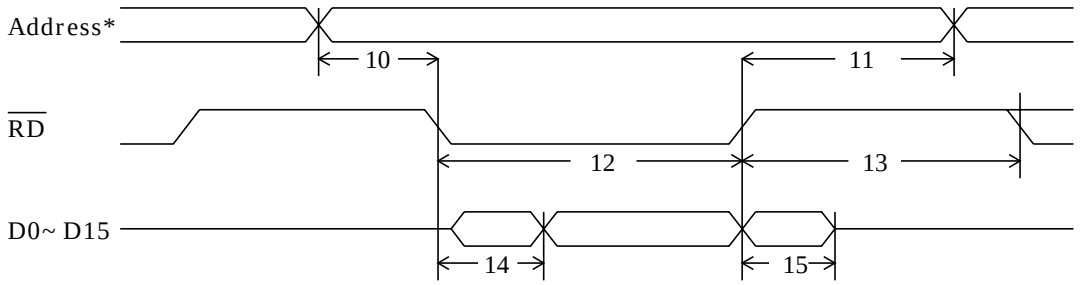
Clock



Write cycle (W/$\overline{B}$="H" or "L")



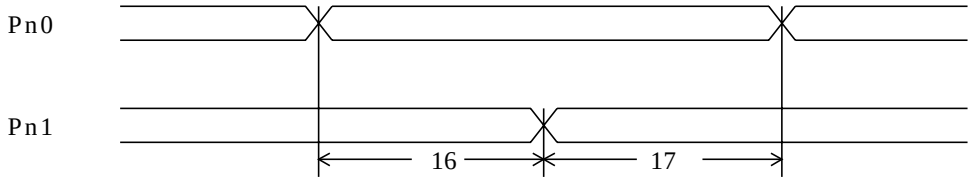
Read cycle (W/$\overline{B}$="H" or "L")



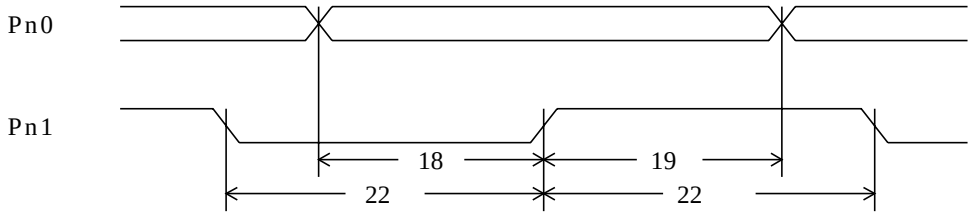
*Address : $\overline{CS}$, AD5~ AD0, $\overline{BHE}$

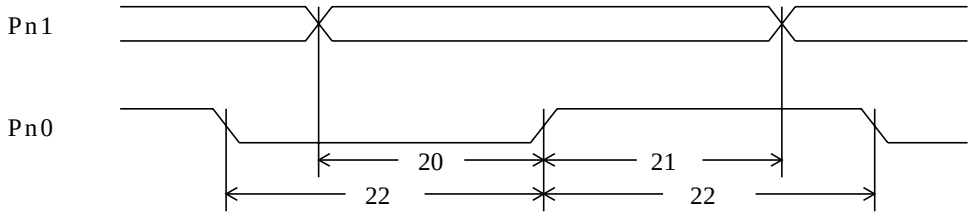
Input timing

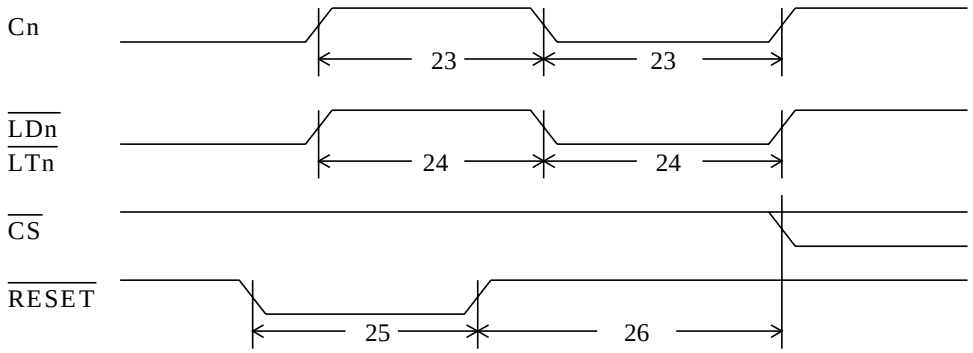
Phase-shifted pulse input



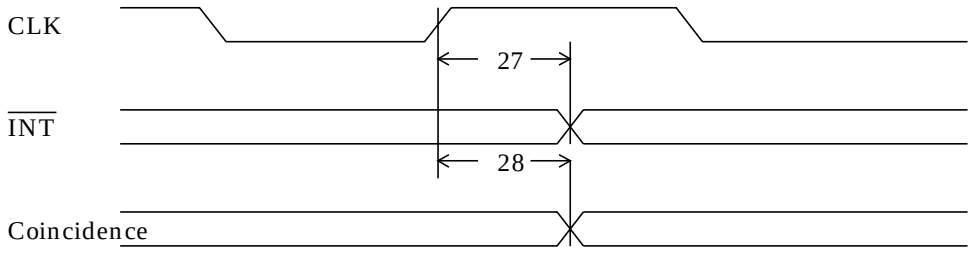
Up/down pulse input





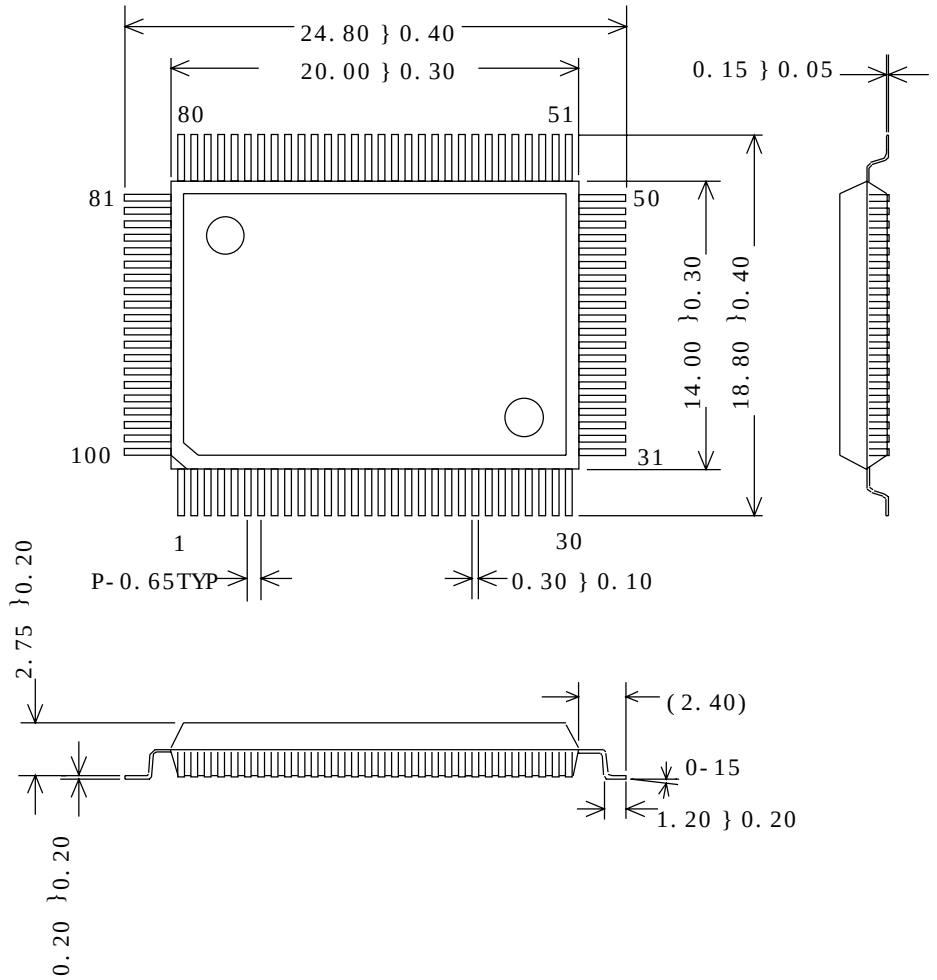


Output timing



*Coincidence output : $\overline{E00}$/O00,$\overline{E01}$/O01,$\overline{E10}$/O10,$\overline{E11}$/O11
$\overline{E20}$/O20,$\overline{E21}$/O21,$\overline{E30}$/O30,$\overline{E31}$/O31
$\overline{EP0}$/O02,$\overline{EP1}$/O12,$\overline{EP2}$/O22,$\overline{EP3}$/O32

11. Package outlines (Dimensions in mm)



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