PRELIMINARY
CUSTOMER PROCUREMENT SPECIFICATION

Z89462

16-BIT, FIXED-POINT DIGITAL SIGNAL PROCESSOR

FEATURES

Part	Prog. RAM (K Words)	Prog./Data (K Words)	Data RAM (Words)	Speed (MHz)
Z89462	1	64	512	20, 40

- 100-Pin QFP and 124-Pin PGA Packages
- 0°C to +70°C Temperature Range
- 3.3- to 5.0-Volt Operating Range
  40 MHz Operation @ 5.0V
  20 MHz Operation @ 3.3V
- Six RAM Pointers for 4K-Word RAM Banks
- Three Maskable Vectored Interrupts, Edge or Level Trigger Selectable
- Enhanced Instruction Set
- Single-Cycle Instruction Execution
- Four-Stage Pipeline

On-Board Peripherals

- Dual 8/16-Bit CODEC Interface
- Wait-State Generator
- Two 16-Bit Timer/Counters
- Dynamic Program Bus Sizing

GENERAL DESCRIPTION

The Z89462 is a high-performance Digital Signal Processor (DSP) optimized for processing and transferring data. This enhanced processor provides an upward migration path for its Z89C00/Z89321 predecessors.

The DSP provides three 12-bit Register Pointers for each RAM bank. These pointers may be incremented or decremented automatically to implement circular buffers without software overhead.

Three prioritized and individually maskable interrupts are provided for use by external peripherals requiring service from the DSP. The interrupt inputs can be individually conditioned for edge or level trigger. Acknowledgement of an activated interrupt occurs at the end of an instruction execution.

Two banks of 512 x 16-bit data RAM are available. Expansion of the on-chip data RAM is provided through future upgrades.

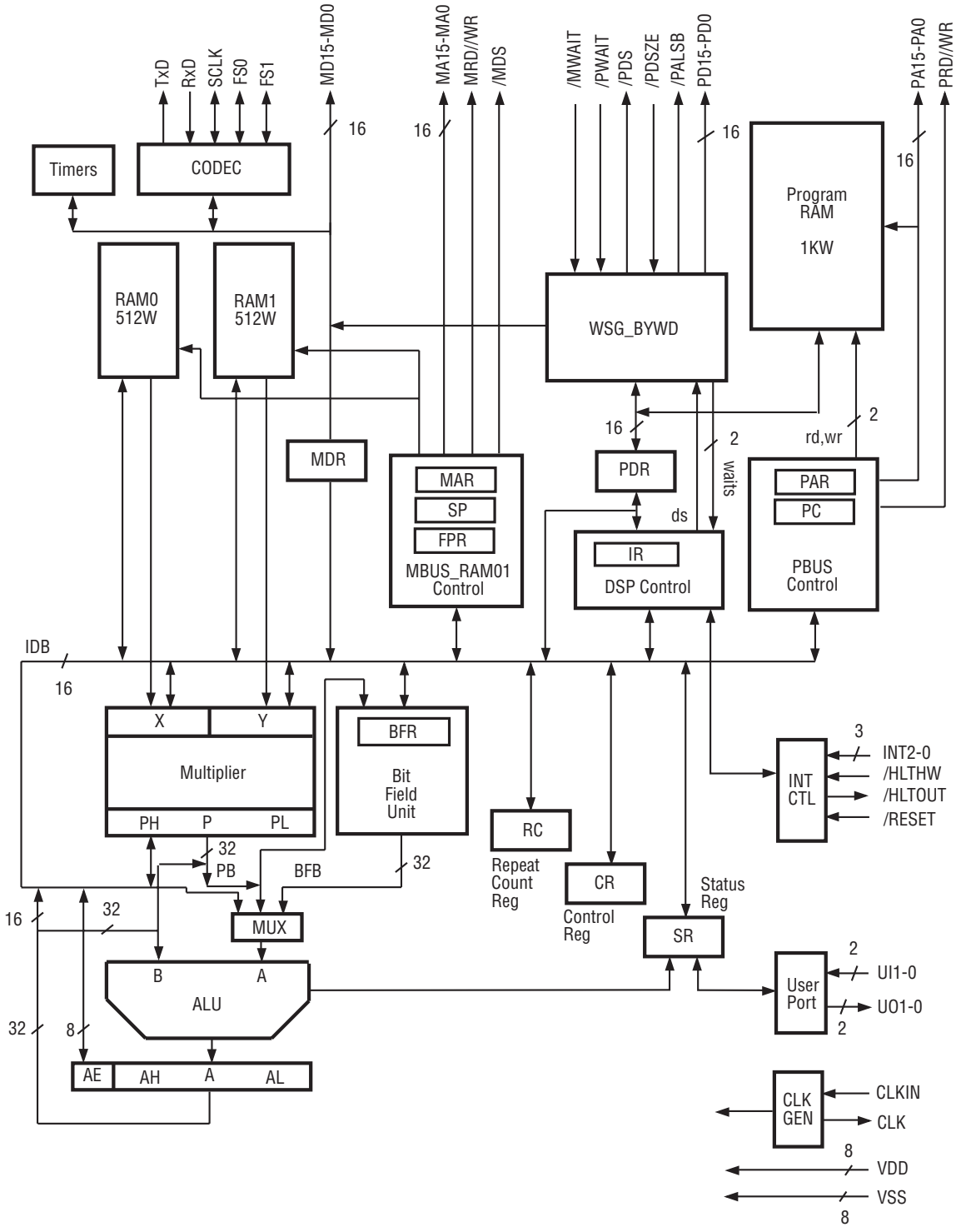
External interfaces include Address Bus and Data Bus for external Program Memory, Address Bus and Data Bus for external Data Memory, three vectored interrupt ports, and two input/two output user ports.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

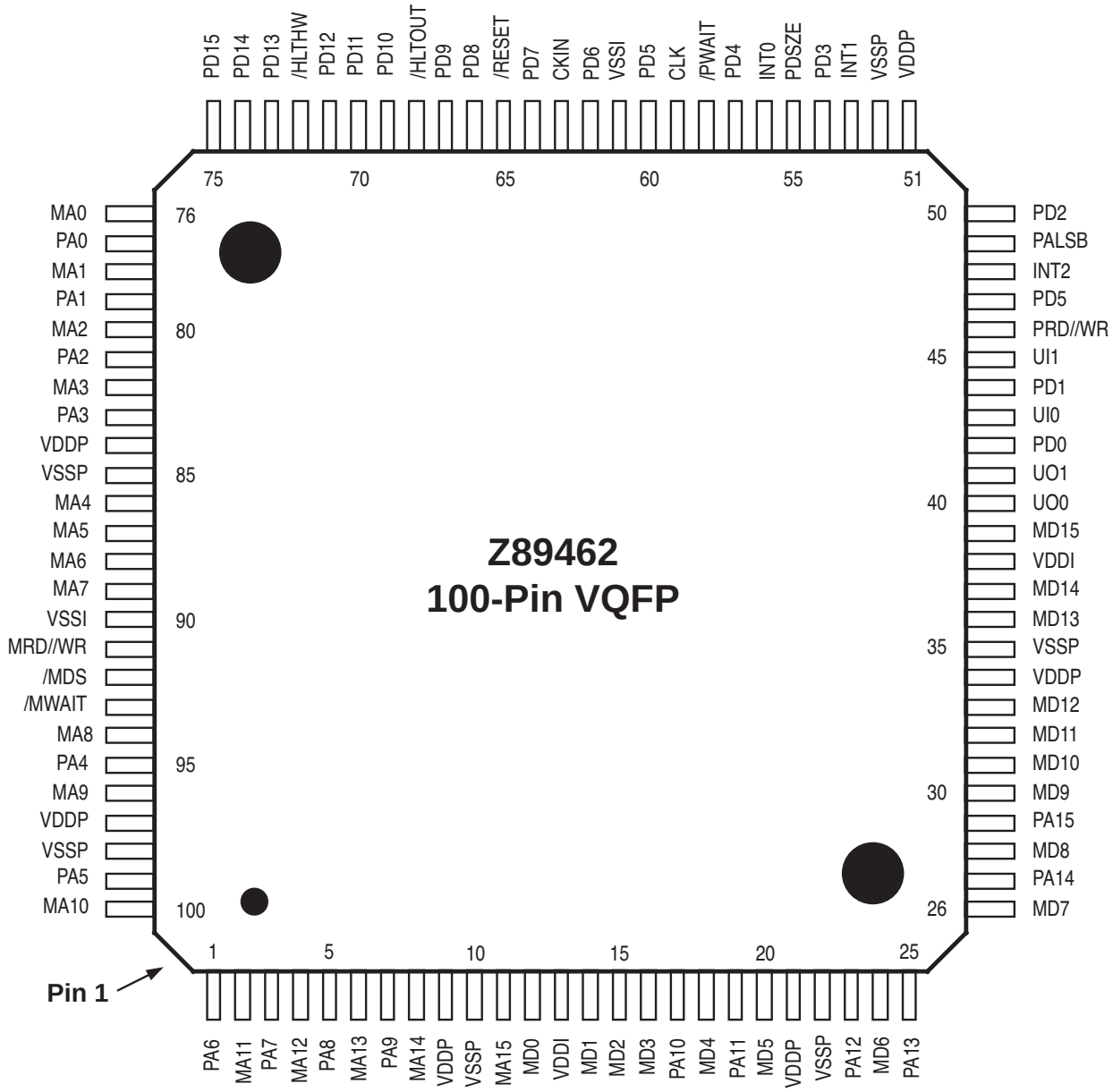
Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



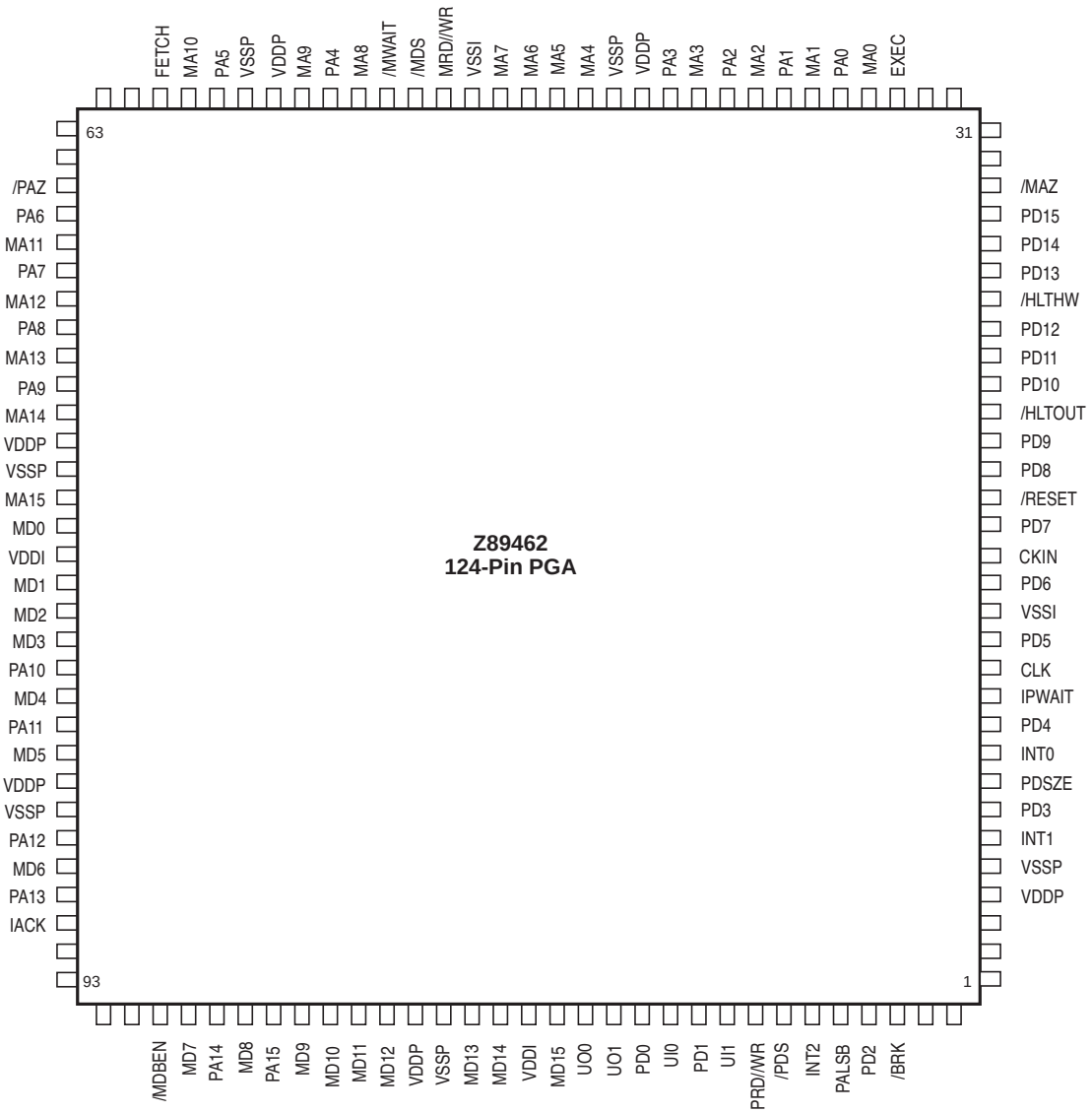
Functional Block Diagram

PIN DESCRIPTION



100-Pin VQFP Pin Assignments

PIN DESCRIPTION (Continued)



124-Pin PGA Pin Assignments

ABSOLUTE MAXIMUM RATINGS

Description		Min.	Max.	Units
Voltages on V_{DD} with Respect to V_{SS}		–0.5	+5.5	V
Voltages on All Pins with Respect to V_{SS}		–0.5	(V_{DD}+0.5)	V
T_{STG}	Storage Temp	–85°	+150°	°C
T_A	Oper Ambient Temp	0°	+70°	°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

STANDARD TEST CONDITIONS

The AC and DC Characteristics listed below apply for standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (= Ground = 0V). Positive current flows into the referenced pin. Standard conditions are as follows:

3.0V < VDD < 3.6V
VSS = 0V
Ambient Temperature = 0°C to +70°C
Standard Test Load on All Outputs

DC ELECTRICAL CHARACTERISTICS

(5.0V Operation)

Sym.	Parameter	Min.	Max.	Unit	Note
V_{IH}	Input High Voltage	2.0	V_{DD} +0.5	V	
V_{IL}	Input Low Voltage	–0.5	0.8	V	
V_{OH1}	Output High Voltage (–4 mA I_{OH})	2.4		V	
V_{OH2}	Output High Voltage (–250 µA I_{OH})	V_{DD} –0.8		V	
V_{OL}	Output Low Voltage (4 mA I_{OL})		0.5	V	
I_{IL}	Input Leakage Current	–10	+10	µA	[1]
I_{TL}	Tri-State Leakage Current	–10	+10	µA	[2]
I_{DD}	Power Supply Current (@ 40 Mhz)		TBD	mA	[3]
I_{DD2}	Stopped Clock Power Supply Current		20	µA	[4]
C_{IN}	Input Capacitance (f = 1 MHz)		15	pF	[5]
C_{OUT}	Output Capacitance (f = 1 Mhz)		15	pF	[5]
C_{IO}	I/O Capacitance (f = 1 MHz)		15	pF	[5]
C_L	Output Load Capacitance		30	pF	

Notes:
[1] V_{IN} = 0.4V
[2] 0.4V < V_{OUT} < 2.4V
[3] V_{DD} = 5.0V, V_{IH} = 4.8V, V_{IL} = 0.2V
[4] V_{DD} = 5.0V, V_{IH} = 4.8V, V_{IL} = 0.2V
[5] Unmeasured pins returned to V_{SS}.

AC ELECTRICAL CHARACTERISTICS
(5.0V Operation)

Symbol	Parameter	Min.	Max.	Unit	Note
TcCI	CLKIN Cycle Time	25		ns	
TwCIh	CLKIN Width High	10		ns	
TwCIl	CLKIN Width Low	10		ns	
TrCI	CLKIN Rise Time		2	ns	
TfCI	CLKIN Fall Time		2	ns	
TdCIr(Cr)	CLKIN Rise to CLK Rise Delay		8	ns	
TdCIf(Cf)	CLKIN Fall to CLK Fall Delay		8	ns	
TrC	CLK Rise Time		2	ns	
TfC	CLK Fall Time		2	ns	
TdCr(PA)	CLK Rise to PA Valid Delay		5	ns	
TdCr(PALSB)	CLK Rise to PALSB Valid Delay		5	ns	
TdCr(PDSr)	CLK Rise to /PDS Rise Delay		4	ns	
TdCf(PDSf)	CLK Fall to /PDS Fall Delay		4	ns	
TsPW(Cr)	/PWAIT to CLK Rise Setup Time	5		ns	
ThPW(Cr)	/PWAIT to CLK Rise Hold Time	0		ns	
TsPSZ(Cr)	PDSZE to CLK Rise Setup Time	5		ns	
ThPSZ(Cr)	PDSZE to CLK Rise Hold Time	0		ns	
TdCr(PRDWR)	CLK Rise to PRD//WR Delay		5	ns	
TsPD(Cr)	PD to CLK Rise Setup Time	5		ns	
ThPD(Cr)	PD to CLK Rise Hold Time	0		ns	
TdCR(PD)	CLK Rise to PD Valid Delay		5	ns	
TdCr(PDt)	CLK Rise to PD Tri-State Delay		5	ns	
TdCr(MA)	CLK Rise to MA Valid Delay		5	ns	
TdCr(MDSr)	CLK Rise to /MDS Rise Delay		4	ns	
TdCf(MDSf)	CLK Rise to /MDS Fall Delay		4	ns	
TsMW(Cr)	/MWAIT to CLK Rise Setup Time	5		ns	
ThMW(Cr)	/MWAIT to CLK Rise Hold Time	0		ns	
TdCr(MRDWR)	CLK Rise to MRD//WR Delay		5	ns	
TsMD(Cr)	MD to CLK Rise Setup Time	5		ns	
ThMD(Cr)	MD to CLK Rise Hold Time	0		ns	
TdCr(MD)	CLK Rise to MD Valid Delay		5	ns	
TdCr(MDt)	CLK Rise to MD Tri-State Delay		5	ns	
TsINT(Cr)	INT2-0 to CLK Rise Setup Time	5		ns	[1]
TwINTh	INT2-0 Width High	10		ns	
TwHLTHWl	/HLTHW Width Low	10		TcCI	[2]
TwHLTHWh	/HLTHW Width High	2		TcCI	[2]
TdCr(HLTOUT)	CLK Rise to HLTOUT Delay		5	ns	
TwRESETl	/RESET Width Low	3		TcCI	[2]

Notes:
[1] INT2-0 can also be asserted/deasserted asynchronously.
[2] These signals are asserted/deasserted asynchronously.

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DC ELECTRICAL CHARACTERISTICS

(3.0V Operation)

Sym.	Parameter	Min.	Max.	Unit	Note
V_{IH}	Input High Voltage	2.0	V_{DD} +0.5	V	
V_{IL}	Input Low Voltage	–0.5	0.6	V	
V_{OH}	Output High Voltage (–200 µA I_{OH})	2.15		V	
V_{OL}	Output Low Voltage (4 mA I_{OL})		0.4	V	
I_{IL}	Input Leakage Current	–10	+10	µA	[1]
I_{TL}	Tri-State Leakage Current	–10	+10	µA	[2]
I_{DD}	Power Supply Current (@ 40 Mhz)		TBD	mA	[3]
I_{DD2}	Stopped Clock Power Supply Current		20	µA	[4]
C_{IN}	Input Capacitance (f = 1 MHz)		15	pF	[5]
C_{OUT}	Output Capacitance (f = 1 Mhz)		15	pF	[5]
C_{IO}	I/O Capacitance (f = 1 MHz)		15	pF	[5]
C_L	Output Load Capacitance		30	pF	

Notes:

[1] V_{IN} = 0.4V

[2] 0.4V < V_{OUT} < 2.15V

[3] V_{DD} = 3.3V, V_{IH} = 3.0V, V_{IL} = 0.2V

[4] V_{DD} = 3.3V, V_{IH} = 3.0V, V_{IL} = 0.2V

[5] Unmeasured pins returned to V_{SS}.

Pre-Characterization Product:
The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

Development Projects:
Customer is cautioned that while reasonable efforts will be employed to meet performance objectives and milestone dates, development is subject to unanticipated problems and delays. No production release is authorized or committed until the Customer and Zilog have agreed upon a Customer Procurement Specification for this project.

Low Margin:
Customer is advised that this product does not meet Zilog's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on Zilog liability stated on the front and back of the acknowledgement, Zilog makes no claim as to quality and reliability under the CPS. The product remains subject to standard warranty for replacement due to defects in materials and workmanship.

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