Z86E64

CMOS Z8 OTP MICROCONTROLLER

FEATURES

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Z86E64	32	236	52	4.5-5V

Note: *General-Purpose

- Low-Power Consumption: 200 mW (max)
- Fast Instruction Pointer: 0.75 µs @ 16 MHz
- Two Standby Modes: STOP and HALT
- Full-Duplex UART
- All Digital Inputs are TTL Levels
- Auto Latches
- RAM and ROM Protect
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Eight Different Sources
- Low EMI Mode Option
- 68-Pin Leaded Chip-Carrier

GENERAL DESCRIPTION

The Z86E64 is a member of the Z8 single-chip microcontroller family. The Z86E64 can address both external memory and pre-programmed ROM, which enables this Z8 MCU™ to be used in high-volume applications where code flexibility is required.

The Z86E64 is a pin compatible, One-Time-Programmable (OTP) version of the Z86C64. The Z86E64 contains 32 KB of EPROM memory in place of the 32 KB of ROM on the Z86C64.

There are three basic address spaces available to support this wide range of configuration: Program Memory, Data Memory, and 236 general-purpose registers.

The Z86E64 offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications demanding powerful I/O capabilities, the Z86E64's dedicated input and output lines are grouped into six ports. Each port consists of eight lines, except port 6, which has four lines. Each port is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

The Z86E64 offers two on-chip counter/timers with a large number of user-selectable modes, and an Universal Asynchronous Receiver/Transmitter (UART). See figure 1 for-Functional Block description.

Note: All Signals with a preceding front slash, "/", are active Low, for example: B//W (WORD is active Low); /B/W (BYTE is active Low, only). Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

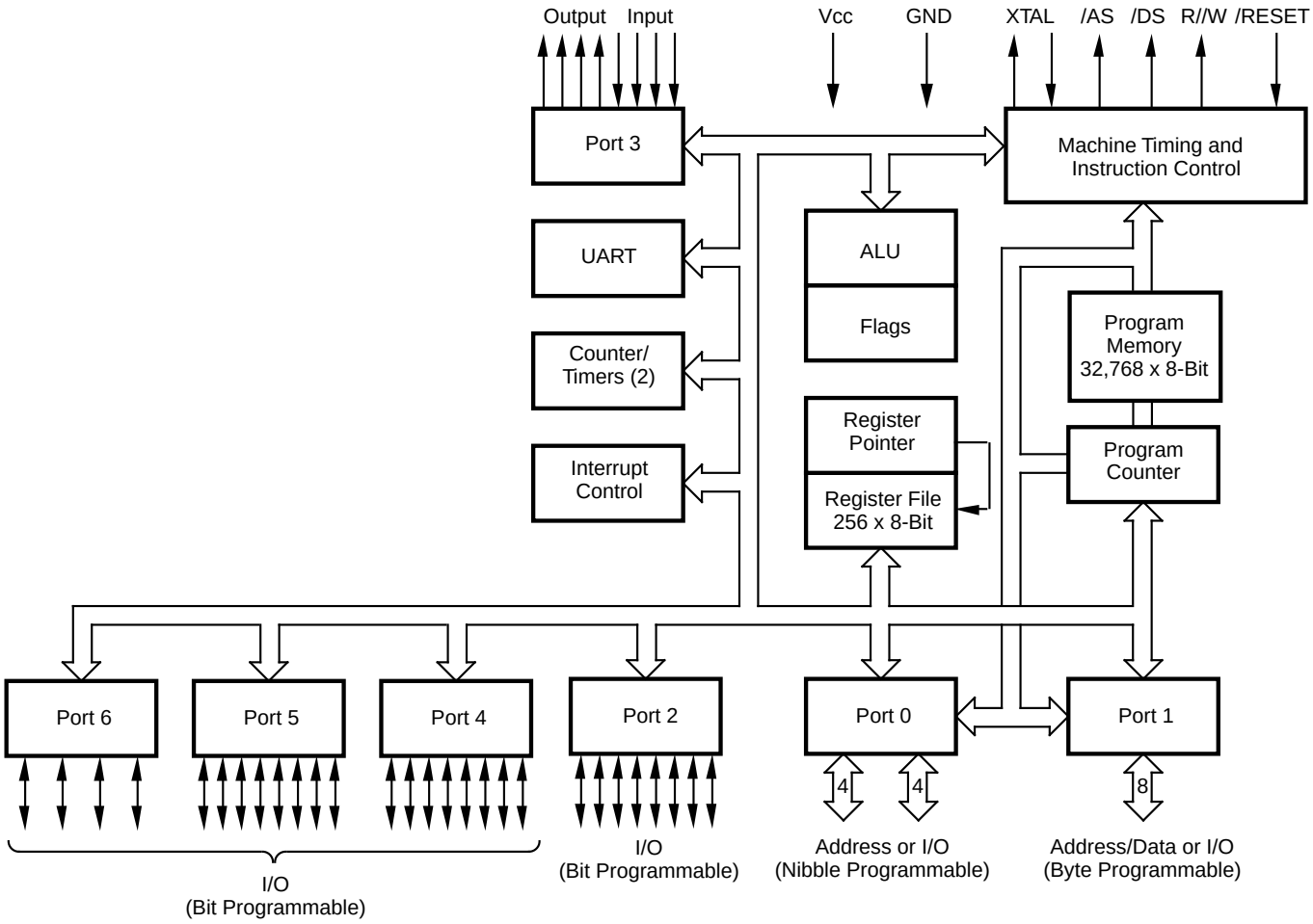

Figure 1. Z86E64 Functional Block Diagram

PIN DESCRIPTION

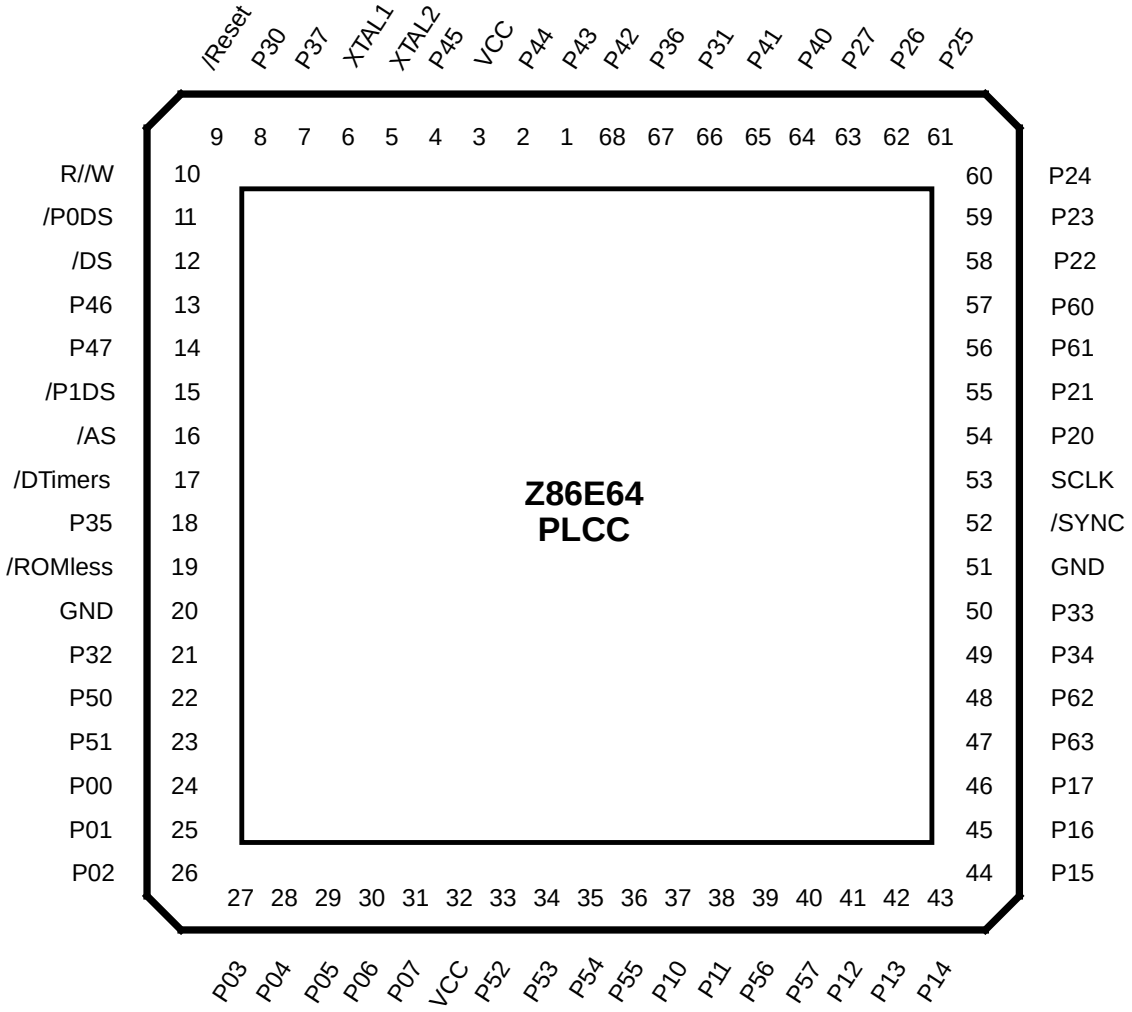

Figure 2. Z86E64 68-Pin PLCC Pin Assignments

PIN DESCRIPTION (Continued)

Table 1. Z86E64 68-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1-2	P44-P43	Port 4, Pins 3,4	In/Output
3	VCC	Power Supply	Input
4	P45	Port 4, Pin 5	In/Output
5	XTAL2	Crystal, Oscillator Clock	Output
6	XTAL1	Crystal, Oscillator Clock	Input
7	P37	Port 3, Pin 7	Output
8	P30	Port 3, Pin 0	Input
9	/RESET	Reset	Input
10	R//W	Read/Write	Output
11	/P0DS	Port 0 Data Strobe	Output
12	/DS	Data Strobe	Output
13-14	P47-P46	Port 4, Pins 6,7	In/Output
15	/P1DS	Port 1, Data Strobe	Output
16	/AS	Address Strobe	Output
17	/DTIMER	DTIMER	Input
18	P35	Port 3, Pin 5	Output
19	/ROMless	ROM/ROMless control	Input
20	GND	Ground	Input
21	P32	Port 3, Pin 2	Input
22-23	P51-P50	Port 5, Pins 0,1	In/Output
24-31	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
32	VCC	Power Supply	Input
33-36	P55-P52	Port 5, Pins 2,3,4,5	In/Output
37-38	P11-P10	Port 1, Pins 0,1	In/Output
39-40	P56-P57	Port 5, Pins 6,7	In/Output
41-46	P17-P12	Port 1, Pins 2,3,4,5,6,7	In/Output
47-48	P63-P62	Port 6, Pins 3,2	In/Output
49	P34	Port 3, Pin 4	Output
50	P33	Port 3, Pin 3	Input
51	GND	Ground	Input
52	/SYNC	Synchronization	Output
53	SCLK	System Clock	Output
54-55	P21-P20	Port 2, Pins 0,1	In/Output
56-57	P60-P61	Port 6, Pins 1,0	In/Output
58-63	P27-P22	Port 2, Pins 2,3,4,5,6,7	In/Output
64-65	P41-P40	Port 4, Pins 0,1	In/Output
66	P31	Port 3, Pin 1	Input
67	P36	Port 3, Pin 6	Output
68	P42	Port 4, Pin 2	In/Output

DC CHARACTERISTICS

V_{CC} = 4.5V to 5.5V

		TA = 0°C to +70°C		Typical at		
Sym	**Parameter**	**Min**	**Max**	**25°C**	**Units**	**Conditions**
	Max Input Voltage		7		V	I_{IN} <250 µA
	Max Input Voltage		12.5V		V	P30-P33 Only in OTP mode
V_{CH}	Clock Input High Voltage	3.8	VCC		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	–0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	VCC		V	
V_{IL}	Input Low Voltage	–0.3	0.8		V	
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –2.0 mA
V_{OL}	Output Low Voltage		0.4		V	I_{OL} = +2.0 mA
V_{RH}	Reset Input High Voltage	3.8	VCC		V	
V_{Rl}	Reset Input Low Voltage	–0.3	0.8		V	
I_{IL}	Input Leakage	–10	10		µA	0V < V_{IN} < +5.25V
I_{OL}	Output Leakage	–10	10		µA	0V < V_{IN} < +5.25V
I_{IR}	Reset Input Current		–50		µA	V_{CC}= +5.25V, VRL = 0V
I_{CC}	Supply Current		50	25	mA	@ 12 MHz
			60	35	mA	@ 16 MHz
I_{CC1}	Standby Current		15	5	mA	
			20	10	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 16 MHz
I_{CC2}	Standby Current		20	5	µA	STOP Mode V_{IN} = 0V, V_{CC} @ 12 MHz
			20	5	µA	STOP Mode V_{IN} = 0V, V_{CC} @ 16MHz

AC CHARACTERISTICS

External I/O or Memory Read or Write Timing Diagram

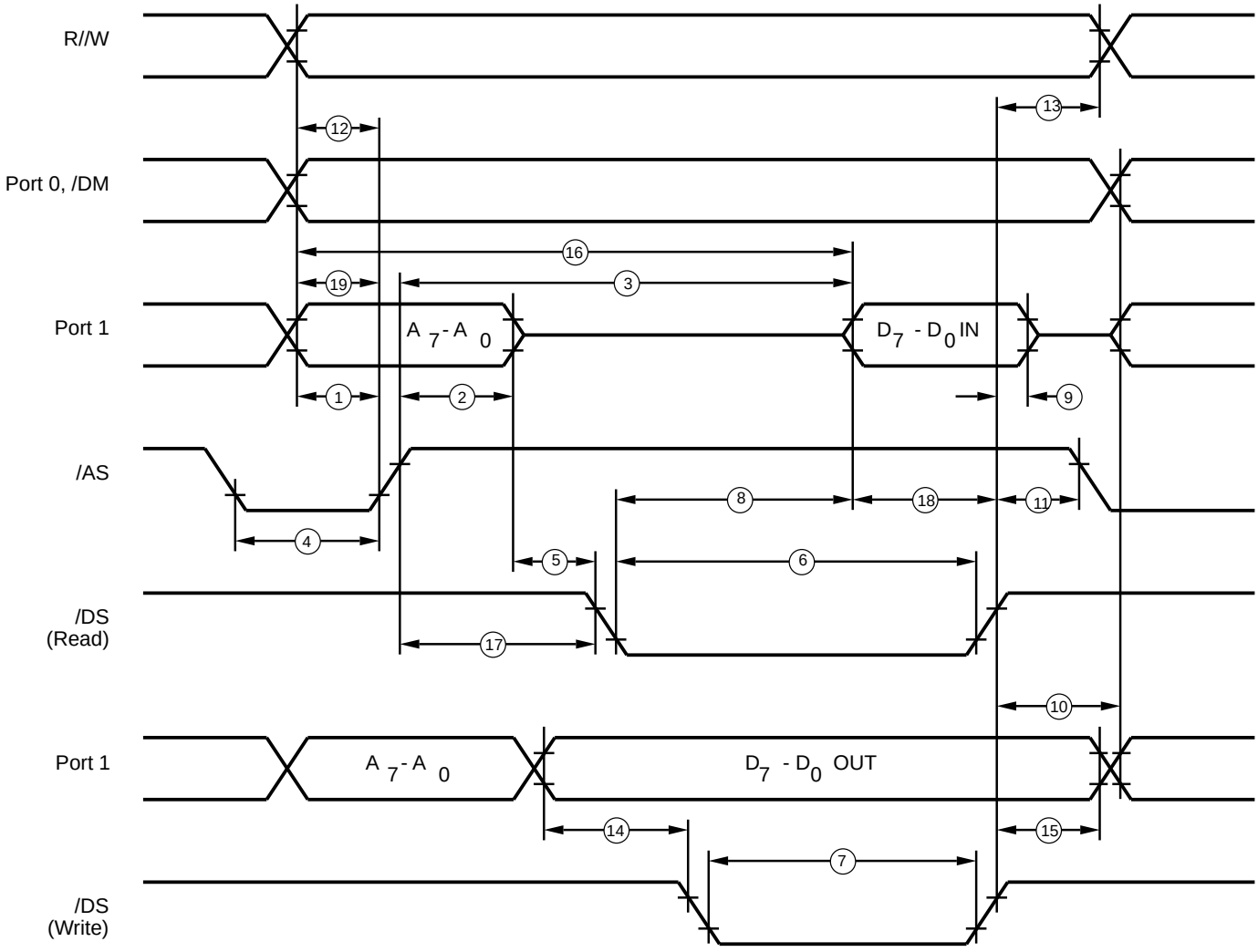

Figure 3. External I/O or Memory Read/Write Timing

External I/O or Memory Read and Write Timing Table

V_{CC} = 4.5V to 5.5V

			TA = 0°C to 70°C					
			12 MHz		16 MHz			
No	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TdA(AS)	Address Valid to /AS Rise Delay	35		20		ns	[2,3]
2	TdAS(A)	/AS Rise to Address Float Delay	45		30		ns	[2,3]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid		220		180	ns	[1,2,3]
4	TwAS	/AS Low Width	55		35		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS Fall	0		0		ns	
6	TwDSR	/DS (Read) Low Width	185		135		ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	110		80		ns	[1,2,3]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid		130		75	ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS Rise Hold Time	0		0		ns	[2,3]
10	TdDS(A)	/DS Rise to Address Active Delay	45		35		ns	[2,3]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	55		30		ns	[2,3]
12	TdR/W(AS)	R//W Valid to /AS Rise Delay	30		20		ns	[2,3]
13	TdDS(R/W)	/DS Rise to R//W Not Valid	35		30		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	35		25		ns	[2,3]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	35		30		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		255		200	ns	[1,2,3]
17	TdAS(DS)	/AS Rise to /DS Fall Delay	55		40		ns	[2,3]
18	TdDI(DS)	Data Input Setup to /DS Rise	75		60		ns	[1,2,3]
19	TdDM(AS)	/DM Valid to /AS Fall Delay	50		30		ns	[2,3]

Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] See clock cycle dependent characteristics.

Standard Test Load
All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.

Clock Dependent Formulas		
Number	**Symbol**	**Equation**
1	TdA(AS)	0.40TpC + 0.32
2	TdAS(A)	0.59TpC – 3.25
3	TdAS(DR)	2.38TpC + 6.14
4	TwAS	0.66TpC – 1.65
6	TwDSR	2.33TpC – 10.56
7	TwDSW	1.27TpC + 1.67
8	TdDSR(DR)	1.97TpC – 42.5

Clock Dependent Formulas		
10	TdDS(A)	0.8TpC
11	TdDS(AS)	0.59TpC – 3.14
12	TdR/W(AS)	0.4TpC
13	TdDS(R/W)	0.8TpC – 15
14	TdDW(DSW)	0.4TpC
15	TdDS(DW)	0.88TpC – 19
16	TdA(DR)	4TpC – 20
17	TdAS(DS)	0.91TpC – 10.7
18	TsDI(DS)	0.8TpC – 10
19	TdDM(AS)	0.9TpC – 26.3

AC CHARACTERISTICS (Continued)

Additional Timing Diagram

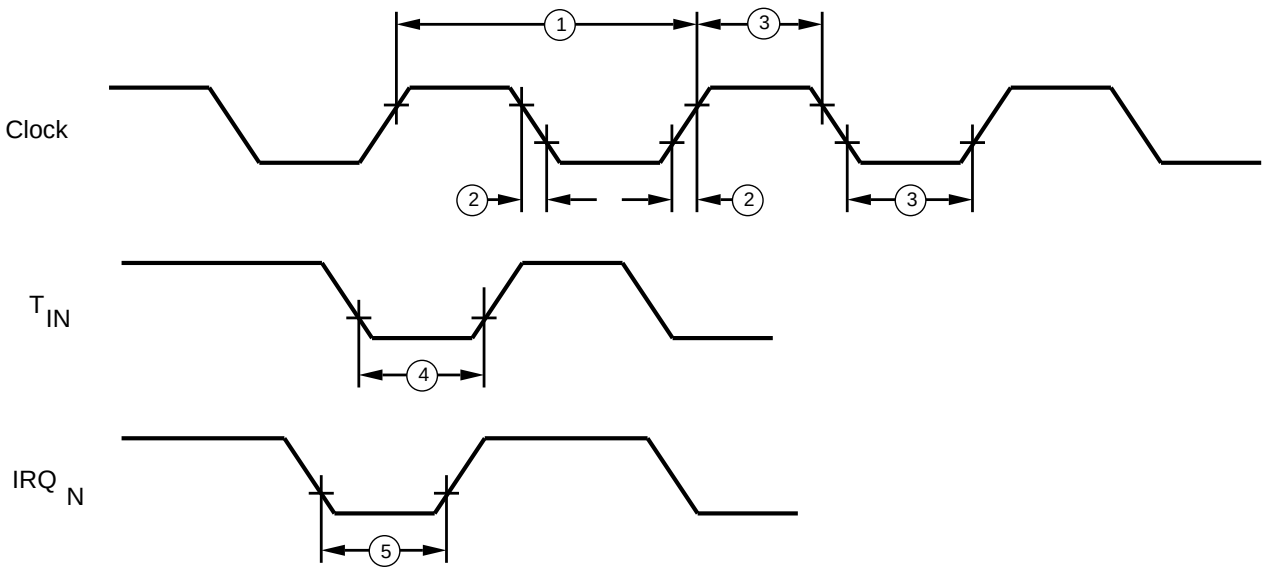

Figure 4. Additional Timing

AC CHARACTERISTICS

Additional Timing Table

V_{CC} = 4.5V to 5.5V

			TA = 0°C to +70°C					
			12 MHz		16 MHz			
No	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	83	500	62.5	500	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		15		10	ns	[1]
3	TwC	Input Clock Width	41		31		ns	[1]
4	TwTinL	Timer Input Low Width	75		50		ns	[2]
5	TwTinH	Timer Input High Width	5TpC		5TpC			[2]
6	TpTin	Timer Input Period	8TpC		8TpC			[2]
7	TrTin,TfTin	Timer Input Rise & Fall Times	100		100		ns	[2]
8A	TwIL	Interrupt Request Input Low Times	70		50		ns	[2,4]
8B	TwIL	Interrupt Request Input Low Times	5TpC		5TpC			[2,5]
9	TwIH	Interrupt Request Input High Times	5TpC		5TpC			[2,3]

Notes:
1. Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
2. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
3. Interrupt references request via Port 3.
4. Interrupt request via Port 3 (P31-P33).
5. Interrupt request via Port 30.

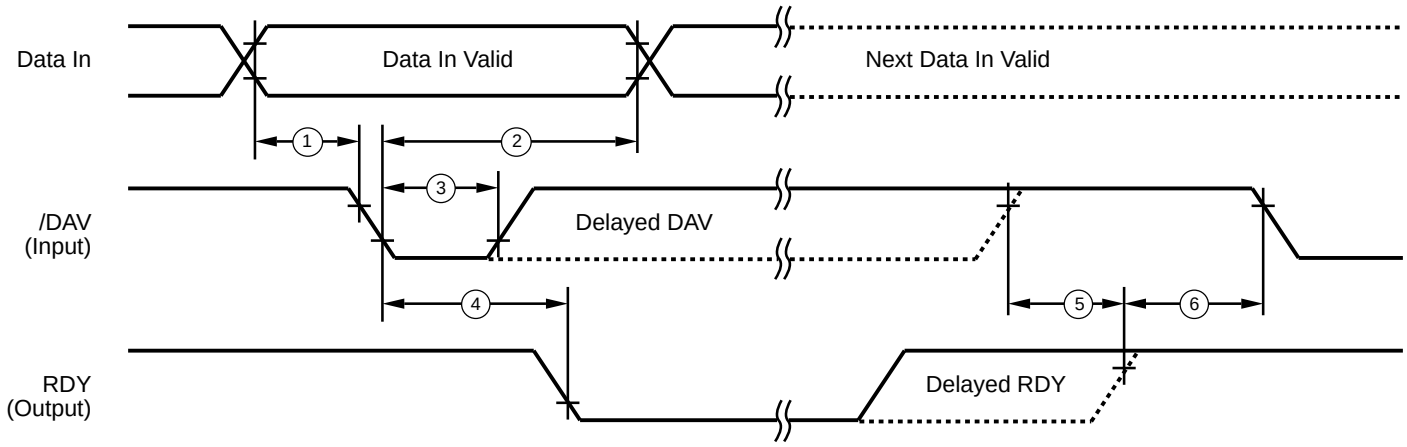

Figure 5. Input Handshake Timing

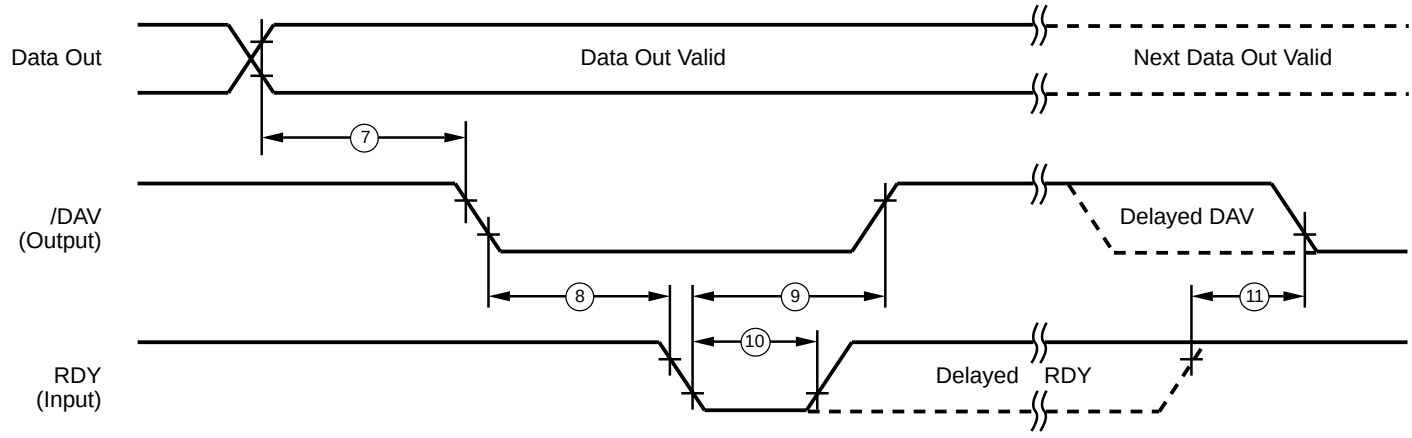

Figure 6. Output Handshake Timing

AC CHARACTERISTICS (Continued)

Handshake Timing Table

VCC = 4.5V to 5.5V

			TA = 0°C to +70°C				Notes
			12 MHz		16 MHz		Data
No	Symbol	Parameter	Min	Max	Min	Max	Direction
1	TsDI(DAV)	Data In Setup Time	0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		IN
3	TwDAV	Data Available Width	110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay		115		115	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay		115		115	IN
6	TdDO(DAV)	RDY Rise to DAV Fall Delay	0		0		IN
7	TcLDAV0(RDY)	Data Out to DAV Fall Delay		TpC		TpC	OUT
8	TcLDAV0(RDY)	DAV Fall to RDY Fall Delay	0		0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay		115		115	OUT
10	TwRDY	RDY Width	110		110		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay		115		115	OUT

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

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