ZILOG

PRELIMINARY PRODUCT SPECIFICATION

Z84C50
Z80 RAM 80
Z80 CPU/2K SRAM

JUNE 1989

FEATURES

- Z80 CPU 2K Static RAM
- Wait State Generator for external memory
- Low power consumption
  - (TBD) Typ (5V,10 MHz under RUN mode)
  - (TBD) Typ (5V, 10 MHz under IDLE1 mode)
  - (TBD) Typ (5V, 10 MHz under IDLE2 mode)
  - (TBD) Typ (5V under STOP mode)
- DC to 10 MHz operation (at 5V ± 10%)
- Single 5V power supply (at 5V ± 10%)
- Operating Temperature (0° C to 70° C)
- On-chip clock generator
- In the HALT state, the following 4 modes are selectable:
  - RUN mode
  - IDLE 1 mode
  - IDLE 2 mode
  - STOP mode
- Powerful set of 158 instructions
- Power Interrupt function
  - Non-Maskable Interrupt terminal (NMI)
  - Maskable Interrupt terminal (INT)
- The following three modes are selectable:
  - 8080 compatible interrupt mode (interrupt by Non-Z80 family peripheral LSI-Mode 0)
  - Restart Interrupt (Mode 1)
  - Daisy-chain structure interrupt using Z80 family peripheral LSI (Mode 2)
- Built-in refresh circuit for dynamic memory
- Available in 40-pin DIP, 44-pin PLCC, and 44-pin QFP packages

GENERAL DESCRIPTION

The Z84C50 is an 8-bit microprocessor integrated with 2K bytes of static memory and a clock generator/controller. The Z84C50 is targeted for a broad range of applications requiring a small amount of RAM. Additionally, the on-chip RAM can be accessed at a much higher rate than the external memory. This will significantly enhance performance, as the most commonly used and time critical software can be placed in on-chip memory.

Built into the Z84C50 is a control function and clock generator for the standby function in addition to: six paired general purpose registers, accumulator, flag registers, an arithmetic-and-logic unit, bus control, memory control and timing control circuits. Also, an on-chip wait state generator can be used for automatically inserting wait states for external memory accesses.

The Z84C50 is fabricated with Zilog CMOS technology and molded in 40-pin DIP, 44-pin PLCC, and 44-pin QFP packages.

PIN CONNECTIONS AND PIN FUNCTIONS

The pin connections and I/O pin names and brief functions of the Z84C50 are shown below.

Pin Connections. The pin connections of the Z84C50 are as show in Figures 1 to 3.

Pin Names and Functions. I/O pin names and functions are as shown in Table 1.

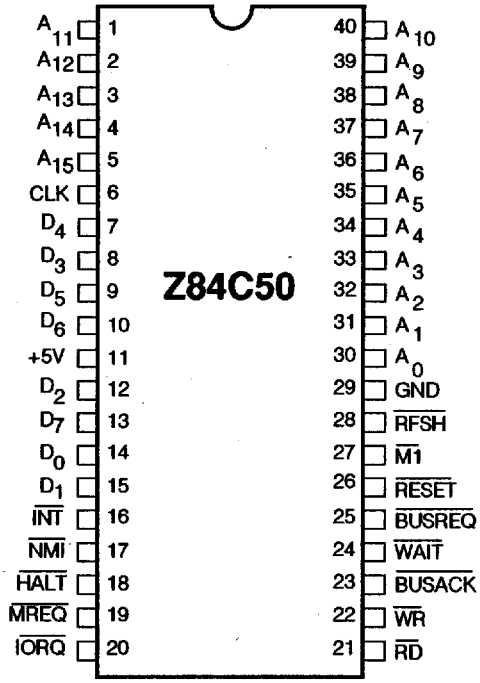


Figure 1. Pin Connections (top view) - DIP Package

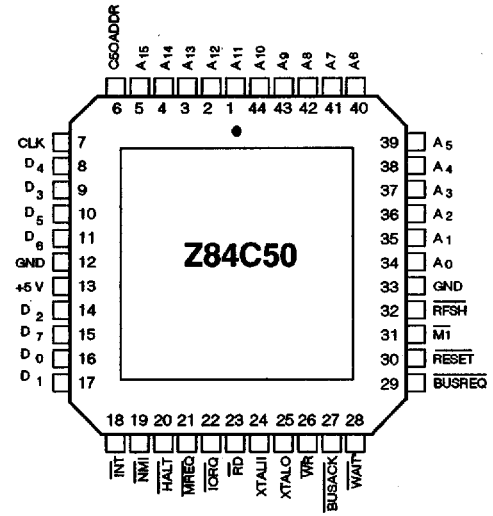


Figure 2. Pin Connections (top view) - PLCC Package

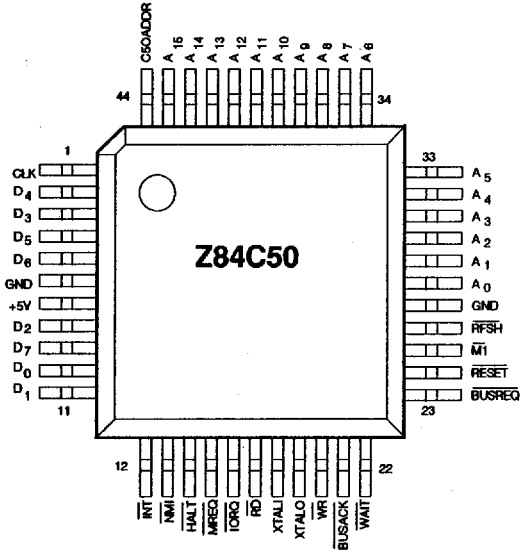


Figure 3. Pin Connections (top view) - QFP Package

TABLE 1. PIN NAMES AND FUNCTIONS

Pin	# of Pins	I/O 3-state	Function
A0-A15	16	I/O 3-state	16-bit address bus. Specifies addresses of memories and I/O to be accessed. During the refresh period, addresses (Aø-A6) for refreshing are output. The bus is an input when the external master is accessing the on-chip RAM.
D0-D7	8	I/O 3-state	8-bit bidirectional data bus.
$\overline{INT}$	1	Input	Maskable Interrupt request signal. $\overline{INT}$ is normally wired-OR and requires an external pull up resistor for these applications.
$\overline{NMI}$	1	Input	Non-Maskable Interrupt request signal. This interrupt request has the higher priority than the maskable interrupt request.
$\overline{HALT}$	1	I/O 3-state	Halt signal. Indicates that the CPU has executed a Halt instruction. ***Input during evaluation mode & BUSACK.***
$\overline{MREQ}$	1	I/O 3-state	Memory Request signal. When an effective address for external memory access is on the address bus, '0' is output. When an external master is accessing the on-chip RAM, it is an input signal.
$\overline{IORQ}$	1	I/O 3-state	Indicating an I/O operation with I/O address on lower 8-bits (A0-A7) of the address bus. $\overline{IORQ}$ signal is output together with $\overline{M1}$ signal at time of interrupt acknowledge cycle to inform peripheral devices that the interrupt response vector may be put on the bus. Input during register accesses by external masters and also to initiate the evaluation mode during reset.
$\overline{RD}$	1	I/O 3-state	Read signal. Asserted for a period when MPU can receive data from a memory of peripheral LSI. When an external master is accessing the on-chip RAM, it is an input signal.
$\overline{WR}$	1	I/O 3-state	Write signal. This signal is output when data to be stored in a specified memory or peripheral LSI is on the MPU data bus. When an external master is accessing the on-chip RAM, it is an input signal.
$\overline{BUSACK}$	1	Output	Bus Acknowledge signal. In response to $\overline{BUSREQ}$ signal, this signal informs a peripheral LSI that the address bus, data bus, $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ signals have been placed in the high impedence state.
$\overline{WAIT}$	1	I/O Wired-OR	Wait signal. $\overline{WAIT}$ signal is asserted by memory or peripheral LSI that is not ready for data transfer. As long as $\overline{WAIT}$ signal is active, MPU is continuously kept in the wait state. Driven out when the wait states are inserted by on-chip wait state generator.

TABLE 1. PIN NAMES AND FUNCTIONS (Continued)

Pin	# of Pins	I/O 3-state	Function
$\overline{BUSREQ}$	1	Input	Bus Request signal. $\overline{BUSREQ}$ signal is a signal asserted by external masters to request placement of $\overline{M1}$, $\overline{HALT}$, address bus, data bus, $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, $\overline{RFSH}$, and $\overline{WR}$ signals in the high impedence state. $\overline{BUSREQ}$ signal is normally wired-OR. In this case, a pull-up resistor is externally connected.
$\overline{RESET}$	1	I/O 3-state	Reset signal. $\overline{RESET}$ signal is used for initializing MPU and other devices in the system. If it is an input, it must be kept in active state for a period of a least 3 clocks. During the power-up sequence, this input is sampled for 50 to 150 micro-seconds after the power supply passes through approx. 2.2V. If it is not active during this window, Z84C50 will drive the power on reset for 25 to 75 msec.
$\overline{M1}$	1	Input Output	Signal indicating an op code fetch. Also asserted during the RETI cycle and interrupt acknowledge cycle (along with the $\overline{IORQ}$ signal). Input during the on-chip accesses by external masters and during evaluation mode. ***Input during evaluation and bus acknowledge modes.***
XTALI XTALO	1 1	I/O 3-state	Crystal Oscillator connecting terminals. A parallel resonant crystal is recommended. A crystal presence is automatically detected by the Z84C50. The input signal is divided by 1 or 2, depending upon bit 4 of the Control Register. The oscillator is used in either case. Also, all the power down modes are available in the 'halt' state. Those pins are not available on 40-pin DIP version.
CLK	1	I/O	The single-phase clock generated by the internal oscillator is output on the CLK pin. When this crystal is not installed the pin becomes an input for connecting the external clock. This is always the case for the 4o-pin DIP device. The oscillator and clock divider are bypassed. Only the IDLE2 and RUN halt modes are applicable in this case.
C50ADDR	1	Output	This signal is asserted by the Z84C50 when the on-chip 2K static RAM and the I/O registers are accessed by the on-chip CPU or the external master. This signal is not available on 40-pin DIP version.
VCC	1	Power	+5V
VSS	2	GND	0V
$\overline{RFSH}$	1	I/O 3-state	$\overline{RFSH}$ together with the $\overline{MREQ}$, indicates that the lower seven bits of system's address bus can be used as a refresh address to the system's dynamic memories. Input signal when the wait-state generator is to be used by external BUS master.

Note: Please make sure that in BUS-acknowledge modes, $\overline{M1}$, $\overline{RFSH}$ and $\overline{HALT}$ become input while on Z84C00 these are output pins.

FUNCTIONAL DESCRIPTION

The system configuration, functions and basic operation of the Z84C50 are described here.

Block Diagram. The block diagram of the internal configuration is shown in Figure 4.

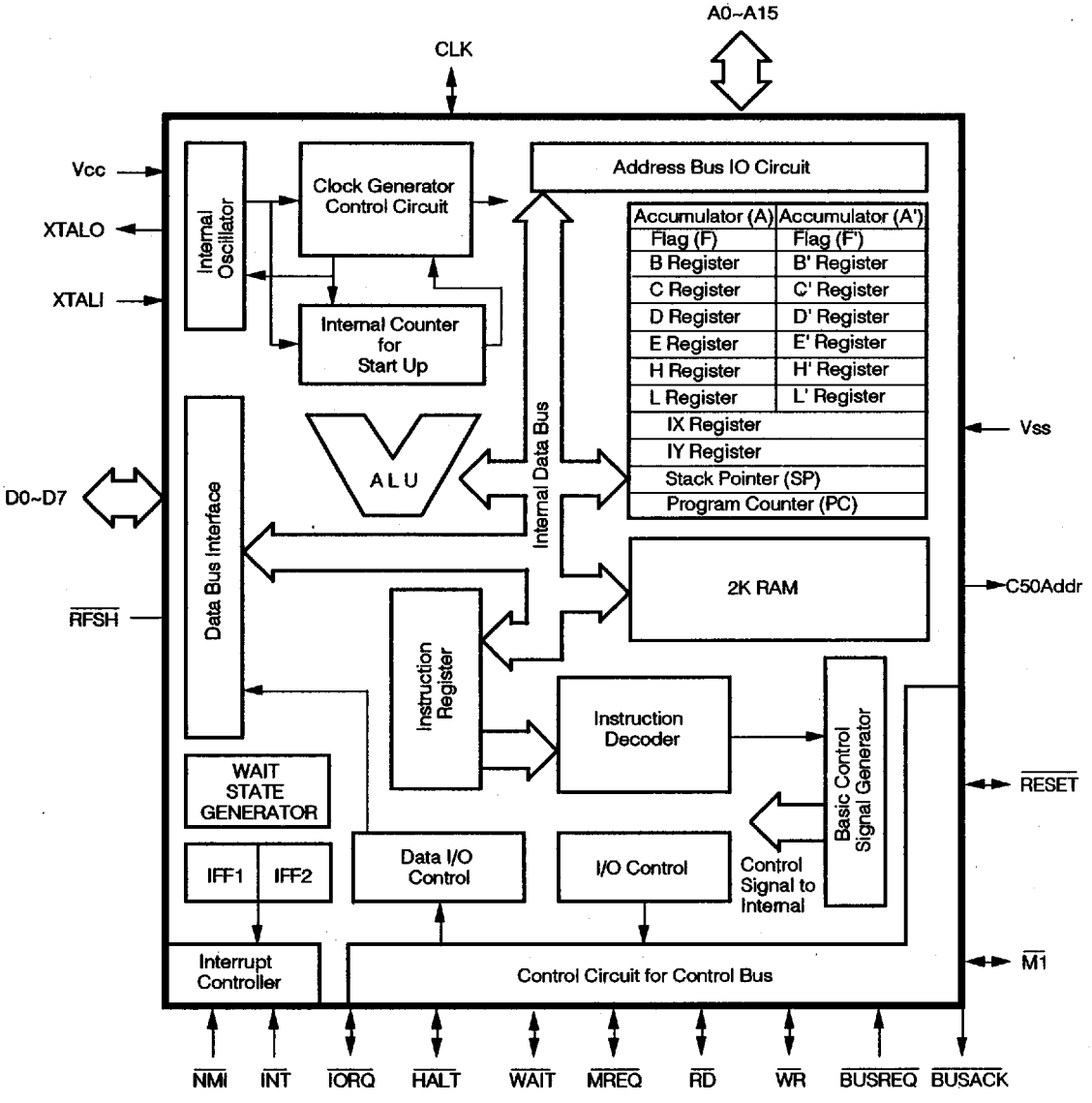


Figure 4. Block Diagram

On-Chip Memory

The Z84C50 has 2K bytes of on-chip memory. This memory is mappable to any 2K boundary of the Z80 memory space by software control. The memory is accessible from the local CPU or the external masters via the Z80 bus request/bus grant handshake. When this memory is accessed, the C50ADDR output signal is asserted. This signal may be used by external logic to control external memory. The on-chip memory is normally disabled on power-up. On power-up reset, if $\overline{BUSREQ}$ precedes the de-assertion of $\overline{RESET}$ (rising edge), the RAM is enabled and one NOP instruction is automatically executed. This allows power-up loading of this RAM from external masters. The automatic execution of one NOP instruction prevents any possibility of executing instructions from external memory. For this case, it is recommended that a NOP instruction be at Location 0000H of the program.

The on-chip memory is always accessed with no wait states. When the external master is accessing RAM, the address lines are input to the chip, while the direction of the data lines is reversed from normal external memory accesses by the local CPU. Thus, both the address and data lines are bi-directional.

The base address of this on-chip memory is selectable to any 2K boundary of the Z80 memory space. This is done by programming bits 0-4 of the Memory Page Address Register. If the on-chip RAM is enabled by setting bit 5 of this register, these 5 bits provide the address lines A11-A15 for the on-chip memory accesses.

Wait State Generator

The Z84C50 has a Wait State Generator for inserting wait states for external memory accesses. The on-chip memory does not require any wait states. The wait state generation is handled separately for the op-code fetches as the transaction timing for the Z80 op-code fetch is tighter. The user can set the "op-code fetch extension" bit (bit 5) of the Control Register (CR) thereby causing the Wait State Generator to insert one additional wait state. The bits 0-1 of the Control Register are set to specify the wait states for the normal external memory accesses. The following table shows the wait states for various cycles:

Table 2. Wait States (Memory)

CR (5)	CR(1)	CR(0)	Op code Fetch	Data
0	0	0	0	0
0	0	1	1	1
0	1	0	2	2
0	1	1	3	3
1	0	0	1	0
1	0	1	2	1
1	1	0	3	2
1	1	1	4	3

Oscillation Detection Circuit

The PLCC or QFP versions of Z84C50 allows crystal input (XTALI, XTALO) or system clock input. If crystal input is provided, an internal oscillator is used to generate clocks for the Z80 as well as external devices. On power-up, it comes up in divide by 2 mode. If external clock (system clock) is provided on the CLK pin (or on 40-pin DIP version), the oscillator and the divide by 2 circuitry are bypassed. If the external clock or crystal input is provided on the XTAL pins, the internal oscillator is used and the divide-by-2 circuit is activated depending upon bit 4 of the Control Register. Also, the power-down modes of the 84C50 vary based on whether the clock is crystal derived or is the system clock (CLK) Pin. If the clock is crystal derived all of the modes in "halt" state are available. If the external system clock is provided on the CLK pin (and 40-pin DIP version), only the IDLE1 mode is applicable and the internal CPU is stopped if this mode is selected.

Power-on Reset

The Z84C50 has a power-up reset circuit. If $\overline{RESET}$ input is asserted within 150 microseconds of power-up (power supply above 2.2V), it is considered an input signal. Otherwise, an internal $\overline{RESET}$ signal is generated after the power is stabilized and output on the $\overline{RESET}$ pin for external use. The $\overline{RESET}$ signal is asserted for 25 to 75 msec. After termination of the "power-on reset" cycle the pin will revert back to an input. It can also become an output again should the next extension operation not be disabled. If not enabled, it will continue as an input.

The 84C50 registers are initialized on power-up reset as follows: Control Register :x010 1111 and Memory Page Register: xx00 0000. The "x" represents unused bits and thus the values should be masked off. Other bits in the Control Register indicate that on reset the chip comes up with: 3 memory wait states, run mode, divide by two clock, op code extension bit enabled, and reset output enabled. The Memory Page Address Register is initialized to: zero page base address, and RAM disabled.

Evaluation Mode

The Z84C50 has a built-in evaluation mode feature which allows the users to utilize standard Z80 development systems very conveniently. During the power-up reset sequence, if the $\overline{IORQ}$ signal is asserted by the user (input), the Z84C50 enters into an evaluation (or development) mode. The $\overline{IORQ}$ signal must meet the setup and hold times with respect to the rising edge of $\overline{RESET}$. In this mode, the internal CPU is immediately disconnected from the internal bus and all 3-state signals are tri-stated. The tri-stated are: A0-A15, D0-D7, $\overline{HALT}$, $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, $\overline{WR}$, $\overline{M1}$, and $\overline{RFSH}$. This allows the development system CPU to take over and use the internal RAM and I/O registers of the 84C50 like the CPU was on-chip. The wait state generator is utilized as before for external memory accesses only. The 84C50 behaves similarly to the situation where during regular operation, the $\overline{BUSREQ}$ signal is asserted by an external master causing all 3-state signals to be tri-stated by the 84C50 after one clock delay. The $\overline{BUSREQ}$ approach was not used for the evaluation mode to avoid significant external circuitry, in order to work around the one clock delay before the external CPU can use the bus for 84C50 accesses.

Clock Generator/Oscillator

The PLCC and QFP versions of the Z84C50 has a built-in system clock generator for CMOS Z80 in addition to the standard functions of the Z84C00 MPU. The explanation is provided in the following section with emphasis placed on the halt function relative to the clock generator, which is an additional function. The internal register group, reset and interrupt function are identical to those of the Z84C00. For details, please refer to the data sheet for the Z84C00.

Generating the System Clock

The PLCC and QFP versions of the Z84C50 have a built-in oscillation circuit and the required clock can be easily generated by connecting a crystal to the external terminals (XTALI, XTALO). Clock output is the same frequency or half the frequency of the external frequency. Examples of oscillator connections are shown in Figure 5. The values will change with crystal frequency.

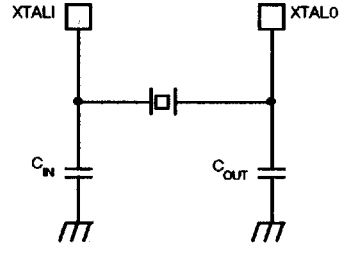


Figure 5a. Example of Oscillator Connection and Constant

C_{IN}	C_{OUT}
22_{PF}	33_{PF}

Figure 5b. Example of Oscillator Connection and Constant

PROGRAMMING

The Z84C50 has two internal 8-bit registers to support its functions. These two registers are called the Control Register and the Memory Page Address register. I/O ports "EE" and "EF" of the Z80 I/O space are allocated for the two registers. The following is a brief description of the software model:

Control Register ("EE")

Bits 1-0. *Memory Wait States.*

00 - No Wait State
01 - 1 Wait State
10 - 2 Wait States
11 - 3 Wait States

On power-on reset, these bits are "11" causing 3 wait states until changed by software.

Bits 3-2. *MS2/MS1 Halt Mode Selection inputs.* One of 4 halt modes is selected as follows:

00 - IDLE1 Mode: Oscillator running, CLK and CPU operations are stopped.

01 - STOP Mode: Oscillator, CLK, and CPU operations are stopped.

10 - IDLE2 Mode: Oscillator and CLK running, CPU operations are stopped.

11 - RUN Mode: CPU continues the operation and supplies clock to the outside.

The detailed operations and timing diagrams for these modes are given elsewhere in this document.

On-power-on reset these bits are "11".

Bit 4. *Clock Divide-by-One Option.* When set to 1, the external clock input on the XTAL pins is divided by 1 as the divided by 2 circuitry is bypassed.

When cleared to 0, the input clock on the XTAL pins is divided by two. The oscillator is used in either case.

When the external system clock is input on the CLK pin, this bit is ignored. Also the on-chip oscillator and divide by two circuits are bypassed.

On Power-on reset, this bit is "0".

Bit 5. *Op Code Fetch Extension Enable.* When set to 1, this bit causes the generation of an additional wait state for external op code fetches. This wait state is in addition to the wait states specified by bits 1-0 for other external memory accesses. On power-on reset, this bit is 1.

Bit 6. *Reset Output Disable.* This bit controls whether the $\overline{\text{RESET}}$ signal is driven out when reset input is used to take the 84C50 out of the "halt" state. $\overline{\text{RESET}}$ pulse is driven out unless this bit is set.

Bit 7. *Unused.* This bit should be set to "0" when writing into this register. When the register is read, this bit is read as "0".

Memory Page Address Register ("EF")

Bits 4-0. *Page Base Address.* These 5 bits select the 2K boundary where the base address of the on-chip 2K RAM is located. This essentially provides the address A15-A11 for the on-chip memory accesses. There are no wait states generated for the on-chip memory accesses. These bits are cleared on reset.

Bit 5. *RAM Enable*

When this bit is set to 1, the on-chip RAM is enabled. This bit is normally "0" on power-up reset except when the $\overline{\text{BUSREQ}}$ precedes the de-assertion of $\overline{\text{RESET}}$.

Bits 6-7. *Unused.*

These bits should be set to "0" when writing to this register. When the register is read, these bits are read as "0".

OPERATION MODES

There are four kinds of operation modes available for the Z84C50 in connection with clock generation; RUN Mode, IDLE1/2 Modes and STOP Mode.

The operation mode is effective when the halt instruction is executed. Restart of MPU from the stopped state under IDLE1/2 Mode or STOP Mode is effected by inputting either $\overline{\text{RESET}}$ or interrupt($\overline{\text{INT}}$ or $\overline{\text{NMI}}$).

Table 3. Clock Generating Operation Modes

Operation Mode	CR(3)	CR(2)	Description at HALT State
Run Mode	1	1	MPU continues the operation and supplies clock to the outside continuously.
IDLE 1 Mode	0	0	The internal oscillator's operation is continued. Clock (CLK) output are as well as internal operations stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.
IDLE 2 Mode	1	0	The internal oscillator's operation and clock (CLK) output are continued but the internal operations are stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.
STOP Mode	0	1	All operations of the internal oscillator, clock (CLK) output, and internal operation are stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.

All of the operating modes listed above are valid with crystal input. For the external clock input on the CLK pin (and 40-pin DIP version); only the IDLE2 and RUN modes are applicable.

Start-up Time at Time of Restart (STOP Mode)

When the MPU is released from the halt state by accepting an interrupt request, it executes an interrupt service routine. Therefore, when an interrupt request is accepted, the MPU starts generating an internal system clock and clock output after a start-up time by the internal counter [(2^{14} +2.5) TcC (TcC: Clock Cycle)] to obtain a stabilized oscillation for MPU operation.

Further, in case of the restart by $\overline{\text{RESET}}$ signal, the internal counter does not operate for a quick operation at time of power-on.

Basic Timing

The basic timing is explained here with emphasis placed on the halt function relative to the clock generator. The following items are identical to those for the Z84C00. Refer to the data sheet for the Z84C00.

Operation code fetch cycle
Memory read/write operation
Input/output operation
Bus request/acknowledge operation
Maskable interrupt request operation
Non-maskable interrupt request operation
Reset operation

Operation When HALT Instruction Is Executed

When the MPU fetches a halt instruction in the operation code fetch cycle, the HALT signal goes active (low) in synchronous with the falling edge of T4 before the peripheral LSI and MPU stops the operation. After this the system clock generating operation after this differs depending upon the operation mode (RUN Mode, IDLE1/2 Mode or STOP Mode). If the internal system clock is running, the MPU continues to execute NOP instructions even in the halt state.

RUN Mode (MS1=1, MS2=1). Shown in Figure 6 is the basic timing when the halt instruction is executed in RUN Mode.

In RUN Mode, system clock (Ø) in MPU and clock output (CLK) are not stopped, even after the halt instruction is executed. Therefore, until the halt state is released by the interrupt signal ($\overline{\text{NMI}}$ or $\overline{\text{INT}}$) or $\overline{\text{RESET}}$ signal, MPU continues to execute NOP instructions.

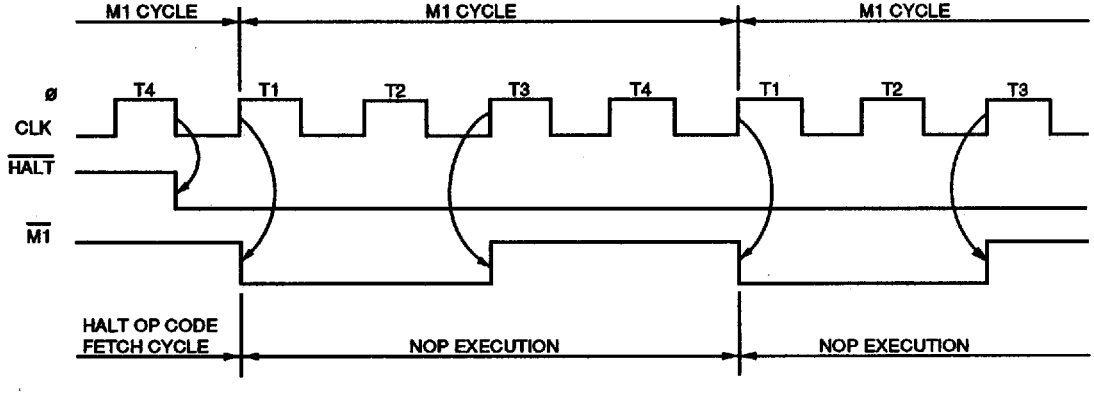


Figure 6. Timing of RUN Mode (at Halt Command Execution)

IDLE1 Mode (MS1=0, MS2=0). Shown in Figure 7 is the basic timing when the halt instruction is executed in IDLE1 Mode.

In IDLE1 Mode, system clock (Ø) in the MPU and clock output (CLK) are stopped, and MPU stops its operation after the halt instruction is executed. However, the internal oscillator continues to operate.

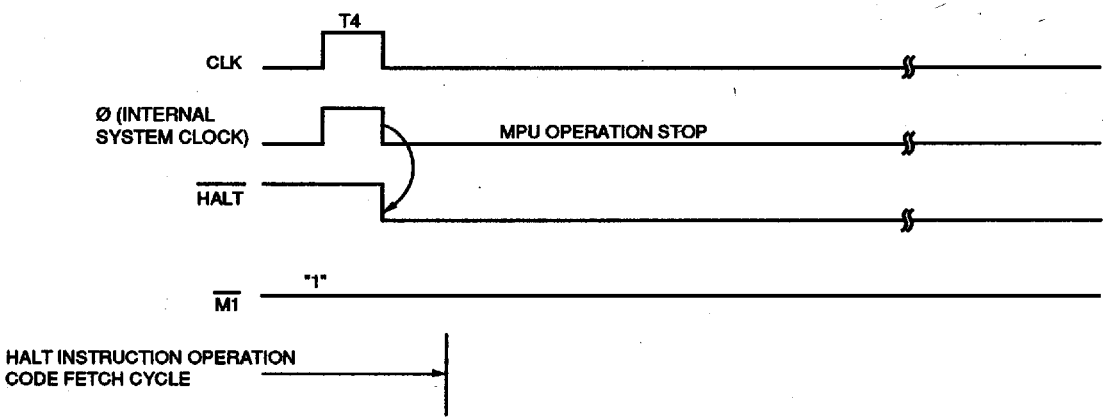


Figure 7. IDLE1 Mode Timing (at Halt Instruction Execution)

IDEL2 Mode (MS1=0, MS2=1). Shown in Figure 8 is the basic timing when the halt instruction is executed in IDLE2 Mode.

In IDLE2 Mode, system clock (Ø) in MPU is stopped and MPU stops its operation after the halt instruction is executed. However, the internal oscillator and clock output (CLK) to the outside of MPU continues to operate.

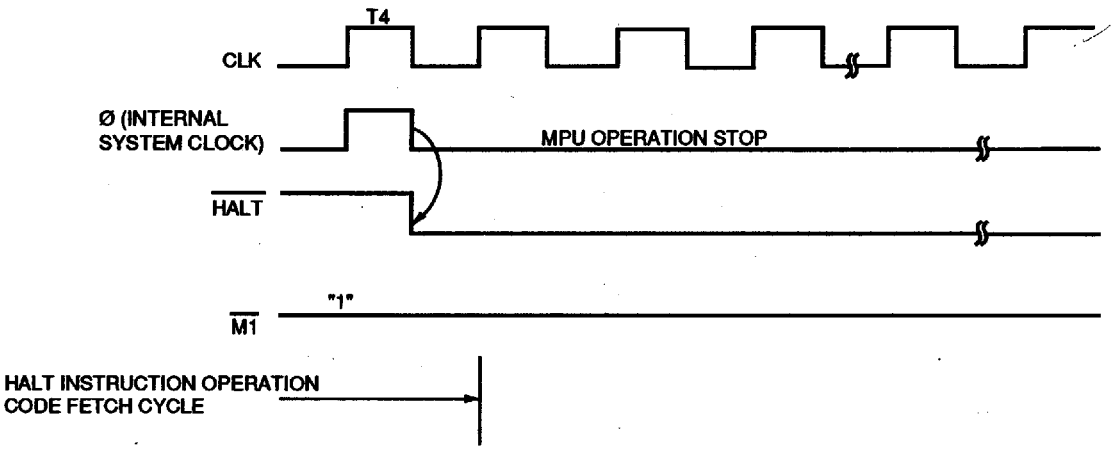


Figure 8. IDLE2 Mode Timing (at Halt Instruction Execution)

STOP Mode (MS1=1, MS2=0). Shown in Figure 9 is the basic timing when the halt instruction is executed in STOP Mode.

In STOP Mode, internal operation and the internal oscillator are stopped after the halt instruction is executed. Therefore, system clock (Ø) in the MPU and clock output (CLK) external to the MPU, are stopped.

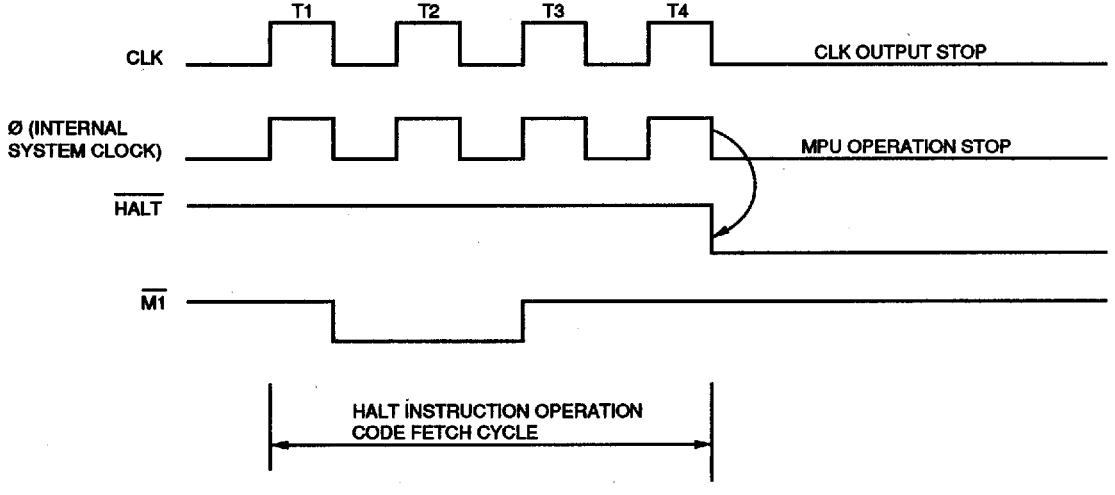


Figure 9. Stop Mode Timing (at Halt Instruction Execution)

Release from Halt State

The halt state of MPU is released when "0" is input to RESET signal and MPU is reset or an interrupt request is accepted. An interrupt request signal is sampled at the leading edge of the last clock cycle (T4 state) of NOP instruction. In case of the maskable interrupt, interrupt will be accepted by an active INT signal ("0" level). Also the interrupt enable flip-flop must have been set to "1". The accepted interrupt process is started from the next cycle.

Further, when the internal system clock is stopped (IDLE1/2 Mode, STOP Mode), it is necessary to first restart the internal system clock. The internal system clock is restarted when RESET or the interrupt signal (NMI or INT) is asserted.

RUN Mode (MS1, MS2=1). The halt release operation by acceptance of interrupt request in RUN Mode is shown in Figure 10.

In RUN Mode the internal system clock is not stopped, and therefore, if the interrupt signal is recognized at the rise of T4 state of the continued NOP instruction, MPU will execute the interrupt process from the next cycle.

The halt release operation, by resetting MPU in RUN Mode, is shown in Figure 11. After reset, MPU will execute an instruction starting from address 0000H. However, in order to reset MPU, it is necessary to keep RESET signal at "0" for a least 3 clocks. In addition, if RESET signal becomes "1", after the dummy cycle for at least two T states, MPU executes an instruction from address 0000H.

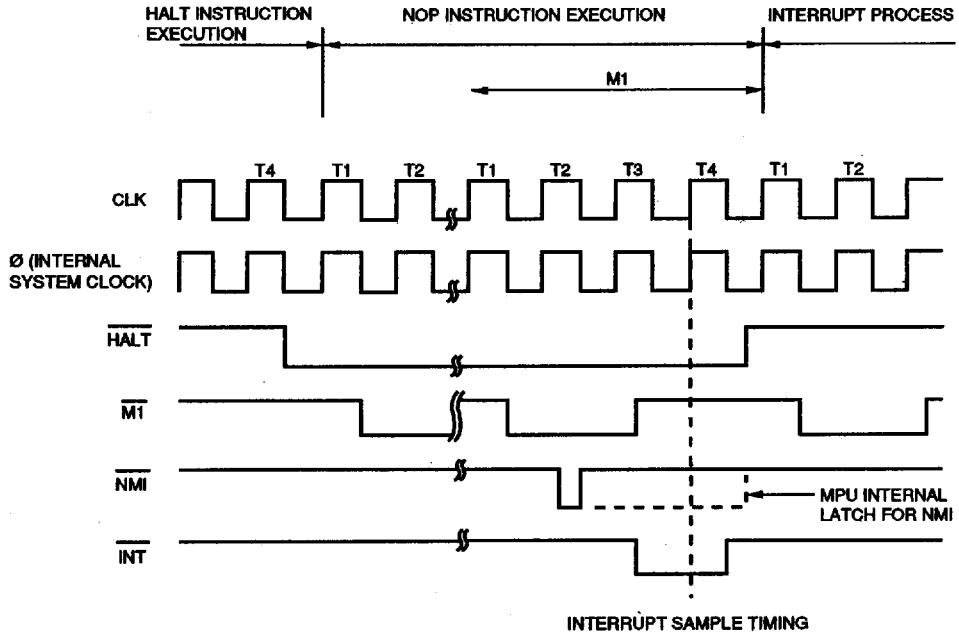


Figure 10. Halt Release Operation Timing by Interrupt Request Signal in RUN Mode

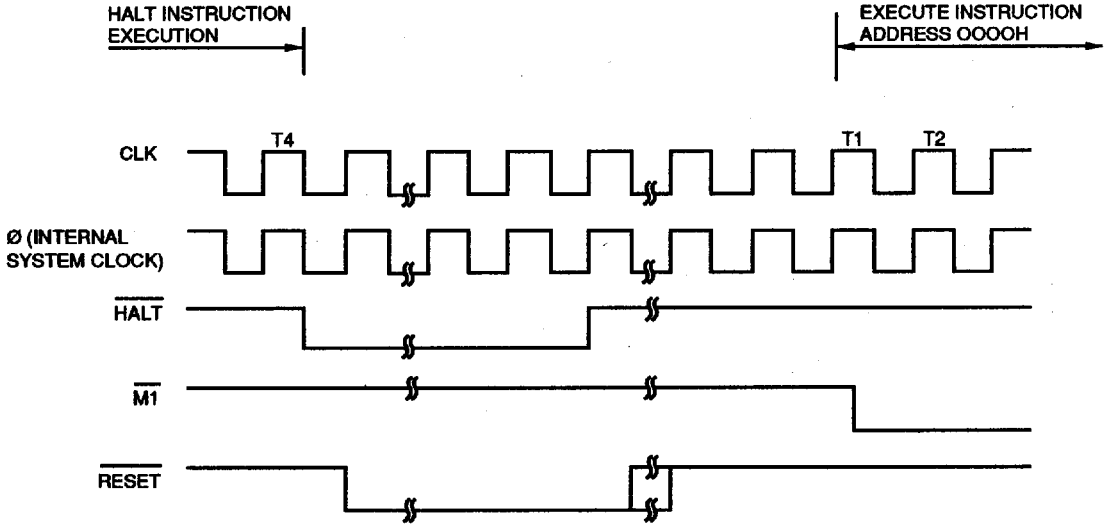


Figure 11. Halt Release Operation Timing by reset in RUN Mode

IDLE1 Mode (MS1=0, MS2=0), IDLE2 Mode (MS1=0, MS2=1). The halt release operation by interrupt signal in IDLE1 Mode is shown in Figure 12 (a) and in IDLE2 Mode in Figure 12 (b).

When receiving $\overline{NMI}$ or $\overline{INT}$ signal, MPU starts the internal system clock operation. In IDLE1 Mode, MPU starts clock output to the outside at the same time.

The operation stop of MPU in IDLE/2 Mode is taking place at "0" level during T4 state in the halt instruction operation code fetch cycle. Therefore, after being restarted by the interruption signal, MPU executes one NOP instruction and samples an interrupt signal at the rise of T4 state during the execution of this NOP instruction, and executes the interrupt process from next cycle.

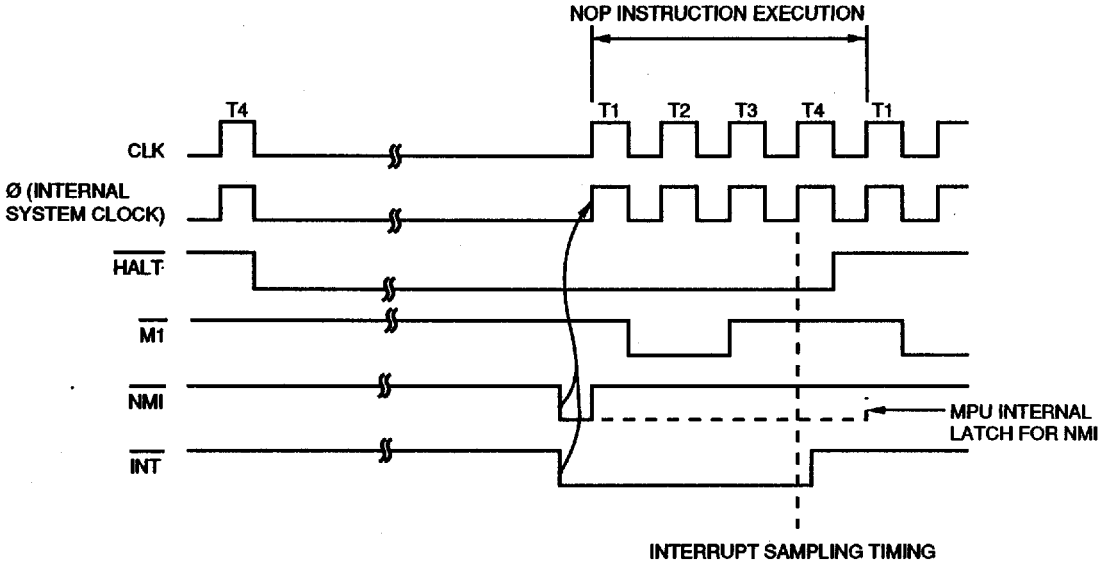


Figure 12. (a) IDLE1 Mode

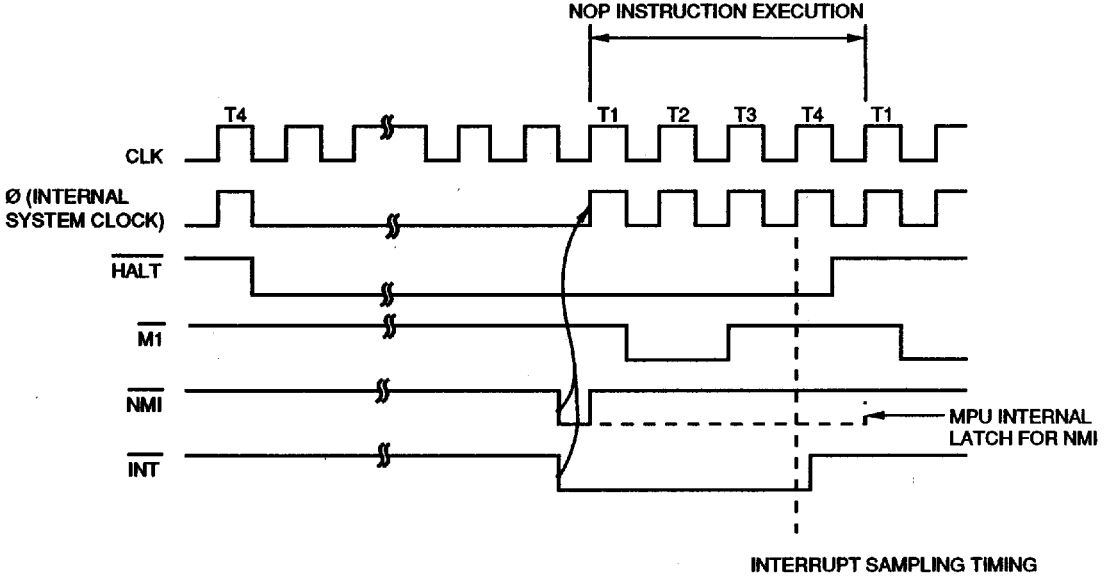


Figure 12. (b) IDLE2 Mode

Figure 12. Halt Release Operation Timing by Interrupt Request Signal in IDLE1/2 Mode

If no interrupt signal is accepted during the execution of the first NOP instruction after the internal system clock is restarted, MPU is not released from the halt state and is placed in IDLE1/2 Mode again at "0" level during T4 state of the NOP instruction, stopping the internal system clock. If INT signal is not at "0" level at the rise of T4 state, no interrupt request is accepted.

The halt release operation, by resetting MPU in IDLE1 Mode, is shown in Figure 13 (a) and that in IDLE2 Mode in Figure 13 (b).

When the $\overline{RESET}$ signal at "0" level is input into MPU, the internal system clock is restarted and MPU will execute an instruction stored in address 0000H.

At the time of $\overline{RESET}$ signal input, it is necessary to take the same care as that in resetting MPU in RUN Mode.

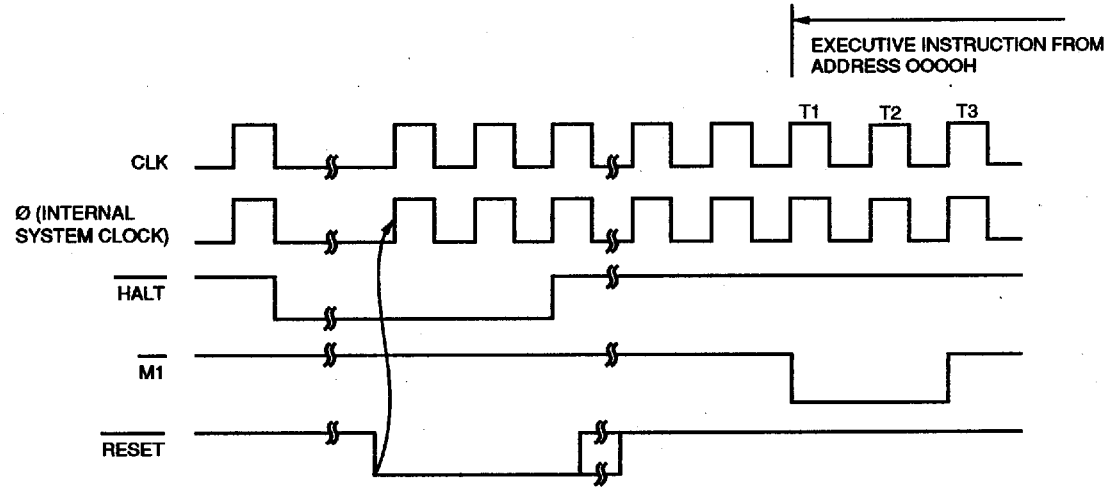


Figure 13. (a) IDLE1 Mode

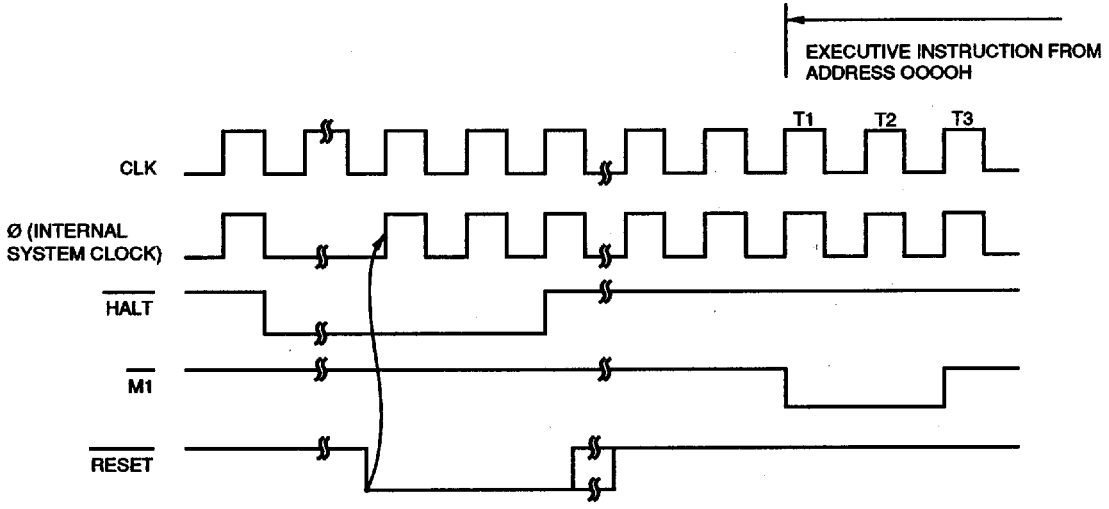


Figure 13. (b) IDLE2 Mode

Figure 13. Halt Release Operation Timing by Reset in IDLE1/2 Mode

STOP Mode (MS1=1, MS2=0). The halt release operation by interrupt signal in STOP Mode is shown in Figure 14.

When MPU receives an interrupt signal, the internal oscillator is restarted. In order to obtain stabilized oscillation, the internal system clock and clock output to the outside are started after a start-up time of [(2^{14} +2.5) TcC (TcC: Clock Cycle)] by the internal counter.

MPU executes one NOP instruction after the internal system clock is restarted and at the same time, sampling an interrupt signal at the rise of T4 state during the execution of this NOP instruction. If the interrupt signal is accepted, MPU executes the interrupt process operation from next cycle.

At time of interrupt signal input, it is necessary to take the same care as that in the interrupt signal input in IDLE1/2 Mode. The halt release operation by MPU resetting in STOP Mode is shown in Figure 15.

When the $\overline{\text{RESET}}$ signal at "0" level is input into MPU, the internal oscillator is restarted. However, since it performs a quick operation at time of power-on, the internal counter does not operate. Therefore, the operation may not be carried out properly due to an unstable clock immediately after the signal in STOP Mode. Thus, it is necessary to hold the $\overline{\text{RESET}}$ signal at "0" level for sufficient time. In the 84C50, the external $\overline{\text{RESET}}$ signal requirements are the same as in the power-up reset. Internally, the reset pulse is stretched by 2^{14} +16 cycles to allow the oscillator to settle down. This elongated reset signal is driven out of the 84C50 on the reset pin if bit 6 of the control register has not been set. Setting bit 6 disables the driving out of reset.

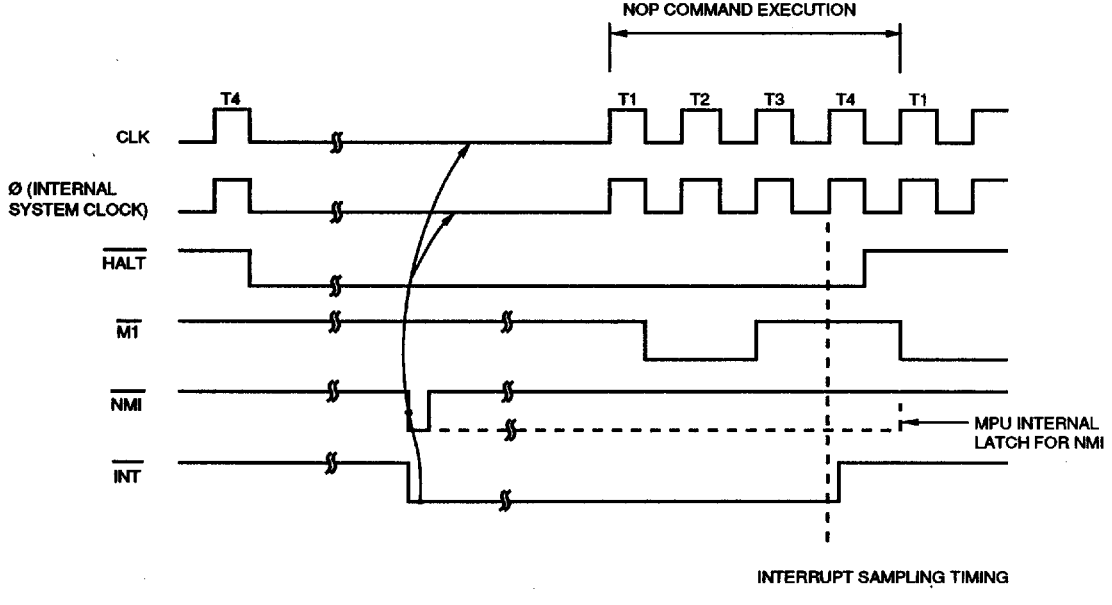


Figure 14. Halt Release Operation Timing by Interrupt Request Signal in STOP Mode

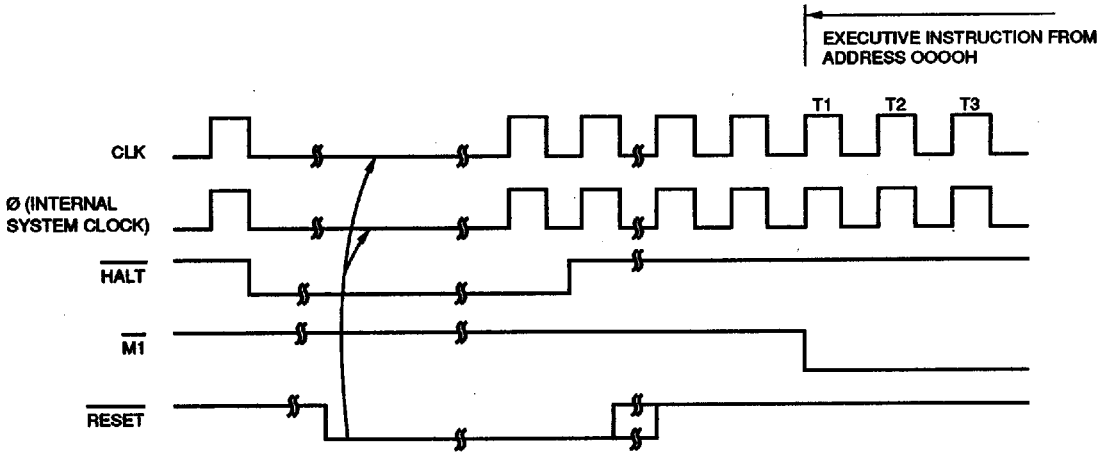


Figure 15. Halt Release Operation Timing by reset in STOP Mode

Instruction Set

Instruction set of the Z84C50 is the same as that for the Z84C00. For details refer to the data sheet for the Z84C00.

CPU TIMING

Timing Diagrams. The Z84C50 CPU executes instructions by proceeding through a specific sequence of operations:

- Memory read or write
- I/O device read or write
- Interrupt acknowledge

The basic clock period is referred to as a Time or Cycle, and three or more T cycles make up a machine cycle (M1, M2 or M3 for instance). Machine cycles can be extended either by the CPU automatically inserting one or more Wait states or by the insertion of one or more Wait states by the user.

Instruction Opcode Fetch. The CPU places the contents of the Program counter (PC) on the address bus at the start of the cycle (Figure 16). Approximately one-half clock cycle later, $\overline{MREQ}$ goes active. When active, $\overline{RD}$ indicates that the memory data can be enabled onto the CPU data bus.

The CPU samples the $\overline{WAIT}$ input with the falling edge of clock state T2. During clock states T3 and T4 of an $\overline{M1}$ cycle, dynamic RAM refresh can occur while the CPU starts decoding and executing the instruction.

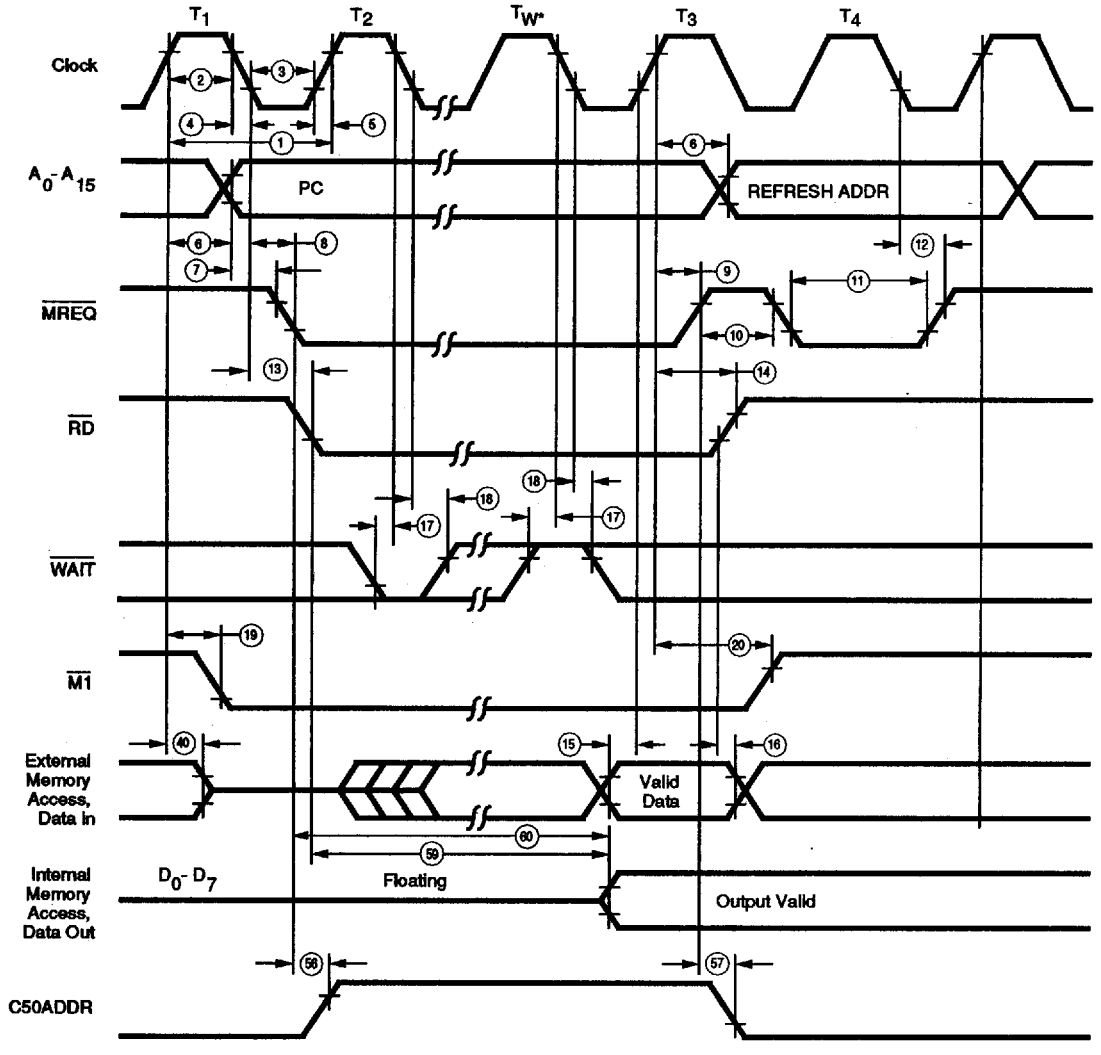


Figure 16. Instruction Op code Fetch

Memory Read or Write Cycles. Figure 17 shows the timing of memory read or write cycles other than an opcode fetch (M1) cycle. The $\overline{MREQ}$ and $\overline{RD}$ signals function exactly as in the fetch cycle.

In a memory write cycle, $\overline{MERQ}$ also becomes active when the address bus is stable. The $\overline{WR}$ line is active when the data bus is stable, so that it can be used directly as an R/$\overline{W}$ pulse to most semiconductor memories.

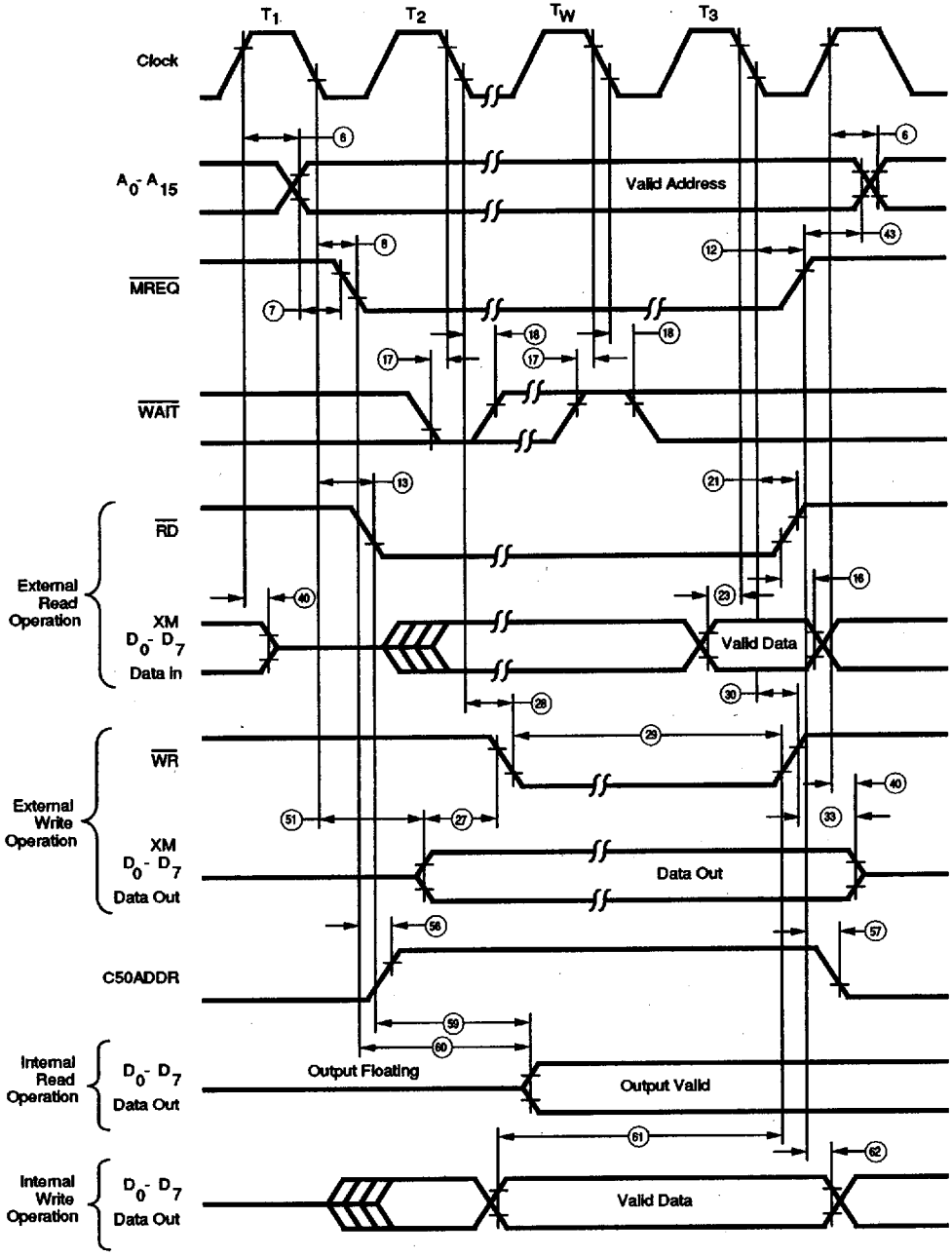


Figure 17. Memory Read or Write Cycles

Input or Output Cycles. Figure 18 shows the timing for an I/O read or I/O write operation. During I/O operation, the CPU automatically inserts a single Wait state (T_{WA}). This extra Wait state allows sufficient time for an I/O port to decode the address from the port address lines.

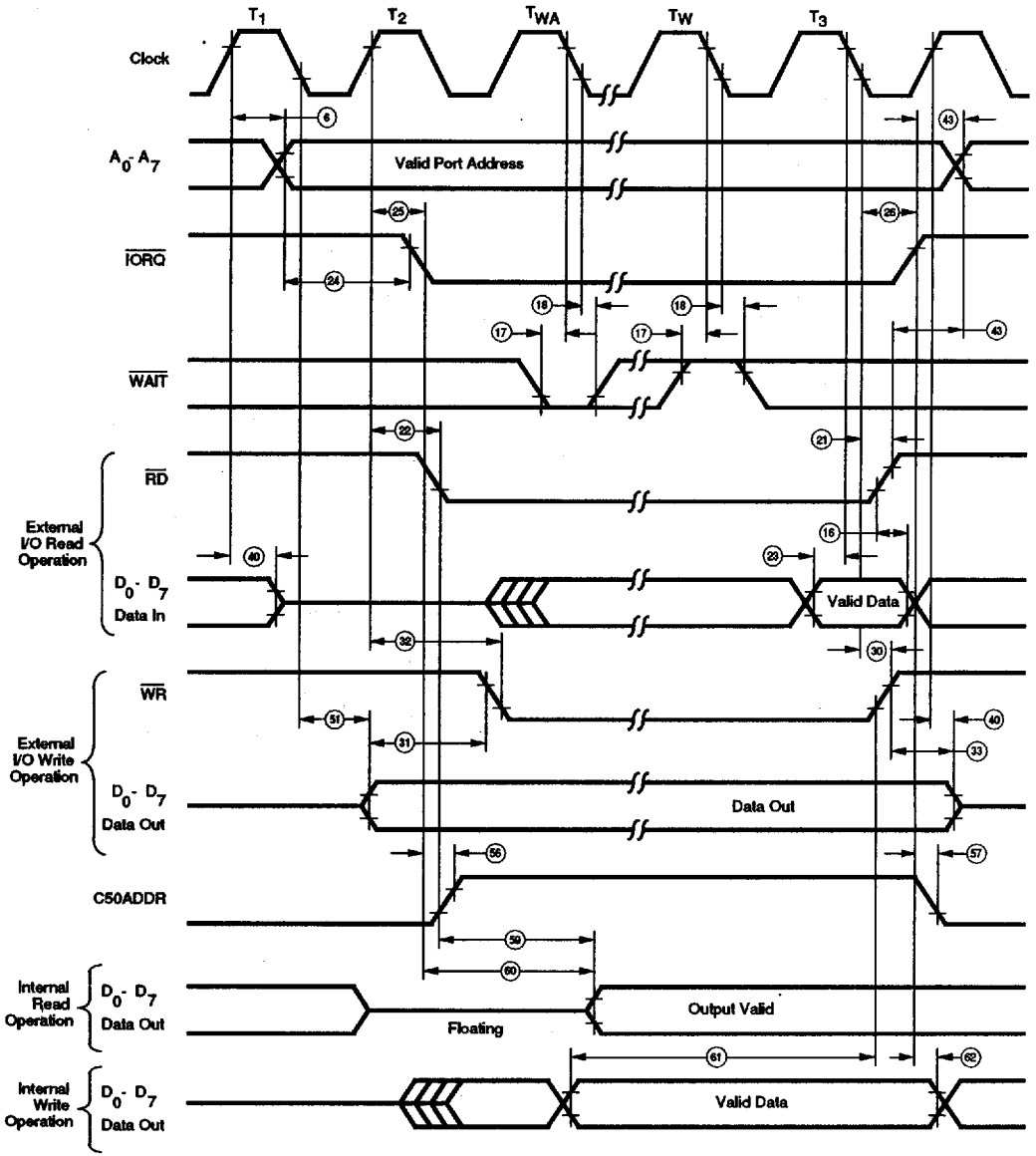
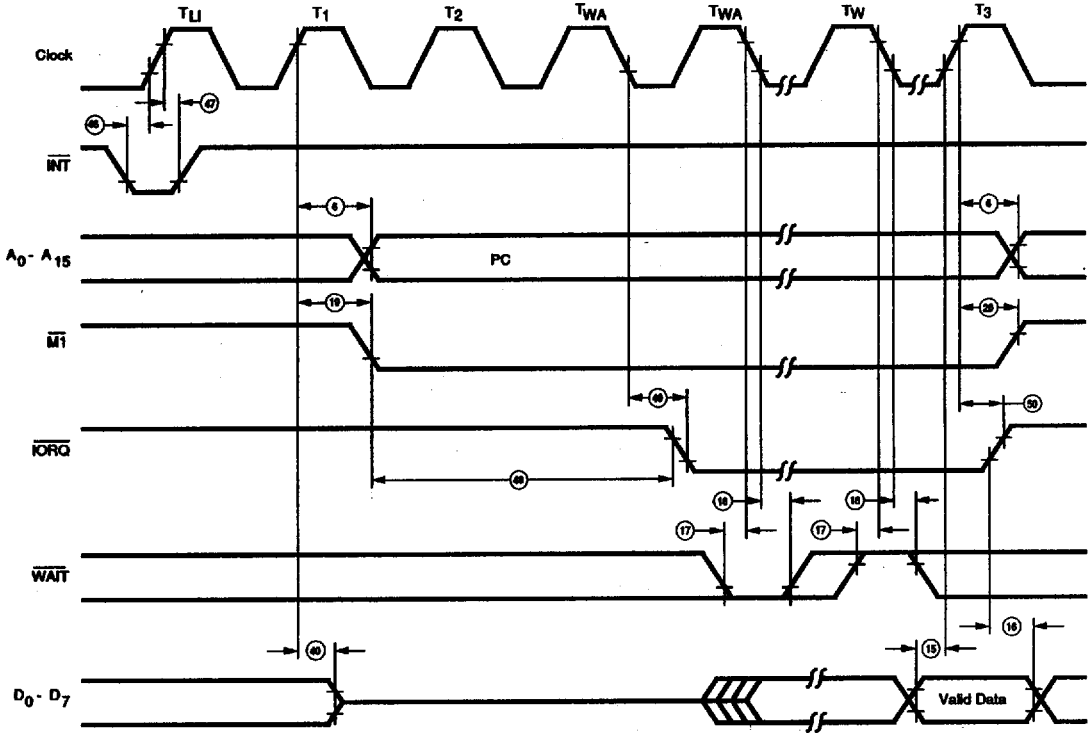


Figure 18. Input or Output Cycles

Interrupt Request/Acknowledge Cycle. The CPU samples the interrupt signal with the rising edge of the last clock cycle at the end of any instruction (Figure 19). When an interrupt is accepted, a special $\overline{M1}$ cycle is generated. During this $\overline{M1}$ cycle, $\overline{IORQ}$ becomes active (instead of $\overline{MREQ}$) to indicate that the interrupting device can place an 8-bit vector on the data bus. The CPU automatically adds two Wait states to this cycle.

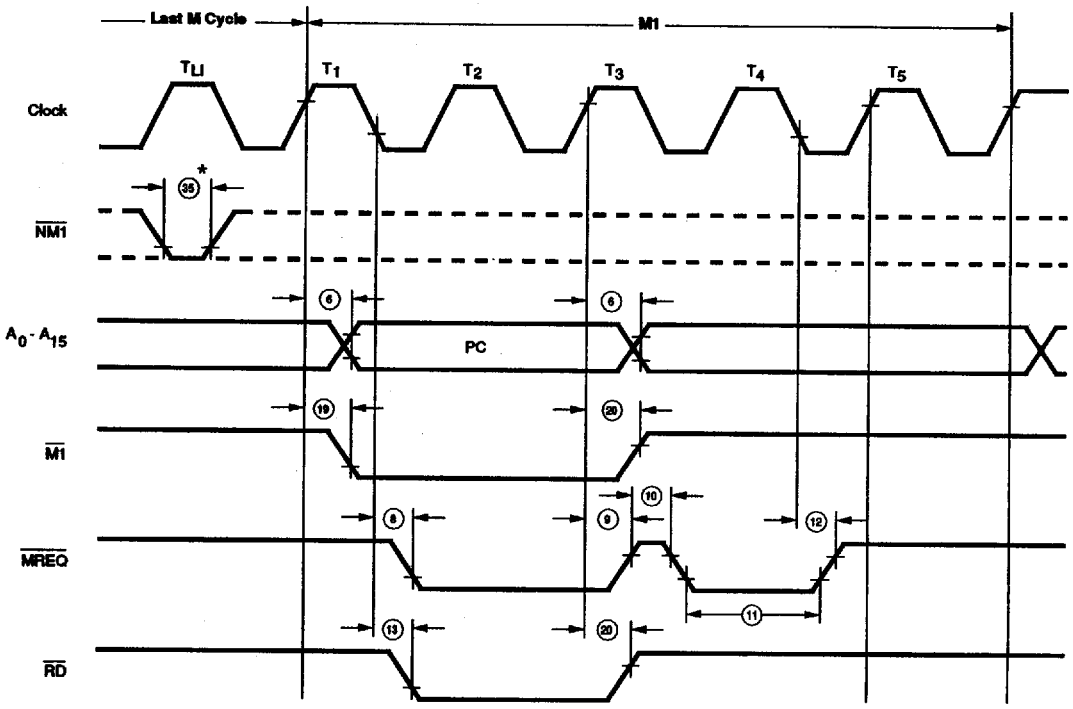


NOTE: 1) T_{LI} = Last state of any instruction cycle.

2) T_{WA} = Wait cycle automatically inserted by CPU.

Figure 19. Interrupt Request/Acknowledge Cycle

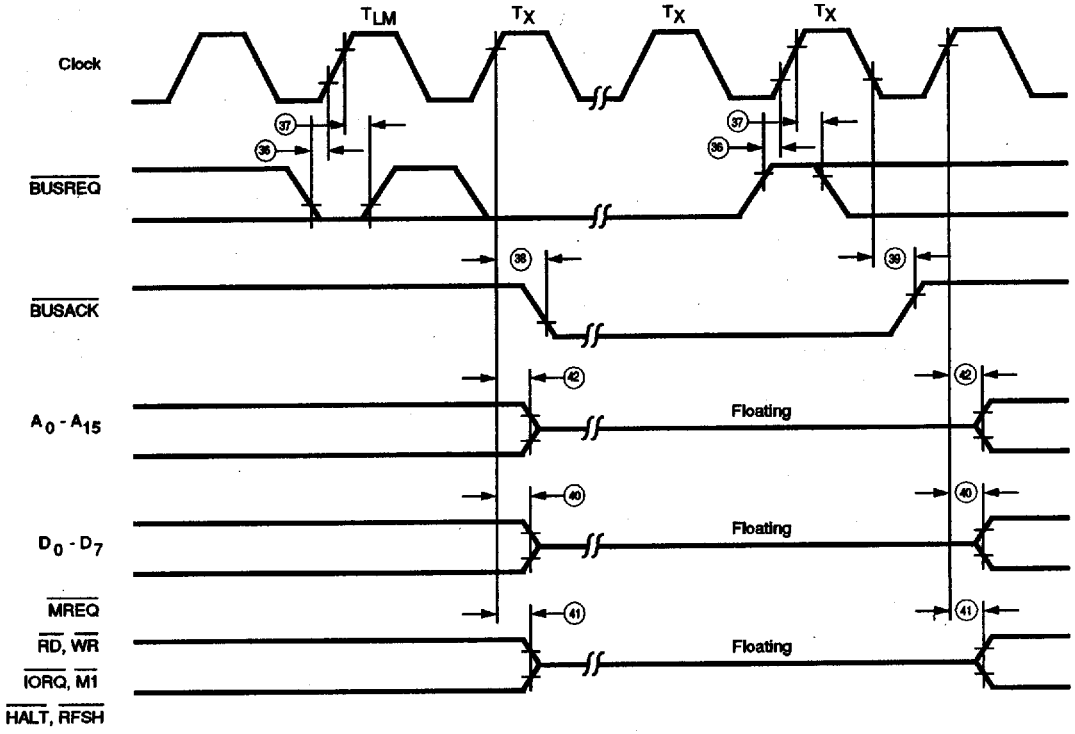
Non-Maskable Interrupt Request Cycle. NMI is sampled at the same time as the maskable interrupt input INT, but has higher priority and cannot be disabled under software control. The subsequent timing is similar to that of a normal memory read operation except that data put on the bus by the memory is ignored. The CPU instead executes a restart (RST) operation and jumps to the NMI service routine located at address 0066H (Figure 20).



* Although $\overline{NMI}$ is an asynchronous input, to guarantee its being recognized on the following machine cycle, $\overline{NMI}$'s falling edge must occur no later than the rising edge of the clock cycle preceding the last state of any instruction cycle (T_{LI}).

Figure 20. Non-Maskable Interrupt Request Operation

Bus Request/Acknowledge cycle. The CPU samples $\overline{BUSREQ}$ with the rising edge of the last clock period of any machine cycle (Figure 21). If $\overline{BUSREQ}$ is active, the CPU sets its address, data, and $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ lines to a high-impedance state with the rising edge of the next clock pulse. At that time, any external device can take control of these lines, usually to transfer data between memory and I/O devices.



Notes: 1) T_{LM} = Last state of any M cycle.

2) T_X = An arbitrary clock cycle used by requesting device.

Figure 21. BUS Request/Acknowledge Cycle

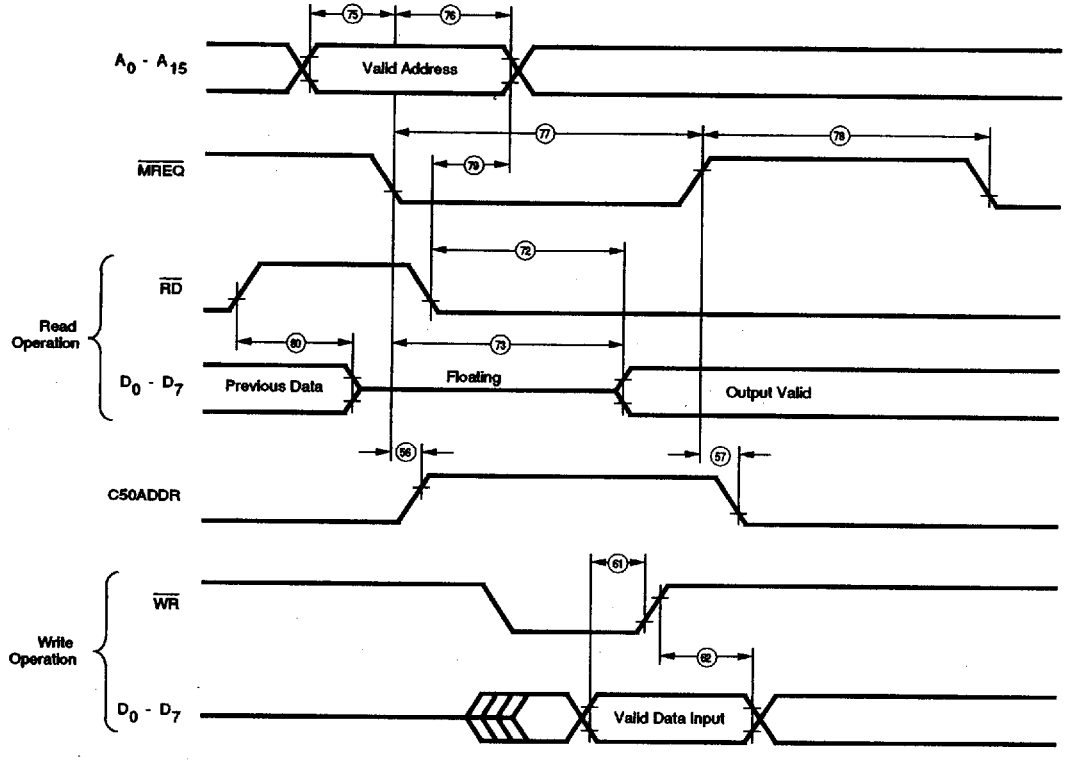


Figure 22(a). Bus Acknowledge Timing for Internal Memory Read or Write Cycles

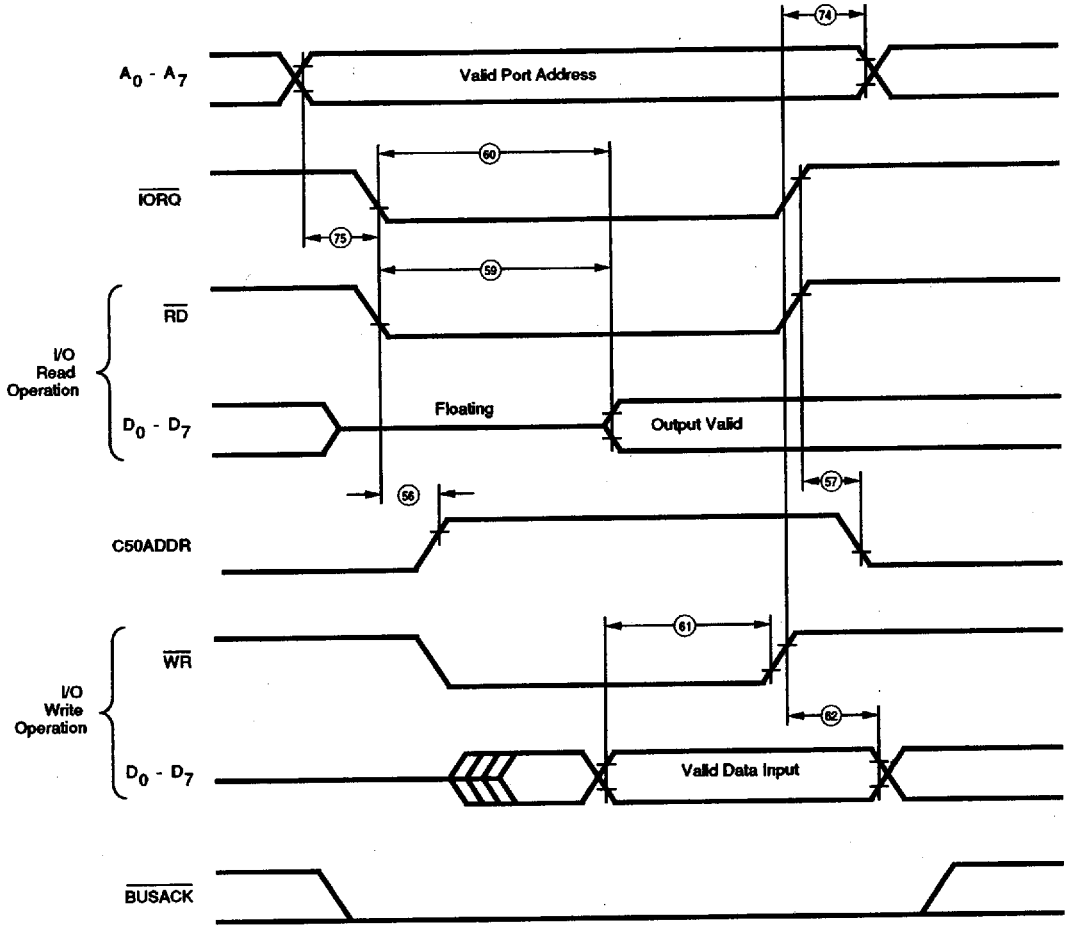
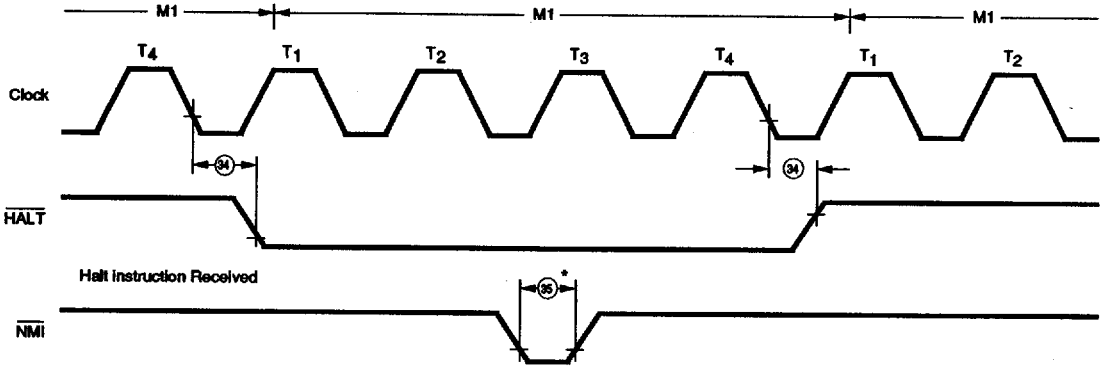


Figure 22(b). Bus Acknowledge Timing for Internal I/O Cycles

Halt Acknowledge Cycle.



* Although NMI is an asynchronous input, to guarantee its being recognized on the following machine cycle, NMI's falling edge must occur no later than the rising edge of the clock cycle preceding the last state of any instruction cycle (T_{Li}).

Figure 23. Halt Acknowledge

Reset Cycle. $\overline{RESET}$ must be active for at least three clock cycles for the CPU to properly accept it. As long as $\overline{RESET}$ remains active, the address and data buses float, and the control outputs are inactive.

Once $\overline{RESET}$ goes inactive, two internal T cycles are consumed before the CPU resumes normal precessing operation. $\overline{RESET}$ clears the PC register, so the first op-code fetch will be location 0000H (Figure 24).

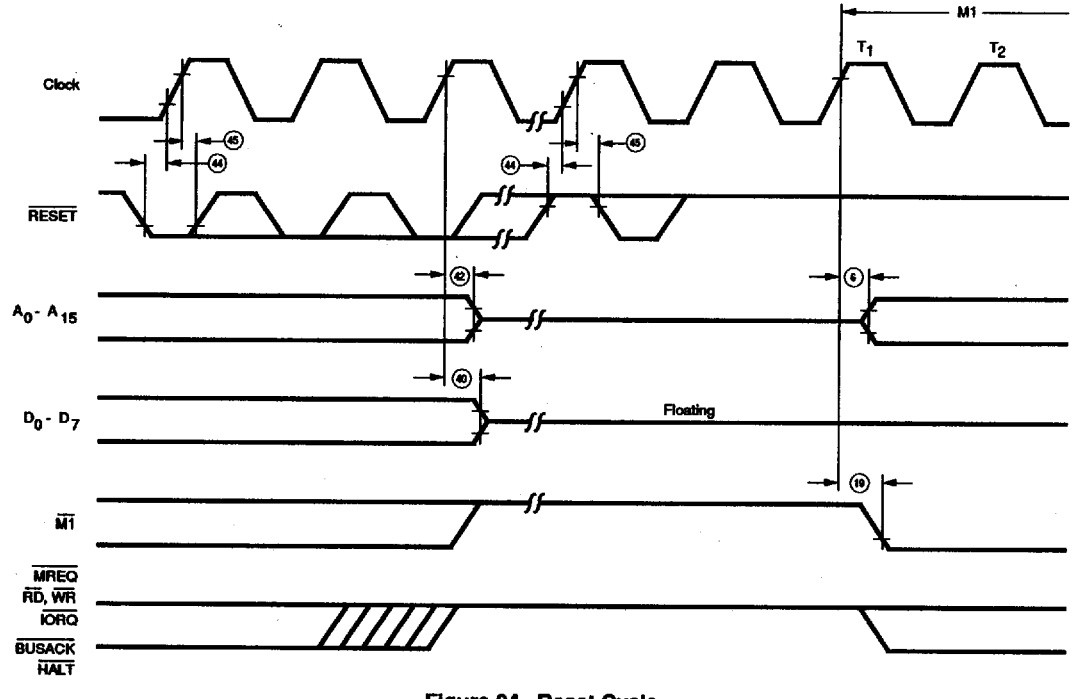


Figure 24. Reset Cycle

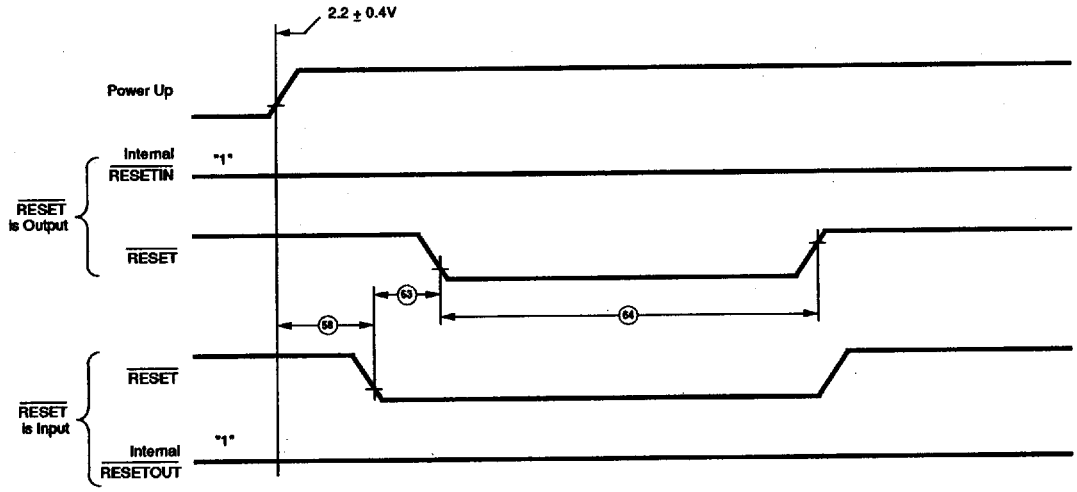


Figure 25. Reset on Power -Up

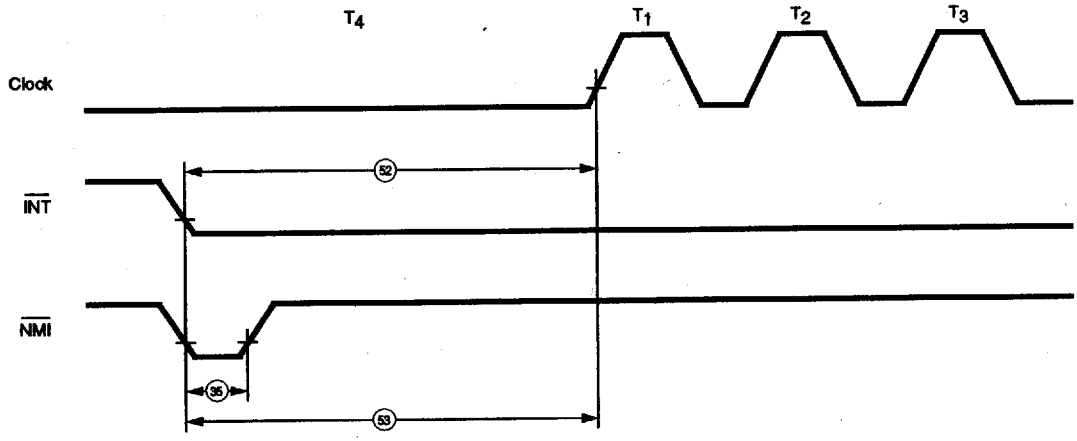


Figure 26. Clock Restart Timing
(STOP Mode)

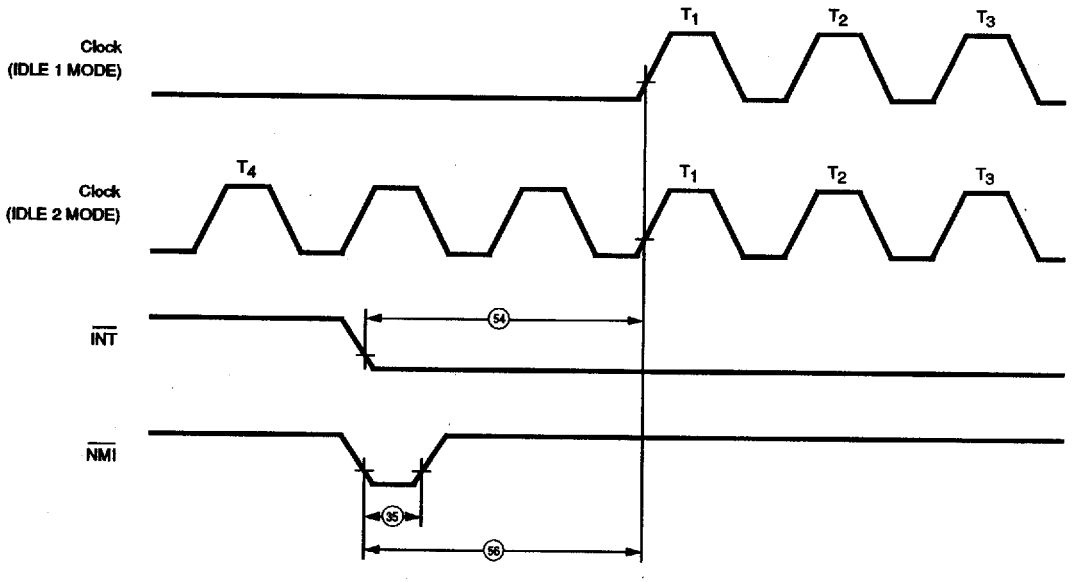


Figure 27. Clock Restart Timing (IDLE1/2 Mode)

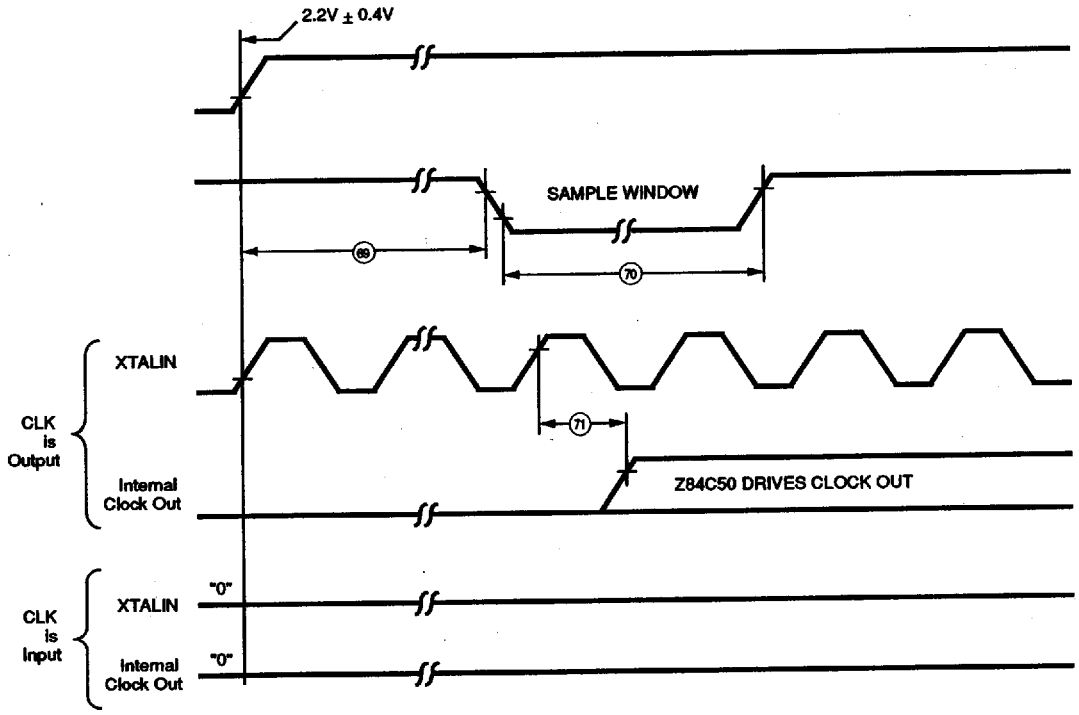


Figure 28. XTALIN Test on Power-up

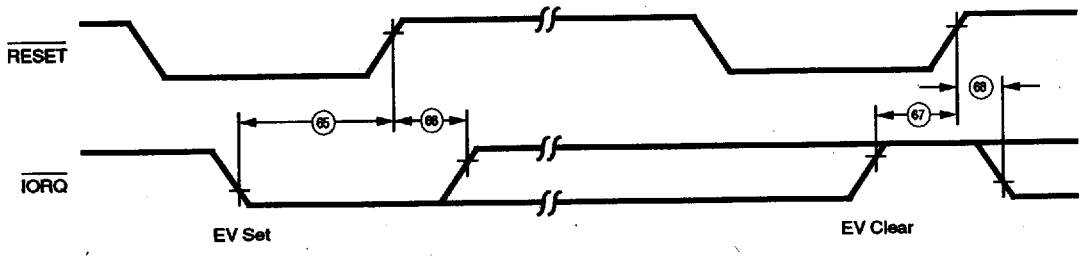


Figure 29. Set/Clear EV During Reset

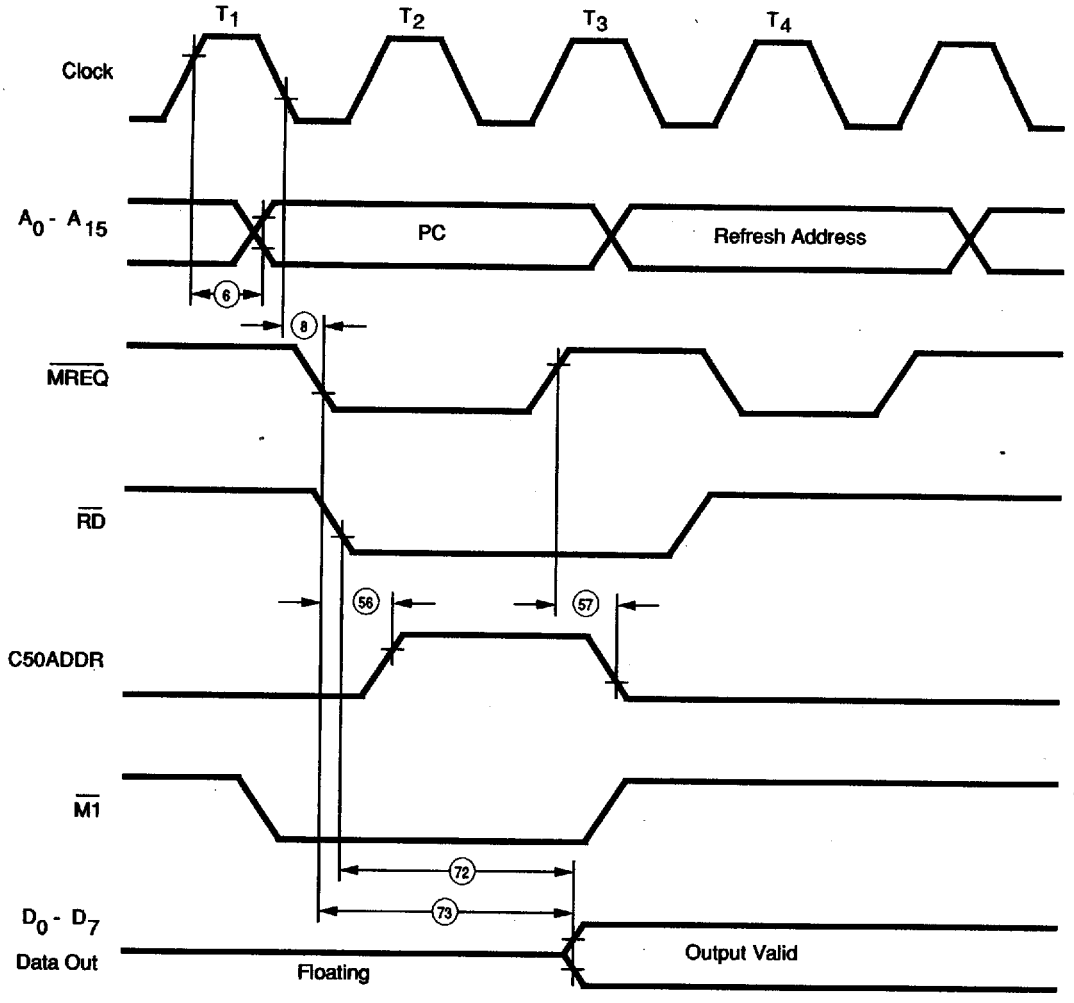


Figure 30. EV Mode Internal Instruction Op-Code Fetch

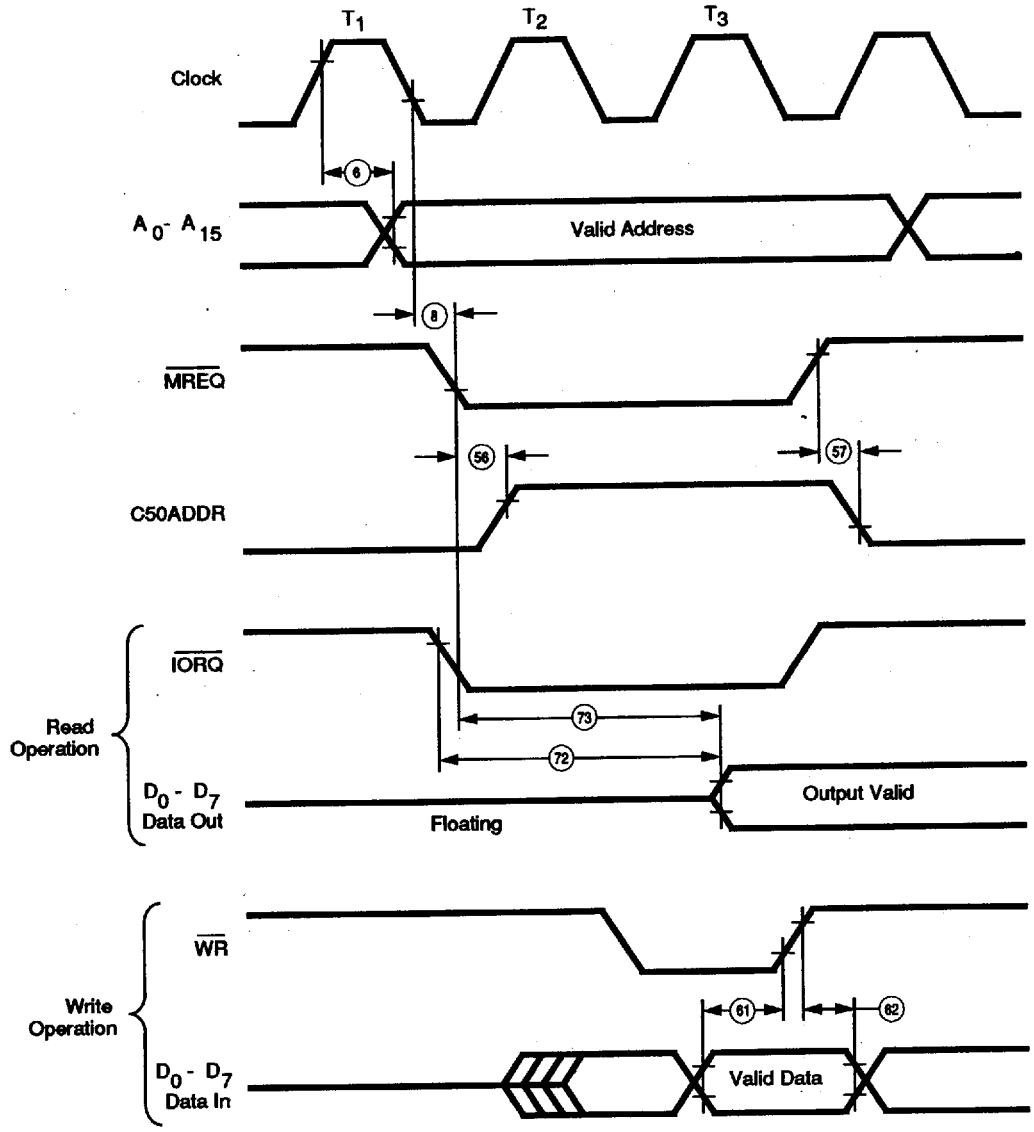


Figure 31. EV Mode Internal Memory Read or Write Cycles

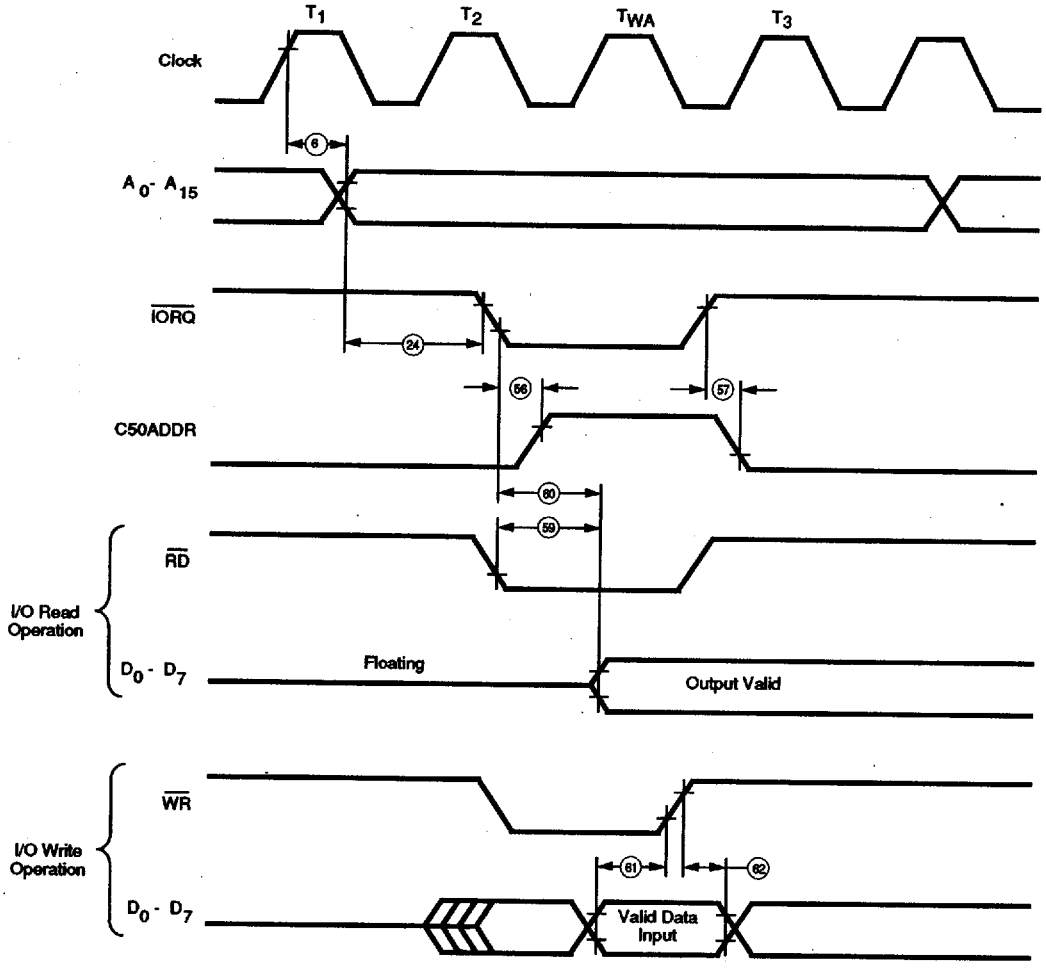


Figure 32. EV Mode Internal I/O Cycles

PRECAUTIONS

To reset the MPU, is is necessary to hold the $\overline{\text{RESET}}$ signal input at "0" level for at least three clocks.

In particular, to release the HALT state by the $\overline{\text{RESET}}$ signal in STOP Mode, hold $\overline{\text{RESET}}$ signal at "0" level for sufficient time in order to stabilize output from the internal oscillator.

In releasing the MPU from the HALT state by interrupt signal in IDLE1/2 Mode and STOP Mode, the MPU will not be released from the HALT state. Also, the internal system clock will stop again unless an interrupt signal is accepted during the execution of an NOP instruction ,even when the internal system clock is restarted by the interrupt signal input. Care must be taken when $\overline{\text{INT}}$ is used.

Other precautions are identical to those for the Z84C00. Refer to the data sheet for the Z84C00.

AC CHARCTERISTICS

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V +/- 10%, VSS = 0V.

No	Symbol	Parameter	Min	Max	Unit
1	TcC	Clock cycle time	100	DC	ns
2	TwCh	High clock pulse width	40	DC	ns
3	TwCl	Low clock pulse width	40	DC	ns
4	TfC	Clock falling time		10	ns
5	TrC	Clock rising time		10	ns
6	TdCr (A)	Effective address output delay from clock rise		60	ns
7	TdA (MREQf)	Address output definite time prior to $\overline{MREQ}$	**		ns
8	TdCf (MREQf)	Delay from clock fall to $\overline{MREQ}$ = 'L'		55	ns
9	TdCf (MREQr)	Delay from clock rise to $\overline{MREQ}$ = 'H'		55	ns
10	TwMREQh	$\overline{MREQ}$ high level pulse width	**		ns
11	TwMREQl	$\overline{MREQ}$ low level pulse width	**		ns
12	TdCf (MREQr)	Delay from clock fall to $\overline{MREQ}$ = 'H'		55	ns
13	TdCf (RDf)	Delay from clock fall to $\overline{RD}$ = 'L'		65	ns
14	TdCr (RDr)	Delay from clock rise to $\overline{RD}$ = 'H'		55	ns
15	TsD (Cr)	Data set-up time for Clock rise	25		ns
16	ThD (RDr)	Data hold time for $\overline{RD}$ rise	0		ns
17	TsWAIT (Cf)	Wait signal set-up time for clock fall	20		ns
18*	ThWAIT (Cf)	Wait hold time after clock fall	10		ns
19	TdCr (Mif)	Delay from clock rise to $\overline{M1}$ = 'L'		65	ns
20	TdCr (Mir)	Delay from clock rise to $\overline{M1}$ = H'		65	ns
21	TdCf (RDr)	Delay from clock fall to $\overline{RD}$ = 'H'		55	ns
22	TdCr (RDF)	Delay from clock rise to $\overline{RD}$ = 'L'		55	ns
23	TsD (Cf)	Data set-up time for clock fall	40		ns
24	TdA (IORQf)	Address definite time prior to $\overline{IORQ}$ fall	**		ns
25	TdCr (IORQf)	Delay from clock rise to $\overline{IORQ}$ = 'L'		50	ns
26	TdCf (IORQr)	Delay from clock fall to $\overline{IORQ}$ = 'H'		55	ns
27	TdD (WRF)	Data definite time prior to $\overline{WR}$ fall	**		ns
28	TdCf (WRF)	Delay from clock fall to $\overline{WR}$ = 'L'		55	ns
29	TwWR	WR pulse width	**		ns
30	TdCf (WRr)	Delay from clock fall to $\overline{WR}$ = 'H'		55	ns
31	TdD (WRf)	Data definite time prior to $\overline{WR}$ fall	**		ns
32	TdCr (WRf)	Delay from clock rise to $\overline{WR}$ = 'L'		50	ns
33	TdWRr (D)	Output data holding after $\overline{WR}$ = 'H'	**		ns
34	TdCf (HALT)	Delay from clock fall to $\overline{HALT}$ = 'L' or 'H'		100	ns
35	TwNMI	$\overline{NMI}$ pulse width	60		ns
36	TsBUSREQ (Cr)	Set-up time for clock rise	35		ns
37*	ThBUSREQ (Cr)	$\overline{BUSREQ}$ hold time after clock rise	15		ns
38	TdCr (BUSACKf)	Time from clock rise to $\overline{BUSACK}$ = 'L'		75	ns
39	TdCf (BUSACKr)	Time from clock fall to $\overline{BUSACK}$ = 'H'		75	ns
40	TdCr (Dz)	Delay from clock rise to data bus float state		65	ns

AC CHARACTERISTICS (Continued)

No	Symbol	Parameter	Min	Max	Unit
41	TdCr (CTz)	Delay from clock rise to control output float state ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, $\overline{WD}$)		60	ns
42	TdCr (Az)	Delay from clock rise to address bus float state		75	ns
43	TdCTr (A)	Address hold time from $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, or $\overline{WR}$	**		ns
44	TsRESET (Cr)	$\overline{RESET}$ set-up time for clock rise	40		ns
45*	ThRESET (Cr)	$\overline{RESET}$ hold time for clock rise	15		ns
46	TsINTf (Cr)	$\overline{INT}$ set-up time for clock rise	50		ns
47*	ThINTr (Cr)	$\overline{INT}$ hold time after clock rise	15		ns
49	TdCf (IORQf)	Delay from clock fall to $\overline{IORQ}$ = 'L'		55	ns
50	TdCr (IORQr)	Delay from clock rise to $\overline{IORQ}$ = 'H'		55	ns
51	TdCf (D)	Delay from clock fall to data output		110	ns
52	TRST1S	Clock (CLK) restart time by $\overline{INT}$ (STOP mode)	(typ)(2^{14}+2.5)xTcC		ns
53	TRST2S	Clock (CLK restart time by $\overline{NMI}$ (STOP mode)	(typ)(2^{14}+2.5)xTcC		ns
54	TRST1I	Clock (CLK) restart time by $\overline{INT}$ (IDLE1/2 mode)	(typ) 2.5 TcC		ns
55	TRST2I	Clock (CLK) restart time by $\overline{NMI}$ (IDLE1/2 mode)	(typ) 2.5 TcC		ns
56	TdMIf (C50ADDRy)	Delay from $\overline{MREQ}$ or $\overline{IORQ}$ falling to C50ADDR = 'H'		35	ns
57	TdMIr (C50ADDRf)	Delay from $\overline{MREQ}$ or $\overline{IORQ}$ rising to C50ADDR = 'L'		30	ns
58	TRESETi	$\overline{RESET}$ input test range	50	150	µs
59	TRDf (D)	$\overline{RD}$ falling to output data valid		60	ns
60	TMI (D)	$\overline{IORQ}$ or $\overline{MREQ}$ falling to output data valid		70	ns
61	TsD (WRr)	Data set-up time prior to $\overline{WR}$ rising	30		ns
62	ThD (WRr)	Data hold time after $\overline{WR}$ rising	5		ns
63	Td RESET	$\overline{RESETIN}$ falling to $\overline{RESETOUT}$ delay		50	ns
64	Tw RESET	Automatic Power-up pulse width	25	75	ms
65	Td IORQf (RESETr)	$\overline{IORQ}$ set-up time before $\overline{RESET}$ rising to set EV mode	15		ns
66	ThRESETr (IORQf)	$\overline{IORQ}$ hold time from $\overline{RESET}$ rising to EV mode	10		ns
67	Tc IORQr (RESETr)	$\overline{IORQ}$ set-up time before $\overline{RESET}$ rising to clear EV mode	15		ns
68	TcRESETr (IORQf)	$\overline{IORQ}$ hold time from $\overline{RESET}$ rising to clear EV mode	10		ns
69	Ts XTALIN	XTALIN sampling start time	15	45	ms
70	TwXTALIN	XTALIN sampling window duration	10	30	ms
71	TCr (CLK)	Clock rising to 84C50 CLK out delay		30	ns
72	TeRDf (D)	$\overline{RD}$ falling to output data valid for external access of on-chip memory		70	ns
73	TeMREQf (D)	$\overline{MREQ}$ falling to output data valid for external access of on-chip memory		80	ns
74	Th WRr	Address hold time from $\overline{WR}$ rising	15		ns
75	Ts MREQf	Address set-up time to $\overline{MREQ}$/$\overline{IORQ}$ falling for $\overline{BUSACK}$ cycle	20		ns
76	Th MREQf	Address hold time from $\overline{MREQ}$ falling for $\overline{BUSACK}$ cycle	20		ns
77	Tl MREQ	$\overline{MREQ}$ low pulse width for $\overline{BUSACK}$ cycle	40		ns
78	Th MREQ	$\overline{MREQ}$ high pulse width for $\overline{BUSACK}$ cycle	30		ns
79	Th RDf	Address hold time from $\overline{RD}$ falling for $\overline{BUSACK}$ cycle	20		ns
80	Td RDr (Df)	$\overline{RD}$ rising to output data floating for $\overline{BUSACK}$ cycle		10	ns

AC CHARACTERISTICS (Continued)

* Test conditions are: CL = 100 pf
** NOTES: AC Characteristics (per line item number).

Number	Symbol	General Parameter
1	TcC	TwCh + TwCl + TrC + TfC
7	TdA (MEREQf)	TwCh + TfC - 45
10	TwMREQh	TwCh + TfC - 25
11	TwMREQl	TcC - 30
24	TdA (IORQf)	TcC - 50
27	TdD (WRf)	TcC - 100
29	TwWR	TcC - 25
31	TdD (WRf)	TwCl + TrC - 100
33	TdWRr (D)	TwCl + TrC - 50
43	TdCTr (A)	TwCl + TrC - 45
48	TdM1f (IORQf)	2TcC + TwCh +TfC - 45

AC Test Conditions:

V_{IH} = 3V V_{OH} = 2V V_{IHC} = V_{CC} -0.6V FLOAT = + -0.5V
V_{IL} = .5V V_{OL} = .8V V_{ILC} = .5V V_{CC} = 4.5 TO 5.5V

DC CHARACTERISTICS

DC CHARACTERISTICS VCC = 5.0 V +/- 10% unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Condition
V_{OHC}	Clock output high voltage	VCC-0.6		V	-2mA
V_{OLC}	Clock output low voltage		0.4	V	+2mA
V_{IH}	Input high voltage	2.2	VCC	V	
V_{IL}	Input low voltage	-0.3	0.8	V	
V_{OL}	Output low voltage		0.4[5]	V	I_{OL} = 2.0mA
V_{OH1}	Output high voltage	2.4[5]		V	I_{OH} = -1.6mA
V_{OH2}	Output high voltage	VCC-0.8[1,5]		V	I_{OH} = -250µA
I_{CC1}	Power supply current 10 MHz		50	mA	V_{CC} = 5V $V_{IH} = V_{CC}$ -0.2V V_{IL} = 0.2V XTALIN = 10 MHz
I_{CC2}	Power supply current (STOP mode)		10[1,3]	µA	V_{CC} = 5V
I_{CC3}	Power supply current (IDLE1 mode)		4[1]	mA	$V_{IH} = V_{CC}$ -0.2V V_{IL} = 0.2V XTALIN = 10 MHz
I_{CC4}	Power supply current (IDLE2 mode)		15[1]	mA	$V_{IH} = V_{CC}$ -0.2V V_{IL} = 0.2V XTALIN = 10 MHz
I_{LI}	Input leakage current	-10	10[4]	µA	V_{IN} = 0.4 to V_{CC}
I_{LO}	3-state output leakage Current in float	-10	10[2]	µA	V_{OUT} = 0.4 to V_{CC}

1. Measurements made with outputs floating
2. A_{15}-A_0, D_7-D_0, $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$. Except on $\overline{RD}$ pin of 40-pin DIP Version, where $I_{LO} = \pm 25$ µA.
3. I_{CC2} standby current is guaranteed when the halt pin is low in STOP mode.
4. All pins except XTALI , where $I_{LI} = \pm 25$ µA.
5. A_{15}-A_0, D_7-D_0, $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, $\overline{WR}$, $\overline{HALT}$, $\overline{M1}$, and $\overline{BUSACK}$.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Voltage on Vcc with respect to Vss.....-0.3V to +7V
Voltages on all inputs with respect to Vss....-0.3V to Vcc +0.3V
Operating Ambient
Temperature.....See Ordering Information
Storage Temperature.....-65° C to 150° C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Test Conditions

The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (OV). Positive current flows into the referenced pin.

Available operating temperature ranges are:

E = -40°C TO +100°C
S=0°C to 70°C
Voltage Supply Range: +4.50V $\leq$ Vcc $\leq$ + 5.50V

All AC parameters assume a load capacitance of 100 pf. Add 10 ns delay for each 50 pf increase in load up to a maximum of 150 pf for the data bus and 100 pf for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points). Maximum capacitive load for CLK is 125 pf.

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.