



YMU769

MA-5S

Mobile Audio 5 Type S

Preliminary

■ Outline

YMU769 has a virtual speaker image function, so that it is the most suitable LSI as a sound source output device which is used in mobile phones for high functional game sounds or high quality ringing melodies, and so on. Synthesizer section in YMU769 adopts "stereophonic hybrid synthesizer system" that is given advantages of both FM synthesizers and Wave Table synthesizers, makes it possible to generate up to 32 FM voices and 32 Wave Table voices simultaneously.

Since FM synthesizer is able to provide countless voices by specifying parameters with only several tens of bytes, memory capacity and communication band can be saved, and thus, the device exhibits the features in operating environment of mobile phones such as allowing distribution of arbitrary melodies with voices. On the other hand, Wave Table synthesizer can pronounce the voice stored in ROM, and in addition it can handle arbitrary ADPCM/PCM voices by sequencer. Furthermore, the Stream Playback function, and the time-variant low pass filter function by AL (Analog Lite) Synthesizer are equipped.

YMU769 has two-channel virtual speaker image functions based on DVX technology, so that natural stereo sounds can be realized even in an environment such as two adjacent speakers on a small body like mobile phones. Integrated stereo speaker amplifiers make external components unnecessary and consequently it saves space. In addition, YMU769 has a built-in circuit to control an LED or a vibrator synchronously to music, and has a power down mode for saving supply current to a minimum.

■ Features

- Simultaneous generation up to 64 tones by stereophonic hybrid synthesizer.
- Equipped with time-variant low pass filter function by AL (Analog Lite) synthesizer.
- Stream replay with ADPCM / PCM is possible.
- Has built-in default voices for FM and Wave Table synthesizers in the ROM, and the voices can be downloaded to SRAM.
- Has built-in SD (Stereo Dipole) function by DVX technology.
- Equipped with speaker amplifier and equalizer circuit.
- Equipped with a stereophonic output pin for headphone.
- Equipped with vibration control circuit, and LED lighting control circuit.
- Has built-in PLL and inputting of master clock up to 20 MHz is possible and supports TCXO (Temperature Compensated Crystal Oscillator).
- Contains a 16-bit stereophonic D/A converter.
- Equipped with general-purpose I/O port (three parties)
- Has a function upwardly compatible to MA-5
- Has power down mode.
- Power supply for internal core 2.65V ~ 3.30V
- Power supply for CPU I/O 1.65V ~ VDD
- Power supply for speaker amplifier VDD ~ 4.50V
- 48-pin QFN plastic package

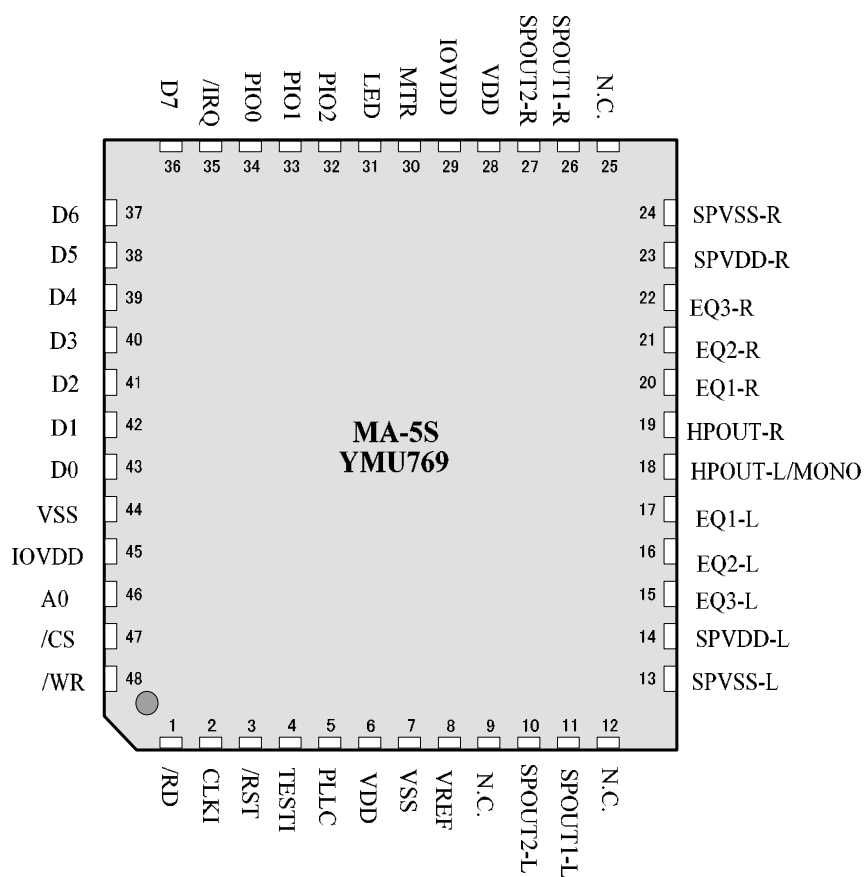
The contents of this booklet are target specifications and they might be changed without notice. Please confirm the finalized specifications again before the use of this LSI.

YAMAHA CORPORATION

YMU769 CATALOG
CATALOG No : 4MU769A1
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www.DataSheet4U.com

■ Pin configuration



<48 pins QFN TOP VIEW>

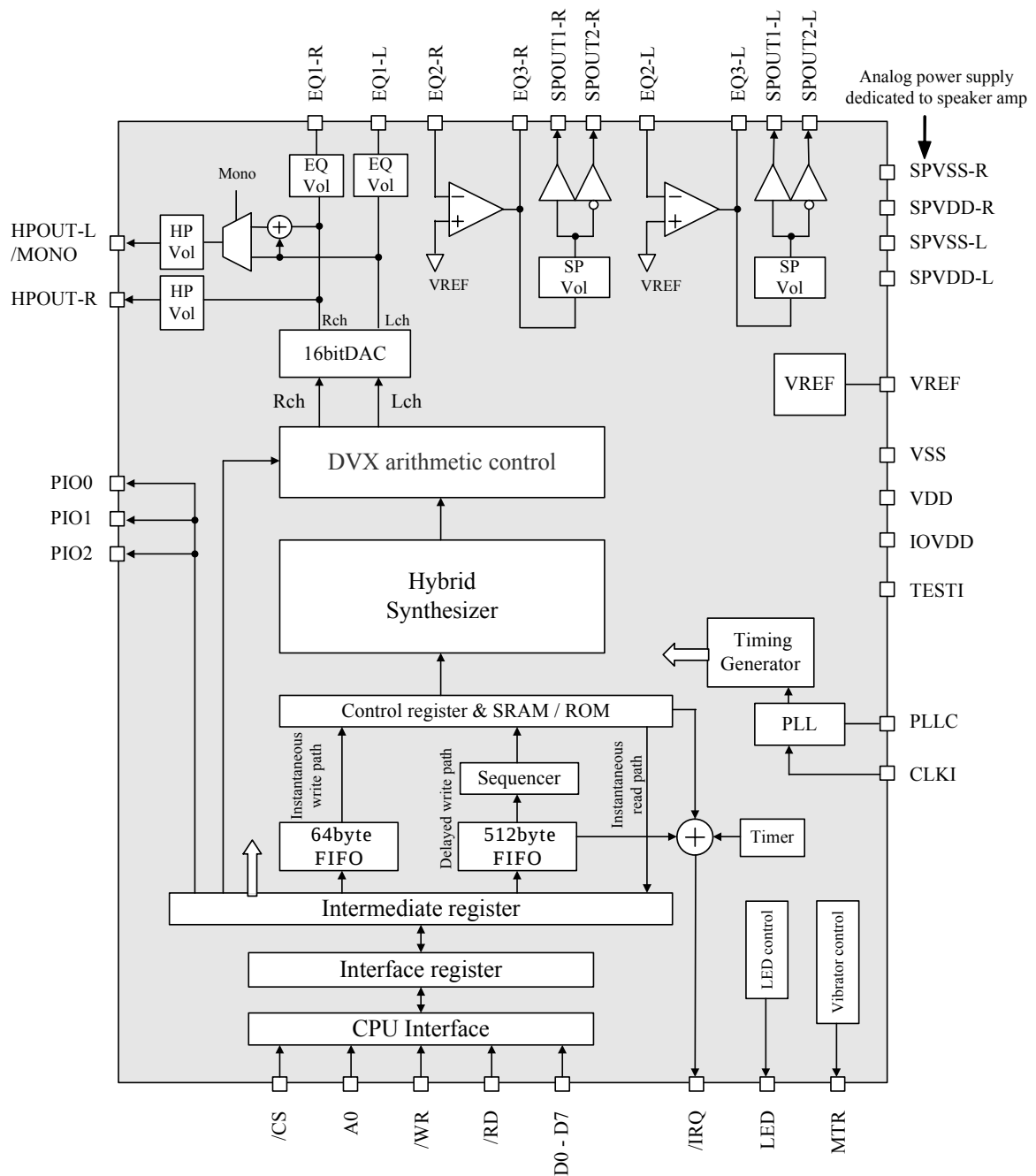
■ Pin Functions

No.	Pin name	I/O	Power supply	Function
1	/RD	I	IOVDD	CPU Interface Read-enable
2	CLKI	Ish	VDD	Pin of input clock (1.5 MHz ~ 20 MHz *Correspondence to TCXO)
3	/RST	Ish	IOVDD	Hardware reset input
4	TESTI	I	IOVDD	TEST input (Make sure, connecting with VSS)
5	PLLC	A	VDD	Connection of capacitor for built-in PLL Connect a series connection of 1000 pF capacitor and 3.3 kΩ resistor between this pin and VSS(*). (*)Directly connect VSS used here and VSS of 8 th pin.
6	VDD	—	—	Power supply (2.65 ~ 3.30V) Connect 0.1 μF and 4.7 μF capacitors between this pin and VSS.
7	VSS	—	—	Ground
8	VREF	A	VDD	Analog reference voltage: Connect 0.1 μF capacitor between this pin and VSS.
9	N.C.	—	—	No Connection (Make sure to use without no connection)
10	SPOUT2-L	A	SPVDD-L	Lch speaker connection pin 2
11	SPOUT1-L	A	SPVDD-L	Lch speaker connection pin 1
12	N.C.	—	—	No Connection (Make sure to use without no connection)
13	SPVSS-L	—	—	Analog ground for Lch speaker amplifier
14	SPVDD-L	—	—	Analog power supply for Lch speaker amplifier (VDD ~ 4.50V) Connect the condenser 0.1μF and 4.7μF into between main pins and SPVSS-L.
15	EQ3-L	A	VDD	Lch equalizer pin 3
16	EQ2-L	A	VDD	Lch equalizer pin 2
17	EQ1-L	A	VDD	Lch equalizer pin 1
18	HPOUT-L / MONO	A	VDD	Headphone output Lch (it is possible to be MONO output)
19	HPOUT-R	A	VDD	Headphone output Rch.
20	EQ1-R	A	VDD	Rch equalizer pin 1
21	EQ2-R	A	VDD	Rch equalizer pin 2
22	EQ3-R	A	VDD	Rch equalizer pin 3
23	SPVDD-R	—	—	Analog power supply for Rch speaker amplifier. (VDD ~ 4.50 V) Connect the capacitor 0.1μF and 4.7μF into between main pins and SPVSS-R.
24	SPVSS-R	—	—	Analog ground for Rch speaker amplifier.
25	N.C.	—	—	No Connection (Make sure to use without no connection)
26	SPOUT1-R	A	SPVDD-R	Rch speaker connection pin 1
27	SPOUT2-R	A	SPVDD-R	Rch speaker connection pin 2
28	VDD	—	—	Power supply (2.65 ~ 3.30V) Connecting the condenser 0.1μF and 4.7μF into between main pins and SPVSS-R.
29	IOVDD	—	—	Power supply for pins (1.65 ~ VDD)
30	MTR	O	IOVDD	Outside vibrator control pin (Drive Capability = 4mA)
31	LED	O	IOVDD	Outside LED pin (Drive Capability = 4mA)
32	PIO2	I/O	IOVDD	General-purpose parallel I/O port 2
33	PIO1	I/O	IOVDD	General-purpose parallel I/O port 1
34	PIO0	I/O	IOVDD	General-purpose parallel I/O port 0
35	/IRQ	O	IOVDD	Interruption output (Drive Capability = 1mA)
36	D7	I/O	IOVDD	CPU interface, Data bus 7
37	D6	I/O	IOVDD	CPU interface, Data bus 6
38	D5	I/O	IOVDD	CPU interface, Data bus 5
39	D4	I/O	IOVDD	CPU interface, Data bus 4
40	D3	I/O	IOVDD	CPU interface, Data bus 3
41	D2	I/O	IOVDD	CPU interface, Data bus 2
42	D1	I/O	IOVDD	CPU interface, Data bus 1
43	D0	I/O	IOVDD	CPU interface, Data bus 0
44	VSS	—	—	Ground
45	IOVDD	—	—	Power supply for pin (1.65 ~ VDD)
46	A0	I	IOVDD	CPU interface, Address signals
47	/CS	I	IOVDD	CPU interface, Chip select
48	/WR	I	IOVDD	CPU interface Write-enable

A : Analog pin Ish : Schmitt input

■ Block Diagram

This section outlines functions of blocks contained in this device and flow of signals.



□ CPU interface

CPU interface is an 8-bit parallel type.

It assumes that a total of 13 pins of 4 control signals (/WR, /RD, /CS, A0 pin), 8 data bus (D0 to D7), and 1 Interrupt pin (/IRQ) are connected to the external CPU.

This block controls the writing and reading of data by the input polarity of control signal.

□ Interface register

This register is able to access directly from the external CPU. There are 2 bytes spaces.

The latter Intermediate register can be accessed through the Interface register.

□ Intermediate register

This register is accessed through the Interface register.

The “Control Register” and ROM/SRAM, which describes below, can be accessed through this register.

This register is called “Intermediate register” since this exists in the middle of the Interface register and the Control register.

In the Intermediate register, there are some registers to control various functions.

□ Control register, ROM/SRAM

The Control register and ROM/SRAM are accessed from “Instantaneous write register”, “Delayed write register”, and “Instantaneous read register” in the Intermediate register.

In the Control register, there is a register to control the following synthesizer mainly.

The voice parameter for FM (GM 128 voices + DRUM 40 voices) and Wave data for WT are stored in ROM.

SRAM is used at the download of arbitrary FM voice parameter and Wave data for WT.

Moreover, it is used as storing buffer at the stream playback of PCM/ADPCM.

□ FIFO

This is an abbreviation of “First In First Out” means the memory which data is read in order of written.

There are 2 paths to write into FIFO in the Intermediate register.

The “Instantaneous write path” is for accessing the Control register and ROM/SRAM immediately, also

“Delayed write path” is for accessing the Control register after managing time through the sequencer.

FIFO size of Instantaneous path is 64-byte, and its size of Delayed path is 512-byte.

□ Sequencer

This is for interpreting the contents of data which is written into the “Delayed write path”.

Generally, “Music data” is written into the Delayed write path. It interprets the contents of music data and controls the synthesizer after sequencer, and then plays the music.

□ Hybrid synthesizer

This device contains a built-in Polyphonic synthesizer that adopts a stereophonic hybrid system that generates up to 64 tones.

FM synthesizer, WT (Wave Table) synthesizer, Stream playback, and AL (Analog Lite) synthesizer are available.

□ DVX Arithmetic control

SD (Stereo Dipole) function that is based on DVX technology makes it possible to create natural stereo sound even in using adjacent two speakers.

☐ **I/O port section**

There are three I/O ports. It is possible to read and write to / from the Intermediate register.

☐ **LED, Vibrator control**

It is possible to synchronize an LED and vibrator with a play, and to control. A synchronous control to a play is also possible.

☐ **Clock generating block**

This device supports a clock input ranging from 1.5 MHz to 20 MHz. (Stop = 0 Hz is possible at power down.)

It is a block to generate a clock which is needed inside of LSI in the PLL.

☐ **DAC**

It converts digital signals from a synthesizer and a digital audio section into analog signals. The length of a data is 16bits.

☐ **Headphone output**

. This is an amplifier of Stereophonic output for Headphone. The monaural output is also possible.

☐ **EQ amplifier**

The change of Filter characteristic and Gain is possible by adjusting the resistors and external parts.

☐ **Speaker amplifier**

The two speakers amplifier, which has a maximum output power of 580 mW at SPVDD_L/_R=3.6V, is integrated in this device. There is a volume to adjust output level in the first stage of amplifier.

■ Electrical Characteristics

● Absolute maximum rating

Item	Symbol	Min.	Max.	Unit
SPVDD-L pin, power supply voltage (Speaker amplifier section)	SPVDD-L	-0.3	6.0	V
SPVDD-R pin, power supply voltage (Speaker amplifier section)	SPVDD-R	-0.3	6.0	V
VDD pin, power supply voltage	VDD	-0.3	4.2	V
IOVDD pin, power supply voltage	IOVDD	-0.3	4.2	V
SPOUT1-L/-R, SPOUT2-L/-R pin, applied voltage	V _{INSP}	-0.3	SPVDD+0.3	V
Analog input voltage	V _{INA}	-0.3	VDD+0.3	V
Digital input voltage 1 (*1)	V _{IND1}	-0.3	IOVDD+0.3	V
Digital input voltage 2 (*2)	V _{IND2}	-0.3	VDD+0.3	V
Permissible loss (*3)	P _d		2487	mW
Storage temperature	T _{STG}	-50	125	°C

VSS = SPVSS = 0V

(*1) Target pin: D0 ~ D7, /CS, A0, /WR, /RD, /RST

(*2) Target pin: CLKI

(*3) Top= 25 °C, and glass epoxy PCB (30mm × 100mm × 1.0mm) is installed.

Operation with Top= 25 °C or higher degrees the permissible loss at the rate of 24.9mW per 1 °C.

● Recommended operating conditions

Item	Symbol	Min.	Typ.	Max.	Unit
SPVDD-L/-R operating voltage (Speaker amplifier section)	SPVDD-L/-R	VDD	3.60	4.50	V
VDD operating voltage	VDD	2.65	3.00	3.30	V
IOVDD operating voltage	IOVDD	1.65	1.80	VDD	V
Operating ambient temperature	T _{OP}	-20	25	85	°C

VSS = SPVSS-L/-R = 0V

● Power consumption

Parameter	Conditions	Min	Typ	Max.	Unit
Power consumption of VDD+IOVDD	Normal operation (*1)		39		mA
At Silent sound generated SPVDD-L/-R side	(*1)		8		mA
At the time of output 400mW / 8ohm load SPVDD-L/-R side	(*1)		420		mA
Power down mode Ta = +25°C	VDD+IOVDD+SPVDD-L/-R (*2)		TBD	TBD	μA
Power down mode Ta = +85°C	VDD+IOVDD+SPVDD-L/-R (*2)		TBD	TBD	μA

(*1): VDD=IOVDD=3.00V, SPVDD=3.60V, T_{OP}=25°C

(*2): VDD=IOVDD=3.30V, SPVDD=4.50V

/CS input pin is fixed to V_{IH}=IOVDD, the other input pins are V_{IL}=VSS and V_{IH}=(IO)VDD.

● DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage "H" level 1	V_{IH}	(*1)	$0.65 \times IOVDD$			V
Input voltage "L" level 1	V_{IL}	(*1)			$0.35 \times IOVDD$	V
Input voltage "H" level 2	V_{IH}	(*2)	$0.75 \times IOVDD$			V
Input voltage "L" level 2	V_{IL}	(*2)			$0.25 \times IOVDD$	V
Input voltage "H" level 3	V_{IH}	(*3)	$0.70 \times VDD$			V
Input voltage "L" level 3	V_{IL}	(*3)			$0.30 \times VDD$	V
Output voltage "H" level	V_{OH}	(*4) $I_{OH} = (*5)$	$0.80 \times IOVDD$			V
Output voltage "L" level	V_{OL}	(*4) $I_{OL} = (*5)$			$0.20 \times IOVDD$	V
Schmitt width 1	V_{sh1}	/RST pin		$0.10 \times IOVDD$		V
Schmitt width 2	V_{sh2}	CLKI pin		$0.10 \times VDD$		V
Input leakage current	IL		-1		1	μA
Input capacity	CI				10	pF

$T_{OP} = -20 \sim 85^{\circ}C$, $VDD = 2.65 \sim 3.30V$, $IOVDD = 1.65 \sim VDD[V]$, Capacitor load=50 pF

(*1) Target pin: D0 ~ D7, /CS, A0, /WR, /RD

(*2) Target pin: /RST

(*3) Target pin: CLKI (In the case of CMOS mode)

(*4) Target pin: D0 ~ D7, /IRQ, LED, MTR, and PIO0 ~ 2

(*5) /IRQ, D0 ~ D7, and PIO0 ~ 2 are $I_{OH} = -1 \text{ mA}$, $I_{OL} = +1 \text{ mA}$

LED, MTR are $I_{OH} = -4 \text{ mA}$, $I_{OL} = +4 \text{ mA}$

However, when IOVDD is less than 2.65V, D0 ~ D7, /IRQ, LED, and MTR become $I_{OH} = -0.2 \text{ mA}$

and $I_{OL} = +0.2 \text{ mA}$

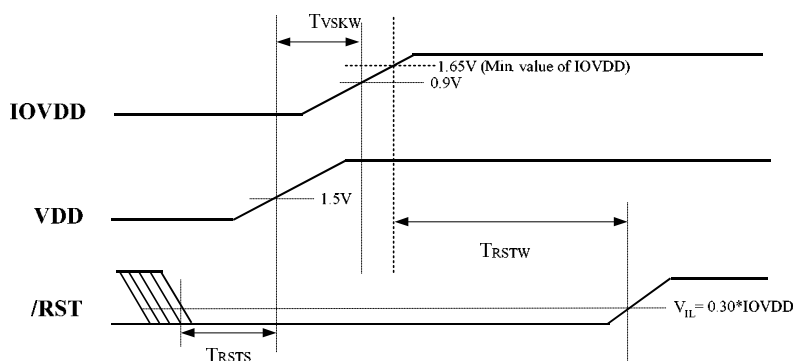
● AC Characteristics

○ /RST, CLKI (CMOS mode), Other input signals

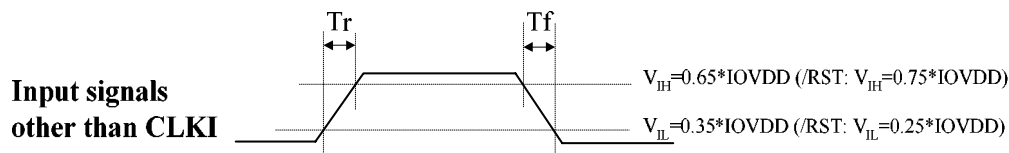
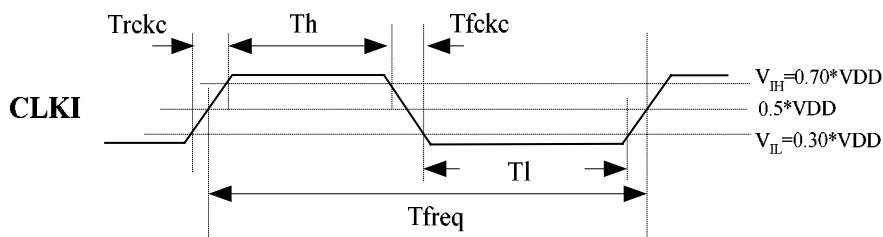
Item	Symbol	Min.	Typ.	Max.	Unit
/RST "L" pulse width	T_{RSTW}	100			μs
/RST (indefinite $\rightarrow$ L) setup time	T_{RSTS}	0			μs
VDD - IOVDD rise time difference	T_{VSKW}	0		3	ms
CLKI frequency	$1 / T_{\text{freq}}$	1.5		20	MHz
CLKI rise / fall time	T_{rckc} / T_{fckc}			30	ns
CLKI High time	T_h	15			ns
CLKI Low time	T_l	15			ns
Input signals other than CLKI rise / fall time	T_r / T_f			20	ns

$T_{\text{OP}} = -20 \sim 85^\circ\text{C}$, $V_{\text{DD}} = 2.65 \sim 3.30\text{V}$, $\text{IOVDD} = 1.65 \sim V_{\text{DD}}[\text{V}]$, Capacitor load = 50 pF

- The input to Clock can be stopped (=0Hz) during reset period and power down state (DP0=1).
However, the input level is to be H or L, and input of intermediate level is prohibited.
- When VDD and IOVDD are used by respectively different power supply, make sure to rise from VDD first.



The reset width is defined as the time from the moment IOVDD has risen to 1.65V.
/RST has to be settled at "L" level at the time VDD has risen to 50%.

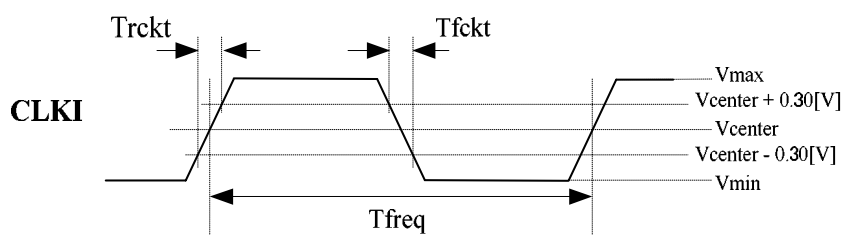


○ CLKI (TCXO mode)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLKI frequency	$1 / T_{\text{freq}}$	1.5		20	MHz
CLKI rise / fall time	$T_{\text{rckt}}, T_{\text{fckt}}$			250	ns
CLKI amplitude H	$V_{\text{max}} - V_{\text{center}}$	0.30		$0.35 \times V_{\text{DD}}$	V
CLKI amplitude L	$V_{\text{center}} - V_{\text{min}}$	0.30		$0.35 \times V_{\text{DD}}$	V
Wait time to stable operation (*1)	T_{wait}	2			ms
Feedback resistance	R_{ck}	30	45	63	k Ω

$T_{\text{OP}} = -20 \sim 85^{\circ}\text{C}$, $V_{\text{DD}} = 2.65 \sim 3.30\text{V}$, Capacitor load = 50pF

(*1) : The value at the AC coupling of TCXO parts and the CLKI pin by the capacity of 1000pF.



- The voltage level which Duty of CLKI becomes 50% (High time = Low time) is defined as V_{center} .
- T_{rckt} and T_{fckt} are defined by the change time between $V_{\text{center}} + 0.30[\text{V}]$ and $V_{\text{center}} - 0.30[\text{V}]$.
- The timing observation level of T_{freq} is to be V_{center} (Duty=50%).

- CPU Interface

The AC characteristics of a CPU interface are measured on condition as follows.

The input conditions at the time of measurement : $V_{IH} = 0.8 \times IOVDD$, $V_{IL} = 0.2 \times IOVDD$
 The measurement points : $V_{IH} = 0.65 \times IOVDD$, $V_{IL} = 0.35 \times IOVDD$
 $V_{OH} = 0.65 \times IOVDD$, $V_{OL} = 0.35 \times IOVDD$

- CPU Interface 1 (In the case of $IOVDD \geq 2.65V$)

(Write cycle)

Item	Symbol	Min	Max.	Unit
Address setup time	T_{ADS}	50		ns
Address hold time	T_{ADH}	0		ns
Chip select setup time	T_{CSS}	50		ns
Chip select hold time	T_{CSH}	0		ns
Write pulse width	T_{WW}	50		ns
Data setup time	T_{WDS}	30		ns
Data hold time	T_{WDH}	0		ns

$T_{OP} = -20 \sim 85^{\circ}C$, $VDD = IOVDD = 2.65 \sim 3.30V$, Capacitor load = 50 pF

(Read cycle)

Item	Symbol	Min	Max.	Unit
Access time from /RD pin	T_{ACCRD}		70	ns
Access time from /CS pin	T_{ACCCS}		70	ns
Access time from /A0 pin	T_{ACCA0}		70	ns
Data hold time from /RD pin	T_{DHRD}	0		ns
Data hold time from /CS pin	T_{DHCS}	0		ns
Data hold time from A0 pin	T_{DHA0}	0		ns
High-impedance transition time from /RD pin	T_{DZRD}		30	ns
High-impedance transition time from /CS pin	T_{DZCS}		30	ns

$T_{OP} = -20 \sim 85^{\circ}C$, $VDD = IOVDD = 2.65 \sim 3.30V$, Capacitor load = 50 pF

$I_{OH} = -1.0mA$, $I_{OL} = +1.0mA$ (D0 ~ D7 pin)

○ CPU Interface 2 (In the case of IOVDD < 2.65)

(Write cycle)

Item	Symbol	Min	Max.	Unit
Address setup time	T_{ADS}	50		ns
Address hold time	T_{ADH}	0		ns
Chip select setup time	T_{CSS}	50		ns
Chip select hold time	T_{CSH}	0		ns
Write pulse width	T_{WW}	50		ns
Data setup time	T_{WDS}	50		ns
Data hold time	T_{WDH}	0		ns

$T_{OP} = -20 \sim 85^{\circ}\text{C}$, $VDD = 2.65 \sim 3.30\text{V}$, $IOVDD = 1.65 \sim \text{less than } 2.65\text{V}$, Capacitor load=30 pF

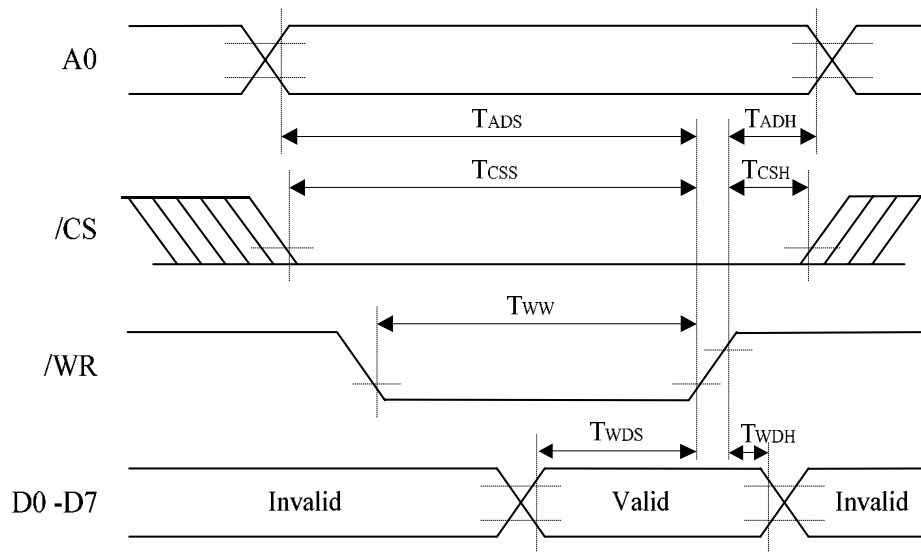
(Read cycle)

Item	Symbol	Min	Max.	Unit
Access time from /RD pin	T_{ACCRD}		80	ns
Access time from /CS pin	T_{ACCS}		80	ns
Access time from /A0 pin	T_{ACCA0}		80	ns
Data hold time from /RD pin	T_{DHRD}	0		ns
Data hold time from /CS pin	T_{DHCS}	0		ns
Data hold time from A0 pin	T_{DHA0}	0		ns
High-impedance transition time from /RD pin	T_{DZRD}		50	ns
High-impedance transition time from /CS pin	T_{DZCS}		50	ns

$T_{OP} = -20 \sim 85^{\circ}\text{C}$, $VDD = 2.65 \sim 3.30\text{V}$, $IOVDD = 1.65 \sim \text{less than } 2.65\text{V}$, Capacitor load=30 pF

$I_{OH} = -0.2\text{mA}$, $I_{OL} = +0.2\text{mA}$ (D0 ~ D7 pin)

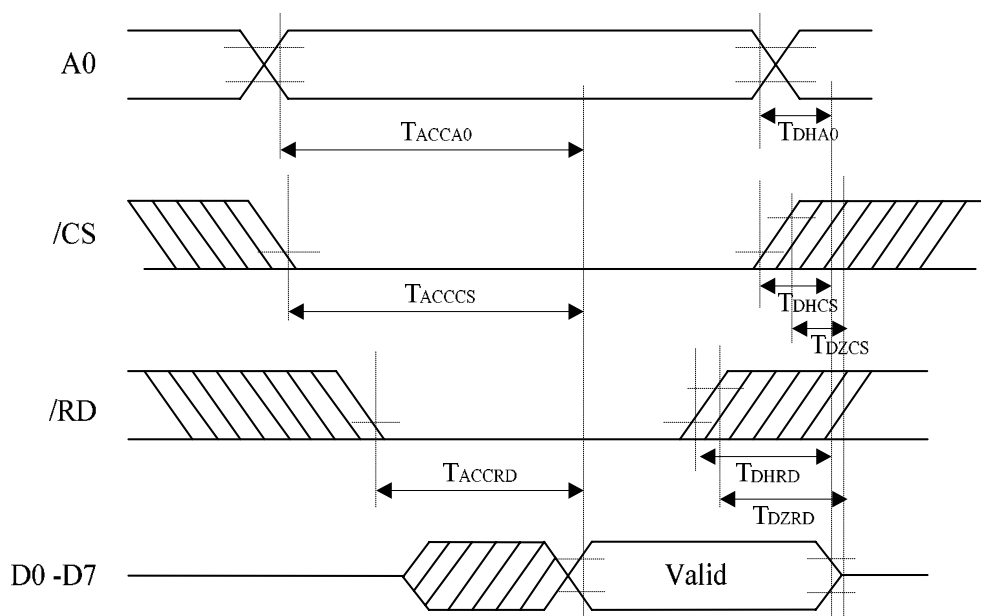
Write cycle



Note :

- T_{ADH} : The hold time of A0 pin, which is defined with respect to the point where the rise of /WR has reached $0.65 \cdot IOVDD$ under the condition that both two specifications (T_{CSH} , T_{WDH}) are secured more than minimum value ($=0ns$).
- T_{CSH} : The hold time of /CS pin, which is defined with respect to the point where the rise of /WR has reached $0.65 \cdot IOVDD$ under the condition that both two specifications (T_{ADH} , T_{WDH}) are secured more than minimum value ($=0ns$).
- T_{WDH} : The hold time of D0 ~ D7 pins, which is defined with respect to the point where the rise of /WR has reached $0.65 \cdot IOVDD$ under the condition that both two specifications (T_{ADH} , T_{CSH}) are secured more than minimum value ($=0ns$).
- T_{ADS} : The hold time of A0 pin, which is defined with respect to the point where /WR has become invalid ($0.35 \cdot IOVDD$) under the condition that all of three specifications (T_{CSS} , T_{WW} , T_{WDS}) are secured more than minimum value.
- T_{CSS} : The hold time of /CS pin, which is defined with respect to the point where /WR has become invalid ($0.35 \cdot IOVDD$) under the condition that all of three specifications (T_{ADS} , T_{WW} , T_{WDS}) are secured more than minimum value.

Read cycle



Note :

T_{ACCA0} : The access time until D0 ~ D7 are defined ($0.65 \cdot IOVDD$ or $0.35 \cdot IOVDD$) after A0 is defined ($0.65 \cdot IOVDD$ or $0.35 \cdot IOVDD$).

Considers that /RD and /CS are defined beforehand (*1).

T_{ACCSS} : The access time until D0 ~ D7 are defined ($0.65 \cdot IOVDD$ or $0.35 \cdot IOVDD$) after /CS is defined ($0.35 \cdot IOVDD$).

Considers that A0 and /RD are defined beforehand (*1).

T_{ACCRD} : The access time until D0 ~ D7 are defined ($0.65 \cdot IOVDD$ or $0.35 \cdot IOVDD$) after /RD is defined ($0.35 \cdot IOVDD$).

Considers that A0 and /CS are defined beforehand (*1).

T_{DHRD} : The time (Hold time) until D0 ~ D7 output valid data after /RD becomes enable ($=0.35 \cdot IOVDD$) under the condition that A0 and /CS secure sufficient hold time (*2).

T_{DHCS} : The time (Hold time) until D0 ~ D7 output valid data after /CS becomes enable ($=0.35 \cdot IOVDD$) under the condition that A0 and /RD secure sufficient hold time (*2).

T_{DHA0} : The time (Hold time) until D0 ~ D7 output valid data after A0 becomes enable ($0.65 \cdot IOVDD$ or $0.35 \cdot IOVDD$) under the condition that /RD and /CS secure sufficient hold time (*2).

T_{DZRD} : The time until D0 ~ D7 become high impedance status after /RD becomes disable ($=0.65 \cdot IOVDD$) under the condition that A0 and /CS secure sufficient hold time (*2).

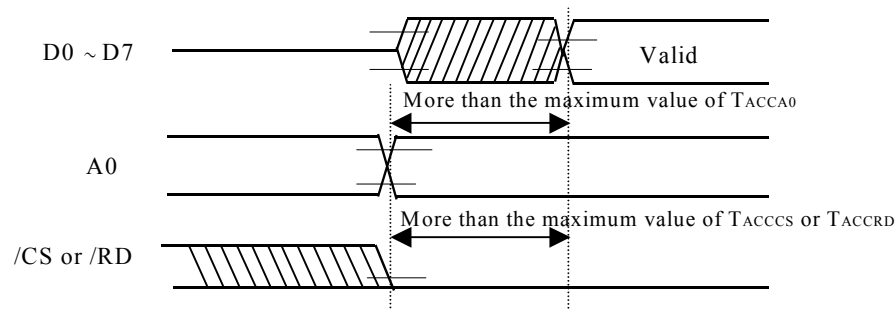
T_{DZCS} : The time until D0 ~ D7 become high impedance status after /CS becomes disable ($=0.65 \cdot IOVDD$) under the condition that A0 and /RD secure sufficient hold time (*2).

(*1) “~ defined beforehand.” means.

In the case of /CS : The status that /CS is defined ($0.35 \times \text{IOVDD}$) before more than the time of T_{ACCSS} with respect to the point where D0 ~ D7 are defined ($0.65 \times \text{IOVDD}$ or $0.35 \times \text{IOVDD}$).

In the case of /RD : The status that /RD is defined ($0.35 \times \text{IOVDD}$) before more than the time of T_{ACCRD} with respect to the point where D0 ~ D7 are defined ($0.65 \times \text{IOVDD}$ or $0.35 \times \text{IOVDD}$).

In the case of A0 : The status that A0 is defined ($0.35 \times \text{IOVDD}$ or $0.65 \times \text{IOVDD}$) before more than the time of T_{ACCA0} with respect to the point where D0 ~ D7 are defined ($0.65 \times \text{IOVDD}$ or $0.35 \times \text{IOVDD}$).



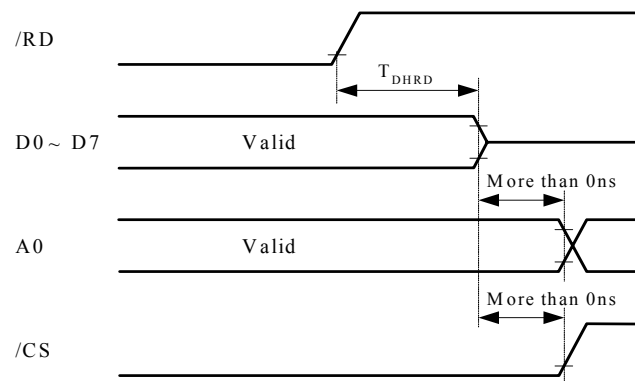
(*2) “~ sufficient hold time” means.

At T_{DHRD} measurement : The status that the enable time of A0 and /CS pins input are secured more than 0ns with respect to the point where D0 ~ D7 can not hold valid data.

At T_{DHCS} measurement : The status that the enable time of A0 and /RD pins input are secured more than 0ns with respect to the point where D0 ~ D7 can not hold valid data.

At T_{DHA0} measurement : The status that the enable time of /CS and /RD pins input are secured more than 0ns with respect to the point where D0 ~ D7 can not hold valid data.

(Example: At T_{DHRD} measurement)



- Analog Characteristics

Conditions of $T_{OP}=25^{\circ}\text{C}$, $V_{DD}=3.00\text{V}$, $IOV_{DD}=1.80\text{V}$ and $SPV_{DD-L/-R}=3.60\text{V}$ apply to all items.

- SP amplifier

Parameter	Min.	Typ.	Max.	Unit
Gain setting (fixed)		± 2		times
Min. load resistance (RL)		8		Ω
Max. output voltage amplitude (RL=8 Ω)		6.0		V _{p-p}
Max. output power (RL=8 Ω , THD+N $\leq$ 1.0%)		580		mW
THD + N (RL=8 Ω , f=1 kHz, output = 400mW)		0.025		%
Noise at no signal (A-filter: weighting filter)		-90		dBV
PSRR (f=1 kHz)		90		dB
Amplitude center potential (VSEL2, VSEL1 =0, 0)		$0.6 \times V_{DD}$		V
(VSEL2, VSEL1 =0, 1)		$0.5 \times V_{DD}$		V
(VSEL2, VSEL1 =1, 0)		$0.67 \times V_{DD}$		V
Differential output voltage		10	50	mV
Max. load capacity connectable to SPOUT1 and SPOUT2 pin (*)			1000	pF

(*) : The maximum of 1000pF can be connected to SPOUT1-L/-R pin,
and the maximum of 1000pF can be connected to SPOUT2-L/-R pin.

- EQ amplifier

Item	Min.	Typical	Max.	Unit
Gain settable range			30	dB
Max. output voltage amplitude		2.7		V _{p-p}
THD + N (f=1 kHz)			0.05	%
Noise at no signal (A-filter)		-90		dBV
Input impedance	10			M Ω
Feedback resistance between EQ2-L/-R and EQ3-L/-R	20			k Ω

- SP Volume

Item	Min.	Typical	Max.	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
THD + N (f=1 kHz)			0.05	%

- EQ Volume

Item	Min.	Typical	Max.	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
Noise at no signal (A-filter)		-90		dBV
Max. output current	120			μA
Max. output voltage amplitude		1.5		V _{p-p}
Output impedance		300	600	Ω

○ HP Volume

Item	Min.	Typical	Max.	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
Noise at no signal (A-filter)		-90		dBV
Max. output current	120			μA
Max. output volt. amplitude		1.5		Vp-p
Output impedance		300	600	Ω

○ VREF

Item	Min.	Typical	Max.	Unit
VREF voltage		0.5×VDD		V

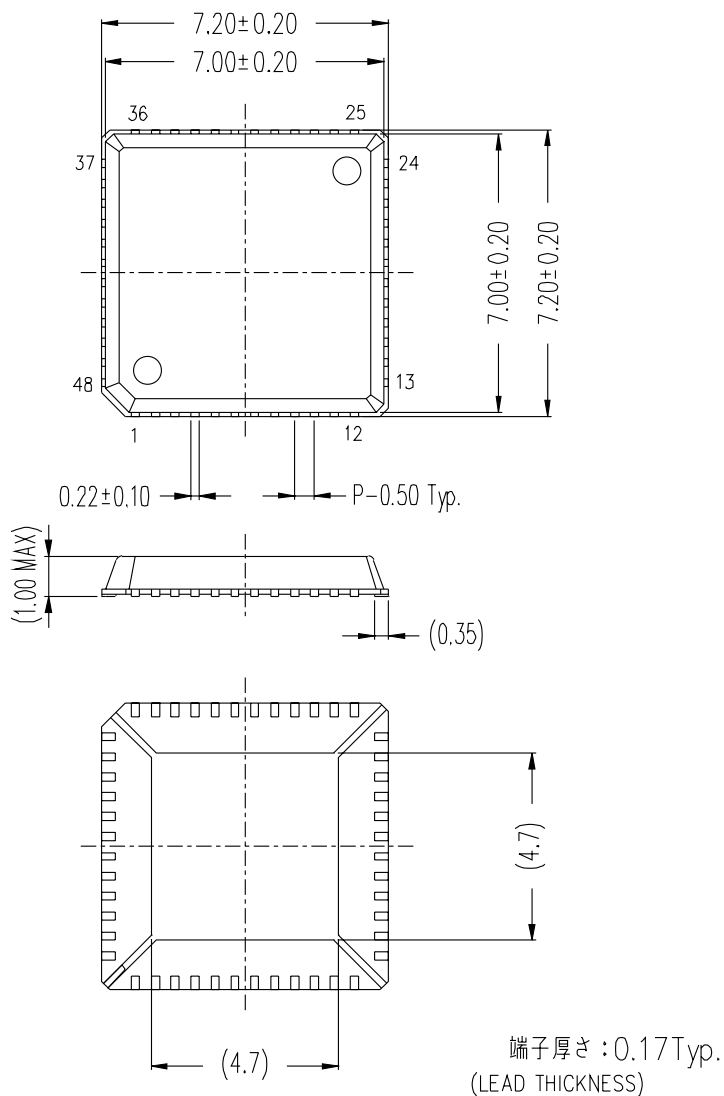
○ DAC

Item	Min.	Typical	Max.	Unit
Resolution		16		Bit
Full scale output volt.		1.5		Vp-p
THD+N (f= 1 kHz)			0.5	%
Noise at no signal (A-filter)		-85	-80	dBV
Frequency response (f=50Hz to 20 kHz)	-3.0 (*)		+0.5	dB

(*): Reduction of response in high frequency range caused by aperture effect

■ External dimensions of package

C-PK48QP-2



モールドコーナー形状は、この図面と若干異なるタイプのものもあります。
 カッコ内の寸法値は参考値とする。
 モールド外形寸法はバリを含まない。
 単位 (UNIT) : mm (millimeters)

The shape of the molded corner may slightly different from the shape in this diagram.
 The figure in the parenthesis () should be used as a reference.
 Plastic body dimensions do not include burr of resin.
 UNIT: mm

注) 表面実装LSIは保管条件及び、半田付けについての特別な配慮が必要です。
 詳しくはヤマハ代理店までお問い合わせ下さい。
 Note: The LSIs for surface mount need special consideration on storage and soldering conditions.
 For detailed information, Please contact your nearest Yamaha agent.

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