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XRT79L74

4 - CHANNEL DS3/E3 ATM UNI/PPP COMBO IC

MARCH 2004 *REV. P1.0.0*

REGISTER MANUAL

The XRT79L74 is a four channel, ATM UNI/PPP Physical Layer Processor with integrated DS3/E3 framing controllers and Line Interface Units with Jitter Attenuators that are designed to support ATM direct mapping and cell delineation as well as PPP mapping and Frame processing. For ATM UNI applications, this device provides the ATM Physical Layer (Physical Medium Dependent and Transmission Convergence sub-layers) interface for the public and private networks at DS3/E3 rates. For Clear-Channel Framer applications, this device supports the transmission and reception of "user data" via the DS3/E3 payload.

The XRT79L74 includes DS3/E3 Framing, Line Interface Unit with Jitter Attenuator that supports mapping of ATM or HDLC framed data. A flexible parallel microprocessor interface is provided for configuration and control. Industry standard UTOPIA II and POS-PHY interface are also provided.

GENERAL FEATURES:

- Integrated T3/E3 Line Interface Unit
- Integrated Jitter Attenuator that can be selected either in Receive or Transmit path
- Flexible integrated Clock Multiplier that takes single frequency clock and generates either DS3 or E3 frequency.
- 8/16 bit UTOPIA Level I and II and PPP Multi-PHY Interface operating at 25, 33 or 50 MHz.
- HDLC Controller that provides the mapping/ extraction of either bit or byte mapped encapsulated packet from DS3/E3 Frame.
- Contains on-chip 16 cell FIFO (configurable in depths of 4, 8, 12 or 16 cells), in both the Transmit (TxFIFO) and Receive Directions (RxFIFO)
- Contains on-chip 54 byte Transmit and Receive OAM Cell Buffer for transmission, reception and processing of OAM Cells
- Supports ATM cell or PPP Packet Mapping
- Supports M13 and C-Bit Parity Framing Formats
- Supports DS3/E3 Clear-Channel Framing.
- Includes PRBS Generator and Receiver
- Supports Line, Cell, and PLCP Loop-backs
- Interfaces to 8 Bit wide Intel, Motorola or PowerPC
- Low power 3.3V, 5V Input Tolerant, CMOS
- Available in 456 Lead PBGA Package
- JTAG Interface

LINE INTERFACE UNIT

- On chip Clock and Data Recovery circuit for high input jitter tolerance
- Meets E3/DS3 Jitter Tolerance Requirements
- Detects and Clears LOS as per G.775.
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE,1995 standards
- Meets ETSI TBR 24 and GR-499 Jitter Transfer Requirements
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock
- On chip advanced crystal-less Jitter Attenuator
- Jitter Attenuator can be selected in Receive or Transmit paths
- 16 or 32 bits selectable FIFO size
- Meets the Jitter and Wander specifications described in T1.105.03b,ETSI TBR-24, Bellcore GR-253 and GR-499 standards
- Jitter Attenuator can be disabled
- Maximum power consumption 3.1W

DS3/E3 FRAMER

- DS3 framer supports both M13 and C-bit parity.
- DS3 framer meets ANSI T1.107 and T1.404 standards.
- Detects OOF,LOF,AIS,RDI/FERF alarms.
- Generation and Insertion of FEBE on received parity errors supported.
- Automatic insertion of RDI/FERF on alarm status.
- E3 framer meets G.832,G.751 standards.
- Framers can be bypassed.

ATM/PPP PROTOCOL PROCESSOR

TRANSMIT CELL PROCESSING

- Extracts ATM cells
- Supports ATM cell payload scrambling
- Maps ATM cells into E3 or DS3 frame
- PLCP frame and mapping of ATM cell streams

RECEIVE CELL PROCESSING

- Extraction of ATM cells from PLCP frame or directly from E3 or DS3 frame
- Termination of PLCP frame
- Supports payload cell de-scrambling

TRANSMIT PACKET PROCESSING

- Inserts PPP packets into data stream
- Maps HDLC data stream directly into DS3 or E3 frame
- Extracts in-band messaging packets
- Supports CRC-16/32, HDLC flag and Idle sequence generation

RECEIVE PACKET PROCESSING

- Extracts HDLC data stream from DS3 or E3 frame
- Inserts in-band messaging packets
- Detects and removes HDLC flags

UTOPIA/ SYSTEM INTERFACE

- 8/16 bit UTOPIA Level I and II and PPP Multi-PHY Interface operating at 25, 33 or 50 MHz.
- Compliant with ATM Forum UTOPIA II interface
- Programmable FIFO size for both Transmit and Receive direction
- Compliant to POS-PHY Level 2 interface

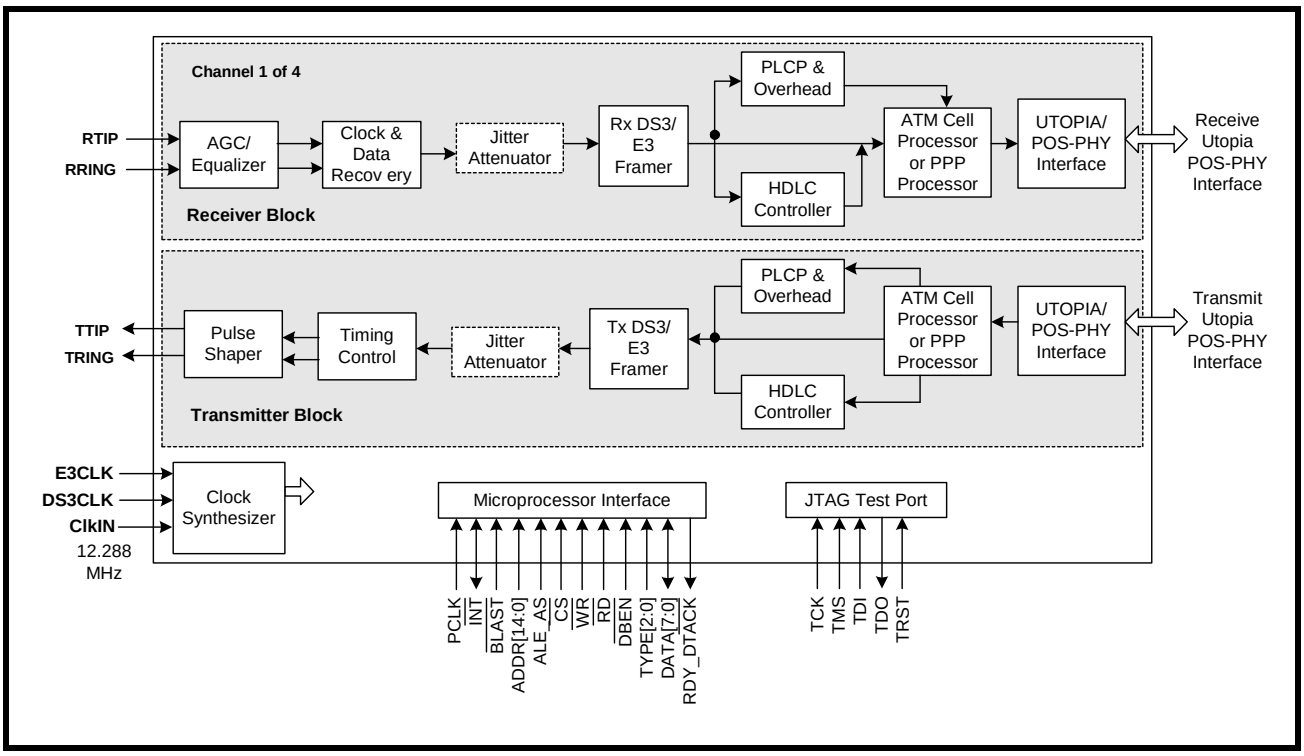
SERIAL INTERFACE

- Serial clock and data interface for accessing DS3/ E3 framer
- Serial clock and data interface for accessing cell/ packet processor

APPLICATIONS

- Digital Access and Cross Connect Systems
- 3G Base Stations
- DSLAMs
- Digital, ATM, WAN and LAN Switches

FIGURE 1. BLOCK DIAGRAM OF THE XRT79L74



PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT79L74IB	456 Lead PBGA	-40°C to +85°C

TABLE OF CONTENTS

REGISTER MANUAL 1
GENERAL FEATURES: 1
Line Interface Unit 1
DS3/E3 Framer 1
ATM/PPP PROTOCOL PROCESSOR 1
Transmit Cell Processing 1
Receive Cell Processing 1
Transmit Packet Processing 2
Receive Packet Processing 2
Utopia/ System Interface 2
Serial Interface 2
APPLICATIONS 2
FIGURE 1. BLOCK DIAGRAM OF THE XRT79L74 2
PRODUCT ORDERING INFORMATION 2
TABLE OF CONTENTS ..... A
REGISTER MAP OF THE XRT79L74 4
COMMONCONTROL REGISTERS OF THE XRT79L74 4
CLEAR-CHANNEL FRAMER BLOCK REGISTERS 5
LIU/JITTER ATTENUATOR CONTROL REGISTERS 9
RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS 10
OPERATION BLOCK INTERRUPT REGISTER BIT FORMATS 18
OPERATION CONTROL REGISTER - BYTE 3 (ADDRESS = 0X0100) 18
OPERATION CONTROL REGISTER - BYTE 2 (ADDRESS = 0X0101) 18
OPERATION CONTROL - LOOP-BACK CONTROL REGISTER (ADDRESS = 0X0102) 19
OPERATION CONTROL REGISTER - BYTE 0 (ADDRESS = 0X0103) 20
DEVICE ID REGISTER (ADDRESS = 0X0104) 20
REVISION ID REGISTER (ADDRESS = 0X0105) 21
OPERATION INTERRUPT STATUS REGISTER - BYTE 1 (ADDRESS = 0X0112) 21
OPERATION INTERRUPT STATUS REGISTER - BYTE 0 (ADDRESS = 0X0113) 22
OPERATION INTERRUPT ENABLE REGISTER - BYTE 1 (ADDRESS = 0X0116) 23
OPERATION INTERRUPT ENABLE REGISTER - BYTE 0 (ADDRESS = 0X0117) 24
CHANNEL INTERRUPT INDICATION REGISTERS 25
CHANNEL INTERRUPT INDICATOR - RECEIVE CELL PROCESSOR/PPP PROCESSOR BLOCK (ADDRESS = 0X0119) 25
CHANNEL INTERRUPT INDICATOR - LIU/JITTER ATTENUATOR BLOCK (ADDRESS = 0X011D) 26
CHANNEL INTERRUPT INDICATOR - TRANSMIT CELL PROCESSOR/PPP PROCESSOR BLOCK (ADDRESS = 0X0121) 26
CHANNEL INTERRUPT INDICATOR - DS3/E3 FRAMER BLOCK (ADDRESS = 0X0127) 27
OPERATION GENERAL PURPOSE PIN DATA REGISTER (ADDRESS = 0X0147) 27
OPERATION GENERAL PURPOSE PIN DIRECTION CONTROL REGISTER (ADDRESS = 0X014B) 27
RECEIVE UTOPIA INTERFACE BLOCK 28
TABLE 1: RECEIVE UTOPIA/POS-PHY INTERFACE BLOCK - REGISTER/ADDRESS MAP 28
RECEIVE UTOPIA/POS-PHY CONTROL REGISTER - BYTE 0 (ADDRESS = 0X0503) 28
RECEIVE UTOPIA PORT ADDRESS REGISTER (ADDRESS = 0X0513) 31
RECEIVE UTOPIA PORT NUMBER REGISTER (ADDRESS = 0X0517) 31
TRANSMIT UTOPIA INTERFACE BLOCK 33
TABLE 2: TRANSMIT UTOPIA INTERFACE BLOCK - REGISTER/ADDRESS MAP 33
TRANSMIT UTOPIA/POS-PHY CONTROL REGISTER - BYTE 0 (ADDRESS = 0X0583) 33
TRANSMIT UTOPIA PORT ADDRESS REGISTER (ADDRESS = 0X0593) 36
TRANSMIT UTOPIA PORT NUMBER REGISTER (ADDRESS = 0X0597) 36
LIU/JITTER ATTENUATOR CONTROL REGISTER BIT-FORMAT 38
LIU TRANSMIT APS/REDUNDANCY CONTROL REGISTER (ADDRESS = 0XN300) 38
LIU INTERRUPT ENABLE REGISTER (ADDRESS = 0XN301) 38
LIU INTERRUPT STATUS REGISTER (ADDRESS = 0XN302) 40

LIU ALARM STATUS REGISTER (ADDRESS = 0XN303) *42*
LIU TRANSMIT CONTROL REGISTER (ADDRESS = 0XN304) *45*
LIU RECEIVE CONTROL REGISTER (ADDRESS = 0XN305) *47*
LIU CHANNEL CONTROL REGISTER (ADDRESS = 0XN306) *49*
JITTER ATTENUATOR CONTROL REGISTER (ADDRESS = 0XN307) *50*
LIU RECEIVE APS/REDUNDANCY CONTROL REGISTER (ADDRESS = 0XN308) *51*
ORDERING INFORMATION 52
PACKAGE DIMENSIONS 52
REVISION HISTORY *53*

REGISTER MAP OF THE XRT79L74

The register map is divided into two main sections, Common Control Registers and Channel Control Registers. The Channel Control Registers are addressed by the MSB of the address bus A[14:13]. These two bits determine which channel is to be accessed. In this document, n is used in place of the channel number where:

Channel 1 (n = 1)

Channel 2 (n = 2)

Channel 3 (n = 3)

Channel 4 (n = 4)

COMMONCONTROL REGISTERS OF THE XRT79L74

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
COMMON CONTROL REGISTERS			
0x0100	Operation Control Register - Byte 3	R/W	0x00
0x0101	Operation Control Register - Byte 2	R/W	0x00
0x0102	Operation Control Register - Byte 1	R/W	0x00
0x0103	Operation Control Register - Byte 0	R/W	0x00
0x0104	Device ID Register	R/W	TBD
0x0105	Revision ID Register	R/W	0x01
0x0106 - 0x0111	Reserved		
0x0112	Operation Block Interrupt Status Register - Byte 1	RO	0x00
0x0113	Operation Block Interrupt Status Register - Byte 0	RO	0x00
0x0114 - 0x0115	Reserved		
0x0116	Operation Block Interrupt Enable Register - Byte 1	R/W	0x00
0x0117	Operation Block Interrupt Enable Register - Byte 0	R/W	0x00
0x0118	Reserved		
0x0119	Channel Interrupt Indicator - Receive Cell Processor/PPP Processor Block	R/O	0x00
0x011A - 0x011C	Reserved		
0x011D	Channel Interrupt Indicator - LIU/Jitter Attenuator Block	R/O	0x00
0x011E - 0x0120	Reserved		
0x0121	Channel Interrupt Indicator - Transmit Cell Processor/PPP Processor Block	R/O	0x00
0x0122 - 0x0126	Reserved		
0x0127	Channel Interrupt Indicator - DS3/E3 Framer Block - Byte 0	R/O	0x00
0x0128 - 0x0146	Reserved		
0x0147	Operation General Purpose Input/Output Register	R/W	0x00
0x0148 - 0x014A	Reserved		

COMMONCONTROL REGISTERS OF THE XRT79L74

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
COMMON CONTROL REGISTERS			
0x014B	Operation General Purpose Input/Output Direction Register	R/W	0x00
0x014C - 0x04FF	Reserved		
0x0501	Receive POS-PHY Control Register - Byte 1	R/W	0x00
0x0502	Receive POS-PHY Control Register - Byte 0	R/W	0x00
0x0503	Receive UTOPIA Control Register	R/W	0x00
0x0504 - 0x0512	Reserved		
0x0513	Receive UTOPIA Port Address Register	R/W	0x00
0x0514 - 0x0516	Reserved		
0x0517	Receive UTOPIA Port Number Register	R/W	0x00
0x0518 - 0x0580	Reserved		
0x0581	Transmit POS-PHY Control Register - Byte 1	R/W	0x00
0x0582	Transmit POS-PHY Control Register - Byte 0	R/W	0x00
0x0583	Transmit UTOPIA Control Register	R/W	0x00
0x0584 - 0x0592	Reserved		
0x0593	Transmit UTOPIA Port Address Register	R/W	0x00
0x0594 - 0x0596	Reserved		
0x0597	Transmit UTOPIA Port Number Register	R/W	0x00

CLEAR-CHANNEL FRAMER BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS (N = CHANNEL NUMBER)			
CLEAR-CHANNEL FRAMER BLOCK REGISTERS			
0xn100	Operating Mode Register	R/W	0x2B
0xn101	I/O Control Register	R/W	0xA4
0xn102 - 0xn103	Reserved		
0xn104	Block Interrupt Enable Register	R/W	0x00
0xn105	Block Interrupt Status Register	R/O	0x00
0xn106 - 0xn10B	Reserved		
0xn10C	DS3 Test Register	R/W	0x00
0xn10D	Payload HDLC Control Register	R/W	0x00
0xn10E - 0xn10F	Reserved		

CLEAR-CHANNEL FRAMER BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS (N = CHANNEL NUMBER)			
CLEAR-CHANNEL FRAMER BLOCK REGISTERS			
0xn110	RxDS3 Configuration and Status RegisterRxE3 Configuration and Status Register # 1 (G.832 & G.751)	R/O	0x12
0xn111	RxDS3 Status RegisterRxE3 Configuration and Status Register # 2 (G.832 & G.751)	R/O	0x00
0xn112	RxDS3 Interrupt Enable RegisterRxE3 Interrupt Enable Register 1 (G.832 & G751)	R/W	0x00
0xn113	RxDS3 Interrupt Status RegisterRxE3 Interrupt Enable Register # 2 (G.832 & G.751)	RUR	0x00
0xn114	RxDS3 Sync Detect RegisterRxE3 Interrupt Status Register # 1 (G.832 & G.751)	R/W & RUR	0x00
0xn115	RxE3 Interrupt Status Register # 2 (G.832 & G.751)	RUR	0x00
0xn116	Reserved		
0xn117	RxDS3 FEAC Interrupt Enable and Status Register	R/W & RUR	0x00
0xn118	RxE3 LAPD Control Register	R/W & RUR	0x00
0xn119	RxLAPD Status Register	R/O	0x00
0xn11A	RxE3 NR Byte Register (G.832)RxE3 Service Bits Register (G.751)	R/O	0x00
0xn11B	RxE3 GC Byte Register (G.832)	R/O	0x00
0xn11C	RxE3 TTB Register # 0 (G.832)	R/O	0x00
0xn11D	RxE3 TTB Register # 1 (G.832)	R/O	0x00
0xn11E	RxE3 TTB Register # 2 (G.832)	R/O	0x00
0xn11F	RxE3 TTB Register # 3 (G.832)	R/O	0x00
0xn120	RxE3 TTB Register # 4 (G.832)	R/O	0x00
0xn121	RxE3 TTB Register # 5 (G.832)	R/O	0x00
0xn122	RxE3 TTB Register # 6 (G.832)	R/O	0x00
0xn123	RxE3 TTB Register # 7 (G.832)	R/O	0x00
0xn124	RxE3 TTB Register # 8 (G.832)	R/O	0x00
0xn125	RxE3 TTB Register # 9 (G.832)	R/O	0x00
0xn126	RxE3 TTB Register # 10 (G.832)	R/O	0x00
0xn127	RxE3 TTB Register # 11 (G.832)	R/O	0x00
0xn128	RxE3 TTB Register # 12 (G.832)	R/O	0x00
0xn129	RxE3 TTB Register # 13 (G.832)	R/O	0x00

CLEAR-CHANNEL FRAMER BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS (N = CHANNEL NUMBER)			
CLEAR-CHANNEL FRAMER BLOCK REGISTERS			
0xn12A	RxE3 TTB Register # 14 (G.832)	R/O	0x00
0xn12B	RxE3 TTB Register # 15 (G.832)	R/O	0x00
0xn12C	RxE3 SSM Register (G.832)	R/O	0x00
0xn12D - 0xn12F	Reserved		
0xn130	Transmit DS3 Configuration RegisterTransmit E3 Configuration Register	R/W	0x07
0xn131	TxDS3 FEAC Configuration and Status Register	RUR & R/W	0x00
0xn132	TxDS3 FEAC Register	R/W	0x7E
0xn133	TxLAPD Configuration Register	R/O & R/W	0x08
0xn134	TxLAPD Status and Interrupt Register	RUR & R/W	0x00
0xn135	TxDS3 M-Bit Mask RegisterTxE3 GC Byte Register (G.832)TxE3 Service Bits Register (G.751)	R/W	0x00
0xn136	TxDS3 F-Bit Mask Register # 1TxE3 MA Byte Register (G.832)	R/W	0x00
0xn137	TxDS3 F-Bit Mask Register # 2TxE3 NR Byte Register (G.832)	R/W	0x00
0xn138	TxDS3 F-Bit Mask Register # 3TxTTB Register # 0 (G.832)	R/W	0x00
0xn139	TxTTB Register # 1 (G.832)	R/W	0x00
0xn13A	TxTTB Register # 2 (G.832)	R/W	0x00
0xn13B	TxTTB Register # 3 (G.832)	R/W	0x00
0xn13C	TxTTB Register # 4 (G.832)	R/W	0x00
0xn13D	TxTTB Register # 5 (G.832)	R/W	0x00
0xn13E	TxTTB Register # 6 (G.832)	R/W	0x00
0xn13F	TxTTB Register # 7 (G.832)	R/W	0x00
0xn140	TxTTB Register # 8 (G.832)	R/W	0x00
0xn141	TxTTB Register # 9 (G.832)	R/W	0x00
0xn142	TxTTB Register # 10 (G.832)	R/W	0x00
0xn143	TxTTB Register # 11 (G.832)	R/W	0x00
0xn144	TxTTB Register # 12 (G.832)	R/W	0x00
0xn145	TxTTB Register # 13 (G.832)	R/W	0x00
0xn146	TxTTB Register # 14 (G.832)	R/W	0x00
0xn147	TxTTB Register # 15 (G.832)	R/W	0x00

CLEAR-CHANNEL FRAMER BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS (N = CHANNEL NUMBER)			
CLEAR-CHANNEL FRAMER BLOCK REGISTERS			
0xn148	TxE3 FA1 Error Mask Register (G.832)TxE3 FAS Error Mask Register # 1 (G.751)	R/W	0x00
0xn149	TxE3 FA2 Error Mask Register (G.832)TxE3 FAS Error Mask Register # 2 (G.751)	R/W	0x00
0xn14A	TxE3 BIP-8 Error Mask Register (G.832)TxE3 BIP-4 Error Mask Register (G.751)	R/W	0x00
0xn14B	TxE3 SSM Register	R/W	0x00
0xn14C - 0xn14F	Reserved	R/O	0x00
0xn150	PMON Line Code Violation Count Register - MSB	RUR	0x00
0xn151	PMON Line Code Violation Count Register - LSB	RUR	0x00
0xn152	PMON Framing Bit/Byte Error Count Register - MSB	RUR	0x00
0xn153	PMON Framing Bit/Byte Error Count Register - LSB	RUR	0x00
0xn154	PMON P-Bit/BIP-8/BIP-4 Error Count Register - MSB	RUR	0x00
0xn155	PMON P-Bit/BIP-8/BIP-4 Error Count Register - LSB	RUR	0x00
0xn156	PMON FEBE Event Count Register - MSB	RUR	0x00
0xn157	PMON FEBE Event Count Register - LSB	RUR	0x00
0xn158	PMON CP-Bit Error Count Register - MSB	RUR	0x00
0xn159	PMON CP-Bit Error Count Register - LSB	RUR	0x00
0xn15A	PMON PLCP BIP-8 Error Count Register - MSB	RUR	0x00
0xn15B	PMON PLCP BIP-8 Error Count Register - LSB	RUR	0x00
0xn15C	PMON PLCP Framing Byte Error Count Register - MSB	RUR	0x00
0xn15D	PMON PLCP Framing Byte Error Count Register - LSB	RUR	0x00
0xn15E	PMON PLCP FEBE Event Count Register - MSB	RUR	0x00
0xn15F	PMON PLCP FEBE Event Count Register - LSB	RUR	0x00
0xn160 - 0xn167	Reserved		
0xn168	PRBS Error Count Register - MSB	RUR	0x00
0xn169	PRBS Error Count Register - LSB	RUR	0x00
0xn16A - 0xn16C	Reserved		
0xn16D	One Second Error Status Register	R/O	0x00
0xn16E	One Second Accumulator - LCV Count Register - MSB	R/O	0x00
0xn16F	One Second Accumulator - LCV Count Register - LSB	R/O	0x00

CLEAR-CHANNEL FRAMER BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS (N = CHANNEL NUMBER)			
CLEAR-CHANNEL FRAMER BLOCK REGISTERS			
0xn170	One Second Accumulator - P-Bit/BIP-8/BIP-4 Error Count Register - MSB	R/O	0x00
0xn171	One Second Accumulator - P-Bit/BIP-8/BIP-4 Error Count Register - LSB	R/O	0x00
0xn172	One Second Accumulator - CP Bit Error Count Register - MSB	R/O	0x00
0xn173	One Second Accumulator - CP Bit Error Count Register - LSB	R/O	0x00
0xn174 - 0xn17F	Reserved		
0xn180	Line Interface Drive Register	R/W	0x08
0xn181	Line Interface Scan Register	R/O	0x00
0xn182	Reserved	R/O	0x00
0xn183	Transmit LAPD Byte Count Register	R/W	0x00
0xn184	Receive LAPD Byte Count Register	R/W	0x00
0xn185 - 0xn18F	Reserved	R/O	0x00
0xn190	RxPLCP Configuration & Status Register	R/O & R/W	0x06
0xn191	RxPLCP Interrupt Enable Register	R/W	0x00
0xn192	RxPLCP Interrupt Status Register	RUR	0x00
0xn193 - 0xn197	Reserved		
0xn198	TxPLCP A1 Byte Error Mask Register	R/W	0x00
0xn199	TxPLCP A2 Byte Error Mask Register	R/W	0x00
0xn19A	TxPLCP BIP-8 Byte Error Mask Register	R/W	0x00
0xn19B	TxPLCP G1 Byte Register	R/W	0x00
0xn19C - 0xn2FF	Reserved		

LIU/JITTER ATTENUATOR CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS (N = CHANNEL NUMBER)			
LIU/JITTER ATTENUATOR CONTROL REGISTERS			
0xn300	LIU Transmit APS/Redundancy Control Register	R/W	0x00
0xn301	LIU Interrupt Enable Register	R/W	0x00
0xn302	LIU Interrupt Status Register	RUR	0x00
0xn303	LIU Alarm Status Register	R/O	0x00

LIU/JITTER ATTENUATOR CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS (N = CHANNEL NUMBER)			
LIU/JITTER ATTENUATOR CONTROL REGISTERS			
0xn304	LIU Transmit Control Register	R/W	0x00
0xn305	LIU Receive Control Register	R/W	0x00
0xn306	LIU Channel Control Register	R/W	0x00
0xn307	Jitter Attenuator Control Register	R/W	0x00
0xn308	LIU Receive APS/Redundancy Control Register	R/W	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS (N = CHANNEL NUMBER)			
RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS			
0xn700	Receive ATM Control - Byte 3	R/W	0x00
0xn701	Receive ATM Control - Byte 2	R/W	0x00
0xn702	Receive ATM Control - Byte 1	R/W	0x00
0xn703	Receive ATM Control - Byte 0Receive PPP Control Register	R/W	0x00
0xn704 - 0xn706	Reserved		
0xn707	Receive ATM Status Register	R/O	0x00
0xn708 - 0xn709	Reserved		
0xn70A	Receive ATM Interrupt Status Register -Byte 1	RUR	0x00
0xn70B	Receive ATM Interrupt Status Register - Byte 0Receive PPP Interrupt Status Register	RUR	0x00
0xn70C - 0xn70D	Reserved		
0xn70E	Receive ATM Interrupt Enable Register - Byte 1	R/W	0x00
0xn70F	Receive ATM Interrupt Enable Register - Byte 0Receive PPP Interrupt Enable Register	R/W	0x00
0xn710	Receive PPP Good Packet Count Register - Byte 3	RUR	0x00
0xn711	Receive PPP Good Packet Count Register - Byte 2	RUR	0x00
0xn712	Receive PPP Good Packet Count Register - Byte 1	RUR	0x00
0xn713	Receive ATM Cell Insertion/Extraction Memory Control RegisterReceive PPP Good Packet Count Register - Byte 0	R/O & R/W	0x00
0xn714	Receive ATM Cell Insertion/Extraction Memory Data Register - Byte 3Receive PPP FCS Error Count Register - Byte 3	R/O & R/W	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS (N = CHANNEL NUMBER)			
RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS			
0xn715	Receive ATM Cell Insertion/Extraction Memory Data Register - Byte 2Receive PPP FCS Error Count Register - Byte 2	R/O & R/W	0x00
0xn716	Receive ATM Cell Insertion/Extraction Memory Data Register - Byte 1Receive PPP FCS Error Count Register - Byte 1	R/O & R/W	0x00
0xn717	Receive ATM Cell Insertion/Extraction Memory Data Register - Byte 0Receive PPP FCS Error Count Register - Byte 0	R/O & R/W	0x00
0xn718	Receive ATM Cell UDF Data Register - Byte 3Receive PPP Abort Count Register - Byte 3	R/W & RUR	0x00
0xn719	Receive ATM Cell UDF Data Register - Byte 2Receive PPP Abort Count Register - Byte 2	R/W & RUR	0x00
0xn71A	Receive ATM Cell UDF Data Register - Byte 1Receive PPP Abort Count Register - Byte 1	R/W & RUR	0x00
0xn71B	Receive ATM Cell UDF Data Register - Byte 0Receive PPP Abort Count Register - Byte 0	R/W & RUR	0x00
0xn71C	Receive PPP Runt Frame Count Register - Byte 3	RUR	0x00
0xn71D	Receive PPP Runt Frame Count Register - Byte 2	RUR	0x00
0xn71E	Receive PPP Runt Frame Count Register - Byte 1	RUR	0x00
0xn71F	Receive PPP Runt Frame Count Register - Byte 0	RUR	0x00
0xn720	Receive ATM - Test Cell Header Byte Register - Byte 0	R/W	0x00
0xn721	Receive ATM - Test Cell Header Byte Register - Byte 1	R/W	0x00
0xn722	Receive ATM - Test Cell Header Byte Register - Byte 2	R/W	0x00
0xn723	Receive ATM - Test Cell Header Byte Register - Byte 3	R/W	0x00
0xn724	Receive ATM - Test Cell Error Count Register - Byte 3	RUR	0x00
0xn725	Receive ATM - Test Cell Error Count Register - Byte 2	RUR	0x00
0xn726	Receive ATM - Test Cell Error Count Register - Byte 1	RUR	0x00
0xn727	Receive ATM - Test Cell Error Count Register - Byte 0	RUR	0x00
0xn728	Receive ATM Cell Count Register - Byte 3	RUR	0x00
0xn729	Receive ATM Cell Count Register - Byte 2	RUR	0x00
0xn72A	Receive ATM Cell Count Register - Byte 1	RUR	0x00
0xn72B	Receive ATM Cell Count Register - Byte 0	RUR	0x00
0xn72C	Receive ATM Cell - Discard Cell Count Register - Byte 3	RUR	0x00
0xn72D	Receive ATM Cell - Discard Cell Count Register - Byte 2	RUR	0x00
0xn72E	Receive ATM Cell - Discard Cell Count Register - Byte 1	RUR	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS (N = CHANNEL NUMBER)			
RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS			
0xn72F	Receive ATM Cell - Discard Cell Count Register - Byte 0	RUR	0x00
0xn730	Receive ATM Correctable HEC Byte Error Count Register - Byte 3	RUR	0x00
0xn731	Receive ATM Correctable HEC Byte Error Count Register - Byte 2	RUR	0x00
0xn732	Receive ATM Correctable HEC Byte Error Count Register - Byte 1	RUR	0x00
0xn733	Receive ATM Correctable HEC Byte Error Count Register - Byte 0	RUR	0x00
0xn734	Receive ATM Uncorrectable HEC Byte Error Count Register - Byte 3	RUR	0x00
0xn735	Receive ATM Uncorrectable HEC Byte Error Count Register - Byte 2	RUR	0x00
0xn736	Receive ATM Uncorrectable HEC Byte Error Count Register - Byte 1	RUR	0x00
0xn737	Receive ATM Uncorrectable HEC Byte Error Count Register - Byte 0	RUR	0x00
0xn738 - 0xn742	Reserved		
0xn743	Receive ATM - User Cell Filter # 0 - Filter Control Register	R/W	0x00
0xn744	Receive ATM - User Cell Filter # 0 - Header Byte # 1 Pattern Register	R/W	0x00
0xn745	Receive ATM - User Cell Filter # 0 - Header Byte # 2 Pattern Register	R/W	0x00
0xn746	Receive ATM - User Cell Filter # 0 - Header Byte # 3 Pattern Register	R/W	0x00
0xn747	Receive ATM - User Cell Filter # 0 - Header Byte # 4 Pattern Register	R/W	0x00
0xn748	Receive ATM - User Cell Filter # 0 - Header Byte # 1 Check Register	R/W	0x00
0xn749	Receive ATM - User Cell Filter # 0 - Header Byte # 2 Check Register	R/W	0x00
0xn74A	Receive ATM - User Cell Filter # 0 - Header Byte # 3 Check Register	R/W	0x00
0xn74B	Receive ATM - User Cell Filter # 0 - Header Byte # 4 Check Register	R/W	0x00
0xn74C	Receive ATM - User Cell Filter # 0 - Filtered Cell Count Register - Byte 3	RUR	0x00
0xn74D	Receive ATM - User Cell Filter # 0 - Filtered Cell Count Register - Byte 2	RUR	0x00
0xn74E	Receive ATM - User Cell Filter # 0 - Filtered Cell Count Register - Byte 1	RUR	0x00
0xn74F	Receive ATM - User Cell Filter # 0 - Filtered Cell Count Register - Byte 0	RUR	0x00
0xn750 - 0xn752	Reserved		
0xn753	Receive ATM - User Cell Filter # 1 - Filter Control Register	R/W	0x00
0xn754	Receive ATM - User Cell Filter # 1 - Header Byte # 1 Pattern Register	R/W	0x00
0xn755	Receive ATM - User Cell Filter # 1 - Header Byte # 2 Pattern Register	R/W	0x00
0xn756	Receive ATM - User Cell Filter # 1 - Header Byte # 3 Pattern Register	R/W	0x00
0xn757	Receive ATM - User Cell Filter # 1 - Header Byte # 4 Pattern Register	R/W	0x00
0xn758	Receive ATM - User Cell Filter # 1 - Header Byte # 1 Check Register	R/W	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS (N = CHANNEL NUMBER)			
RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS			
0xn759	Receive ATM - User Cell Filter # 1 - Header Byte # 2 Check Register	R/W	0x00
0xn75A	Receive ATM - User Cell Filter # 1 - Header Byte # 3 Check Register	R/W	0x00
0xn75B	Receive ATM - User Cell Filter # 1 - Header Byte # 4 Check Register	R/W	0x00
0xn75C	Receive ATM - User Cell Filter # 1 - Filtered Cell Count Register - Byte 3	RUR	0x00
0xn75D	Receive ATM - User Cell Filter # 1 - Filtered Cell Count Register - Byte 2	RUR	0x00
0xn75E	Receive ATM - User Cell Filter # 1 - Filtered Cell Count Register - Byte 1	RUR	0x00
0xn75F	Receive ATM - User Cell Filter # 1 - Filtered Cell Count Register - Byte 0	RUR	0x00
0xn760 - 0xn762	Reserved		
0xn763	Receive ATM - User Cell Filter # 2 - Filter Control Register	R/W	0x00
0xn764	Receive ATM - User Cell Filter # 2 - Header Byte # 1 Pattern Register	R/W	0x00
0xn765	Receive ATM - User Cell Filter # 2 - Header Byte # 2 Pattern Register	R/W	0x00
0xn766	Receive ATM - User Cell Filter # 2 - Header Byte # 3 Pattern Register	R/W	0x00
0xn767	Receive ATM - User Cell Filter # 2 - Header Byte # 4 Pattern Register	R/W	0x00
0xn768	Receive ATM - User Cell Filter # 2 - Header Byte # 1 Check Register	R/W	0x00
0xn769	Receive ATM - User Cell Filter # 2 - Header Byte # 2 Check Register	R/W	0x00
0xn76A	Receive ATM - User Cell Filter # 2 - Header Byte # 3 Check Register	R/W	0x00
0xn76B	Receive ATM - User Cell Filter # 2 - Header Byte # 4 Check Register	R/W	0x00
0xn76C	Receive ATM - User Cell Filter # 2 - Filtered Cell Count Register - Byte 3	RUR	0x00
0xn76D	Receive ATM - User Cell Filter # 2 - Filtered Cell Count Register - Byte 2	RUR	0x00
0xn76E	Receive ATM - User Cell Filter # 2 - Filtered Cell Count Register - Byte 1	RUR	0x00
0xn76F	Receive ATM - User Cell Filter # 2 - Filtered Cell Count Register - Byte 0	RUR	0x00
0xn770 - 0xn772	Reserved		
0xn773	Receive ATM - User Cell Filter # 3 - Filter Control Register	R/W	0x00
0xn774	Receive ATM - User Cell Filter # 3 - Header Byte # 1 Pattern Register	R/W	0x00
0xn775	Receive ATM - User Cell Filter # 3 - Header Byte # 2 Pattern Register	R/W	0x00
0xn776	Receive ATM - User Cell Filter # 3 - Header Byte # 3 Pattern Register	R/W	0x00
0xn777	Receive ATM - User Cell Filter # 3 - Header Byte # 4 Pattern Register	R/W	0x00
0xn778	Receive ATM - User Cell Filter # 3 - Header Byte # 1 Check Register	R/W	0x00
0xn779	Receive ATM - User Cell Filter # 3 - Header Byte # 2 Check Register	R/W	0x00
0xn77A	Receive ATM - User Cell Filter # 3 - Header Byte # 3 Check Register	R/W	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS (N = CHANNEL NUMBER)			
RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS			
0xn77B	Receive ATM - User Cell Filter # 3 - Header Byte # 4 Check Register	R/W	0x00
0xn77C	Receive ATM - User Cell Filter # 3 - Filtered Cell Count Register - Byte 3	RUR	0x00
0xn77D	Receive ATM - User Cell Filter # 3 - Filtered Cell Count Register - Byte 2	RUR	0x00
0xn77E	Receive ATM - User Cell Filter # 3 - Filtered Cell Count Register - Byte 1	RUR	0x00
0xn77F	Receive ATM - User Cell Filter # 3 - Filtered Cell Count Register - Byte 0	RUR	0x00
0xn780 - 0xnEFF	Reserved		
0xnF00	Transmit ATM Control Register - Byte 3	R/W	0x00
0xnF01	Transmit ATM Control Register - Byte 2	R/W	0x00
0xnF02	Transmit ATM Control Register - Byte 1	R/W	0x00
0xnF03	Transmit ATM Control Register - Byte 0Transmit PPP Control Register - Byte 2	R/W	0x00
0xnF04	Transmit ATM Status Register - Byte 3	R/O	0x00
0xnF05	Transmit ATM Status Register - Byte 2	R/O	0x00
0xnF06	Transmit ATM Status Register - Byte 1	R/O	0x00
0xnF07	Transmit ATM Status Register - Byte 0	R/O	0x00
0xnF08 - 0xnF0A	Reserved		
0xnF0B	Transmit ATM Cell Processor Interrupt Status RegisterTransmit PPP Interrupt Status Register	RUR	0x00
0xnF0C - 0xnF0E	Reserved		
0xnF0F	Transmit ATM Cell Processor Interrupt Enable Register Transmit PPP Interrupt Enable Register	R/W	0x00
0xnF10 - 0xnF12	Reserved		
0xnF13	Transmit ATM Cell Insertion/Extraction Memory Control Register	R/O & R/W	0x00
0xnF14	Transmit ATM Cell Insertion/Extraction Data Register - Byte 3	R/O & R/W	0x00
0xnF15	Transmit ATM Cell Insertion/Extraction Data Register - Byte 2	R/O & R/W	0x00
0xnF16	Transmit ATM Cell Insertion/Extraction Data Register - Byte 1	R/O & R/W	0x00
0xnF17	Transmit ATM Cell Insertion/Extraction Data Register - Byte 0	R/O & R/W	0x00
0xnF18	Transmit ATM - Idle Cell Header Byte # 1 Register	R/W	0x00
0xnF19	Transmit ATM - Idle Cell Header Byte # 2 Register	R/W	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS (N = CHANNEL NUMBER)			
RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS			
0xnF1A	Transmit ATM - Idle Cell Header Byte # 3 Register	R/W	0x00
0xnF1B	Transmit ATM - Idle Cell Header Byte # 4 Register	R/W	0x00
0xnF1C - 0xnF1E	Reserved		
0xnF1F	Transmit ATM - Idle Cell Payload Byte Register	R/W	0x00
0xnF20	Transmit ATM - Test Cell Header Byte # 1 Register	R/W	0x00
0xnF21	Transmit ATM - Test Cell Header Byte # 2 Register	R/W	0x00
0xnF22	Transmit ATM - Test Cell Header Byte # 3 Register	R/W	0x00
0xnF23	Transmit ATM - Test Cell Header Byte # 4 Register	R/W	0x00
0xnF24 - 0xnF27	Reserved		
0xnF28	Transmit ATM Cell Count Register - Byte 3	RUR	0x00
0xnF29	Transmit ATM Cell Count Register - Byte 2	RUR	0x00
0xnF2A	Transmit ATM Cell Count Register - Byte 1	RUR	0x00
0xnF2B	Transmit ATM Cell Count Register - Byte 0	RUR	0x00
0xnF2C	Transmit ATM - Discarded Cell Count Register - Byte 3	RUR	0x00
0xnF2D	Transmit ATM - Discarded Cell Count Register - Byte 2	RUR	0x00
0xnF2E	Transmit ATM - Discarded Cell Count Register - Byte 1	RUR	0x00
0xnF2F	Transmit ATM - Discarded Cell Count Register - Byte 0	RUR	0x00
0xnF30	Transmit ATM HEC Byte Error Count Register - Byte 3	RUR	0x00
0xnF31	Transmit ATM HEC Byte Error Count Register - Byte 2	RUR	0x00
0xnF32	Transmit ATM HEC Byte Error Count Register - Byte 1	RUR	0x00
0xnF33	Transmit ATM HEC Byte Error Count Register - Byte 0	RUR	0x00
0xnF34	Transmit ATM Cell Processor - Parity Error Count Register - Byte 3	RUR	0x00
0xnF35	Transmit ATM Cell Processor - Parity Error Count Register - Byte 2	RUR	0x00
0xnF36	Transmit ATM Cell Processor - Parity Error Count Register - Byte 1	RUR	0x00
0xnF37	Transmit ATM Cell Processor - Parity Error Count Register - Byte 0	RUR	0x00
0xnF38 - 0xnF42	Reserved		
0xnF43	Transmit ATM - User Cell Filter # 0 - Filter Control Register	R/W	0x00
0xnF44	Transmit ATM - User Cell Filter # 0 - Header Byte # 1 Pattern Register	R/W	0x00
0xnF45	Transmit ATM - User Cell Filter # 0 - Header Byte # 2 Pattern Register	R/W	0x00
0xnF46	Transmit ATM - User Cell Filter # 0 - Header Byte # 3 Pattern Register	R/W	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS (N = CHANNEL NUMBER)			
RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS			
0xnF47	Transmit ATM - User Cell Filter # 0 - Header Byte # 4 Pattern Register	R/W	0x00
0xnF48	Transmit ATM - User Cell Filter # 0 - Header Byte # 1 Check Register	R/W	0x00
0xnF49	Transmit ATM - User Cell Filter # 0 - Header Byte # 2 Check Register	R/W	0x00
0xnF4A	Transmit ATM - User Cell Filter # 0 - Header Byte # 3 Check Register	R/W	0x00
0xnF4B	Transmit ATM - User Cell Filter # 0 - Header Byte # 4 Check Register	R/W	0x00
0xnF4C	Transmit ATM - User Cell Filter # 0 - Filtered Cell Count Register - Byte 3	RUR	0x00
0xnF4D	Transmit ATM - User Cell Filter # 0 - Filtered Cell Count Register - Byte 2	RUR	0x00
0xnF4E	Transmit ATM - User Cell Filter # 0 - Filtered Cell Count Register - Byte 1	RUR	0x00
0xnF4F	Transmit ATM - User Cell Filter # 0 - Filtered Cell Count Register - Byte 0	RUR	0x00
0xnF50 - 0xnF52	Reserved		
0xnF53	Transmit ATM - User Cell Filter # 1 - Filter Control Register	R/W	0x00
0xnF54	Transmit ATM - User Cell Filter # 1 - Header Byte # 1 Pattern Register	R/W	0x00
0xnF55	Transmit ATM - User Cell Filter # 1 - Header Byte # 2 Pattern Register	R/W	0x00
0xnF56	Transmit ATM - User Cell Filter # 1 - Header Byte # 3 Pattern Register	R/W	0x00
0xnF57	Transmit ATM - User Cell Filter # 1 - Header Byte # 4 Pattern Register	R/W	0x00
0xnF58	Transmit ATM - User Cell Filter # 1 - Header Byte # 1 Check Register	R/W	0x00
0xnF59	Transmit ATM - User Cell Filter # 1 - Header Byte # 2 Check Register	R/W	0x00
0xnF5A	Transmit ATM - User Cell Filter # 1 - Header Byte # 3 Check Register	R/W	0x00
0xnF5B	Transmit ATM - User Cell Filter # 1 - Header Byte # 4 Check Register	R/W	0x00
0xnF5C	Transmit ATM - User Cell Filter # 1 - Filtered Cell Count Register - Byte 3	RUR	0x00
0xnF5D	Transmit ATM - User Cell Filter # 1 - Filtered Cell Count Register - Byte 2	RUR	0x00
0xnF5E	Transmit ATM - User Cell Filter # 1 - Filtered Cell Count Register - Byte 1	RUR	0x00
0xnF5F	Transmit ATM - User Cell Filter # 1 - Filtered Cell Count Register - Byte 0	RUR	0x00
0xnF60 - 0xnF62	Reserved		
0xnF63	Transmit ATM - User Cell Filter # 2 - Filter Control Register	R/W	0x00
0xnF64	Transmit ATM - User Cell Filter # 2 - Header Byte # 1 Pattern Register	R/W	0x00
0xnF65	Transmit ATM - User Cell Filter # 2 - Header Byte # 2 Pattern Register	R/W	0x00
0xnF66	Transmit ATM - User Cell Filter # 2 - Header Byte # 3 Pattern Register	R/W	0x00
0xnF67	Transmit ATM - User Cell Filter # 2 - Header Byte # 4 Pattern Register	R/W	0x00
0xnF68	Transmit ATM - User Cell Filter # 2 - Header Byte # 1 Check Register	R/W	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS (N = CHANNEL NUMBER)			
RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS			
0xnF69	Transmit ATM - User Cell Filter # 2 - Header Byte # 2 Check Register	R/W	0x00
0xnF6A	Transmit ATM - User Cell Filter # 2 - Header Byte # 3 Check Register	R/W	0x00
0xnF6B	Transmit ATM - User Cell Filter # 2 - Header Byte # 4 Check Register	R/W	0x00
0xnF6C	Transmit ATM - User Cell Filter # 2 - Filtered Cell Count Register - Byte 3	RUR	0x00
0xnF6D	Transmit ATM - User Cell Filter # 2 - Filtered Cell Count Register - Byte 2	RUR	0x00
0xnF6E	Transmit ATM - User Cell Filter # 2 - Filtered Cell Count Register - Byte 1	RUR	0x00
0xnF6F	Transmit ATM - User Cell Filter # 2 - Filtered Cell Count Register - Byte 0	RUR	0x00
0xnF70 - 0xnF72	Reserved		
0xnF73	Transmit ATM - User Cell Filter # 3 - Filter Control Register	R/W	0x00
0xnF74	Transmit ATM - User Cell Filter # 3 - Header Byte # 1 Pattern Register	R/W	0x00
0xnF75	Transmit ATM - User Cell Filter # 3 - Header Byte # 2 Pattern Register	R/W	0x00
0xnF76	Transmit ATM - User Cell Filter # 3 - Header Byte # 3 Pattern Register	R/W	0x00
0xnF77	Transmit ATM - User Cell Filter # 3 - Header Byte # 4 Pattern Register	R/W	0x00
0xnF78	Transmit ATM - User Cell Filter # 3 - Header Byte # 1 Check Register	R/W	0x00
0xnF79	Transmit ATM - User Cell Filter # 3 - Header Byte # 2 Check Register	R/W	0x00
0xnF7A	Transmit ATM - User Cell Filter # 3 - Header Byte # 3 Check Register	R/W	0x00
0xnF7B	Transmit ATM - User Cell Filter # 3 - Header Byte # 4 Check Register	R/W	0x00
0xnF7C	Transmit ATM - User Cell Filter # 3 - Filtered Cell Count Register - Byte 3	RUR	0x00
0xnF7D	Transmit ATM - User Cell Filter # 3 - Filtered Cell Count Register - Byte 2	RUR	0x00
0xnF7E	Transmit ATM - User Cell Filter # 3 - Filtered Cell Count Register - Byte 1	RUR	0x00
0xnF7F	Transmit ATM - User Cell Filter # 3 - Filtered Cell Count Register - Byte 0	RUR	0x00
0xnF80 - 0xnFFF	Reserved		

OPERATION BLOCK INTERRUPT REGISTER BIT FORMATS

OPERATION CONTROL REGISTER - BYTE 3 (ADDRESS = 0X0100)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							Configuration Control
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 6	Unused	R/O	
0	Configuration Control	R/W	**Configuration Control:** This READ/WRITE bit-field permits the user to configure the XRT79L74 device to support any of the following configurations. • ATM/PPP • Clear Channel/HDLC The following table presents the relationship between the value written into these register bits and the corresponding Mode of operation.

Configuration Control	Mode
0	ATM/PPP
1	Clear Channel/HDLC

OPERATION CONTROL REGISTER - BYTE 2 (ADDRESS = 0X0101)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					Interrupt WC/INT*	Enable Interrupt Auto-Clear	Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 3	Unused	R/O	Please set to "0" for normal operation.
2	Interrupt Write to Clear/ RUR	R/W	**Interrupt - Write to Clear/RUR Select:** This READ/WRITE bit-field permits the user to configure all of the "Source-Level" Interrupt Status bits (within the XRT79L74 device) to either be "Write to Clear" (WTC) or "Reset-upon-Read" (RUR) bits. 0 - Configures all "Source-Level" Interrupt Status register bits to function as "Reset-upon-Read" (RUR). 1 - Configures all "Source-Level" Interrupt Status register bits to function as "Write-to-Clear" (WTC).

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	Enable Interrupt Clear	R/W	**Enable Auto-Clear of Interrupts Select:** This READ/WRITE bit-field permits the user to configure the XRT79L74 device to automatically disable all interrupts that are activated. 0 - Configures the chip to NOT automatically disable any Interrupts following their activation. 1 - Configures the chip to automatically disable all Interrupts following their activation.
0	Interrupt Enable	R/W	**Interrupt Enable:** This READ/WRITE bit-field permits the user to configure the XRT79L74 device to generate interrupt requests to the Microprocessor. 0 - Configures the chip to NOT generate interrupt to the Microprocessor. All interrupts are disabled and the Microprocessor must poll the register bits. 1 - Configures the chip to generate interrupts the Microprocessor.

OPERATION CONTROL - LOOP-BACK CONTROL REGISTER (ADDRESS = 0X0102)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Loop-back Control [3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3 - 0	Loop-back Control [3:0]	R/W	**Loop-back Mode Select:** These READ/WRITE bit-fields permit the user to configure the XRT79L74 to operate in any of the following loop-back modes. • Local Medium Loop-back • Remote Host Loop-back The following table presents the contents of these bit-fields and the corresponding Loop-back Modes.

Loop-back Control [3:0]	Resulting Loop-back Mode
0000 - 0011	Reserved
0100	Local Medium Loop-back Mode
0101	Remote Host Loop-back Mode
0110 - 1111	Reserved

OPERATION CONTROL REGISTER - BYTE 0 (ADDRESS = 0X0103)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit UTOPIA PLL OFF	Receive UTOPIA PLL OFF	Reserved			PPP/ATM*	Reserved	Software RESET*
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Transmit UTOPIA PLL OFF	R/W	
6	Receive UTOPIA PLL OFF	R/W	
5 - 3	Unused	R/O	
2	PPP/ATM*	R/W	**PPP/ATM UNI Mode Select:** This READ-WRITE bit-field permits the user to configure the XRT79L74 device to operate in either the ATM UNI or PPP Mode. If Bit 3 (Dual Bus), within the "Operation Control Register - Byte 3" is set to "0", then this bit-field will then dictate the operating mode of the XRT79L74 device. 0 - Configures the "Dedicated" UTOPIA/POS-PHY bus to operate in the UTOPIA (ATM) Mode. 1 - Configures the "Dedicated" UTOPIA/POS-PHY Bus to operate in the POS-PHY Mode. ***NOTE:*** *This bit-field is ignored if Bit 3 (Dual-Bus) within the "Operation Control Register - Byte 3" is set to "1".*
1	Reserved	R/O	
0	Software RESET	R/W	**Software RESET:** This READ-WRITE bit-field permits the user to reset the XRT79L74 device. 0 - Configure the XRT79L74 device into RESET mode. 1 - Normal operation.

DEVICE ID REGISTER (ADDRESS = 0X0104)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DEVICE_ID_VALUE [7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	1	1	1	1	1	0	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Device ID Value	R/O	**Device ID Value:** This READ-ONLY bit-field is set to the value "0x7D" and permits the user's software code to uniquely identify this device as the XRT79L74 device.

REVISION ID REGISTER (ADDRESS = 0X0105)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Revision Number Value							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Revision Number Value	R/O	**Revision Number Value:** This READ-ONLY bit-field is set to the value that corresponds to its revision number. Revision A silicon will be set to the value "0x01". This register permits the user's software code to uniquely identify the revision number of the XRT79L74 device.

OPERATION INTERRUPT STATUS REGISTER - BYTE 1 (ADDRESS = 0X0112)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				DS3/E3 LIU/JA Block Interrupt Status	DS3/E3 Framer Block Interrupt Status	Unused	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	DS3/E3 LIU/JA Block Interrupt Status	R/O	**DS3/E3 LIU/JA Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not a "DS3/E3 LIU/JA Block" interrupt is awaiting service. 0 - No "DS3/E3 LIU/JA" block interrupt is awaiting service. 1 - At least one "DS3/E3 LIU/JA" block interrupt is awaiting service.
2	DS3/E3 Framer Block Interrupt Status	R/O	**DS3/E3 Framer Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not a "DS3/E3 Framer Block" interrupt is awaiting service. 0 - No "DS3/E3 Framer" block interrupt is awaiting service. 1 - At least one "DS3/E3 Framer" block interrupt is awaiting service.
1 - 0	Unused	R/O	

OPERATION INTERRUPT STATUS REGISTER - BYTE 0 (ADDRESS = 0X0113)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive UTOPIA/ POS-PHY Interface Block Interrupt Status	Unused		Receive ATM Cell/PPP Processor Block Interrupt Status	Transmit UTOPIA/ POS-PHY Interface Block Interrupt Status	Unused		Transmit ATM Cell/PPP Processor Block Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Receive UTOPIA POS-PHY Interface Block Interrupt Status	R/O	**Receive UTOPIA/POS-PHY Interface Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not a "Receive UTOPIA/POS-PHY Interface" block interrupt is awaiting service. 0 - No "Receive UTOPIA/POS-PHY Interface" block interrupt is awaiting service. 1 - At least one "Receive UTOPIA/POS-PHY Interface" block interrupt is awaiting service.
6 -5	Unused	R/O	
4	Receive ATM Cell/PPP Processor Block Interrupt Status	R/O	**Receive ATM Cell/PPP Processor Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not a "Receive ATM Cell/PPP Processor Block" Interrupt is awaiting service. 0 - No "Receive ATM Cell/PPP Processor block" interrupt is awaiting service. 1 - At least one "Receive ATM Cell/PPP Processor" block interrupt is awaiting service.
3	Transmit UTOPIA POS-PHY Interface Block Interrupt Status		**Transmit UTOPIA/POS-PHY Interface Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not a "Transmit UTOPIA/POS-PHY Interface" block interrupt is awaiting service. 0 - No "Transmit UTOPIA/POS-PHY Interface" block interrupt is awaiting service. 1 - At least one "Transmit UTOPIA/POS-PHY Interface" block interrupt is awaiting service.
2 - 1	Unused	R/O	
0	Transmit ATM Cell/PPP Processor Block Interrupt Status	R/O	**Receive ATM Cell/PPP Processor Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not a "Receive ATM Cell/PPP Processor Block" Interrupt is awaiting service. 0 - No "Receive ATM Cell/PPP Processor block" interrupt is awaiting service. 1 - At least one "Receive ATM Cell/PPP Processor" block interrupt is awaiting service.

OPERATION INTERRUPT ENABLE REGISTER - BYTE 1 (ADDRESS = 0X0116)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				DS3/E3 LIU/JA Block Interrupt Enable	DS3/E3 Framer Block Interrupt Enable	Unused	
R/O	R/O	R/O	R/O	R/W	R/W	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused		
3	DS3/E3 LIU/JA Block Interrupt Enable	R/W	**DS3/E3 LIU/JA Block Interrupt Enable:** This READ/WRITE bit permit the user to either enable or disable the DS3/E3 LIU/JA Block for interrupt generation. If the user writes a "0" to this register bit and disables the "DS3/E3 LIU/JA Block" (for interrupt generation), then all "DS3/E3 LIU/JA Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "DS3/E3 LIU/JA Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 - Disable all "DS3/E3 LIU/JA Block" interrupts within the device. 1 - Enables the "DS3/E3 LIU/JA Block" at the "Block-Level".
2	DS3/E3 Framer Block Interrupt Enable	R/W	**DS3/E3 Framer Block Interrupt Enable:** This READ/WRITE bit permits the user to either enable or disable the DS3/E3 Framer Block for interrupt generation. If the user writes a "0" to this register bit and disables the "DS3/E3 Framer Block" (for interrupt generation), then all "DS3/E3 Framer Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "DS3/E3 Framer Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 - Disable all "DS3/E3 Framer Block" interrupts within the device. 1 - Enables the "DS3/E3 Framer Block" at the "Block-Level".
1 - 0	Unused		

OPERATION INTERRUPT ENABLE REGISTER - BYTE 0 (ADDRESS = 0X0117)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive UTOPIA/ POS-PHY Interface Block Interrupt Enable	Unused		Receive ATM Cell/PPP Processor Block Interrupt Enable	Transmit UTOPIA/ POS-PHY Interface Block Interrupt Enable	Unused		Transmit ATM Cell/PPP Processor Block Interrupt Enable
R/W	R/O	R/O	R/W	R/W	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Receive UTOPIA/POS-PHY Interface Block Interrupt Enable	R/W	**Receive UTOPIA/POS-PHY Interface Block Interrupt Enable:** This READ/WRITE bit permit the user to either enable or disable the Receive UTOPIA/POS-PHY Interface Block for interrupt generation. If the user writes a "0" to this register bit and disables the "Receive UTOPIA/POS-PHY Interface Block" (for interrupt generation), then all "Receive UTOPIA/POS-PHY Interface Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Receive UTOPIA/POS-PHY Interface Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 - Disable all "Receive UTOPIA/POS-PHY Interface Block" interrupts within the device. 1 - Enables the "Receive UTOPIA/POS-PHY Interface Block" at the "Block-Level".
6 - 5	Unused	R/O	
4	Receive ATM Cell/PPP Processor Block Interrupt Enable	R/W	**Receive ATM Cell/PPP Processor Block Interrupt Enable:** This READ/WRITE bit permit the user to either enable or disable the Receive ATM Cell/PPP Processor Block for interrupt generation. If the user writes a "0" to this register bit and disables the "Receive ATM Cell/PPP Processor Block" (for interrupt generation), then all "Receive ATM Cell/PPP Processor Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Receive ATM Cell/PPP Processor Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 - Disable all "Receive ATM Cell/PPP Processor Block" interrupts within the device. 1 - Enables the "Receive ATM Cell/PPP Processor Block" at the "Block-Level".

BIT NUMBER	NAME	TYPE	DESCRIPTION
3	Transmit UTOPIA/POS-PHY Interface Block Interrupt Enable	R/W	**Transmit UTOPIA/POS-PHY Interface Block Interrupt Enable:** This READ/WRITE bit permit the user to either enable or disable the Transmit UTOPIA/POS-PHY Interface Block for interrupt generation. If the user writes a "0" to this register bit and disables the "Transmit UTOPIA/POS-PHY Interface Block" (for interrupt generation), then all "Transmit UTOPIA/POS-PHY Interface Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Transmit UTOPIA/POS-PHY Interface Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 - Disable all "Transmit UTOPIA/POS-PHY Interface Block" interrupts within the device. 1 - Enables the "Transmit UTOPIA/POS-PHY Interface Block" at the "Block-Level".
2 - 1	Unused	R/O	
0	Transmit ATM Cell/PPP Processor Block Interrupt Enable	R/W	**Transmit ATM Cell/PPP Processor Block Interrupt Enable:** This READ/WRITE bit permit the user to either enable or disable the Transmit ATM Cell/PPP Processor Block for interrupt generation. If the user writes a "0" to this register bit and disables the "Transmit ATM Cell/PPP Processor Block" (for interrupt generation), then all "Transmit ATM Cell/PPP Processor Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Transmit ATM Cell/PPP Processor Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 - Disable all "Transmit ATM Cell/PPP Processor Block" interrupts within the device. 1 - Enables the "Transmit ATM Cell/PPP Processor Block" at the "Block-Level".

CHANNEL INTERRUPT INDICATION REGISTERS

CHANNEL INTERRUPT INDICATOR - RECEIVE CELL PROCESSOR/PPP PROCESSOR BLOCK (ADDRESS = 0X0119)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							Receive Cell Processor Block Interrupt
R/O							R/O
0							0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 1	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Receive Cell Processor Block Interrupt - XRT79L74	R/O	**Receive Cell Processor Block Interrupt - XRT79L74:** This READ/ONLY bit-field indicates whether or not the "Receive Cell Processor" block, associated with XRT79L74 is declaring an Interrupt, as described below. 0 - The Receive Cell Processor block, associated with XRT79L74 is NOT declaring an Interrupt. 1 - The Receive Cell Processor block, associated with XRT79L74 is currently declaring an interrupt.

CHANNEL INTERRUPT INDICATOR - LIU/JITTER ATTENUATOR BLOCK (ADDRESS = 0X011D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							LIU/JA Block Interrupt
R/O							R/O
0							0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 1	Unused	R/O	
0	LIU/JA Block Interrupt - XRT79L74	R/O	**LIU/JA Block Interrupt - XRT79L74:** This READ/ONLY bit-field indicates whether or not the "LIU/JA" block, associated with XRT79L74 is declaring an Interrupt, as described below. 0 - The LIU/JA block, associated with XRT79L74 is NOT declaring an Interrupt. 1 - The LIU/JA block, associated with XRT79L74 is currently declaring an interrupt.

CHANNEL INTERRUPT INDICATOR - TRANSMIT CELL PROCESSOR/PPP PROCESSOR BLOCK (ADDRESS = 0X0121)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							Transmit Cell Processor Block Interrupt
R/O							R/O
0							

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 1	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Transmit Cell Processor Block Interrupt - XRT79L74	R/O	**Transmit Cell Processor Block Interrupt - XRT79L74:** This READ/ONLY bit-field indicates whether or not the "Transmit Cell Processor" block, associated with XRT79L74 is declaring an Interrupt, as described below. 0 - The Transmit Cell Processor block, associated with XRT79L74 is NOT declaring an Interrupt. 1 - The Transmit Cell Processor block, associated with XRT79L74 is currently declaring an interrupt.

CHANNEL INTERRUPT INDICATOR - DS3/E3 FRAMER BLOCK (ADDRESS = 0X0127)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							DS3/E3 Framer Block Interrupt
R/O							R/O
0							0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 1	Unused	R/O	
0	DS3/E3 Framer Block Interrupt - XRT79L74	R/O	**DS3/E3 Framer Block Interrupt - XRT79L74:** This READ/ONLY bit-field indicates whether or not the "DS3/E3 Framer" block, associated with XRT79L74 is declaring an Interrupt, as described below. 0 - The DS3/E3 Framer block, associated with XRT79L74 is NOT declaring an Interrupt. 1 - The DS3/E3 Framer block, associated with XRT79L74 is currently declaring an interrupt.

OPERATION GENERAL PURPOSE PIN DATA REGISTER (ADDRESS = 0X0147)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				General Purpose Data [3]	General Purpose Data [2]	General Purpose Data [1]	General Purpose Data [0]
R/O				R/W	R/W	R/W	R/W
0				0	0	0	0

OPERATION GENERAL PURPOSE PIN DIRECTION CONTROL REGISTER (ADDRESS = 0X014B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				General Purpose Pin Direction [3]	General Purpose Pin Direction [2]	General Purpose Pin Direction [1]	General Purpose Pin Direction [0]
R/O				R/W	R/W	R/W	R/W
0				0	0	0	0

RECEIVE UTOPIA INTERFACE BLOCK

This section presents the Register Description/Address Map of the control registers associated with the Receive UTOPIA/POS-PHY Interface block.

TABLE 1: RECEIVE UTOPIA/POS-PHY INTERFACE BLOCK - REGISTER/ADDRESS MAP

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
RECEIVE UTOPIA/POS-PHY- CONTROL REGISTERS			
0x0501	Receive UTOPIA/POS-PHY Control Register - Byte 2	R/W	0x00
0x0502	Receive UTOPIA/POS-PHY Control Register - Byte 1	R/W	0x00
0x0503	Receive UTOPIA/POS-PHY Control Register - Byte 0	R/W	0x00
0x0504 - 0x0512	Reserved	R/O	0x00
0x0513	Receive UTOPIA Port Address Register	R/W	0x00
0x0514 - 0x0516	Reserved	R/O	0x00
0x0517	Receive UTOPIA Port Number Register	R/W	0x00
0x0518 - 0x0580	Reserved	R/O	0x00

RECEIVE UTOPIA/POS-PHY CONTROL REGISTER - BYTE 0 (ADDRESS = 0X0503)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UTOPIA Level 3 Disable	Multi-PHY Polling Enable	Back to Back Polling Enable	Direct Status Indication Enable	UTOPIA/POS-PHY Data Bus Width		Cell Size[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	UTOPIA Level 3 Disable	R/W	
6	Multi-PHY Polling Enable	R/W	**Multi-PHY Polling Enable:** This READ/WRITE bit-field permits the user to either enable or disable Multi-PHY Polling for the Receive UTOPIA Interface block. If the user implements this feature (and configures the XRT79L74 device to operate in the Multi-PHY Mode) then the RxUClav output pin will be driven (either "high" or "low") based upon the fill-status of the Receive FIFO within the Channel that corresponds to the "Receive UTOPIA Address" that is currently being applied to the "RxUAddr[4:0]" input pins. If the user does not implement this feature (and then configures the XRT79L74 device to operate in the Single-PHY Mode), then the "RxUClav" output pin will unconditionally reflect the "Receive FIFO fill-status" for Channel 0. No attention will be paid to the address values placed upon the "RxUAddr[4:0]" input pins. 0 - Configures the Receive UTOPIA Interface block to operate in the Single-PHY Mode. 1 - Configures the Receive UTOPIA Interface block to operate in the Multi-PHY Mode.

<table>
<tr><th>BIT NUMBER</th><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>5</td><td>Back-to-Back Polling Enable</td><td>R/W</td><td>Back-to-Back Polling Enable:
This READ/WRITE bit-field permits the user to configure the Receive UTOPIA Interface block to support "Back-to-Back Polling".
Ordinarily, for Multi-PHY polling, the user is required to interleave all UTOPIA Address values (that are to be placed on the "RxUAddr[4:0]" input pins) with the NULL Address (e.g., 0xnF). However, if the user configures the Receive UTOPIA Interface block to operate in the "UTOPIA Level 3" Mode, and if the user also enables "Back-to-Back Polling", then he/she does not need interleave the UTOPIA Addresses with the NULL Address. In this case, the user can simply apply a "back-to-back" stream of "relevant" UTOPIA Addresses to the "RxUAddr[4:0]" input pins, and the XRT79L74 device will respond by driving the RxUClav output pins to the appropriate states (depending upon the Receive FIFO fill-status).
0 - Disables "Back-to-Back" Polling. In this mode, the user must interleave all UTOPIA Addresses (that are to be applied to the "RxUAddr[4:0]" input pins) with the NULL Address.
1 - Enables "Back-to-Back" Polling. In this mode, the user does not need to interleave all UTOPIA Addresses (that are to be applied to the "RxUAddr[4:0]" input pins) with the NULL Address.
NOTE: In order to configure the Receive UTOPIA Interface block to operate in the "Back-to-Back Polling" Mode, the user must also do the following.
a. Configure the Receive UTOPIA Interface to operate in the "UTOPIA Level 3" Mode. This is accomplished by setting Bit 7 (UTOPIA Level 3 Disable) within this Register to "0".
b. Configure the Receive UTOPIA Interface to support "Multi-PHY" Polling. This is accomplished by setting Bit 6 (Multi-PHY Polling Enable) within this register to "1".</td></tr>
<tr><td>4</td><td>Direct Status Indication Enable</td><td>R/W</td><td></td></tr>
<tr><td>3 - 2</td><td>UTOPIA/POS-PHY Data Bus Width[1:0]</td><td>R/W</td><td>UTOPIA/POS-PHY Data Bus Width[1:0]:
These READ/WRITE bit-fields permit the user to select the width of the Receive UTOPIA and POS-PHY Data Buses. The relationship between the contents of these bit-fields and the corresponding widths of the Receive UTOPIA and POS-PHY Data Bus is tabulated below.
<table>
<tr><th colspan="2">UTOPIA/POS-PHY Data Bus Width[1:0]</th><th>Corresponding UTOPIA/POS-PHY Data Bus Width</th></tr>
<tr><td>0</td><td>0</td><td>Not Valid</td></tr>
<tr><td>0</td><td>1</td><td>8 bits</td></tr>
<tr><td>1</td><td>0</td><td>16 bits</td></tr>
<tr><td>1</td><td>1</td><td>Not Valid</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT NUMBER</th><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>1 - 0</td><td>Cell Size[1:0]</td><td></td><td>
Cell Size[1:0]:
These two READ/WRITE bit-fields permit the user to specify the size of the ATM cell that will be handled by the Receive UTOPIA Interface blocks. The relationship between the contents of these bit-fields and the corresponding Cell Sizes are tabulated below.
<table>
<tr><th colspan="2">Cell Size[1:0]</th><th>Resulting Cell Size (Bytes)</th></tr>
<tr><td>0</td><td>0</td><td>52 bytes</td></tr>
<tr><td>0</td><td>1</td><td>53 bytes (Only valid for UTOPIA Level 1, and if the UTOPIA Data Bus Width is set to 8 bits)</td></tr>
<tr><td>1</td><td>0</td><td>54 bytes (Only valid for UTOPIA Levels 1 and 2)</td></tr>
<tr><td>1</td><td>1</td><td>56 bytes</td></tr>
</table>
NOTE: The user must bear in mind the UTOPIA Level and the UTOPIA Data Bus width selected, when selecting the Cell Size.
</td></tr>
</table>

RECEIVE UTOPIA PORT ADDRESS REGISTER (ADDRESS = 0X0513)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Receive UTOPIA Port Address[4:0]				
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	
4 - 0	Receive UTOPIA Port Address[4:0]	R/W	**Receive UTOPIA Port Address[4:0]:** These READ/WRITE register bits, along with the "Receive UTOPIA Port Number[4:0]" bits (within the "Receive UTOPIA Port Number" Register (Address = 0x0517) permit the user to assign a unique Receive UTOPIA address to each of the XRT79L74 device. For UTOPIA Level 2/3 applications, the user can write in any value, ranging from 0x00 through 0x1E into this register. **The Receive UTOPIA Address Assignment Procedure:** In order to assign a UTOPIA Address to a given Channel (or Port) within the XRT79L74 device, the user must do the following. **a.** Write the value corresponding to a given XRT79L74 Channel into the "Receive UTOPIA Port Number" Register (Address = 0x0517). **b.** Write the corresponding UTOPIA Address value into this register. Once this "two-step" procedure has been executed, then the XRT79L74 Channel (as specified during step "a") will be assigned the "Receive UTOPIA Address" value (as specified during step "b").

RECEIVE UTOPIA PORT NUMBER REGISTER (ADDRESS = 0X0517)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Receive UTOPIA Port Number[4:0]				
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
4 - 0	Receive UTOPIA Port Number[4:0]	R/W	**Receive UTOPIA Port Number[4:0]:** These READ/WRITE register bits, along with the "Receive UTOPIA Port Address[4:0]" bits (within the "Receive UTOPIA Port Address" Register (Address = 0x0513) permit the user to assign a unique Receive UTOPIA address to the XRT79L74 device. **The Receive UTOPIA Address Assignment Procedure:** In order to assign a UTOPIA Address to a given Channel (or Port) within the XRT79L74 device, the user must do the following. **a.** Write the value corresponding to a given XRT79L74 Channel into this register. **b.** Write the corresponding UTOPIA Address value into the "Receive UTOPIA Port Address" Register (Address = 0x0513). Once this "two-step" procedure has been executed, then the XRT79L74 Channel (as specified during step "a") will be assigned the "Receive UTOPIA Address" value (as specified during step "b").

TRANSMIT UTOPIA INTERFACE BLOCK

This section presents the Register Description/Address Map of the control registers associated with the Transmit UTOPIA/POS-PHY Interface blocks.

TABLE 2: TRANSMIT UTOPIA INTERFACE BLOCK - REGISTER/ADDRESS MAP

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
TRANSMIT UTOPIA/POS-PHY CONTROL REGISTERS			
0x0581	Transmit UTOPIA/POS-PHY Control Register - Byte 2	R/W	0x38
0x0582	Transmit UTOPIA/POS-PHY Control Register - Byte 1	R/W	0x00
0x0583	Transmit UTOPIA/POS-PHY Control Register - Byte 0	R/W	0x00
0x0584 - 0x0592	Reserved	R/O	0x00
0x0593	Transmit UTOPIA Port Address Register	R/W	0x00
0x0594 - 0x0596	Reserved	R/O	0x00
0x0597	Transmit UTOPIA Port Number Register	R/W	0x00
0x0598 - 0x10FF	Reserved	R/O	0x00

TRANSMIT UTOPIA/POS-PHY CONTROL REGISTER - BYTE 0 (ADDRESS = 0X0583)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UTOPIA Level 3 Disable	Multi-PHY Polling Enable	Back to Back Polling Enable	Direct Status Indication Enable	UTOPIA/POS-PHY Data Bus Width		Cell Size[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	UTOPIA Level 3 Disable	R/W	
6	Multi-PHY Polling Enable	R/W	**Multi-PHY Polling Enable:** This READ/WRITE bit-field permits the user to either enable or disable Multi-PHY Polling for the Transmit UTOPIA Interface block. If the user implements this feature (and configures the XRT79L74 device to operate in the Multi-PHY Mode) then the TxUClav output pin will be driven (either "high" or "low") based upon the fill-status of the Transmit FIFO within the Channel that corresponds to the "Transmit UTOPIA Address" that is currently being applied to the "TxUAddr[4:0]" input pins. If the user does not implement this feature (and then configures the XRT79L74 device to operate in the Single-PHY Mode), then the "TxUClav" output pin will unconditionally reflect the "Transmit FIFO fill-status" for Channel 0. No attention will be paid to the address values placed upon the "TxUAddr[4:0]" input pins. 0 - Configures the Transmit UTOPIA Interface block to operate in the Single-PHY Mode. 1 - Configures the Transmit UTOPIA Interface block to operate in the Multi-PHY Mode.

<table>
<tr><th>BIT NUMBER</th><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>5</td><td>Back-to-Back Polling Enable</td><td>R/W</td><td>Back-to-Back Polling Enable:
This READ/WRITE bit-field permits the user to configure the Transmit UTOPIA Interface block to support "Back-to-Back Polling".
Ordinarily, for Multi-PHY polling, the user is required to interleave all UTOPIA Address values (that are to be placed on the "TxUAddr[4:0]" input pins) with the NULL Address (e.g., 0xnF). However, if the user configures the Transmit UTOPIA Interface block to operate in the "UTOPIA Level 3" Mode, and if the user also enables "Back-to-Back Polling", then he/she does not need interleave the UTOPIA Addresses with the NULL Address. In this case, the user can simply apply a "back-to-back" stream of "relevant" UTOPIA Addresses to the "TxUAddr[4:0]" input pins, and the XRT79L74 device will respond by driving the TxUClav output pins to the appropriate states (depending upon the Transmit FIFO fill-status).
0 - Disables "Back-to-Back" Polling. In this mode, the user must interleave all UTOPIA Addresses (that are to be applied to the "TxUAddr[4:0]" input pins) with the NULL Address.
1 - Enables "Back-to-Back" Polling. In this mode, the user does not need to interleave all UTOPIA Addresses (that are to be applied to the "TxUAddr[4:0]" input pins) with the NULL Address.
NOTE: In order to configure the Transmit UTOPIA Interface block to operate in the "Back-to-Back Polling" Mode, the user must also do the following.
a. Configure the Transmit UTOPIA Interface to operate in the "UTOPIA Level 3" Mode. This is accomplished by setting Bit 7 (UTOPIA Level 3 Disable) within this Register to "0".
b. Configure the Transmit UTOPIA Interface to support "Multi-PHY" Polling. This is accomplished by setting Bit 6 (Multi-PHY Polling Enable) within this register to "1".</td></tr>
<tr><td>4</td><td>Direct Status Indication Enable</td><td>R/W</td><td></td></tr>
<tr><td>3 - 2</td><td>UTOPIA/POS-PHY Data Bus Width[1:0]</td><td>R/W</td><td>UTOPIA/POS-PHY Data Bus Width[1:0]:
These READ/WRITE bit-fields permit the user to select the width of the Transmit UTOPIA and POS-PHY Data Buses. The relationship between the contents of these bit-fields and the corresponding widths of the Transmit UTOPIA and POS-PHY Data Bus is tabulated below.
<table><tr><th colspan="2">UTOPIA/POS-PHY Data Bus Width[1:0]</th><th>Corresponding UTOPIA/POS-PHY Data Bus Width</th></tr><tr><td>0</td><td>0</td><td>Not Valid</td></tr><tr><td>0</td><td>1</td><td>8 bits</td></tr><tr><td>1</td><td>0</td><td>16 bits</td></tr><tr><td>1</td><td>1</td><td>Not Valid</td></tr></table></td></tr>
</table>

BIT NUMBER	NAME	TYPE	DESCRIPTION
1 - 0	Cell Size[1:0]		**Cell Size[1:0]:** These two READ/WRITE bit-fields permit the user to specify the size of the ATM cell that will be handled by the Transmit UTOPIA Interface blocks. The relationship between the contents of these bit-fields and the corresponding Cell Sizes are tabulated below.

Cell Size[1:0]		Resulting Cell Size (Bytes)
0	0	52 bytes
0	1	53 bytes (Only valid for UTOPIA Level 1, and if the UTOPIA Data Bus Width is set to 8 bits)
1	0	54 bytes (Only valid for UTOPIA Levels 1 and 2)
1	1	56 bytes

NOTE: *The user must bear in mind the UTOPIA Level and the UTOPIA Data Bus width selected, when selecting the Cell Size.*

TRANSMIT UTOPIA PORT ADDRESS REGISTER (ADDRESS = 0X0593)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Transmit UTOPIA Port Address[4:0]				
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	
4 - 0	Transmit UTOPIA Port Address[4:0]	R/W	**Transmit UTOPIA Port Address[4:0]:** These READ/WRITE register bits, along with the "Transmit UTOPIA Port Number[4:0]" bits (within the "Trasnmit UTOPIA Port Number" Register (Address = 0x0597) permit the user to assign a unique Transmit UTOPIA address the XRT79L74 device. For UTOPIA Level 2/3 applications, the user can write in any value, ranging from 0x00 through 0x1E into this register. **The Transmit UTOPIA Address Assignment Procedure:** In order to assign a UTOPIA Address to a given Channel (or Port) within the XRT79L74 device, the user must do the following. **a.** Write the value corresponding to a given XRT79L74 Channel into the "Transmit UTOPIA Port Number" Register (Address = 0x0597). **b.** Write the corresponding UTOPIA Address value into this register. Once this "two-step" procedure has been executed, then the XRT79L74 Channel (as specified during step "a") will be assigned the "Transmit UTOPIA Address" value (as specified during step "b").

TRANSMIT UTOPIA PORT NUMBER REGISTER (ADDRESS = 0X0597)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Transmit UTOPIA Port Number[4:0]				
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
4 - 0	Transmit UTOPIA Port Number[4:0]	R/W	**Transmit UTOPIA Port Number[4:0]:** These READ/WRITE register bits, along with the "Transmit UTOPIA Port Address[4:0]" bits (within the "Transmit UTOPIA Port Address" Register (Address = 0x0593) permit the user to assign a unique Transmit UTOPIA address to each XRT79L74 device. **The Transmit UTOPIA Address Assignment Procedure:** In order to assign a UTOPIA Address to a given Channel (or Port) within the XRT79L74 device, the user must do the following. **a.** Write the value corresponding to a given XRT79L74 Channel into this register. **b.** Write the corresponding UTOPIA Address value into the "Transmit UTOPIA Port Address" Register (Address = 0x0593). Once this "two-step" procedure has been executed, then the XRT79L74 Channel (as specified during step "a") will be assigned the "Transmit UTOPIA Address" value (as specified during step "b").

LIU/JITTER ATTENUATOR CONTROL REGISTER BIT-FORMAT

LIU TRANSMIT APS/REDUNDANCY CONTROL REGISTER (ADDRESS = 0XN300)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							TxON
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 1	Reserved	R/O	0	
0	TxON	R/W	0	**Transmit Section ON:** This READ/WRITE bit-field permits the user to either turn on or turn off the Transmit Driver of XRT79L74. If the user turns on the Transmit Driver, then XRT79L74 will begin to transmit DS3 or E3 (on the line) via the TTIP and TRING output pins. Conversely, if the user turns off the Transmit Driver, then the TTIP and TRING output pins will be tri-stated. 0 - Shuts off the Transmit Driver associated with XRT79L74 and tri-states the TTIP and TRING0 output pins. 1 - Turns on (or enables) the Transmit Driver associated the XRT79L74. ***NOTE:*** *If the user wishes to exercise software control over the state of the Transmit Driver of the XRT79L74, then it is imperative that the user pull the TxON (pin R15) to a logic "low" level.*

LIU INTERRUPT ENABLE REGISTER (ADDRESS = 0XN301)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Change of FL Condition Interrupt Enable	Change of LOL Condition Interrupt Enable	Change of LOS Condition Interrupt Enable	Change of DMO Condition Interrupt Enable
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 4	Reserved	R/O	0	

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
3	Change of FL Condition Interrupt Enable	R/W	0	**Change of FL (FIFO Limit Alarm) Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of FL Condition" Interrupt. If the user enables this interrupt, then the XRT79L74 device will generate an interrupt any time any of the following events occur. • Whenever the Jitter Attenuator (within XRT79L74) declares the FL (FIFO Limit Alarm) condition. • Whenever the Jitter Attenuator (within XRT79L74) clears the FL (FIFO Limit Alarm) condition. 0 - Disables the "Change in FL Condition" Interrupt. 1 - Enables the "Change in FL Condition" Interrupt.
2	Change of LOL Condition Interrupt Enable	R/W	0	**Change of Receive LOL (Loss of Lock) Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of Receive LOL Condition" Interrupt. If the user enables this interrupt, then the XRT79L74 device will generate an interrupt any time any of the following events occur. • Whenever the Receive Section (within XRT79L74) declares the "Loss of Lock" Condition. • Whenever the Receive Section (within XRT79L74) clears the "Loss of Lock" Condition. 0 - Disables the "Change in Receive LOL Condition" Interrupt. 1 - Enables the "Change in Receive LOL Condition" Interrupt.
1	Change of LOS Condition Interrupt Enable	R/W	0	**Change of the Receive LOS (Loss of Signal) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of the Receive LOS Defect Condition" Interrupt. If the user enables this interrupt, then the XRT79L74 device will generate an interrupt any time any of the following events occur. • Whenever the Receive Section (within XRT79L74) declares the LOS Defect Condition. • Whenever the Receive Section (within XRT79L74) clears the LOS Defect condition. 0 - Disables the "Change in the LOS Defect Condition" Interrupt. 1 - Enables the "Change in the LOS Defect Condition" Interrupt.

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
0	Change of DMO Condition Interrupt Enable	R/W	0	**Change of Transmit DMO (Drive Monitor Output) Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of Transmit DMO Condition" Interrupt. If the user enables this interrupt, then the XRT79L74 device will generate an interrupt any time any of the following events occur. • Whenever the Transmit Section toggles the DMO output pin (or bit-field) to "1". • Whenever the Transmit Section toggles the DMO output pin (or bit-field) to "0". 0 - Disables the "Change in the DMO Condition" Interrupt. 1 - Enables the "Change in the DMO Condition" Interrupt.

LIU INTERRUPT STATUS REGISTER (ADDRESS = 0XN302)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Change of FL Condition Interrupt Status	Change of LOL Condition Interrupt Status	Change of LOS Condition Interrupt Status	Change of DMO Condition Interrupt Status
R/O	R/O	R/O	R/O	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 4	Unused	R/O	0	
3	Change of FL Condition Interrupt Status	RUR	0	**Change of FL (FIFO Limit Alarm) Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of FL Condition" Interrupt has occurred since the last read of this register. 0 - Indicates that the "Change of FL Condition" Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the "Change of FL Condition" Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine the current state of the "FIFO Alarm condition" by reading out the contents of Bit 3 (FL Alarm Declared) within the "Alarm Status Register".*

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
2	Change of LOL Condition Interrupt Status	RUR	0	**Change of Receive LOL (Loss of Lock) Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of Receive LOL Condition" Interrupt has occurred since the last read of this register. 0 - Indicates that the "Change of Receive LOL Condition" Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the "Change of Receive LOL Condition" Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine the current state of the "Receive LOL Defect condition" by reading out the contents of Bit 2 (Receive LOL Defect Declared) within the "Alarm Status Register".*
1	Change of LOS Condition Interrupt Status	RUR	0	**Change of Receive LOS (Loss of Signal) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of the Receive LOS Defect Condition" Interrupt has occurred since the last read of this register. 0 - Indicates that the "Change of the Receive LOS Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the "Change of the Receive LOS Defect Condition" Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine the current state of the "Receive LOS Defect condition" by reading out the contents of Bit 1 (Receive LOS Defect Declared) within the "Alarm Status Register".*
0	Change of DMO Condition Interrupt Status	RUR	0	**Change of Transmit DMO (Drive Monitor Output) Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of the Transmit DMO Condition" Interrupt has occurred since the last read of this register. 0 - Indicates that the "Change of the Transmit DMO Condition" Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the "Change of the Transmit DMO Condition" Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine the current state of the "Transmit DMO Condition" by reading out the contents of Bit 0 (Transmit DMO Condition) within the "Alarm Status Register".*

LIU ALARM STATUS REGISTER (ADDRESS = 0XN303)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Unused	Digital LOS Defect Declared	Analog LOS Defect Declared	FL (FIFO Limit) Alarm Declared	Receive LOL Defect Declared	Receive LOS Defect Declared	Transmit DMO Condition
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 6	Unused	R/O	0	
5	Digital LOS Defect Declared	R/O	0	**Digital LOS Defect Declared:** This READ-ONLY bit-field indicates whether or not the Digital LOS (Loss of Signal) detector is declaring the LOS Defect condition. For DS3 application, the Digital LOS Detector will declare the LOS Defect condition whenever it detects an absence of pulses (within the incoming DS3 data-stream) for 160 consecutive bit-periods. Further, (again for DS3 applications) the Digital LOS Detector will clear the LOS Defect condition whenever it determines that the pulse density (within the incoming DS3 signal) is at least 33%. 0 - Indicates that the Digital LOS Detector is NOT declaring the LOS Defect Condition. 1 - Indicates that the Digital LOS Detector is currently declaring the LOS Defect condition. ***NOTES:*** *1. LOS Detection (within each channel of the XRT79L74 device) is performed by both an Analog LOS Detector and a Digital LOS Detector. The LOS state of a given Channel is simply a WIRED-OR of the "LOS Defect Declare" states of these two detectors.2.* *2. The current LOS Defect Condition (for the channel) can be determined by reading out the contents of Bit 1 (Receive LOS Defect Declared) within this register.*

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
4	Analog LOS Defect Declared	R/O	0	**Analog LOS Defect Declared:** This READ-ONLY bit-field indicates whether or not the Analog LOS (Loss of Signal) detector is declaring the LOS Defect condition. For DS3 application, the Analog LOS Detector will declare the LOS Defect condition whenever it determines that the amplitude of the pulses (within the incoming DS3 line signal) drops below a certain "Analog LOS Defect Declaration" threshold level. Conversely, (again for DS3 application) the Analog LOS Detector will clear the LOS Defect condition whenever it determines that the amplitude of the pulses (within the incoming DS3 line signal) has risen above a certain "Analog LOS Defect Clearance" threshold level. It should be noted that, in order to prevent "chattering" within the Analog LOS Detector output, there is some built-in hysteresis between the "Analog LOS Defect Declaration" and the "Analog LOS Defect Clearance" threshold levels. 0 - Indicates that the Analog LOS Detector is NOT declaring the LOS Defect Condition. 1 - Indicates that the Analog LOS Detector is currently declaring the LOS Defect condition. ***NOTES:*** *1. LOS Detection (within each channel of the XRT79L74 device) is performed by both an Analog LOS Detector and a Digital LOS Detector. The LOS state of a given Channel is simply a WIRED-OR of the "LOS Defect Declare" states of these two detectors.2.* *2. The current LOS Defect Condition (for the channel) can be determined by reading out the contents of Bit 1 (Receive LOS Defect Declared) within this register.*

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
3	FL Alarm Declared	R/O	0	**FL (FIFO Limit) Alarm Declared:** This READ-ONLY bit-field indicates whether or not the Jitter Attenuator block (within the XRT79L74 device) is currently declaring the FIFO Limit Alarm. The Jitter Attenuator block will declare the "FIFO Limit" Alarm anytime the "Jitter Attenuator" FIFO comes within two bit-periods of either overflowing or under-running. Conversely, the Jitter Attenuator block will clear the "FIFO Limit" Alarm anytime the "Jitter Attenuator" FIFO is NO longer within two bit-periods of either overflowing or under-running. Typically, this Alarm will only be declared whenever there is a very serious problem with timing or jitter in the system. 0 - Indicates that the Jitter Attenuator block (within the XRT79L74 device) is NOT currently declaring the "FIFO Limit" Alarm condition. 1 - Indicates that the Jitter Attenuator block (within the XRT79L74 device) is currently declaring the "FIFO Limit" Alarm condition. ***NOTE:*** *This bit-field is only active if the Jitter Attenuator (within the XRT79L74 device) has been enabled.*
2	Receive LOL Condition Declared	R/O	0	**Receive LOL (Loss of Lock) Condition Declared:** This READ-ONLY bit-field indicates whether or not the Receive Section (within the XRT79L74 device) is currently declaring the LOL (Loss of Lock) condition. The Receive Section (of XRT79L74) will declare the LOL Condition, if any one of the following conditions is met. • If the frequency of the Recovered Clock signal differs from that of the signal provided to the E3CLK input (for E3 applications) or the DS3CLK input (for DS3 applications) by 0.5% (or 5000ppm) or more. • If the frequency of the Recovered Clock signal differs from the "line-rate" clock signal (for XRT79L74) that has been generated by the "SFM Clock Synthesizer" PLL (for SFM Mode Operation) by 0.5% (or 5000ppm) or more. 0 - Indicates that the Receive Section of XRT79L74 is NOT currently declaring the LOL Condition. 1 - Indicates that the Receive Section of XRT79L74 is currently declaring the LOL Condition.

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
1	Receive LOS Defect Condition Declared	R/O	0	**Receive LOS (Loss of Signal) Defect Condition Declared:** This READ-ONLY bit-field indicates whether or not the Receive Section (within the XRT79L74 device) is currently declaring the LOS defect condition. The Receive Section (of XRT79L74) will declare the LOS defect condition, if any one of the following conditions is met. • If the Digital LOS Detector declares the LOS defect condition (for DS3 application)· If the Analog LOS Detector declares the LOS defect condition (for DS3 application) • If the "ITU-T G.775" LOS Detector declares the LOS defect condition (for E3 application). 0 - Indicates that the Receive Section is NOT currently declaring the LOS Defect Condition. 1 - Indicates that the Receive Section is currently declaring the LOS Defect condition.
0	Transmit DMO Condition Declared	R/O	0	**Transmit DMO (Drive Monitor Output) Condition Declared:** This READ-ONLY bit-field indicates whether or not the Transmit Section is currently declaring the "DMO" Alarm condition. If configured accordingly, the Transmit Section will either internally or externally check the "Transmit Output" DS3/E3 Line signal for bipolar pulses via the TTIP and TRING output signals. If the Transmit Section were to detect no bipolar for 128 consecutive bit-periods, then it will declare the "Transmit DMO" Alarm condition. This particular alarm can be used to check for fault conditions on the "Transmit Output Line Signal" path. The Transmit Section will clear the "Transmit DMO" Alarm condition the instant that it detects some bipolar activity on the "Transmit Output Line" signal. 0 - Indicates that the Transmit Section of XRT79L74 is NOT currently declaring the "Transmit DMO Alarm" condition. 1 - Indicates that the Transmit Section of XRT79L74 is currently declaring the "Transmit DMO Alarm" condition.

LIU TRANSMIT CONTROL REGISTER (ADDRESS = 0XN304)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Internal Transmit Drive Monitor	Unused		TAOS	Unused	TxLEV
R/O	R/O	R/W	R/O	R/O	R/W	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 6	Unused	R/O	0	
5	Internal Transmit Drive Monitor	R/W	0	**Internal Transmit Drive Monitor Enable:** This READ/WRITE bit-field permits the user to configure the Transmit Section of XRT79L74 to either internally or externally monitor the TTIP and TRING output pins for bipolar pulses, in order to determine whether to declare the "Transmit DMO" Alarm condition. If the user configures the Transmit Section to externally monitor the TTIP and TRING output pins (for bipolar pulses) then the user must make sure that he/she has connected the MTIP and MRING input pins to their corresponding TTIP and TRING output pins (via a 274 ohm series resistor). If the user configures the Transmit Section to internally monitor the TTIP and TRING output pins (for bipolar pulses) then the user does NOT need to make sure that the MTIP and MRING input pins are connected to the TTIP and TRING output pins (via series resistors). This monitoring will be performed right at the TTIP and TRING output pads. 0 - Configures the Transmit Drive Monitor to externally monitor the TTIP and TRING output pins for bipolar pulses. 1 - Configures the Transmit Drive Monitor to internally monitor the TTIP and TRING output pins for bipolar pulses.
4	Unused	R/O	0	
3	Unused	R/O	0	
2	TAOS	R/W	0	**Transmit All OneS Pattern - XRT79L74:** This READ/WRITE bit-field permits the user to command the Transmit Section of XRT79L74 to generate and transmit an unframed, All Ones pattern via the DS3 or E3 line signal (to the remote terminal equipment). Whenever the user implements this configuration setting then the Transmit Section will ignore the data that it is accepting from the System-side equipment and overwrite this data with the "All Ones" Pattern. 0 - Configures the Transmit Section to transmit the data that it accepts from the "System-side" Interface. 1 - Configures the Transmit Section to generate and transmit the Unframed, All Ones pattern.
1	Unused	R/O	0	

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
0	TxLEV	R/W	0	**Transmit Line Build-Out Select - XRT79L74:** This READ/WRITE bit-field permits the user to either enable or disable the "Transmit Line Build-Out (e.g., pulse-shaping) circuit within the corresponding channel. The user should set this bit-field to either "0" or to "1" based upon the following guidelines. 0 - If the cable length between the Transmit Output (of the corresponding Channel) and the DSX-3/STSX-1 location is 225 feet or less. 1 - If the cable length between the Transmit Output (of the corresponding Channel) and the DSX-3/STSX-1 location is 225 feet or more. The user must follow these guidelines in order to insure that the Transmit Section (of XRT79L74) will always generate a DS3 pulse that complies with the Isolated Pulse Template requirements per Bellcore GR-499-CORE. ***NOTE:*** *This bit-field is ignored if the channel has been configured to operate in the E3 Mode.*

LIU RECEIVE CONTROL REGISTER (ADDRESS = 0XN305)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Disable DLOS Detector	Disable ALOS Detector	Unused	LOSMUT Enable	Receive Monitor Mode Enable	Receive Equalizer Enable
R/O	R/O	R/W	R/W	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 6	Unused	R/O	0	
5	Disable DLOS Detector	R/W	0	**Disable Digital LOS Detector - XRT79L74:** This READ/WRITE bit-field permits the user to either enable or disable the Digital LOS (Loss of Signal) Detector within the XRT79L74 device, as described below. 0 - Enables the Digital LOS Detector within the XRT79L74 device. (NOTE: This is the default condition). 1 - Disables the Digital LOS Detector within the XRT79L74 device. ***NOTE:*** *This bit-field is only active if XRT79L74 has been configured to operate in the DS3 Mode.*

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
4	Disable ALOS Detector	R/W	0	**Disable Analog LOS Detector - XRT79L74:** This READ/WRITE bit-field permits the user to either enable or disable the Analog LOS (Loss of Signal) Detector within the XRT79L74 device, as described below. 0 - Enables the Analog LOS Detector within the XRT79L74 device. (NOTE: This is the default condition). 1 - Disables the Analog LOS Detector within the XRT79L74 device. ***NOTE:*** *This bit-field is only active if XRT79L74 has been configured to operate in the DS3 Modes.*
3	Unused	R/O	0	
2	LOSMUT Enable	R/W	0	**Muting upon LOS Enable - XRT79L74:** This READ/WRITE bit-field permits the user to configure the Receive Section (within the XRT79L74 device) to automatically pull their corresponding Recovered Data Output pins (e.g., RPOS and RNEG) to GND anytime (and for the duration that) the Receive Section declares the LOS defect condition. In other words, this feature (if enabled) will cause the Receive Channel to automatically "mute" the Recovered data anytime (and for the duration that) the Receive Section declares the LOS defect condition. 0 - Disables the "Muting upon LOS" feature. In this setting the Receive Section will NOT automatically mute the Recovered Data whenever it is declaring the LOS defect condition. 1 - Enables the "Muting upon LOS" feature. In this setting the Receive Section will automatically mute the Recovered Data whenever it is declaring the LOS defect condition.
1	Receive Monitor Mode Enable	R/W	0	**Receive Monitor Mode Enable - XRT79L74:** This READ/WRITE bit-field permits the user to configure the Receive Section of XRT79L74 to operate in the "Receive Monitor" Mode. If the user configures the Receive Section to operate in the "Receive Monitor Mode", then it will be able to receive a nominal DSX-3/STSX-1 signal that has been attenuator by 20dB of flat loss along with 6dB of cable loss, in an error-free manner, and without declaring the LOS defect condition. 0 - Configures the corresponding channel to operate in the "Normal" Mode. 1 - Configure the corresponding channel to operate in the "Receive Monitor" Mode.

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
0	Receive Equalizer Enable	R/W	0	**Receive Equalizer Enable - XRT79L74:** This READ/WRITE register bit permits the user to either enable or disable the Receive Equalizer block within the Receive Section of XRT79L74, as listed below. 0 - Disables the Receive Equalizer within the corresponding channel. 1 - Enables the Receive Equalizer within the corresponding channel. ***NOTE:*** *For virtually all applications, we recommend that the user set this bit-field to "1" and enable the Receive Equalizer.*

LIU CHANNEL CONTROL REGISTER (ADDRESS = 0XN306)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	SFM Clock Out Enable	SFM Enable	RLB	LLB	Unused		
R/O	R/O	R/O	R/W	R/W	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7	Unused	R/O	0	
6	SFM Clock Out Enable	R/W	0	
5	SFM Enable	R/W	0	
4	RLB	R/W	0	**Loop-Back Select - RLB Bit:** This READ/WRITE bit-field along with the corresponding LLB bit-field permits the user to configure the XRT79L74 device into various loop-back modes. The relationship between the settings for this input pin, the corresponding LLB bit-field and the resulting Loop-back Mode is presented below.
3	LLB	R/W	0	**Loop-Back Select - LLB Bit-field:** Please see the description (above) for RLB.
2 - 0	Unused	R/O	0	

LLB	RLB	Loop-back Mode
0	0	Normal (No Loop-back) Mode
0	1	Remote Loop-back Mode
1	0	Analog Local Loop-back Mode
1	1	Digital Local Loop-back Mode

JITTER ATTENUATOR CONTROL REGISTER (ADDRESS = 0XN307)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				JA RESET	JA1	JA in Tx Path	JA0
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 4	Unused	R/O	0	
3	JA RESET	R/W	0	**Jitter Attenuator RESET:** Writing a "0 to 1" transition within this bit-field will configure the Jitter Attenuator (within the XRT79L74 device) to execute a RESET operation. Whenever the user executes a RESET operation, then all of the following will occur. • The "READ" and "WRITE" pointers (within the Jitter Attenuator FIFO) will be reset to their default values. • The contents of the Jitter Attenuator FIFO will be flushed. ***NOTE:*** *The user must follow up any "0 to 1" transition with the appropriate write operate to set this bit-field back to "0", in order to resume normal operation with the Jitter Attenuator.*
2	JA1 Ch	R/W	0	**Jitter Attenuator Configuration Select Input - Bit 1:** This READ/WRITE bit-field, along with Bit 0 (JA0) permits the user to do any of the following. • To enable or disable the Jitter Attenuator corresponding to XRT79L74. • To select the FIFO Depth for the Jitter Attenuator within the XRT79L74 device. The relationship between the settings of these two bit-fields and the Enable/Disable States, and FIFO Depths is presented below.

JA0	JA1	Jitter Attenuator Mode
0	0	FIFO Depth = 16 bits
0	1	FIFO Depth = 32 bits
1	0	Disabled
1	1	Disabled

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
1	JA in Tx Path Ch	R/W	0	**Jitter Attenuator in Transmit/Receive Path Select Bit:** This input pin permits the user to configure the Jitter Attenuator (within the XRT79L74 device) to operate in either the Transmit or Receive path, as described below. 0 - Configures the Jitter Attenuator (within the XRT79L74 device) to operate in the Receive Path. 1 - Configures the Jitter Attenuator (within the XRT79L74 device) to operate in the Transmit Path.
0	JA0 Ch	R/W	0	**Jitter Attenuator Configuration Select Input - Bit 0:** Please see the description for Bit 2 (JA1) within this Register.

LIU RECEIVE APS/REDUNDANCY CONTROL REGISTER (ADDRESS = 0XN308)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							RxON
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 1	Reserved	R/O	0	
0	RxON	R/W	0	**Receiver Section ON - XRT79L74:** This READ/WRITE bit-field permits the user to either turn on or turn off the Receive Section of XRT79L74. If the user turns on the Receive Section, then XRT79L74 will begin to receive the incoming DS3 or E3 data-stream via the RTIP and RRING input pins. Conversely, if the user turns off the Receive Section, then the entire Receive Section (e.g., AGC and Receive Equalizer Block, Clock Recovery PLL, etc) will be powered down. 0 - Shuts off the Receive Section of XRT79L74. 1 - Turns on the Receive Section of XRT79L74.

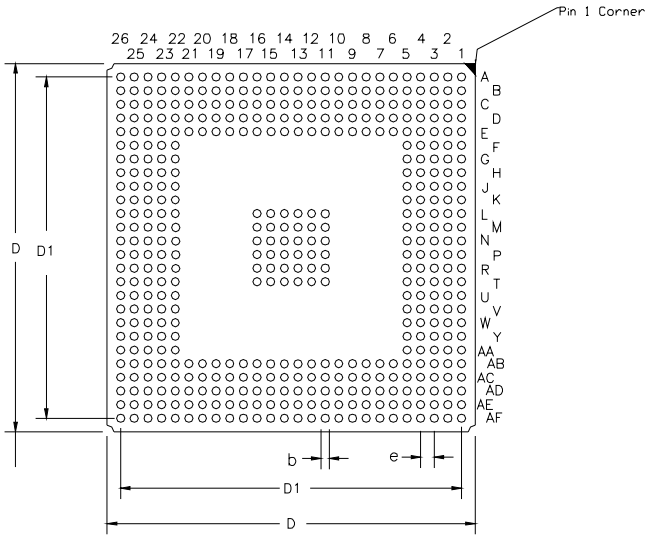
ORDERING INFORMATION

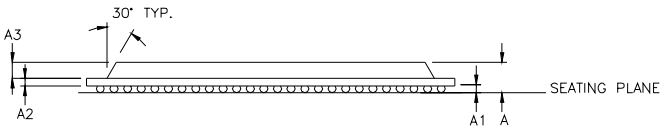
PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT79L74IB	456 Lead PBGA	-40^0C to $+85^0$C

PACKAGE DIMENSIONS

456 Ball Plastic Ball Grid Array
(27 mm x 27 mm 1.00mm pitch, PBGA)

Rev. 1.00





	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.083	0.138	2.10	3.50
A1	0.012	0.024	0.30	0.60
A2	0.010	0.028	0.25	0.70
A3	0.039	0.098	1.00	2.50
D	1.055	1.071	26.80	27.20
D1	0.984 BSC		25.00 BSC	
b	0.020	0.028	0.50	0.70
e	0.039 BSC		1.00 BSC	

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
P1.0.0	03/05/04	First release of the XRT79L74 preliminary register manual.

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