XRT7295AE

DS3/Sonet STS-1 Integrated Line Receiver

December 2000-2

FEATURES

- Fully Integrated Receive Interface for DS3 and STS-1 Rate Signals
- Integrated Equalization (Optional) and Timing Recovery
- Loss-of-Signal and Loss-of-Lock Alarms
- Variable Input Sensitivity Control
- 5V Power Supply
- Pin Compatible with XRT7295AT
- Companion Device to T7296 Transmitter

APPLICATIONS

- Interface to DS-3 Networks
- Digital Cross-Connect Systems
- CSU/DSU Equipment
- PCM Test Equipment
- Fiber Optic Terminals

GENERAL DESCRIPTION

The XRT7295AE DS3/SONET STS-1 integrated line receiver is a fully integrated receive interface that terminates a bipolar DS3 (44.736Mbps) or Sonet STS-1 (51.84Mbps) signal transmitted over coaxial cable. (See *Figure 13*).

The device also provides the functions of receive equalization (optional), automatic-gain control (AGC), clock-recovery and data retiming, loss-of-signal and loss-of-frequency-lock detection. The digital system interface is dual-rail, with received positive and negative 1s appearing as unipolar digital signals on separate output leads. The on-chip equalizer is designed for cable distances of 0 to 450ft. from the cross-connect frame to the device. The receive input has a variable input sensitivity control, providing three different sensitivity settings, to adapt longer cables. High input sensitivity allows for significant amounts of flat loss within the system. *Figure 1* shows the block diagram of the device.

The XRT7295AE device is manufactured using linear CMOS technology. The XRT7295AE is available in a 20-pin plastic SOJ package for surface mounting.

Two versions of the chip are available, one is for either DS3 or STS-1 operation (the XRT7295AE, this data sheet), and the other is for E3 operation (the XRT7295AT, refer to the XRT7295AT data sheet). Both versions are pin compatible.

For either DS3 or STS-1, an input reference clock at 44.736MHz or 51.84MHz provides the frequency reference for the device.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XRT7295AEIW	20 Lead 300 Mil JEDEC SOJ	-40°C to + 85°C

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ FAX (510) 668-7017

BLOCK DIAGRAM

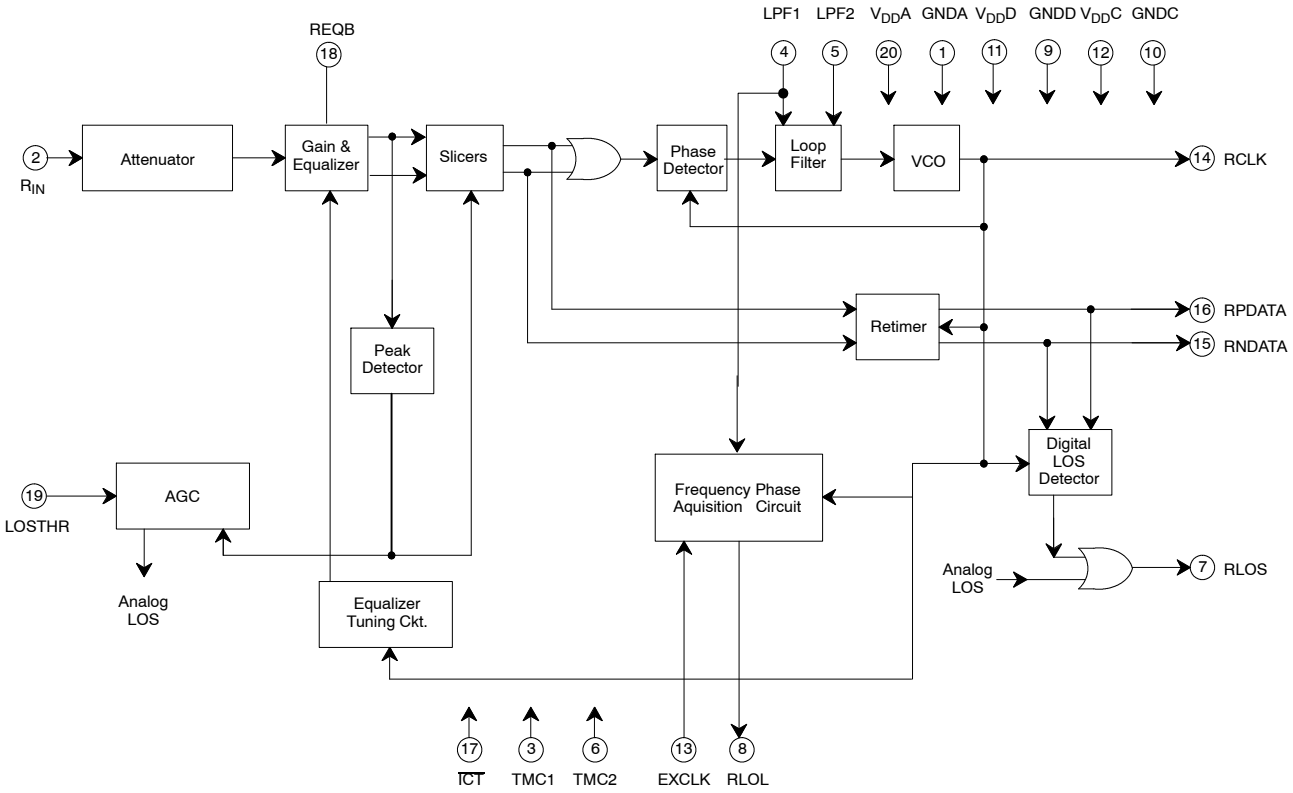
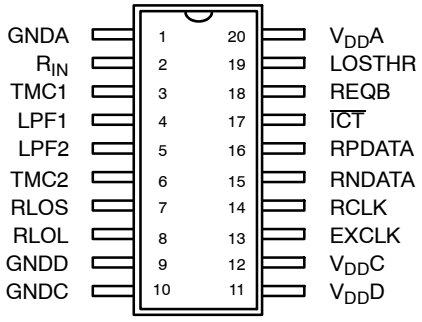


Figure 1. Block Diagram

PIN CONFIGURATION



20 Lead SOJ (Jedec, 0.300")

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	GNDA		**Analog Ground.**
2	R_{IN}	I	**Receive Input.** Analog receive input. This pin is internally biased at about 1.5V in series with 50 kΩ.
3,6	TMC1-TMC2	I	**Test Mode Control 1 and 2**. Internal test modes are enabled within the device by using TMC1 and TMC2. Users must tie these pins to the ground plane.
4,5	LPF1-LPF2	I	**PLL Filter 1 and 2**. An external capacitor (0.1μF 20%) is connected between these pins.
7	RLOS	O	**Receive Loss-of-signal.** This pin is set high on loss of the data signal at the receive input. (See *Table 6*)
8	RLOL	O	**Receive PLL Loss-of-lock.** This pin is set high on loss of PLL frequency lock.
9	GNDD		**Digital Ground for PLL Clock**. Ground lead for all circuitry running synchronously with PLL clock.
10	GNDC		**Digital Ground for EXCLK**. Ground lead for all circuitry running synchronously with EXCLK.
11	V_{DD}D		**5V Digital Supply (10%) for PLL Clock.** Power for all circuitry running synchronously with PLL clock.
12	V_{DD}C		**5V Digital Supply (10%) for EXCLK**. Power for all circuitry running synchronously with EXCLK.
13	EXCLK	I	**External Reference Clock**. A valid DS3 (44.736MHz 100ppm) or STS-1 (51.84MHz + 100ppm) clock must be provided at this input. The duty cycle of EXCLK, referenced to V_{DD} /2 levels, must be within 40% - 60% with a minimum rise and fall time (10% to 90%) of 5ns.
14	RCLK	O	**Receive Clock**. Recovered clock signal to the terminal equipment.
15	RNDATA	O	**Receive Negative Data**. Negative pulse data output to the terminal equipment. (See *Figure 11.*)
16	RPDATA	O	**Receive Positive Data**. Positive pulse data output to the terminal equipment. (See *Figure 11*)
17	$\overline{ICT}$	I	**In-circuit Test Control (Active-low)**. If ICT is forced low, all digital output pins (RCLK, RPDATA, RNDATA, RLOS, RLOL) are placed in a high-impedance state to allow for in-circuit testing. There is an internal pull-up on this pin.
18	REQB	I	**Receive Equalization Bypass**. A high on this pin bypasses the internal equalizer. A low places the equalizer in the data path.
19	LOSTHR	I	**Loss-of-signal Threshold Control**. The voltage forced on this pin controls the input loss-of-signal threshold. Three settings are provided by forcing GND, V_{DD}/2, or V_{DD}. This pin must be set to the desired level upon power-up and should not be changed during operation.
20	V_{DD}A		5V **Analog Supply** (10%).

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = -40°C to +85°C, V_{DD} = 5V ± 10%
Typical Values are for V_{DD} = 5.0 V, 25°C, and Random Data. Maximum Values are for V_{DD} = 5.5V all 1s Data.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
Electrical Characteristics						
I_{DD}	Power Supply Current					
	DS3		82	106	mA	REQB=0
			79	103	mA	REQB=1
	STS–1		87	111	mA	REQB=0
			83	108	mA	REQB=1
Logic Interface Characteristics						
	Input Voltage					
V_{IL}	Low	GNDD		0.5	V	
V_{IH}	High	V_{DD}D-0.5		V_{DD}D	V	
	Output Voltage					
V_{OL}	Low	GNDD		0.4	V	-5.0mA
V_{OH}	High	V_{DD}D-0.5		V_{DD}D	V	5.0mA
C_I	Input Capacitance			10	pF	
C_L	Load Capacitance			10	pF	
I_L	Input Leakage	-10		10	µA	-0.5 to V_{DD} + 0.5V (all input pins except 2, 3, 4, 5, 6, 17, 18, & 19)
		20		500	µA	0 V (pin 17)
		10		100	µA	V_{DD} (pin 2)
		-50		-5	µA	GNDD (pin 2)

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Power Supply . . . . . -0.5V to +6.5V
Storage Temperature . . . . . -40°C to +125°C
Power Dissipation . . . . . 700 mW

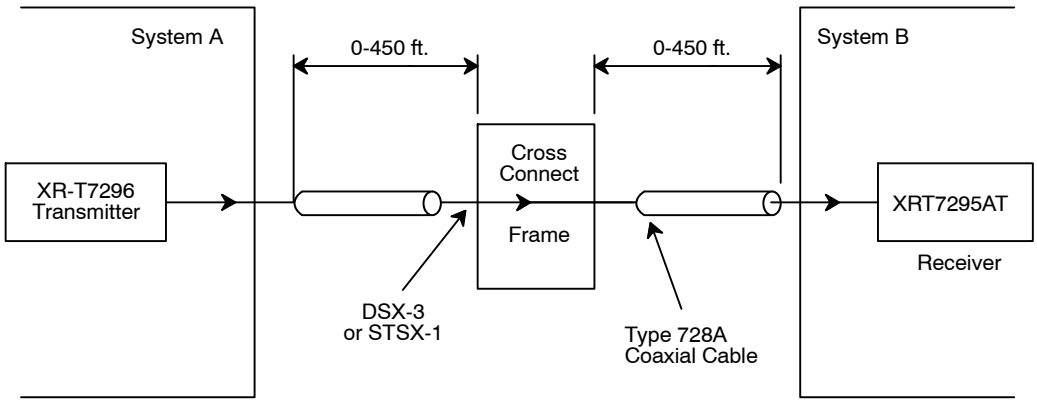


Figure 2. Application Diagram

SYSTEM DESCRIPTION

Receive Path Configurations

In the receive signal path (see *Figure 1*), the internal equalizer can be included by setting REQB = 0 or bypassed by setting REQB = 1. The equalizer bypass option allows easy interfacing of the XRT7295AE device into systems already containing external equalizers. *Figure 3* illustrates the receive path options.

In Case 1 of *Figure 3*, the signal from the DSX-3 cross-connect feeds directly into R_{IN}. In this mode, the user should set REQB = 0, engaging the equalizer in the data path.

In Case 2 of *Figure 3*, external line build-out (LBO) and equalizer networks precede the XRT7295AE device. In this mode, the signal at R_{IN} is already equalized, and the on-chip filters should be bypassed by setting REQB=1.

In applications where the XRT7295AE device is used to monitor DS3 transmitter outputs directly, the receive equalizer should be bypassed.

Maximum input amplitude under all conditions is 850mV pk.

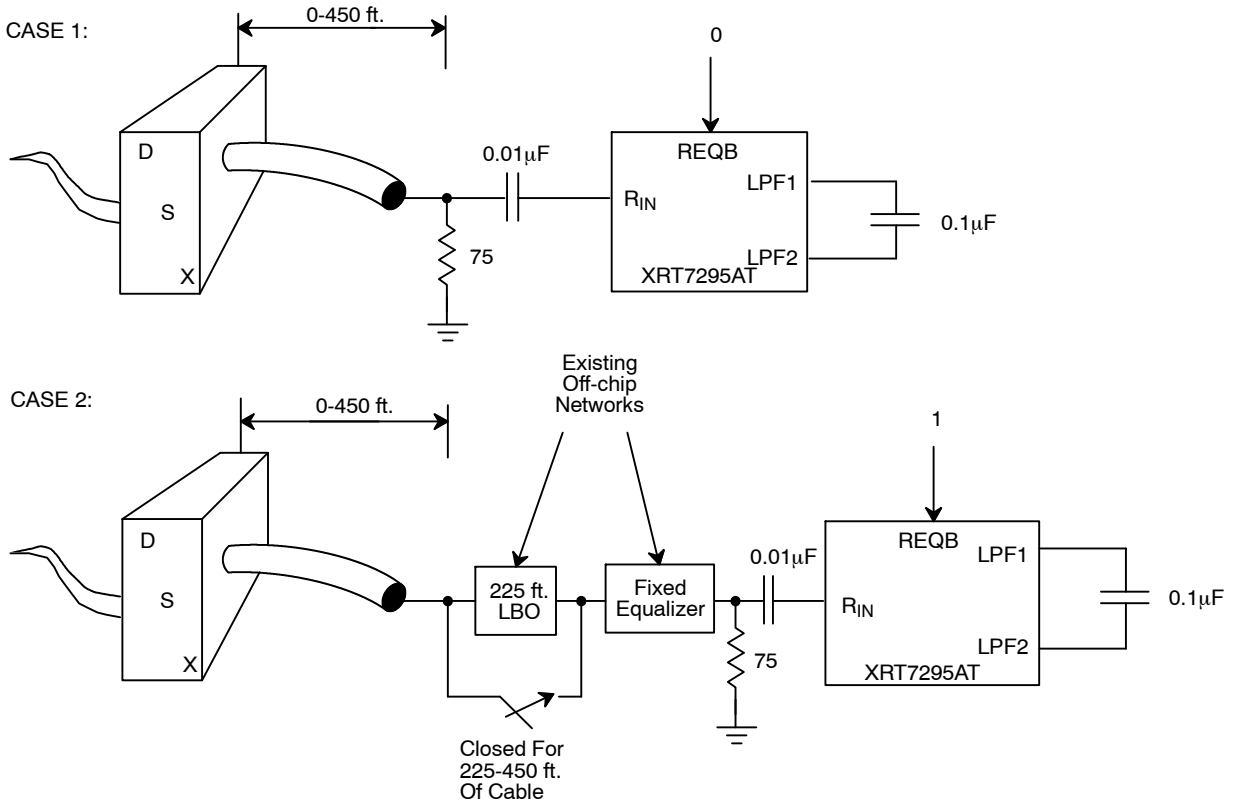


Figure 3. Receiver Configurations

DS3 SIGNAL REQUIREMENTS AT THE DSX

Pulse characteristics are specified at the DSX-3, which is an interconnection and test point referred to as the cross-connect (see *Figure 2.*) The cross-connect exists at the point where the transmitted signal reaches the distribution frame jack. *Table 1* lists the signal requirements. Currently, two isolated pulse template requirements exist: the ACCUNET T45 pulse template (see *Table 2* and *Figure 4*)and the G.703 pulse template (see *Table 3* and *Figure 5*). *Table 2* and *Table 3* give the associated boundary equations for the templates. The XRT7295AE correctly decodes any transmitted signal that meets one of these templates at the cross-connect.

Parameter	Specification
Line Rate	44.736 Mbps $\pm$20 ppm
Line Code	Bipolar with three-0 substitution (B3ZS)
Test Load	75 Ω $\pm$5%
Pulse Shape	An isolated pulse must fit the template in *NO TAG* or *Figure 5*.[1] The pulse amplitude may be scaled by a constant factor to fit the template. The pulse amplitude must be between 0.36vpk and 0.85vpk, measured at the center of the pulse.
Power Levels	For and all 1s transmitted pattern, the power at 22.368 0.002MHz must be -1.8 to +5.7dBm, and the power at 44.736 0.002MHz must be -21.8dBm to -14.3dBm.[2, 3]

Notes

[1] *The pulse template proposed by G.703 standards is shown in Figure 5 and specified in Table 3. The proposed G.703 standards further state that the voltage in a time slot containing a 0 must not exceed 5% of the peak pulse amplitude, except for the residue of preceding pulses.*

[2] *The power levels specified by the proposed G.703 standards are identical except that the power is to be measured in 3kHz bands.*

[3] *The all 1s pattern must be a pure all 1s signal, without framing or other control bits.*

Table 1. DSX-3 Interconnection Specification

Lower Curve		Upper Curve	
Time	**Equation**	**Time**	**Equation**
$T \leq -0.36$	0	$T \leq -0.68$	0
$-0.36 \leq T \leq +0.28$	$0.5\ (1+\sin\{\pi/2\}[1+T/0.18])$	$-0.68 \leq T \leq +0.36$	$0.5\ (1+\sin\{\pi/2\}[1+T/0.34])$
$0.28 \leq T$	$0.11e^{-3.42(T-0.3)}$	$0.36 \leq T$	$0.05 + 0.407e^{-1.84(T-0.36)}$

Table 2. DSX-3 Pulse Template Boundaries for ACCUNET T45 Standards (See *Figure 4.*)

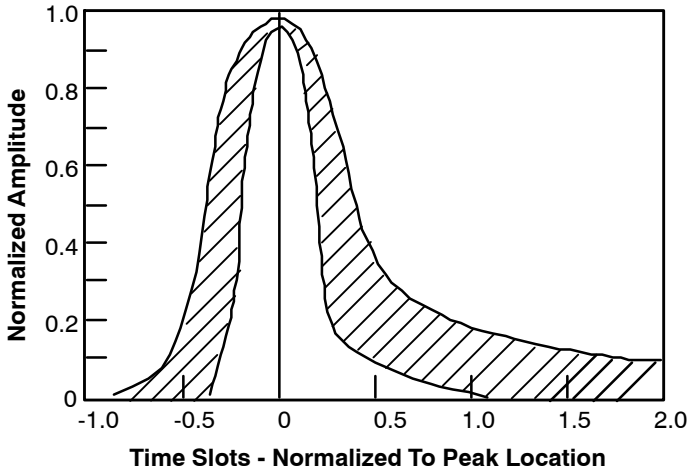


Figure 4. DSX-3 Isolated Pulse Template for ACCUNET T45 Standards

Lower Curve		Upper Curve	
Time	**Function**	**Time**	**Function**
$T \leq -0.36$	0	$T \leq -0.65$	0
$-0.36 \leq T \leq +0.28$	$0.5\ (1+\sin\{\pi/2\}[1+T/0.18])$	$-0.65 \leq T \leq 0$	$1.05\ [1-e^{-4.6(T+0.65)}]$
$0.28 \leq T$	$0.11e^{-3.42(T-0.3)}$	$0 \leq T \leq 0.36$	$0.5\ (1+\sin\{\pi/2\}[1+T/0.34])$
		$0.36 \leq T$	$0.05+0.407e^{-1.84(T-0.36)}$

Table 3. DSX-3 Pulse Template Boundaries for G.703 Standards (See *Figure 5*)

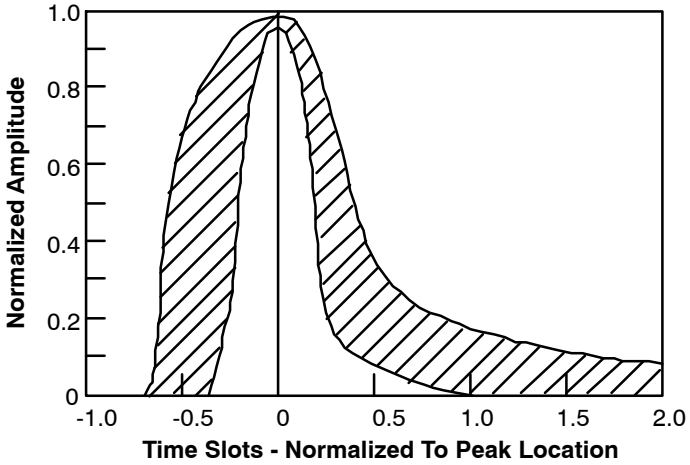


Figure 5. DSX-3 Isolated Pulse Template for G.703 Standards

STS-1 SIGNAL REQUIREMENTS AT THE STSX

For STS-1 operation, the cross-connect is referred at the STSX-1. *Table 4* lists the signal requirements at the STSX-1. Instead of the DS3 isolated pulse template, an eye diagram mask is specified for STS-1 operation (TA-TSY-000253). The XRT7295AE correctly decodes any transmitted signal that meets the mask shown in *Figure 6* at the STSX-1.

Parameter	Specification
Line Rate	51.84 Mbps
Line Code	Bipolar with three-0 substitution (B3ZS)
Test Load	75Ω 5%
Power Levels	A wide-band power level measurement at the STSX-1 interface using a low-pass filter with a 3dB cutoff frequency of at least 200MHz is within -2.7 dBm and 4.7 dBm.

Table 4. STSX-1 Interconnection Specification

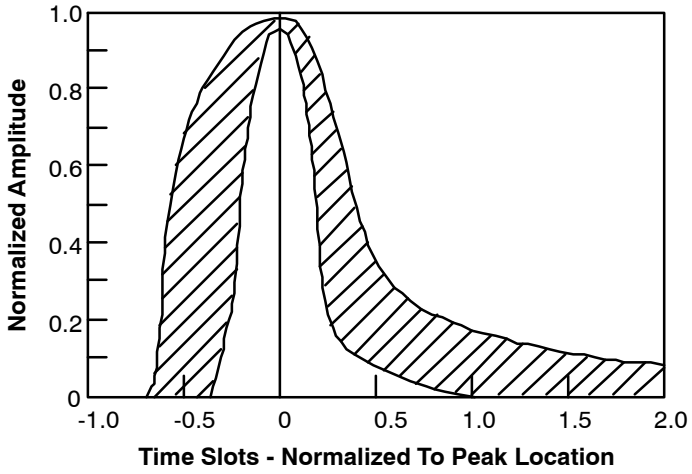


Figure 6. STSX-1 Isolated Pulse Template for Bellcore TA-TSY-000253

LINE TERMINATION AND INPUT CAPACITANCE

The recommended receive termination is shown in *Figure 3* The 75 Ω resistor terminates the coaxial cable with its characteristic impedance. The 0.01μF capacitor to R_{IN} couples the signal into the receive input without disturbing the internally generated DC bias level present on R_{IN}. The input capacitance at the R_{IN} pin is 2.8pF typical.

LOSS LIMITS FROM THE DSX-3 TO THE RECEIVE INPUT

The signal at the cross-connect may travel through a distribution frame, coaxial cable, connector, splitters, and back planes before reaching the XRT7295AE device. This section defines the maximum distribution frame and cable loss from the cross-connect to the XRT7295AE input.

The distribution frame jack may introduce 0.6 0.55 dB of loss. This loss may be any combination of flat or shaped (cable) loss.

The maximum cable distance between the point where the transmitted signal exits the distribution frame jack and the XRT7295AE device is 450 ft. (see *Figure 2.*) The coaxial cable (Type 728A) used for specifying this distance limitation has the loss and phase characteristics shown in *Figure 7* and *Figure 8*. Other cable types also may be acceptable if distances are scaled to maintain cable loss equivalent to Type 728A cable loss.

TIMING RECOVERY

External Loop Filter Capacitor

Figure 3 shows the connection to an external 0.1μF capacitor at the LPF1/LPF2 pins. This capacitor is part of the PLL filter. A non-polarized, low-leakage capacitor should be used. A ceramic capacitor with the value 0.1μF 20% is acceptable.

OUTPUT JITTER

The total jitter appearing on the RCLK output during normal operation consists of two components. First, some jitter appears on RCLK because of jitter on the incoming signal. (The next section discusses the jitter transfer characteristic, which describes the relationship between input and output jitter.) Second, noise sources within the XRT7295AE device and noise sources that are coupled into the device through the power supplies and data pattern dependent jitter due to misequalization of the input signal, all create jitter on RCLK. The magnitude of this internally generated jitter is a function of the PLL bandwidth, which in turn is a function of the input 1s density. For higher 1s density, the amount of generated jitter decreases. Generated jitter also depends on the quality of the power supply bypassing networks used. *Figure 12* shows the suggested bypassing network, and *Table 5* lists the typical generated jitter performance.

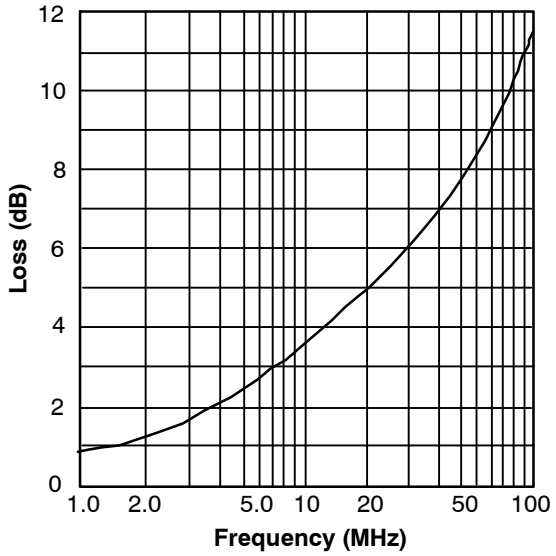


Figure 7. Loss Characteristic of 728A Coaxial Cable (450 ft.)

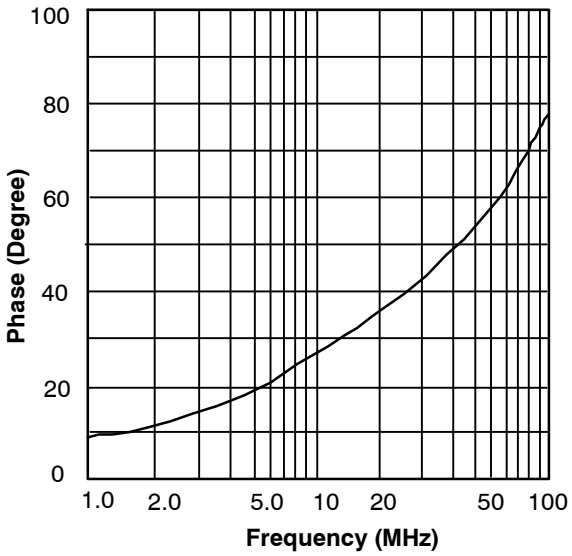


Figure 8. Phase Characteristic of 728A Coaxial Cable (450 ft.)

JITTER TRANSFER CHARACTERISTIC

The jitter transfer characteristic indicates the fraction of input jitter that reaches the RCLK output as a function of input jitter frequency. *Table 5* shows Important jitter transfer characteristic parameters. *Figure 9* also shows a typical characteristic, with the operating conditions as described in *Table 5.* Although existing standards do not specify jitter transfer characteristic requirements, the XRT7295AT information is provided here to assist in evaluation of the device.

Parameter	Typ	Max	Unit
Generated Jitter[1]			
All 1s pattern	1.0		ns peak-to-peak
Repetitive "100" pattern	1.5		ns peak-to-peak
Jitter Transfer Characteristic[2]			
Peaking	0.05		dB
f 3dB	205		kHz

Notes

[1] Repetitive input data pattern at nominal DSX-3 level with V_{DD} = 5V T_A = 25°C.

[2] Repetitive "100 " input at nominal DSX-3 level with V_{DD} = 5V, T_A = 25°C.

Table 5. Generated Jitter and Jitter Transfer Characteristics

JITTER ACCOMMODATION

Under all allowable operating conditions, the jitter accommodation of the XRT7295AE device exceeds all system requirements for error-free operation (BER<1E^{-9}). The typical (V_{DD} = 5V, T = 25°C, DSX-3 nominal signal level) jitter accommodation for the XRT7295AE is shown in *Figure 10.*

FALSE-LOCK IMMUNITY

False-lock is defined as the condition where a PLL recovered clock obtains stable phase-lock at a frequency not equal to the incoming data rate. The XRT7295AE device uses a combination frequency/phase-lock architecture to prevent false-lock. An on-chip frequency comparator continuously compares the EXCLK reference to the PLL clock. If the frequency difference between the EXCLK and PLL clock exceeds approximately 0.5%, correction circuitry forces re-acquisition of the proper frequency and phase.

ACQUISITION TIME

If a valid input signal is assumed to be already present at R_{IN}, the maximum time between the application of device power and error-free operation is 20ms. If power has already been applied, the interval between the application of valid data (or the action of valid data following a loss of signal) and error-free operation is 4ms.

LOSS-OF-LOCK DETECTION

As stated above, the PLL acquisition aid circuitry monitors the PLL clock frequency relative to the EXCLK frequency. The RLOL alarm is activated if the difference between the PLL clock and the EXCLK frequency exceeds approximately 0.5%.

This will not occur until at least 250 bit periods after loss of input data.

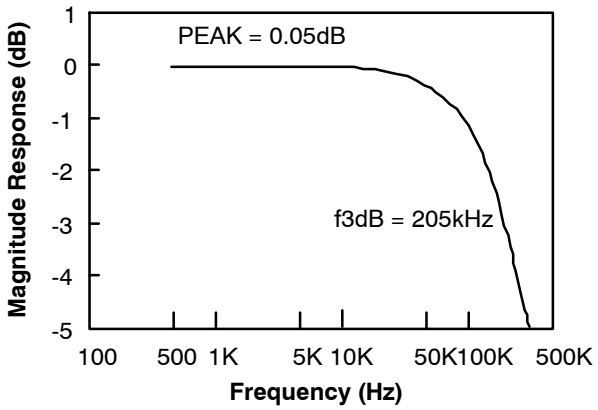
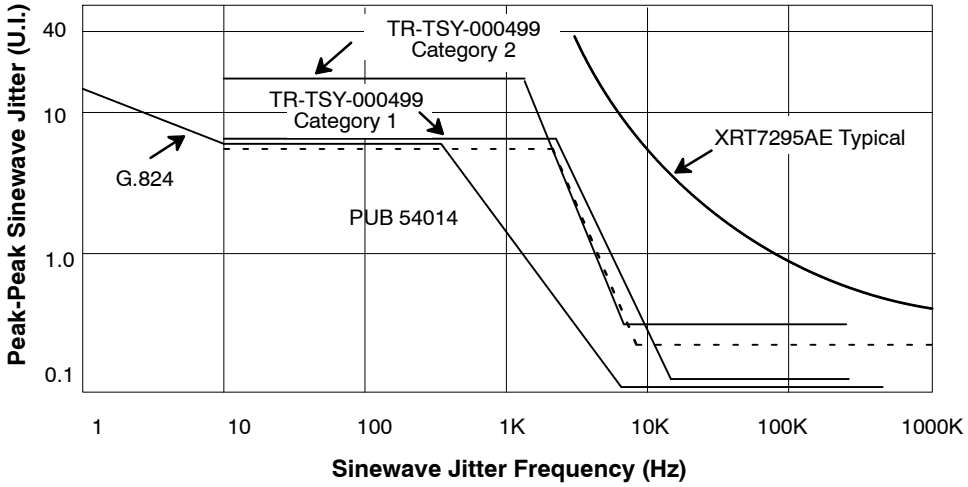


Figure 9. Typical PLL Jitter Transfer Characteristic



XRT7295AE Typical	
Jitter Frequency (Hz)	Jitter Amplitude (U.I.)
5k	10
10k	5
60k	1
300k	0.5
1M	0.4

Figure 10. Input Jitter Tolerance at DSX-3 Level

A high RLOL output indicates that the acquisition circuit is working to bring the PLL into proper frequency lock. RLOL remains high until frequency lock has occurred; however, the minimum RLOL pulse width is 32 clock cycles.

PHASE HITS

In response to a phase hit in the input data, the XRT7295AT returns to error free operation in less than 2ms. During the requisition time, RLOS may temporarily be indicated.

LOSS-OF-SIGNAL DETECTION

Figure 1 shows that analog and digital methods of loss-of-signal (LOS) detection are combined to create the RLOS alarm output. RLOS is set if either the analog or digital detection circuitry indicates LOS has occurred.

ANALOG DETECTION

The analog LOS detector monitors the peak input signal amplitude. RLOS makes a high-to-low transition (input signal regained) when the input signal amplitude exceeds the loss-of signal threshold defined in *Table 6.* The RLOS low-to-high transition (input signal loss) occurs at a level typically 1.0 dB below the high-to-low transition level. The hysteresis prevents RLOS chattering. Once set, the RLOS alarm remains high for at least 32 clock cycles, allowing for system detection of a LOS condition without the use of an external latch.

To allow for varying levels of noise and crosstalk in different applications, three loss-of-signal threshold settings are available using the LOSTHR pin. Setting LOSTHR = V_{DD} provides the lowest loss-of-signal threshold; LOSTHR = $V_{DD}/2$ (can be produced using two 50 kΩ 10% resistors as a voltage divider between V_{DD}D and GNDD) provides an intermediate threshold; and LOSTHR = GND provides the highest threshold. The LOSTHR pin must be set to its desired value at power-up and must not be changed during operation.

DIGITAL DETECTION

In addition to the signal amplitude monitoring of the analog LOS detector, the digital LOS detector monitors the recovered data 1s density. The RLOS alarm goes high if 160 32 or more consecutive 0s occur in the receive data stream. The alarm goes low when at least ten 1s occur in a string of 32 consecutive bits. This hysteresis prevents RLOS chattering and guarantees a minimum RLOS pulse width of 32 clock cycles. Note, however, that RLOS chatter can still occur. When REQB=1, input signal levels above the analog RLOS threshold can still be low enough to result in a high bit error rate. The resultant data stream (containing) errors can temporarily activate the digital LOS detector, and RLOS chatter can occur. Therefore, RLOS should not be used as a bit error rate monitor.

RLOS chatter can also occur when RLOL is activated (high).

Data Rate	REQB	LOSTHR	Min. Threshold	Max. Threshold	Unit
DS3	0	0	60	220	mV pk
		$V_{DD}/2$	40	145	mV pk
		V_{DD}	25	90	mV pk
	1	0	45	175	mV pk
		$V_{DD}/2$	30	115	mV pk
		V_{DD}	20	70	mV pk
STS-1	0	0	75	275	mV pk
		$V_{DD}/2$	50	185	mV pk
		V_{DD}	30	115	mV pk
	1	0	55	220	mV pk
		$V_{DD}/2$	35	145	mV pk
		V_{DD}	25	90	mV pk

Notes
- Lower threshold is 1.5 dB below upper threshold.
- The RLOS alarm is an indication of the absence of an input signal, not a bit error rate indication (independent of the RLOS state). The device will attempt to recover correct timing data. The RLOS low-to-high transition typically occurs 1dB below the high to low transition.

Table 6. Analog Loss-of-Signal Thresholds

RECOVERED CLOCK AND DATA TIMING

Table 7 and *Figure 11* summarize the timing relationships between the logic signals RCLK, RPDATA, and RNDATA. The duty cycle is referenced to $V_{DD}/2$ threshold level. RPDATA and RNDATA change on the rising edge of RCLK and are valid during the falling edge of RCLK. A positive pulse at R_{IN} creates a high level on RPDATA and a low level on RNDATA. A negative pulse at the input creates a high level on RNDATA and a low level on RPDATA, and a received zero produces low levels on both RPDATA and RNDATA.

IN-CIRCUIT TEST CAPABILITY

When pulled low, the $\overline{ICT}$ pin forces all digital output buffers (RCLK, RPDATA, RNDATA, RLOS, RLOL pins) to be placed in a high output impedance state. This feature allows in-circuit testing to be done on neighboring devices without concern for XRT7295AT device buffer damage. An internal pull-up device (nominally 50kΩ) is provided on this pin therefore, users can leave this pin unconnected for normal operation. Test equipment can pull $\overline{ICT}$ low during in-circuit testing without damaging the device. This is the only pin for which internal pull-up/pull-down is provided.

TIMING CHARACTERISTICS

Test Conditions: All Timing Characteristics are Measrured with 10pF Loading, -40°C $\leq T_A \leq$ +85°C, V_{DD} = 5V 10%

Symbol	Parameter	Min	Typ	Max	Unit
tRCH1RCH2	Clock Rise Time (10% - 90%)			4	ns
tRCL2RCL1	Clock Fall Time (10% - 90%)			4	ns
tRCHRDV	Receive Propagation Delay[1]	0.6		3.7	ns
	Clock Duty Cycle	45	50	55	%

Table 7. System Interface Timing Characteristics

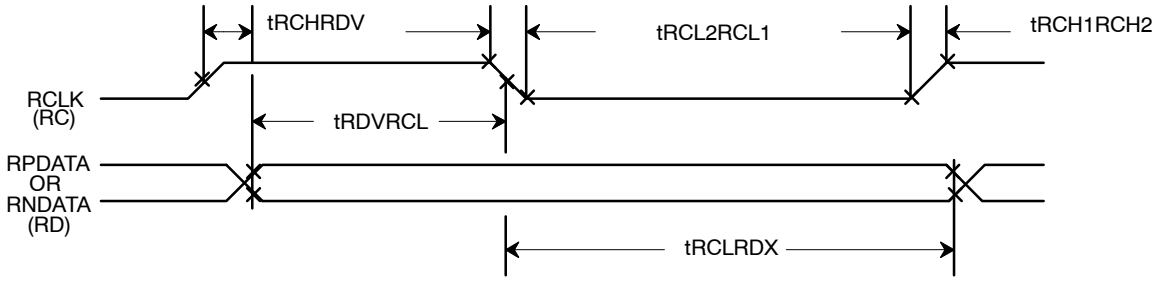


Figure 11. Timing Diagram for System Interface

BOARD LAYOUT CONSIDERATIONS

Power Supply Bypassing

Figure 12 illustrates the recommended power supply bypassing network. A 0.1μF capacitor bypasses the digital supplies. The analog supply V_{DD}A is bypassed by using a 0.1μF capacitor and a shield bead that removes significant amounts of high-frequency noise generated by the system and by the device logic. Good quality, high-frequency (low lead inductance) capacitors should be used. Finally, it is most important that all ground connections be made to a low-impedance ground plane.

Receive Input

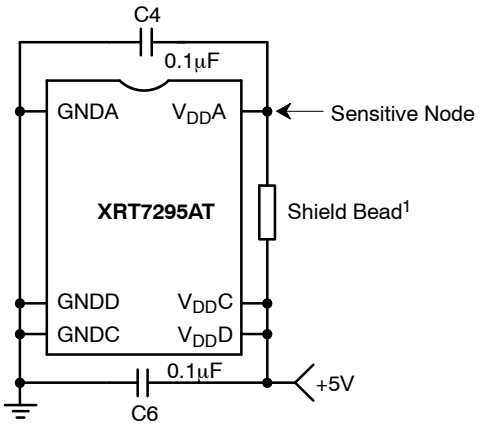
The connections to the receive input pin, R_{IN}, must be carefully considered. Noise-coupling must be minimized along the path from the signal entering the board to the input pin. Any noise coupled into the XRT7295AT input directly degrades the signal-to-noise ratio of the input signal and may degrade sensitivity.

PLL Filter Capacitor

The PLL filter capacitor between pins LPF1 and LPF2 must be placed as close to the chip as possible. The LPF1 and LPF2 pins are adjacent, allowing for short lead lengths with no crossovers to the external capacitor. Noise-coupling into the LPF1 and LPF2 pins may degrade PLL performance.

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting.



Notes

[1] Recommended shield beads are the Fair-Rite 2643000101 or the Fair-Rite 2743019446 (surface mount).

Figure 12. Recommended Power Supply Bypassing Network

COMPLIANCE SPECIFICATIONS

- Compliance with *AT&T Publication 54014, "ACCUNET* ® T45 Service Description and Interface Specifications," June 1987.
- Compliance with *ANSI Standard T1.102*-1989, "Digital Hierarchy - Electrical Interfaces, " 1989.
- Compliance with *Compatibility Bulletin 119,* "Interconnection Specification for Digital Cross-Connects," October 1979.
- Compliance with *CCITT Recommendations G.703 and G.824,* 1988.
- Compliance with *TR-TSY-000499,* "Transport Systems Generic Requirements (TSGR): Common Requirements," December 1988.
- Compliance with *TA-TSY-000253,* "Synchronous Optical Network (SONET) Transport System Generic Criteria," February 1990.

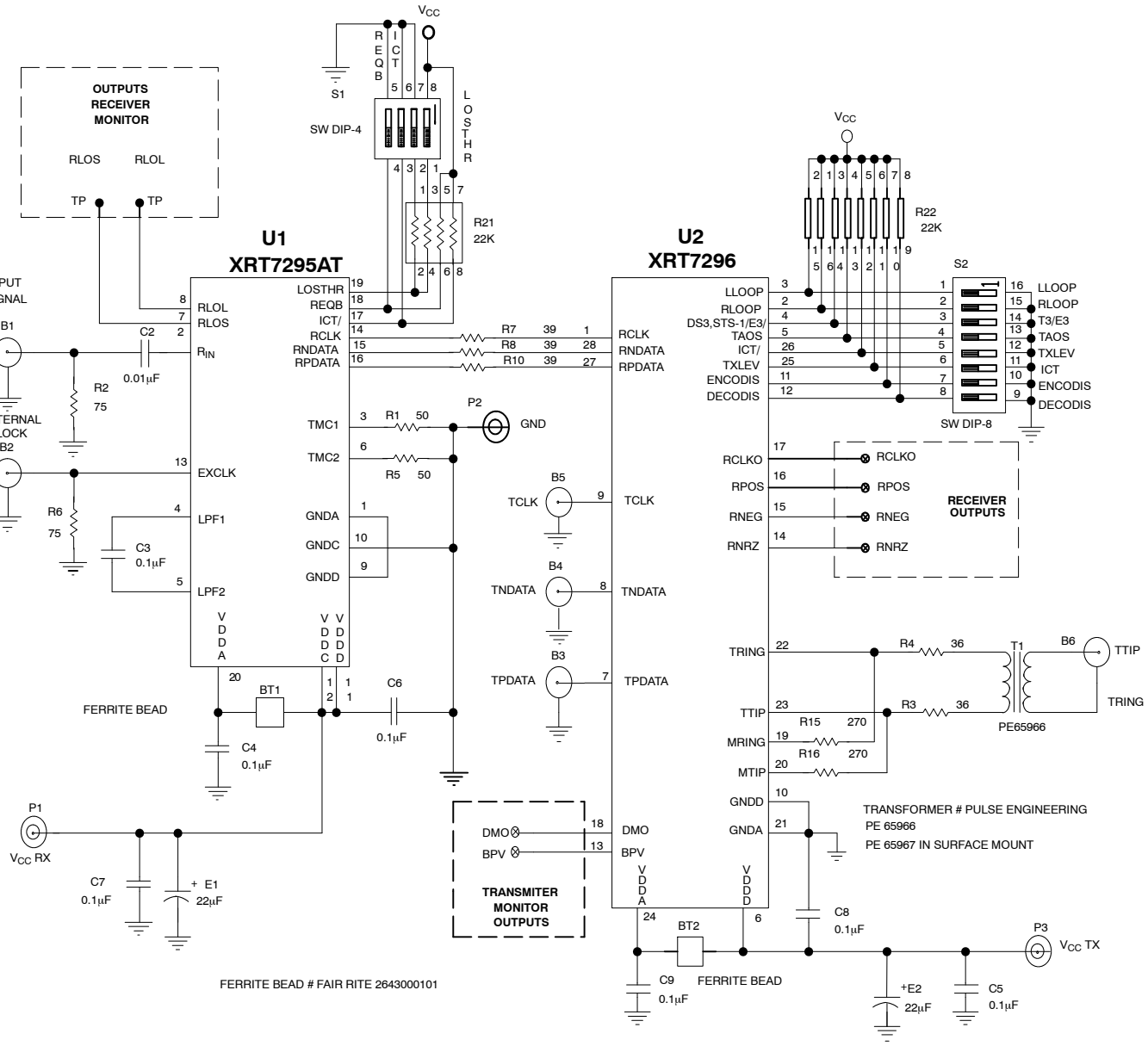


Figure 13. Typical Application Schematic

20 LEAD SMALL OUTLINE J LEAD (300 MIL JEDEC SOJ)

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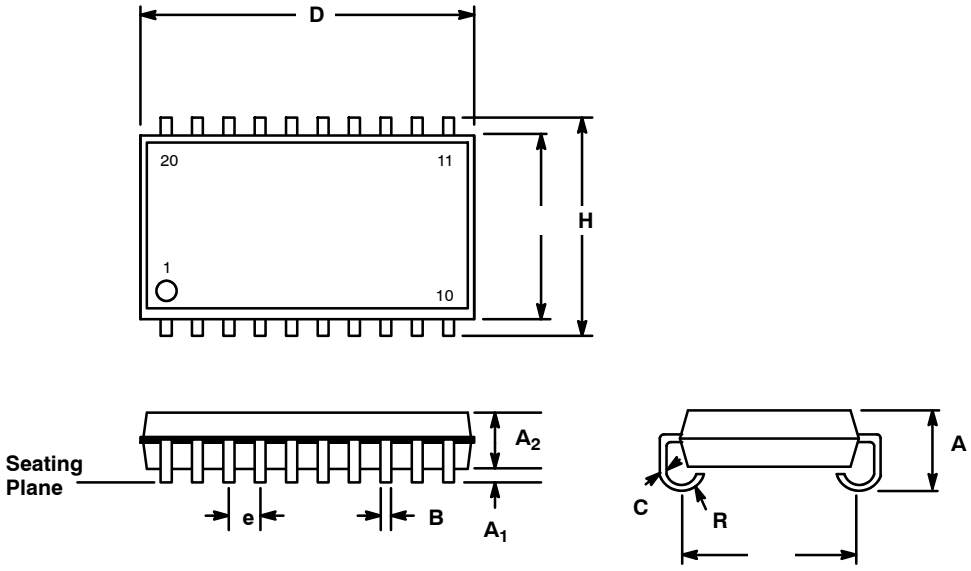

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.200	3.60	5.08
A_1	0.025	---	0.64	---
A_2	0.120	0.140	3.05	3.56
B	0.014	0.020	0.36	0.51
C	0.008	0.013	0.20	0.30
D	0.496	0.512	12.60	13.00
E	0.292	0.300	7.42	7.62
E_1	0.262	0.272	6.65	6.91
e	0.050 BSC		1.27 BSC	
H	0.335	0.347	8.51	8.81
R	0.030	0.040	0.76	1.02

Note: The control dimension is the inch column

NOTICE

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