FUNCTIONAL DESCRIPTION

The XRK39910 is a high fanout phase locked-loop clock driver intended for high performance computing and data-communications applications. It has eight zero delay LVTTL outputs.

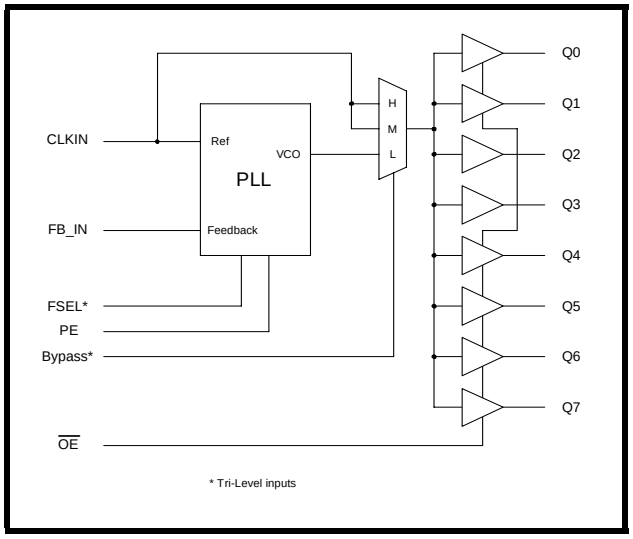
When the $\overline{OE}$ pin is held low, all the outputs are synchronously enabled. However, if $\overline{OE}$ is held high, all the outputs except Q_2 and Q_3 are synchronously disabled.

Furthermore, when the PE is held high, all the outputs are synchronized with the positive edge of the CLKIN. When PE is held low, all the outputs are synchronized with the negative edge of CLKIN.

The FB_IN signal is compared with the input CLKIN signal at the phase detector in order to drive the VCO. Phase differences cause the VCO of the PLL to adjust upwards or downwards accordingly.

An internal loop filter moderates the response of the VCO to the phase detector. The loop filter transfer function has been chosen to provide minimal jitter (or frequency variation) while still providing accurate responses to input frequency changes.

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM



FEATURES

- Eight zero delay outputs
- 12mA balanced drive outputs
- Output frequency: 15MHz to 85MHz
- <250ps of output to output skew
- Low Jitter: <200ps peak-to-peak
- 3 skew grades
- External feedback, internal loop filter
- Selectable positive or negative edge synchronization
- Synchronous output enable
- 3-level inputs for PLL range control
- PLL bypass for DC testing
- Available in SOIC package

FIGURE 2. PIN CONFIGURATION

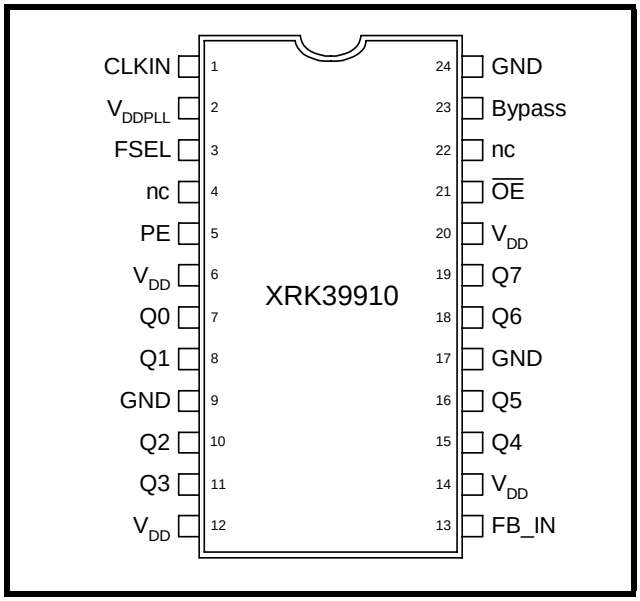


TABLE 1: ORDERING INFORMATION

PRODUCT NUMBER	ACCURACY	TEMP RANGE
XRK39910CD-2	250ps	0°C to +70°C
XRK39910ID-2	250ps	-40°C to +85°C
XRK39910CD-5	500ps	0°C to +70°C
XRK39910ID-5	500ps	-40°C to +85°C
XRK39910CD-7	750ps	0°C to +70°C
XRK39910ID-7	750ps	-40°C to +85°C

TABLE 2: ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	DESCRIPTION	MAX	UNIT
	Supply Voltage to Ground	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{DD}+0.5	V
	CLKIN Input Voltage	-0.5 to +5.5	V
	Maximum Power Dissipation (T_A = 85°C)	530	mW
T_{STG}	Storage Temperature	-65 to +150	°C

NOTE: *(1) Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.*

TABLE 3: CAPACITANCE (T_A= +25°C, f= 1MHz, V_{IN}= 0V)

PARAMETER	DESCRIPTION	TYP	MAX	UNIT
C_{IN}	Input Capacitance	5	7	pF

NOTE: *Capacitance applies to all inputs except BYPASS and FSEL. It is characterized but not production tested*

.

TABLE 4: PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
CLKIN	1	IN	Reference Clock Input
V_{DDPLL}	2	PWR	Power supply for phase locked loop and other internal circuitry.
FSEL(1,3)	3	IN	Frequency range select: FSEL = GND:15 to 35MHz FSEL = MID (or open): 25 to 60MHz FSEL = V_{DD}: 40 to 85MHz
PE	5	IN	Selectable positive or negative edge control. When LOW/HIGH the outputs are synchronized with the negative/positive edge of the reference clock.
V_{DD}	6,12,14,20	PWR	Power supply for output buffers.

TABLE 4: PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
Q_0 - Q_7	7,8,10,11, 15,16,18,19	OUT	Eight clock output.
GND	9,17,24	PWR	Ground.
FB_IN	13	IN	Feedback Input
$\overline{OE}$(2)	21	IN	Synchronous Output Enable. When HIGH, it stops clock outputs (except Q_2 and Q_3) in a LOW state - Q_2 and Q_3 may be used as the feedback signal to maintain phase lock. Set $\overline{OE}$ LOW for normal operation.
BYPASS(1,2)	23	IN	When MID or HIGH, disable PLL (except for conditions of Note 2). CLKIN goes to all outputs. Set LOW for normal operations.

NOTE:

1. *Tri-Level Input*
2. *When BYPASS = MID and $\overline{OE}$ = HIGH, PLL remains active.*
3. *This input is wired to V_{DD}, GND, or unconnected. Default is MID level. If it is switched in the real time mode, the outputs may glitch, and the PLL may require an additional lock time before all data sheet limits are achieved.*

TABLE 5: RECOMMENDED OPERATING RANGE

SYMBOL	DESCRIPTION	XRK39910-2, -5, -7 (INDUSTRIAL)		XRK39910-2, -5, -7 (COMMERCIAL)		UNIT
		MIN.	MAX.	MIN.	MAX.	
V_{DD}	Power Supply Voltage	3	3.6	3	3.6	V
T_A	Ambient Operating Temperature	-40	+85	0	+70	°C

TABLE 6: DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{IH}	Input HIGH Voltage	Guranteed Logic HIGH (CLKIN, FB_IN, $\overline{OE}$, PE Inputs Only)	2		V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW (CLKIN, FB_IN, $\overline{OE}$, PE Inputs Only)		0.8	V
V_{IHH}	Input HIGH Voltage (1)	3-Level Inputs Only (FSEL, BYPASS)	V_{DD}-0.6		V
V_{IMM}	Input MID Voltage (1)	3-Level Inputs Only (FSEL, BYPASS)	V_{DD}/2-0.3	V_{DD}/2+0.3	V
V_{ILL}	Input LOW Voltage (1)	3-Level Inputs Only (FSEL, BYPASS)		0.6	V
I_{IN}	Input Leakage Current (CLKIN, FB_IN Inputs Only)	V_{IN} = V_{DD} or GND V_{DD} = Max.		±5	µA

TABLE 6: DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
I_3	3-Level Input DC Current (BYPASS, FSEL)	$V_{IN} = V_{DD}$	HIGH Level		±400	µA
		$V_{IN} = V_{DD}/2$	MID Level		±200	
		V_{IN} = GND	LOW Level		±400	
I_{PU}	Input Pull-Up current (PE)	V_{DD} = Max., V_{IN} = GND			±100	µA
I_{PD}	Input Pull-Down Current ($\overline{OE}$)	V_{DD}= Max., $V_{IN} = V_{DD}$			±100	µA
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = -12mA		2.4		V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 12mA			0.55	V

NOTE: *(1) These inputs are normally wired to V_{DD}, GND, or unconnected. Internal termination resistors bias unconnected inputs to $V_{DD}/2$. If these inputs are switched, the function and timing of the outputs may be glitched, and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.*

TABLE 7: POWER SUPPLY CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS(1)	TYP.	MAX.	UNIT
I_{DDQ}	Quiescent Power Supply Current	V_{DD}=Max., BYPASS=MID, CLKIN=LOW V_{DD}/PE=LOW, $\overline{OE}$=LOW, All outputs unloaded	8	25	mA
I_{TOT}	Total Power Supply Current	V_{DD}=3.3V, F_{REF}=25MHz, C_L=160pF(1)	34		mA
		V_{DD}=3.3V, F_{REF}=33MHz, C_L=160pF(1)	42		
		V_{DD}=3.3V, F_{REF}=66MHz, C_L=160pF(1)	76		

NOTE: *(1) For eight outputs, each loaded with 20pF.*

TABLE 8: INPUT TIMING REQUIREMENTS

SYMBOL	DESCRIPTION(1)	MIN.	MAX.	UNIT
t_R, t_F	Maximum input rise and fall times, 0.8V to 2V		10	ns/V
t_{PWC}	Input clock pulse, HIGH or LOW	3		ns
D_H	Input duty cycle	10	90	%
Ref	Reference Clock Input	15	85	MHz

NOTE: *(1) Where pulse width implied by D_H is less than t_{PWC} limit, t_{PWC} limit applies.*

TABLE 9: SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER		XRK39910-2			XRK39910-5			XRK39910-7			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
FREF	CLKIN Frequency Range	FSEL = LOW	15		35	15		35	15		35	MHz
		FSEL = MED	25		60	25		60	25		60	
		FSEL = HIGH	40		85	40		85	40		85	
tRPWH	CLKIN Pulse Width HIGH		3			3			3			ns
tRPWL	CLKIN Pulse Width LOW		3			3			3			ns
tSKEW	Output Skew (All Outputs) [1, 3, 4]			0.1	0.25		0.25	0.5		0.3	0.75	ns
tDEV	Device-to-Device Skew [1, 2, 5]				0.75			1.25			1.65	ns
tPD	CLKIN Input to FB_IN Propagation Delay [1, 7]		-0.25	0	0.25	-0.5	0	0.5	-0.7	0	0.7	ns
tODCV	Output Duty Cycle Variation from 50% [1]		-1.2	0	1.2	-1.2	0	1.2	-1.2	0	1.2	ns
tORISE	Output Rise Time [1]		0.15	1	1.2	0.15	1	1.5	0.15	1.5	2.5	ns
tOFALL	Output Fall Time [1]		0.15	1	1.2	0.15	1	1.5	0.15	1.5	2.5	ns
tLOCK	PLL Lock Time [1,6]				0.5			0.5			0.5	ms
tJR	Cycle-to-Cycle Output Jitter [1]	RMS			25			25			25	ps
		Peak-to-Peak			200			200			200	

NOTES:

1. *All timing and jitter tolerances apply for F_{NOM} > 25MHz.*
2. *Skew is the time between the earliest and the latest output transition among all outputs with the specified load.*
3. *t_{SKEW} is the skew between all outputs. See AC TEST LOADS.*
4. *For XRK39910-2 t_{SKEW} is measured with C_L = 0pF; for C_L = 20pF, t_{SKEW} = 0.35ns Max.*
5. *t_{DEV} is the output-to-output skew between any two devices operating under the same conditions.*
6. *t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{DD} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at CLKIN or FB_IN until t_{PD} is within specified limits.*
7. *t_{PD} is measured with CLKIN input rise and fall times (from 0.8V to 2V) of 1ns.*

FIGURE 3. AC TIMING DIAGRAM (PE= HIGH TIMING)

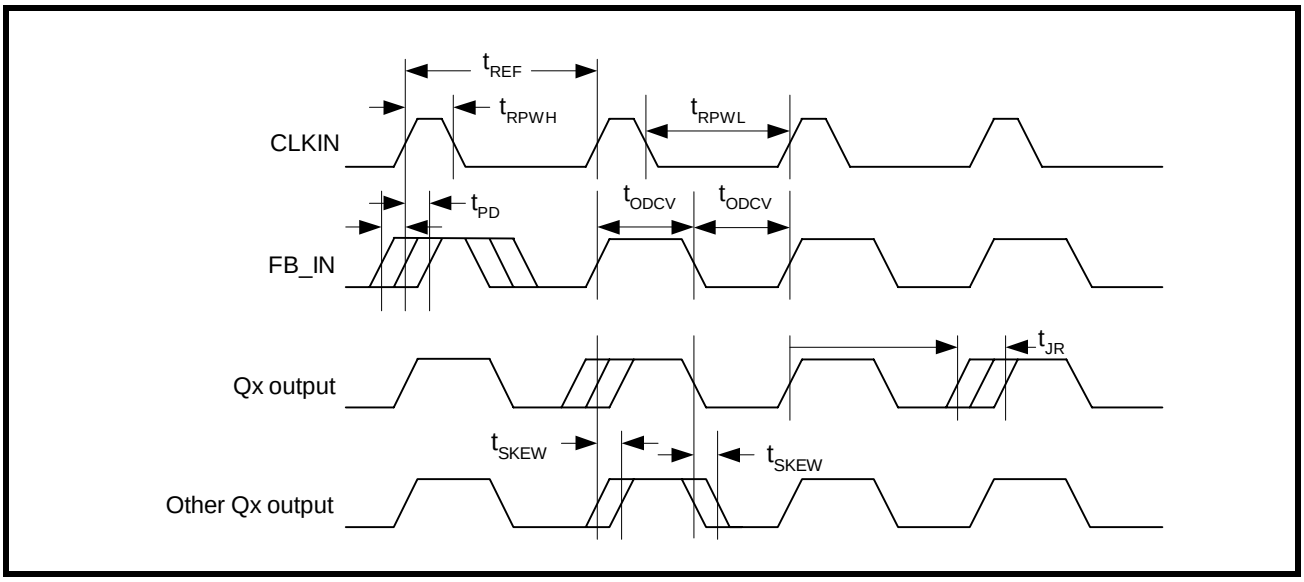
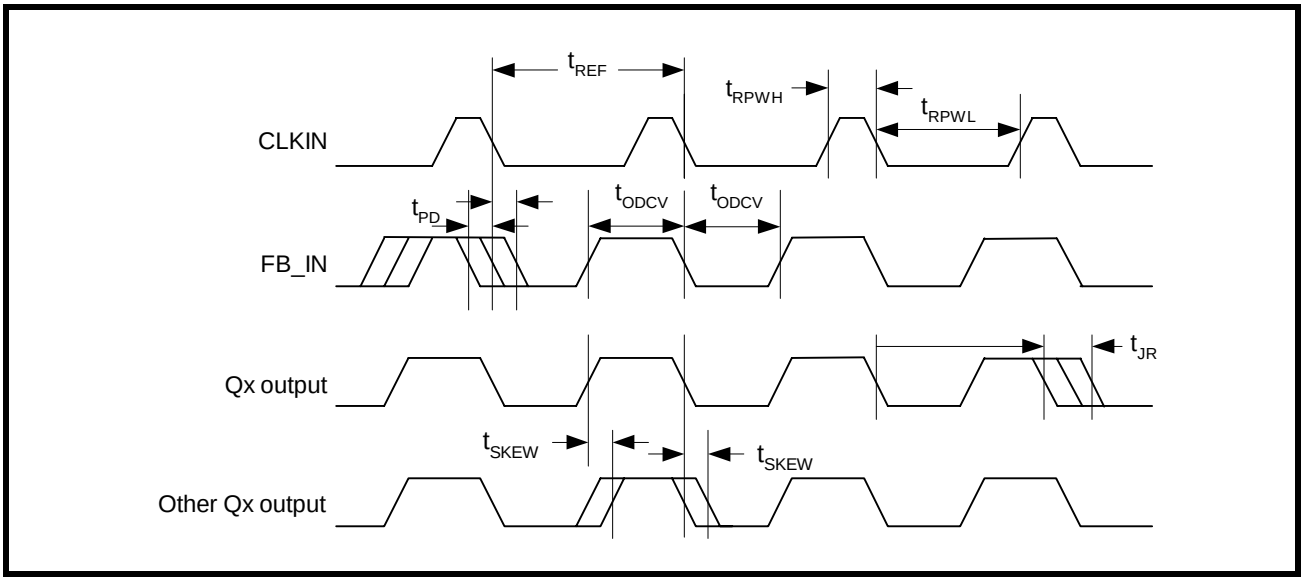


FIGURE 4. AC TIMING DIAGRAM (PE= LOW TIMING)



NOTE:

Skew: The time between the earliest and the latest output transition among all outputs when all are loaded with 20pF and terminated with 75Ω to $V_{DD}/2$.

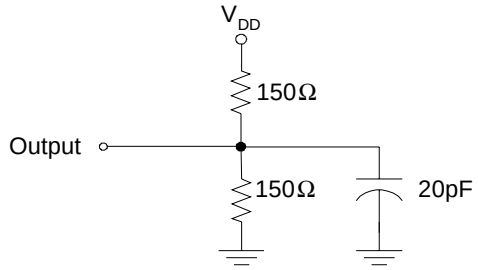
t_{DEV}: The output-to-output skew between any two devices operating under the same conditions (V_{DD}, ambient temperature, air flow, etc.).

t_{ODCV}: The deviation of the output from a 50% duty cycle.

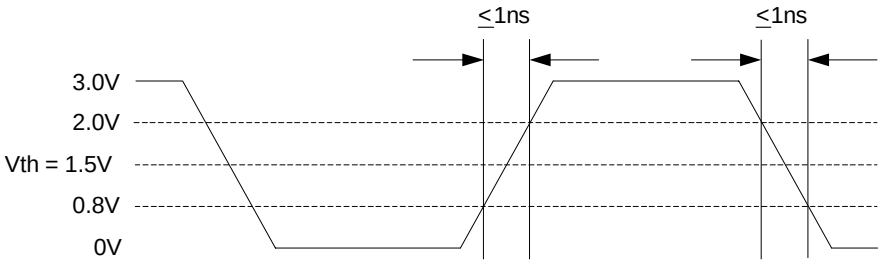
t_{ORISE} and t_{OFALL} are measured between 0.8V and 2V.

t_{LOCK}: The time that is required before synchronization is achieved. This specification is valid only after V_{DD} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at CLKIN or FB_IN until t_{PD} is within specified limits.

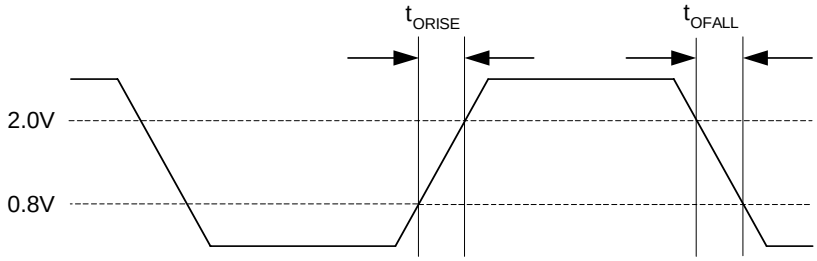
FIGURE 5. AC TEST LOADS AND WAVEFORMS



AC Test Loads



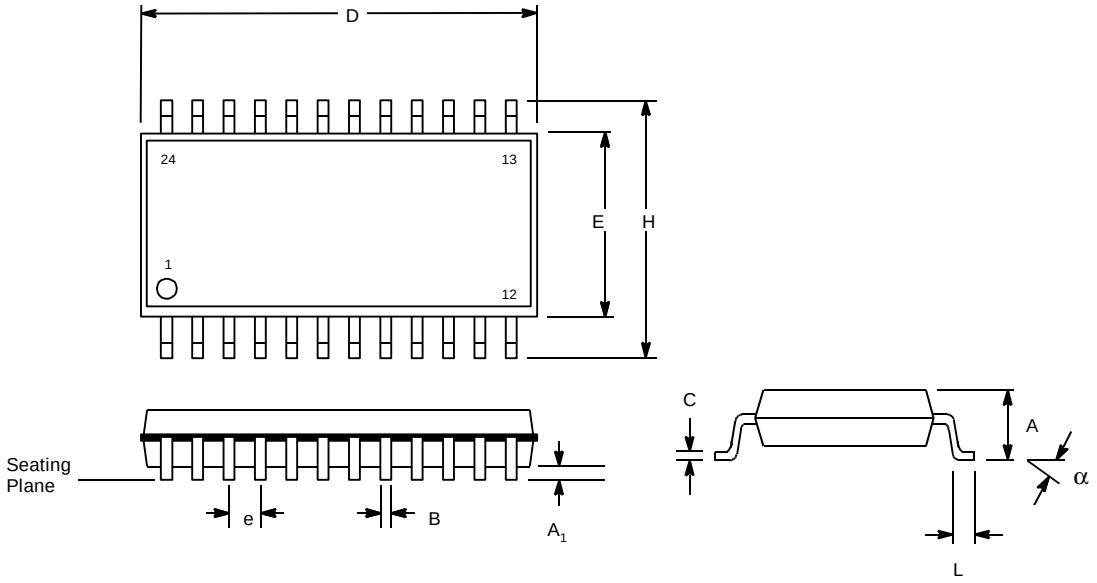
LVTTL Input Test Waveform



LVTTL Output Waveform

PACKAGE DIMENSIONS

24 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
rev. 1.00



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A_1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.598	0.614	15.20	15.60
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
1.0.0	July 18, 2006	Initial release.

NOTICE