XRK32510

3.3V PHASE-LOCK LOOP CLOCK DRIVER WITH 10 CLOCK OUTPUTS

GENERAL DESCRIPTION

The XRK32510 is a high performance, low jitter, low skew clock driver. The XRK32510 uses phase-lock loop (PLL) tecnology to synthesize the CLK_IN signal into 10 output signals (QA), synchronized in both phase and frequency. XRK32510 features low skew, low jitter and 50% duty cycle making it a perfect fit in dual in line memory module (DIMM) board clocking, PC133 SDRAM designs and other server applications.

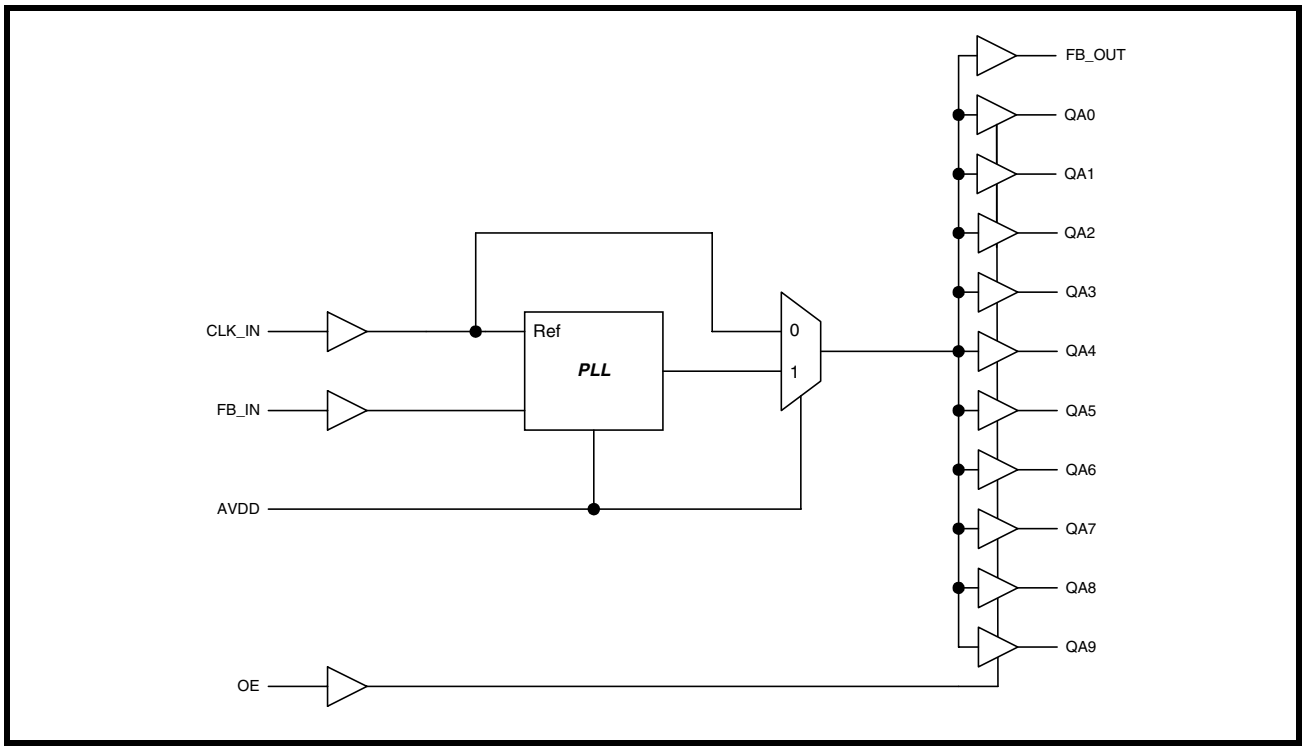
The 10 outputs can be disabled using the Output Enable (OE) pin.

By connecting the Feedback Output (FB_OUT) signal to the Feedback Input (FB_IN) signal, the propagation delay from CLK_IN to the 10 buffered Outputs is nearly zero.

FEATURES

- Spread Spectrum Clock Compatible
- Operating frequency range: 25MHz to 175MHz
- Low noise
- Low jitter internal PLL
- No external RC filter components required
- Meets or exceeds DPC133 registered DIMM specification 1.1
- Output Enable (OE) pin can be used to disable the CLCK_OUT pins
- Operating supply of 3.3V VDD
- Plastic 24 Pin TSSOP package

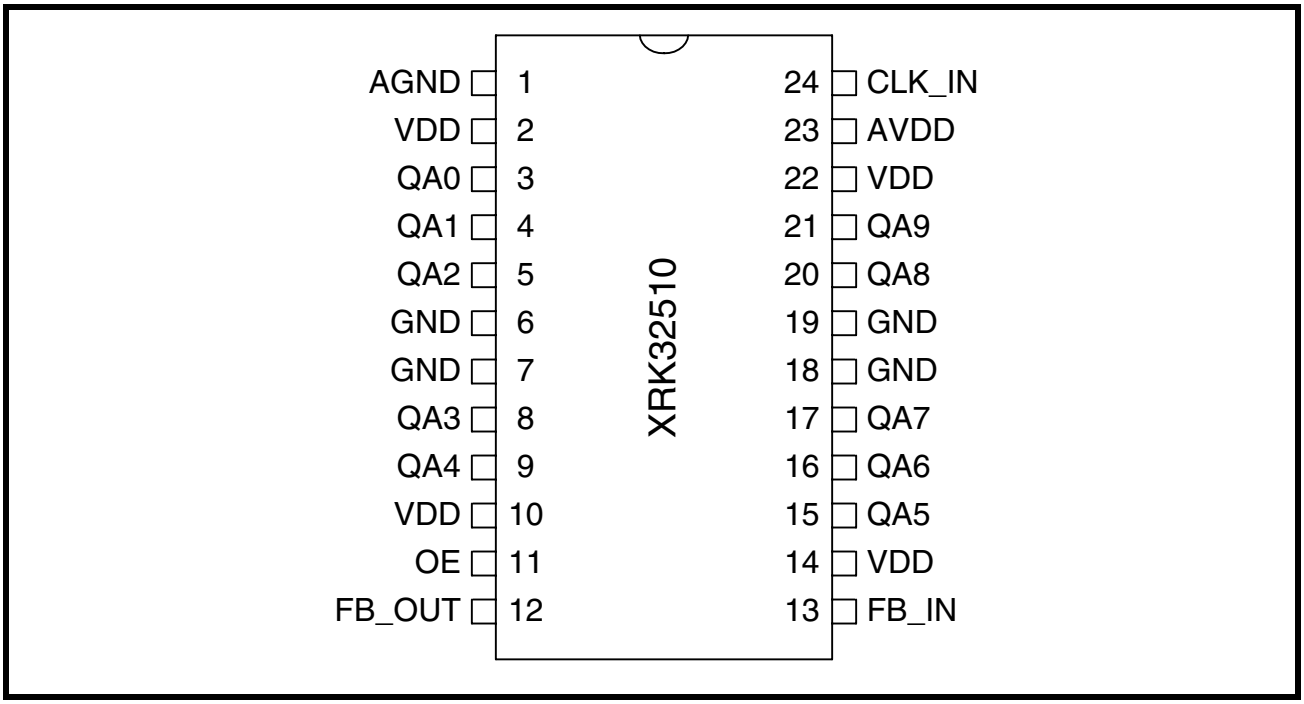
FIGURE 1. BLOCK DIAGRAM OF THE XRK32510



PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRK32510CG	24 Pin TSSOP	0°C to +70°C

FIGURE 2. PIN OUT OF THE XRK32510



PIN DESCRIPTIONS

PIN #	PIN NAME	TYPE	PIN DESCRIPTION
1	AGND	****	**Analog Ground**
2 10 14	VDD VDD VDD	****	**3.3V Power Supply**
11	OE	INPUT	**Output Enable:** "High" = Normal operation, Clock outputs (QA[0:9]) enabled "Low" = Clock outputs (QA[0:9]) disabled
12	FB_OUT	OUTPUT	**Feedback Output:** When this pin is connected to FB_IN, the propagation delay from CLK_IN to any of the 10 QA pins will be nearly zero.
13	FB_IN	INPUT	**Feedback Input**
3 4 5 8 9 15 16 17 20 21	QA0 QA1 QA2 QA3 QA4 QA5 QA6 QA7 QA8 QA9	OUTPUT(S)	**Buffered Clock Outputs:** These 10 outputs provide low-skew, low jitter, 50% duty cycle renditions of CLK_IN
22	VDD	****	**3.3V Digital Power Supply**
23	AVDD	****	**3.3V Analog Supply:** If this pin is connected to ground, the PLL is disabled and will be bypassed and the CLK_IN signal will be connected directly to the output buffers of the 10 QA pins.
24	CLK_IN	INPUT	**Reference Clock Input**

FUNCTIONAL OPERATION

INPUTS		OUTPUTS			PLL CONDITION
OE	AVDD	QA[0:9]	FB_OUT	SOURCE	
0	3.3V	0	Driven	PLL	ON
1	3.3V	Driven	Driven	PLL	ON
BUFFER MODE					
0	0	0	Driven	CLK_IN	OFF
1	0	Driven	Driven	CLK_IN	OFF

ABSOLUTE MAXIMUM RATINGS

Analog Supply Voltage (AVDD)	AVDD < (VDD +0.7V)
Supply Voltage (VDD)	4.3V
Logic Inputs	GND- 0.5V to VDD + 0.5V
Ambient Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS -OUTPUT

T_A = 0 - 70°C, VDD = AVDD = 3.3V +/- 10%, C_L = 20 - 30pF, R_L = 470Ω, (unless otherwise stated)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
R_{DSP}	Output Impedance		36		Ω	V_O = VDD/2
R_{DSN}	Output Impedance		32		Ω	V_O = VDD/2
V_{OH}	Output High Voltage	2.4	3.0		V	I_{OH} = -8mA
V_{OL}	Output Low Voltage		0.2			I_{OL} = 8mA
I_{OH}	Output High Current		-33	-13.6	mA	V_{OH} = 2.4V
			-48	-22		V_{OH} = 2.0V
I_{OL}	Output Low Current	19	28		mA	V_{OL} = 0.8V
		13	19			V_{OL} =0.55V
T_r	Rise Time[1]	0.5	0.8	2.1	ns	V_{OH} = 2.0V, V_{OL} = 0.8V
T_f	Fall Time[1]	0.5	0.9	2.7	ns	V_{OL} = 0.8V, V_{OH} = 2.0V
D_t	Duty Cycle[1]	45	50	55	%	VT = 1.5V, C_L = 30pF
Tcyc-cyc	Cycle to Cycle Jitter[1]		28.7	100	ps	@66 - 100MHz, loaded outputs
			25	75		@133MHz, loaded outputs
T_jABS	Absolute Jitter[1]		57		ps	10,000 cycles, C_L = 30 pF
T_{sk}	Skew[1]		29	150	ps	VT = 1.5V (Window) Output to Output
T_{pe}	Phase Error[1]	-150		150	ps	V_T = VDD/2, CLK_IN to FB_IN
T_{pej}	Phase Error Jitter[1]	-50	35	50	ps	V_T = VDD/2, CLK_IN to FB_IN, Delay Jitter
D_{R1}	Delay Input to Output[1]		3.5	3.7	ns	V_T = 1.5V, PLL Disabled (AVDD = 0)

NOTE:

1. Guaranteed by design, not 100% tested in production

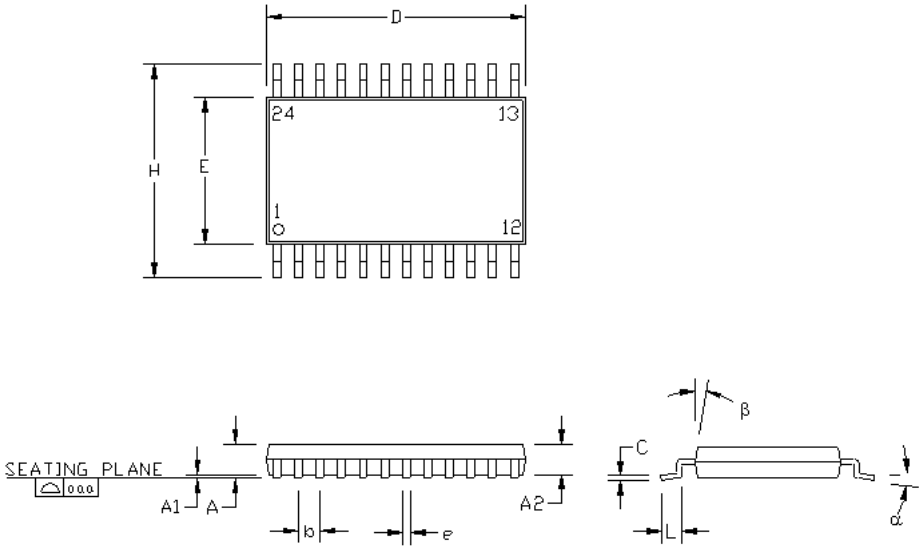
ELECTRICAL CHARACTERISTICS - INPUT AND SUPPLY

T_A = 0 - 70°C, VDD= AVDD = 3.3V +/- 10% (unless otherwise stated)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IH}	Input High Voltage	2		VDD + 0.3	V	
V_{IL}	Input Low Voltage	GND - 0.3		0.8	V	
I_{IH}	Input High Current		0.1	100	µA	V_{IN} = VDD
I_{IL}	Input Low Current		19	50	µA	V_{IN} = 0V
I_{DD}	Operating Current		140	170	mA	C_L = 0pF, F_{IN} = 66MHz
C_{IN}	Input Capacitance		4		pF	Logic Inputs
C_O	Output Capacitance		8		pF	Logic Outputs

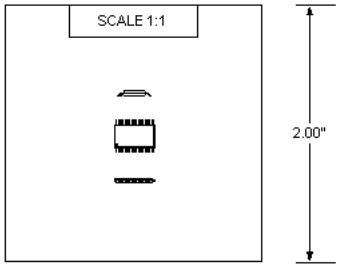
FIGURE 3. PACKAGE OUTLINE DRAWING

EXAR 24 LEAD THIN SHRINK SMALL OUTLINE
(4.4 mm TSSOP)



	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.033	0.047	0.85	1.20
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.80	1.05
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.303	0.311	7.70	7.90
E	0.169	0.177	4.30	4.50
e	0.0256 BSC		0.65 BSC	
H	0.248	0.256	6.30	6.50
L	0.018	0.030	0.45	0.75
α	0°	8°	0°	8°
β	7° typ		7° typ	
aaa	-	0.004	-	0.10

REVISIONS			
REV	DESCRIPTION	DATE	
A	NEW FORMAT	08/16/00	AG



Title: 24 LD TSSOP (4.4 mm/0.9 mmt)

Spec. #:	Rev.: A	Pkg. Code: G24	Ref.: MO-150
Controlled Dimension: millimeters	Reference Dimension: inches		Scale: Not to Scale
ECN #:	Date:		Sheet: 1 of 1

REV

REVISIONS

REV. #	DATE	DESCRIPTION OF CHANGES
1.0.0	9/23/05	Initial issue.
1.0.1	10/06/05	Product ordering information: Remove "F" product numbers and Lead Free column.

NOTICE

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