Introduction

EXAR's family of high resolution and high speed analog-to-digital and digital-to-analog converters are often used in digital video, digital graphics and other mixed signal systems where sampled data phenomenon must be accounted for in optimizing performance. The amplitude attenuation introduced by the "hold" function when recreating analog signals from sampled data is an example. A simple, one amplifier circuit to compensate for this unwanted frequency response loss, while preserving constant group delay, is introduced.

Circuit Description and Results

A diagram of a sample-hold and the proposed compensation circuit is shown in *Figure 1.* When data is taken directly from the output of the sample–hold (OUT1), the magnitude of the frequency response follows a SIN(X)/X curve. Adding the compensation circuit produces a modified and significantly improved frequency response (OUT2). The value of the RC product in the compensation circuit is determined by the sampling frequency (1/4 of sampling period) as shown.

Plots of these effects are shown in *Figure 2.* and *Figure 3.* The frequency responses shown were generated by a SPICE simulation of the circuit shown in *Figure 1.* The sampling frequency (F_S) used was 15 MHz. The RC product for the compensation circuit was 16.6 ns. An ideal op amp was used for the simulation.

The amplitude plot in *Figure 2.* displays three curves. Curve "A" represents the hold transfer function alone. Curve "B" shows the improved transfer characteristics after compensation. Curve "C" shows the amplitude of the first order lead response supplied by the compensation circuit to hold the overall response flat to higher frequencies. If the compensation circuit was only a simple first order lead, it would introduce phase distortion into the modified frequency response. To prevent this, a portion of the compensation section is an all pass, phase equalization circuit to keep the phase shift linear. The group delay plot in *Figure 2.* presents the results. Curve "D" shows the ideally constant group delay of the hold circuit. Curve "E" shows group delay after amplitude compensation and phase linearization. Note that only a few nanoseconds deviation from constant group delay exist for frequencies lower than half the sampling rate (7.5 MHz).

Figure 3. repeats the information of *Figure 2.* but uses an expanded scale so more detail is visible in the signal band. It can be seen that the amplitude error at half sampling frequency (7.5 MHz) can be lowered from almost 4 dB to less than 0.25 dB. Curve "F" was added to the group delay plot, This shows the group delay response to be expected with lead compensation alone. This demonstrates that the phase equalization is desirable since considerable phase distortion would be present otherwise.

Conclusion

The circuit to compensate for the effects of the sample/hold operation can also be placed in the analog path prior to the A/D converter when linear operations are being performed on the signals. Antialiasing and smoothing filters sometimes have the SIN(X)/X compensation function built in.

The single amplifier circuit proposed in *Figure 1.* approximately implements the transfer function:

$$\frac{OUT2(s)}{OUT1(s)} = \frac{(1 \bullet s \bullet RC)(1 + 1.4 \bullet RC \bullet s)}{(1 + s \bullet RC)(1 + 0.25 \bullet RC \bullet s)}$$

Any alternate circuit having this transfer function will produce the same results. The resistors, capacitors, and op amps used must be selected carefully to be compatible with the frequency requirements. The SPICE file used to generate the frequency response plots is listed below.

PSPICE CIRCUIT FILE

```
hold compensation test
**************************************************
.ac oct 200 1k 100meg
**************************************************
vin 1 0 ac 1

ehold 2 0 LAPLACE {v(1)}={(1-exp(-s/15e6))/(s/15e6)}  ;hold


e1 14 0 11 10 1000
r1 2 10 1.0k
r2 2 11 1.0k
r3 10 12 1.0k
r4 14 12 .1k
r5 13 0 .02k
c1 11 0 16.5p
c2 12 13 200p


rn1 1 0 1t
rn2 2 0 1t
**********************************************************
.OPTIONS   ITL5=0 ITL4=140 itl1=150 itl2=150 RELTOL=.001
NOPAGE NUMDGT=6 abstol=1e-15
**********************************************************
.probe
.END
```

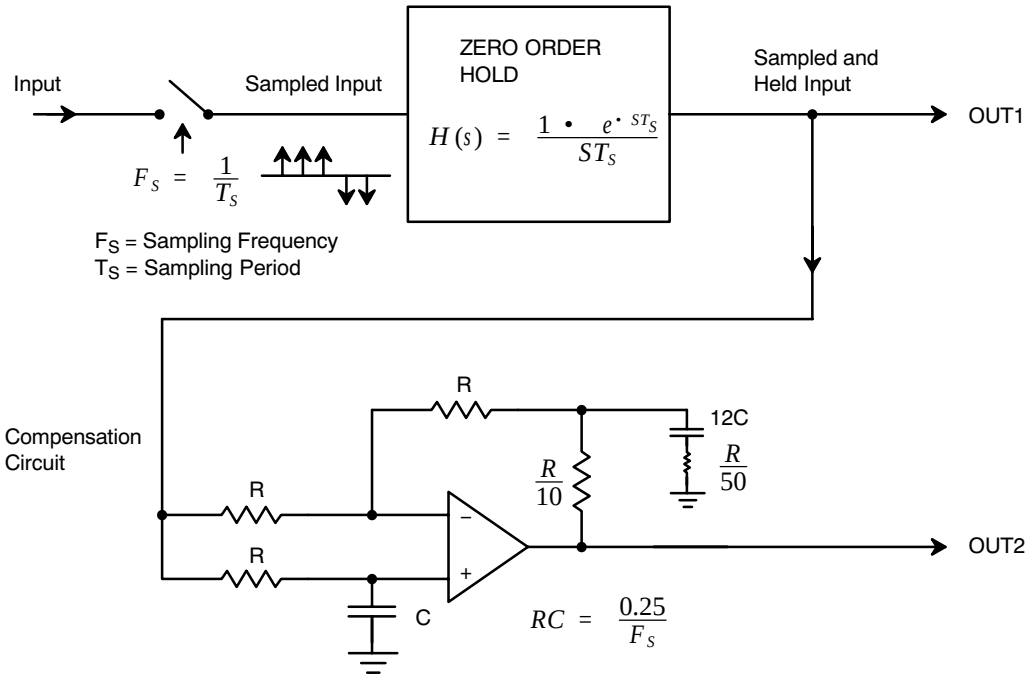

Figure 3. Compensating for Zero Order Hold Amplitude Attenuation

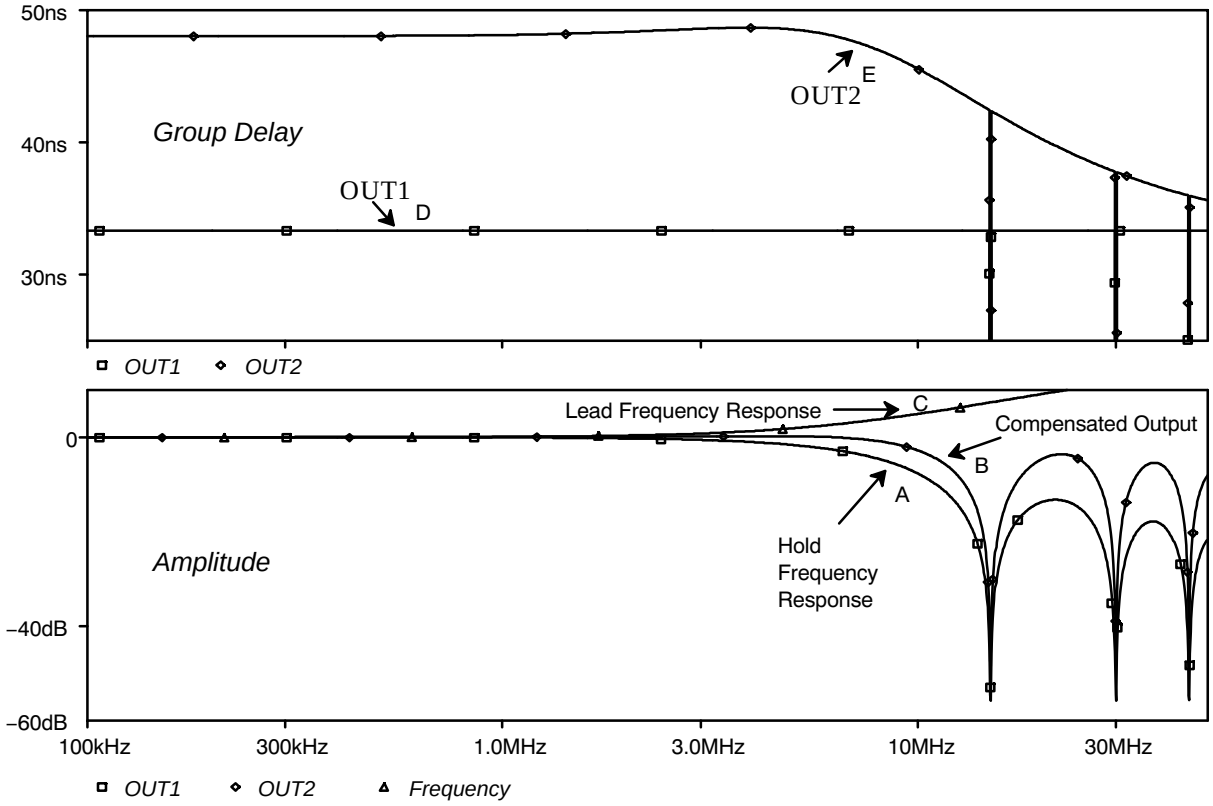

Figure 4. Comparison of Hold Response before and after Compensation

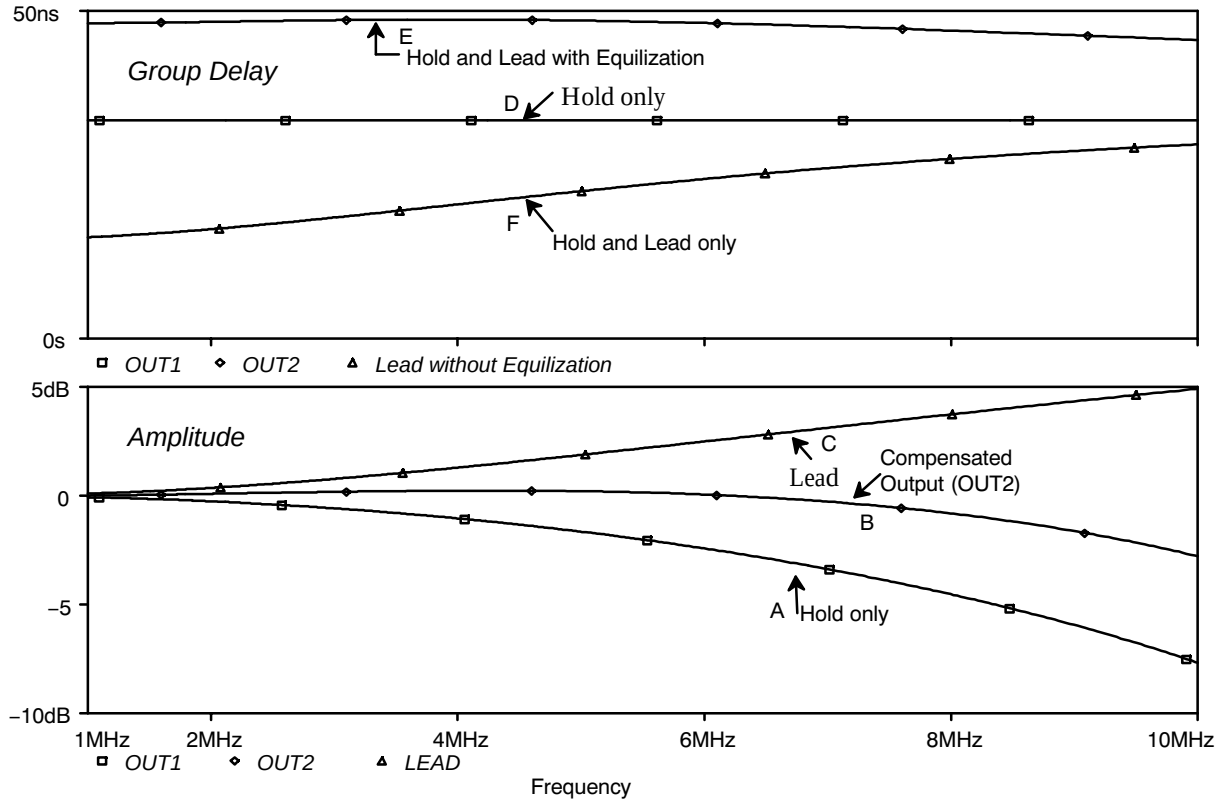

Figure 5. Comparison of Hold Response before and after Compensation