# T1C PCM Repeater Chip Set

## GENERAL DESCRIPTION

The IC pair, XR-C587 and XR-C588, provides all the active circuitry needed to form one side of a T1C PCM Repeater (3.152 MBits/sec). Each chip is packaged in a 16-Pin CERDIP package, with an operating temperature range of -40°C to +85°C. The supply voltage range is 6.0 to 6.8 $V_{DC}$, with a typical supply current for the pair of 16 mA.

The XR-C587 contains an amplifier, three ALBO ports, and an npn transistor. The amplifier is a modified version of the amplifier in Exar's XR-C262 T1 repeater chip. This amplifier has its own ground pin for isolation, as well as for eliminating the amplifier current drain if only the XR-C587 ALBO diodes and/or the transistor are used. Each of the three ALBO ports has a separate ground and one common drive input. Any number, up to three, can be used while eliminating current in any not used. The npn transistor is provided for incidental uses.

The XR-C588 contains a preamplifier, an ALBO drive output, a voltage reference, comparators, a clock recovery circuit, ECL latches and two output drivers. The XR-C588 is a modified version of XR-C262 for T1C performance. The amplifiers in the XR-C587 and XR-C588 are the same. The clock driver output is modified to drive a crystal and has higher gain. Both inputs to the clock amplifier are available. The clock amplifier may be biased, both from the center tap voltage (Pin 14), and the clock bias voltage (Pin 7).

Two options for the clock comparator threshold voltage are provided. Option 1 is 65% of ALBO threshold, and Option 2 is 50% (the same as C262).

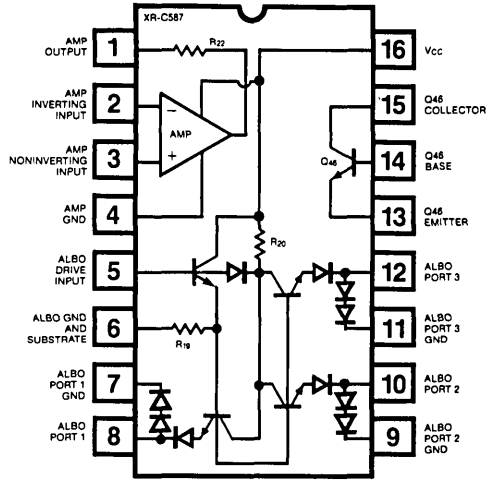
## FEATURES

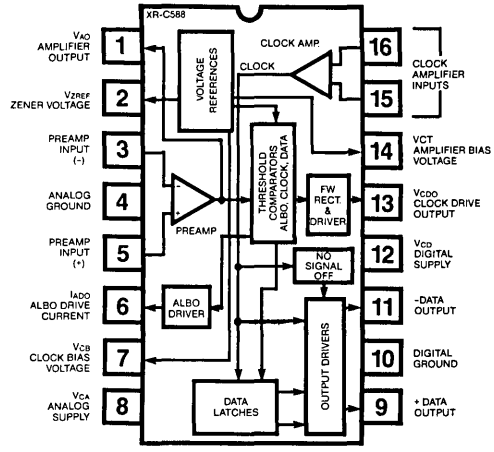
Modified Preamplifier with Improved Phase Margin
Separate Grounds for Preamplifier and ALBO Ports
Crystal Drive Capability for High Q Operation
Optional Clock Comparator Threshold Levels (50% & 65%)

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Supply Voltage | -0.5V to 10V |
| Digital Supply Voltage | -0.5V to 10V |
| Differential Input Voltage | -5V to 5V |
| Output Voltage | -0.5V to 20V |
| Storage Temperature | -65°C to +150°C |
| Operating Temperature | -40°C to +85°C |
| Lead Soldering (10 seconds) | 300°C |

## FUNCTIONAL BLOCK DIAGRAMS




## ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-C587 | Ceramic | -45°C to +85°C |
| XR-C588 | Ceramic | -45°C to +85°C |

## ELECTRICAL CHARACTERISTICS – XR-C587/C588

**Test Conditions:** $T_A$ = -40°C to +85°C, at a supply voltage of $V_{CC}$ = 6.0V to 6.8V dc, Unless otherwise specified.

| PARAMETERS | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| SUPPLY | | | | | |
| Supply Voltage | 6.0 | 6.4 | 6.8 | V dc | |
| Supply Current | 2.3 | 2.7 | 3.3 | mA | All ALBO Pins open $V_{CC}$ = 6.3V |
| ALBO Bias Current | 200 | 280 | 360 | mA | ALBO Grounds open<br>ALBO drive pin at 3.5V (≈ 5 $V_{BE's}$) |
| AMPLIFIER | | | | | |
| DC open-loop gain | 54 | 60 | 68 | dB | 1V p-p output level, $R_L$ = 4 kΩ |
| AC gain at 1 MHz | 34 | | | dB | returned to $V_{CM}$ = 2.7V |
| Corner Frequency | | 110 | | kHz | |
| Input Offset Voltage | -15 | 0 | +15 | mV | $R_S$ = 10 kΩ to both inputs |
| Input Bias Current | | 1 | 4 | μA | |
| Output Sink Current | 300 | 400 | 500 | μA | |
| ALBO | | | | | |
| One Common Drive Input, Three Ports, Each With Its Own Ground | | | | | |
| Max ALBO Current | 2.5 | 4.5 | 6 | mA | Total current to Ground through all ALBO Ground Pins, Drive input returned to $V_{CC}$ = 6.0V through 51 kΩ. |
| ALBO Current Mismatch | -5 | 0 | +5 | % | Measured with 1 mA nominal level in each ALBO Ground Pin. |
| ALBO Port Voltage | 1.2V | 1.45 | 1.7V | V dc | Two $V_{BE}$ above Ground, 1 mA in each Port. |
| ALBO OFF Impedance | 10 | | | kΩ | Drive input and ALBO Ground Pins Grounded Frequency = 1.5 MHz |
| SINGLE TRANSISTOR | | | | | |
| Beta (β) | 75 | 150 | 400 | | $V_{CE}$ = 6.8V, $I_C$ = 100 mA |
| Leakage | 0.01 | 1 | 5 | μA | $V_{CEO}$ = 6.8V |

## ELECTRICAL CHARACTERISTICS – XR-C588

**Test Conditions:** $T_A$ = -40°C to +85°C, at a supply voltage of $V_{CC} = V_{CA} = V_{CD}$ = 6.0V to 6.8V dc, Unless otherwise specified.

| PARAMETERS | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| SUPPLY CURRENTS | | | | | |
| $I_{CA}$, $V_{CA}$ Supply Current | 1.8 | 3.5 | 5 | mA | $V_{CA}$ is Analog Supply Voltage |
| $I_{CD}$, $V_{CD}$ Supply Current | 5 | 8 | 12 | mA | $V_{CD}$ is Digital Supply Voltage<br>Outputs off, $V_{AO} = V_{CT}$ |
| $I_{CCT}$, $I_{CA} + I_{CD}$ | 7 | 12.5 | 14.5 | mA | Outputs off, $V_{AO} = V_{CT}$ |
| AMPLIFIER | | | | | |
| Same specification as amplifier in C587 | | | | | $V_{AO}$ = Amplifier Output Voltage |
| VOLTAGE REFERENCES | | | | | |
| $V_{zref}$, Zener Voltage | 5.0 | 5.4 | 5.65 | Volts | No external loading |
| $V_{CT}$, Center Tap Voltage | 2.35 | 2.70 | 2.90 | Volts | No external loading |
| $V_{CB}$, Clock Bias | 3.5 | 4.0 | 4.3 | Volts | No external loading |
| THRESHOLD VOLTAGES | | | | | |
| ALBO Comparator | | | | | |
| $V_{APD}^+$, ALBO + peak detector voltage | .75 | .9 | 1.05 | Volts | $V_{AO}$ measured w/respect to $V_{CT}$, with $I_{ADO}$ = 100 µA |
| $V_{APD}^-$, ALBO - peak detector voltage | -.75 | -.9 | -1.05 | Volts | |
| $V_{APD}^+ - V_{APD}^-$ | -50 | 0 | 50 | mV | |
| Data Comparators | | | | | |
| $V_{DT}^+$, + data threshold | 42 | 48 | 53 | % of $V_{APD}^+$ | $V_{AO}$ varied, clock drive input = 3.152 MHz sine wave at .5V pp. Detect onslaught of output pulses at 3.152 MHz, measure $V_{AO}$. |
| $V_{DT}^-$, - data threshold | 42 | 48 | 53 | % of $V_{APD}^-$ | Same as for $V_{DT}^+$ |
| $V_{DT}^+ - V_{DT}^-$ | 30 | 0 | 30 | mV | |
| Clock Comparator | | | | | |
| $V_{CLK}^+$, + clock threshold | *57/42 | 62/48 | 67/53 | % of $V_{APD}^+$ | $V_{AO}$ varied, detect 100 mV change in $V_{CDO}$. |
| $V_{CLK}^-$, - clock threshold | *57/42 | 62/48 | 67/53 | % of $V_{APD}^-$ | |
| $V_{CLK}^+ - V_{CLK}^-$ | 35/30 | 0/0 | 35/30 | mV | |

* Upper limits are for Option 1, lower limits are for Option 2.

**ELECTRICAL CHARACTERISTICS – XR-C588** (Continued)

**Test Conditions:** $T_A$ = -40°C to +85°C, at a supply voltage of $V_{CC} = V_{CA} = V_{CD}$ = 6.0V to 6.8V dc, Unless otherwise specified.

| PARAMETERS | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| CLOCK DRIVE OUTPUT $V_{CDO}$ | | | | | |
| $A_{CD}$+, gain from $V_{AO}$ to $V_{CDO}$ | -2.7 | -3.0 | -3.3 | V/V | $V_{AO}$ changed from $V_{CLK}$+ to ($V_{CLK}$+ + .5V) measure change in $V_{CDO}$. |
| $A_{CD}$- | 2.7 | 3.0 | 3.3 | V/V | $V_{AO}$ changed from $V_{CLK}$- to ($V_{CLK}$- - .5V) measure change in $V_{CDO}$. |
| $A_{CD}$+/$A_{CD}$- | -1.1 | -1.0 | -.9 | | |
| $V_{CDO}$ High | -1.8 | -1.5 | -1.1 | V | $V_{CDO}$ measured w/respect to $V_{CC}$. $V_{AO}$=$V_{CT}$ |
| $V_{CDO}$+ Low | | | -3.2 | V | $V_{CDO}$ measured w/respect to $V_{CC}$. $V_{AO}$ = $V_{CT}$ + 1.5 volts. |
| $V_{CDO}$- Low | | | -3.2 | V | $V_{CDO}$ measured w/respect to $V_{CC}$. $V_{AO}$ = $V_{CT}$ – 1.5 volts. |
| CLOCK AMPLIFIER | | | | | |
| $V_{CACM}$, Clock input Common Mode Bias Voltage | 2.35 | | 4.3 | V | $V_{CT}$ or $V_{CB}$ can be used as $V_{CACM}$ |
| Input Offset Voltage | -15 | | 15 | mV | |
| Input Bias Current | | 1 | 4 | μA | |
| ALBO DRIVE $I_{ADO}$ | | | | | |
| $I_{ADO}$ Max | .7 | 1.5 | 3.0 | mA | $V_{AO}$ at $V_{CT}$ ± 1.5 volts $I_{ADO}$ measured to Gnd. |
| $I_{ADO}$ Off | | | 10 | μA | $V_{AO}$ = $V_{CT}$, $I_{ADO}$ measured to Gnd. |
| OUTPUT DRIVER | | | | | |
| $I_O$± Leak | | 100 | | μA | Output off and returned to 20 volts. |
| $V_{OL}$± | .5 | .8 | 1.0 | Volts | $I_{LOAD}$ = 15 mA |
| $V_{OL}$+ - $V_{OL}$- | -80 | 0 | +80 | mV | $I_{LOAD}$ = 15 mA |
| $T_{OPW}$±, output pulse width | 143 | 159 | 175 | nsec | 50% Pts. $R_L$ = 350Ω |
| $T_{OPW}$+ - $T_{OPW}$- | -10 | 0 | 10 | nsec | |
| $T_{RT}$±, Rise time | | | 40 | nsec | $R_L$ = 350Ω 20% to 80% Pts. |
| $T_{FT}$±, Fall time | | | 40 | nsec | $R_L$ = 350Ω 20% to 80% Pts. |
| NO SIGNAL PROTECTION | | | | | With no clock signal, Output will be off. |

## PRINCIPLES OF OPERATION

T1C is a digital line system operating at 3.152 Mbits/sec, very similar, in principle, to the T1 line system. It provides 48 digitally encoded and time division multiplexed voice channel repeaters containing 2 regenerators which have the approximate spacing of 6300 ft. Power is provided by a simplex arrangement with a line current of 120 mA. Two regenerators share a common power supply. Basic repeater functions, namely reshaping, retiming and regenerating, are performed for cable losses from 6 to 54 dB, as measured at 1.576 MHz.

The bipolar PCM signal, which is attenuated and distorted due to transmission medium, is applied to a preamplifier through a pulse-shaping network. This network, and the variolosser diodes, forms the ALBO circuitry which provides attenuation and shaping to automatically adjust for varying cable characteristics.

A feedback network is used around the preamplifier for gain equalization, as well as to reject out-of-band noise. The output of the preamplifier is controlled to swing between two established peak levels, and drives a set of data comparators which are internally biased from a voltage reference and precision voltage divider network. The preamplifier output is sliced at various voltage levels to eliminate the effects of baseline noise. This output is full wave rectified, and applied to a crystal time extraction circuit. The sinusoidal wave shape from the time extraction circuit is differentially coupled to a clock slicer block to produce the internal square wave clock signal.

The regeneration of data is achieved through a pair of data comparators and ECL latches. The data slicing levels are set to ± 50% of the preamplifier output peak voltages ECL latch outputs and clock signal are then gated to produce two precisely timed output data signals. The positive and negative data paths are separate but identical in design.

A zero input protection circuit is provided for the dual task of preventing the output switches from latching in an ON state, as well as reducing the likelihood of output pulses with no input signal.

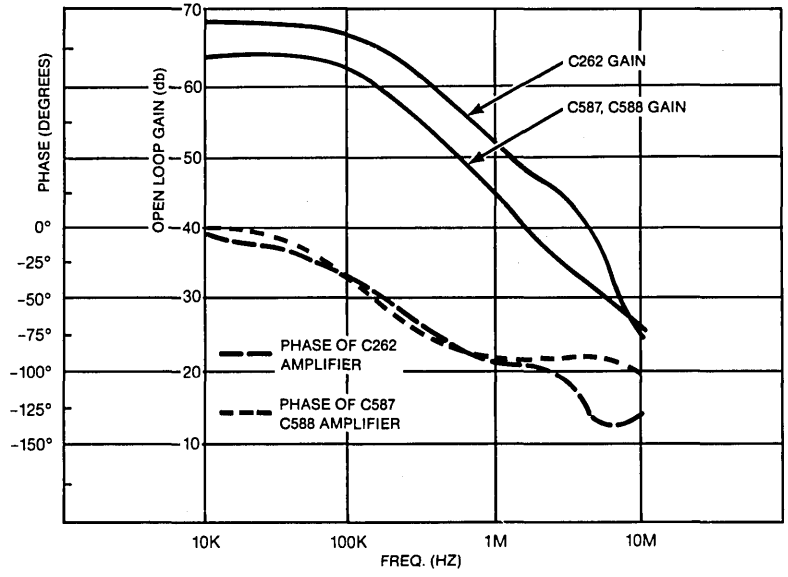



**Figure 1: Bode Plot of C262 and C587/C588 Amplifiers.**

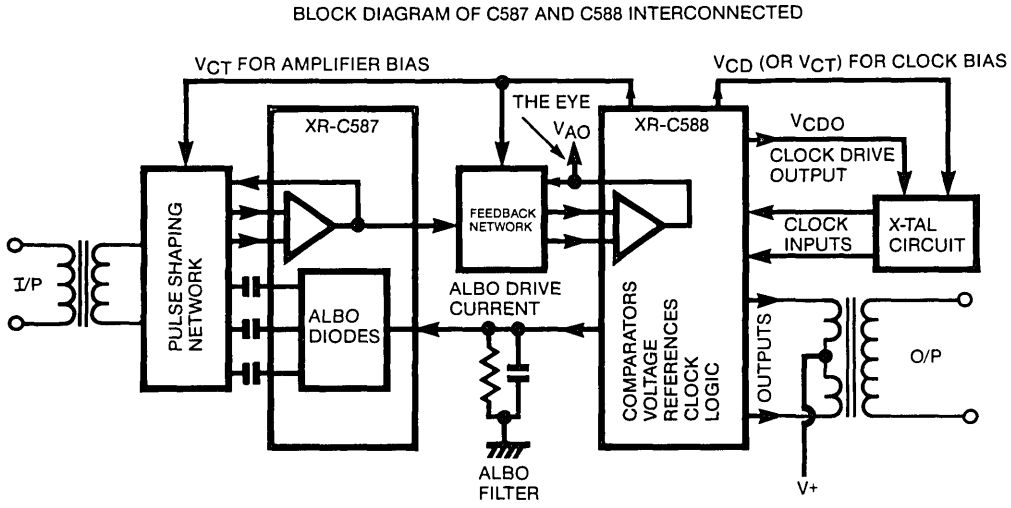



**Figure 2: Block Diagram of C587/C588 Interconnected.**