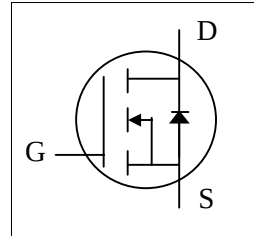


- ▼ 100% R_g & UIS Test
- ▼ Simple Drive Requirement
- ▼ Lower On-resistance
- ▼ RoHS Compliant & Halogen-Free

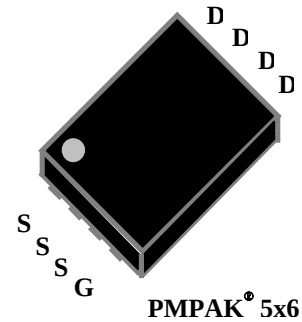


BV_{DSS}	60V
$R_{DS(ON)}$	3.28m Ω

Description

XP6NA3R2 series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK[®] 5x6 package is special for DC-DC converters application and the foot print is compatible with SO-8 with backside heat sink and lower profile.



Absolute Maximum Ratings@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ\text{C}$	Drain Current, V_{GS} @ 10V ⁴ (Silicon Limited)	112	A
$I_D@T_C=25^\circ\text{C}$	Drain Current, V_{GS} @ 10V ⁴	100	A
$I_D@T_A=25^\circ\text{C}$	Drain Current, V_{GS} @ 10V ³	30	A
$I_D@T_A=70^\circ\text{C}$	Drain Current, V_{GS} @ 10V ³	24	A
I_{DM}	Pulsed Drain Current ¹	350	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation	69.4	W
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation ³	5	W
E_{AS}	Single Pulse Avalanche Energy ⁵	125	mJ
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
R_{thj-c}	Maximum Thermal Resistance, Junction-case	1.8	$^\circ\text{C}/\text{W}$
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	25	$^\circ\text{C}/\text{W}$

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	60	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =20A	-	-	3.28	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	2	-	4	V
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =20A	-	60	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =48V, V _{GS} =0V	-	-	25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} = ±20V, V _{DS} =0V	-	-	±0.1	uA
Q _g	Total Gate Charge	I _D =20A	-	62	99.2	nC
Q _{gs}	Gate-Source Charge	V _{DS} =30V	-	18	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	17	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =30V	-	18	-	ns
t _r	Rise Time	I _D =20A	-	52	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =6Ω	-	42	-	ns
t _f	Fall Time	V _{GS} =10V	-	63	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	3400	5440	pF
C _{oss}	Output Capacitance	V _{DS} =50V	-	560	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	30	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1	2	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =20A, V _{GS} =0V	-	-	1.3	V
t _{rr}	Reverse Recovery Time	I _S =20A, V _{GS} =0V,	-	42	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	37	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board, t ≤10sec; 60°C/W at steady state.
- 4.Package limitation current is 100A .
- 5.Starting T_j=25°C , V_{DD}=30V , L=0.1mH , R_G=25Ω , V_{GS}=10V

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT, AUTOMOTIVE OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

XSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

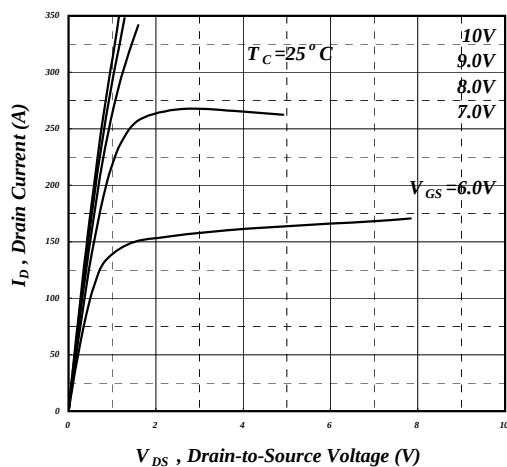


Fig 1. Typical Output Characteristics

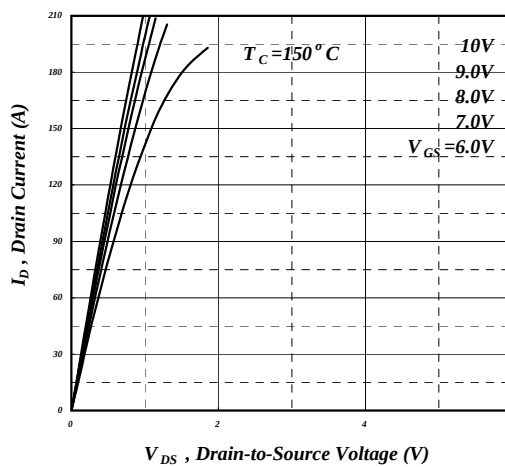


Fig 2. Typical Output Characteristics

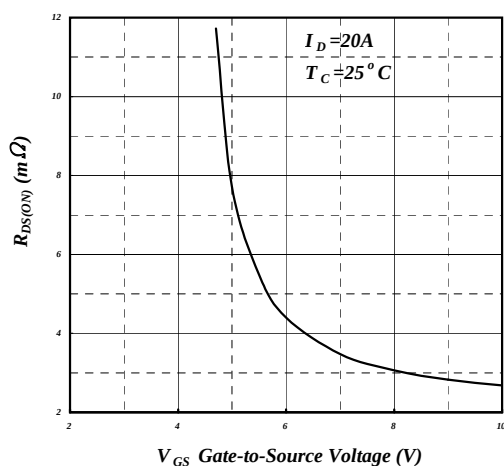


Fig 3. On-Resistance v.s. Gate Voltage

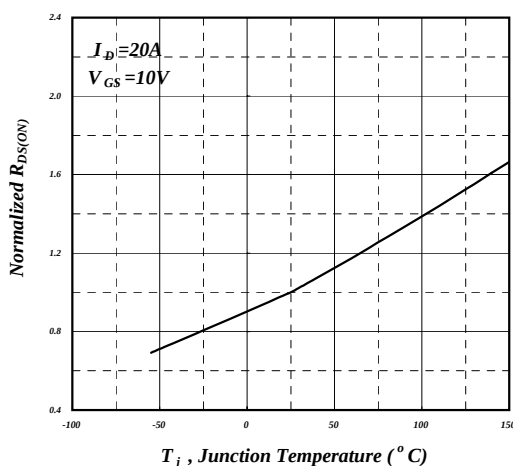


Fig 4. Normalized On-Resistance v.s. Junction Temperature

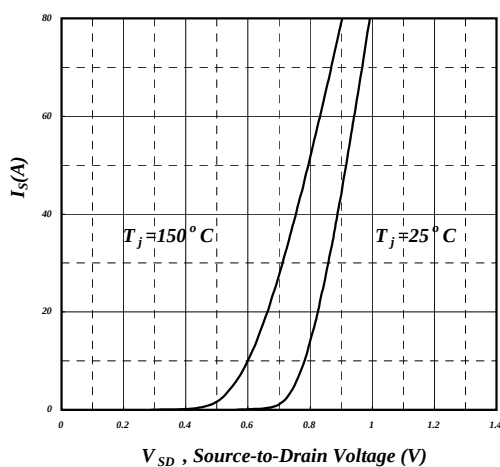


Fig 5. Forward Characteristic of Reverse Diode

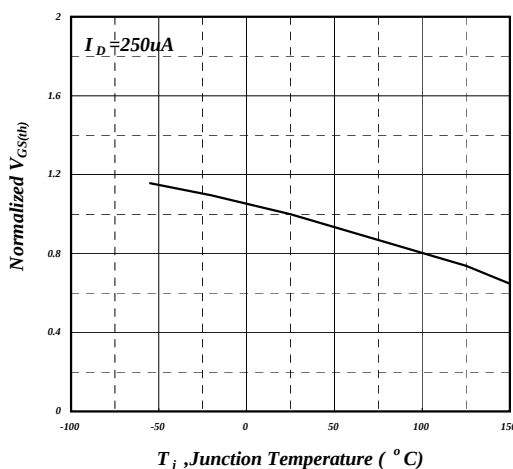


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

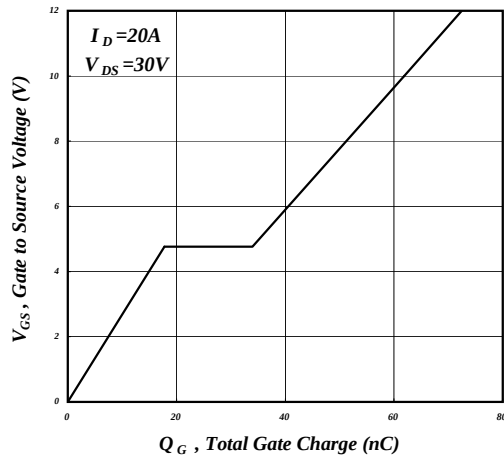


Fig 7. Gate Charge Characteristics

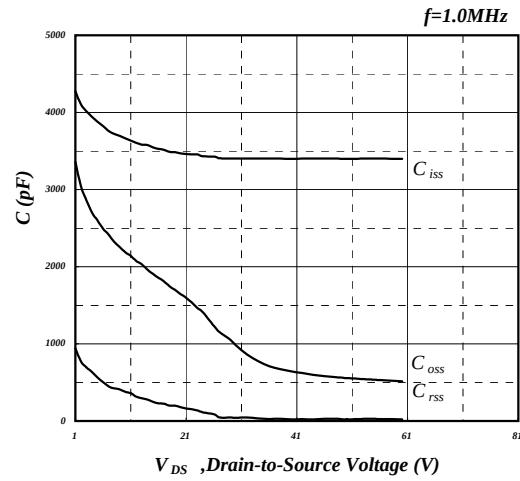


Fig 8. Typical Capacitance Characteristics

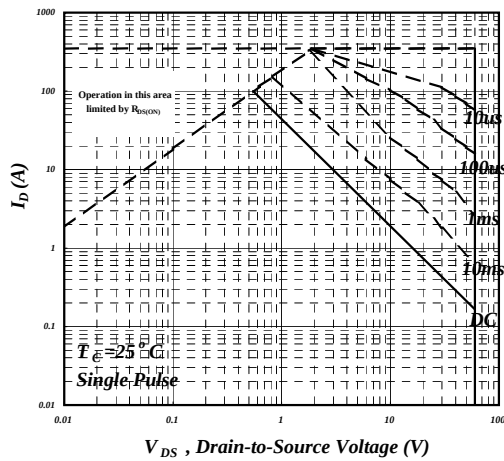


Fig 9. Maximum Safe Operating Area

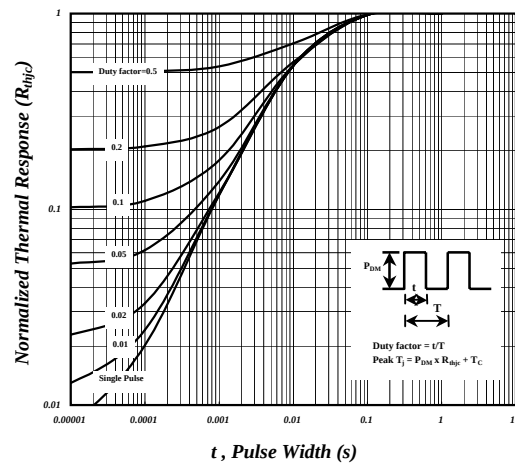


Fig 10. Effective Transient Thermal Impedance

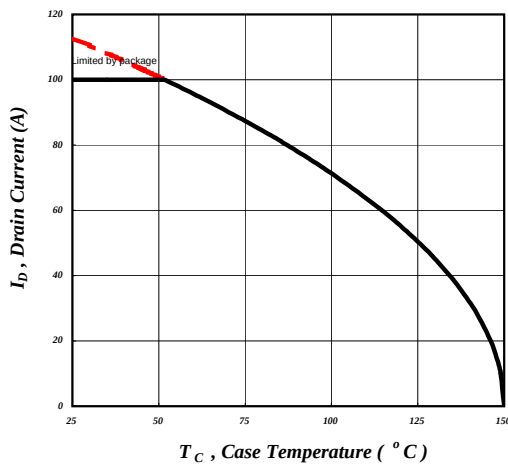


Fig 11. Drain Current v.s. Case Temperature

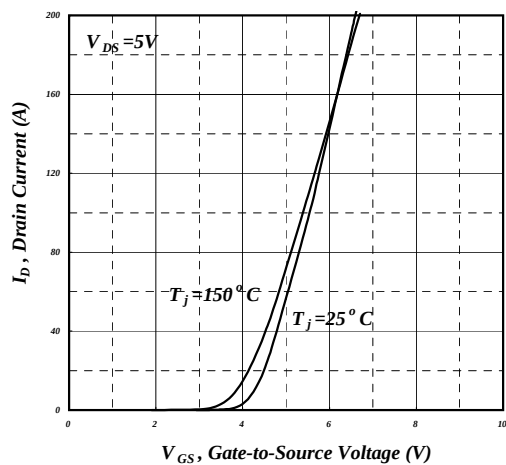


Fig 12. Transfer Characteristics

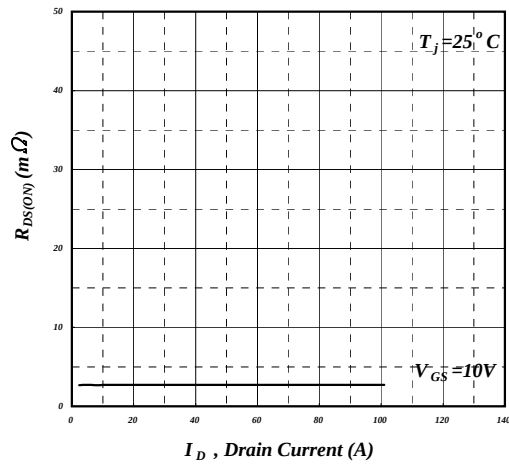


Fig 13. Typ. Drain-Source on State Resistance

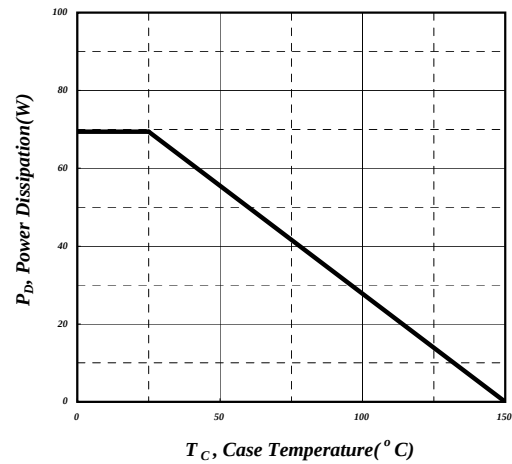


Fig 14. Total Power Dissipation

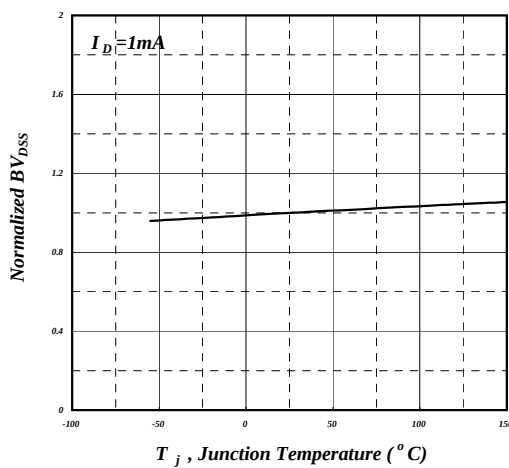
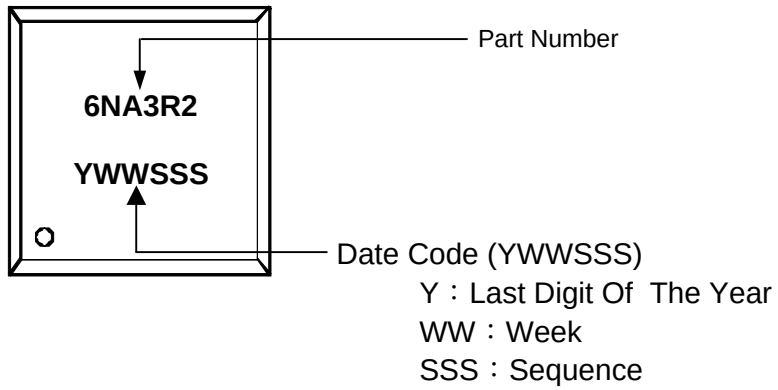
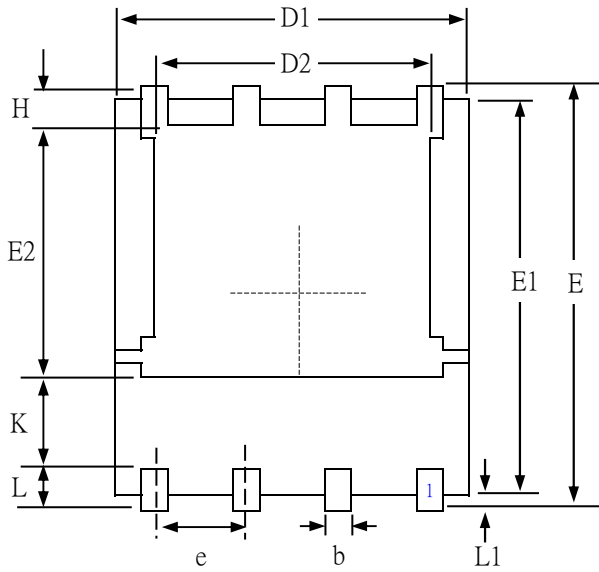


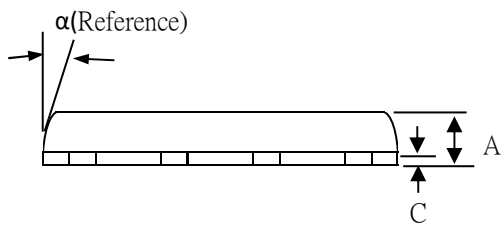
Fig 15. Normalized BV_{DS} v.s. Junction Temperature

MARKING INFORMATION

Package Outline : PMPAK 5x6



BACKSIDE VIEW



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.90	1.10	1.30
b	0.33	0.41	0.51
C	0.254(Ref.)		
D1	4.80	4.90	5.10
D2	3.61	4.00	4.40
E	5.80	6.03	6.25
E1 (Ref.)	5.60	5.75	5.90
E2 (Ref.)	3.30	3.55	3.80
e	1.27 BSC		
H	0.35	—	0.90
K (Ref.)	1.00	1.275	—
L	0.35	0.55	0.75
L1	0.06	0.13	0.20
$\alpha(\text{Ref.})$	0°	—	12°

- 1.All dimension are in millimeters.
- 2.Dimension does not include burrs and mold flash/protrusions.
- 3.The outline schematic is not to scale and slightly different from the actual product appearance.

Technical drawing showing the front and top views of a mechanical part with the following dimensions:

- Front View (Top):**
 - Overall width: 5.1
 - Distance from left edge to centerline: 2.55
 - Height of the top profile: 0.9
 - Overall height of the part: 4.45
- Top View (Bottom):**
 - Overall width: 5.1
 - Distance from left edge to centerline: 2.55
 - Distance from centerline to right edge: 2.55
 - Overall height of the part: 6.5
 - Distance from left edge to first hole center: 0.95
 - Distance between first and second hole centers: 1.27
 - Distance between second and third hole centers: 0.72
 - Distance between fourth and fifth hole centers: 0.55
 - Distance from fifth hole center to right edge: 0.95
 - Distance from bottom edge to first hole center: 1.1

Draw No. M1-MT-8-EIFMRL-G-v08