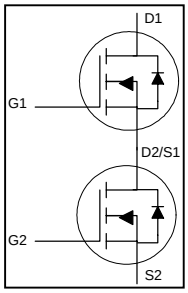
XP6932MT

Halogen-Free Product

ASYMMETRIC DUAL N-CHANNEL

ENHANCEMENT MODE POWER MOSFET

- **Simple Drive Requirement**
- **Easy for DC/DC Buck Converter Application**
- **RoHS Compliant & Halogen-Free**

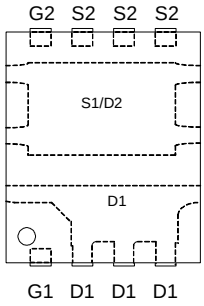


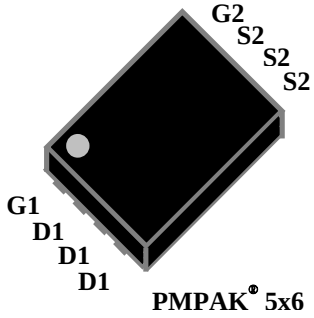
CH-1	BV_{DSS}	30V
	$R_{DS(ON)}$	5.5mΩ
CH-2	BV_{DSS}	30V
	$R_{DS(ON)}$	2.5mΩ

Description

XP6932 series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The control MOSFET (CH-1) and synchronous MOSFET (CH-2) co-package for synchronous buck converters.





Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating		Units
		CH-1	CH-2	
V_{DS}	Drain-Source Voltage	30	30	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D@T_C=25℃	Drain Current (Package Limited)	28	40	A
I_D@T_A=25℃	Drain Current , V_{GS} @ 10V[3]	14.2	22.9	A
I_D@T_A=70℃	Drain Current , V_{GS} @ 10V[3]	11.3	18.4	A
I_{DM}	Pulsed Drain Current[1]	112	160	A
P_D@T_A=25℃	Total Power Dissipation[3]	1.78	2.08	W
E_{AS}	Single Pulse Avalanche Energy[6]	18	32	mJ
T_{STG}	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃

Thermal Data

Symbol	Parameter	Rating		Units
		CH-1	CH-2	
Rthj-c	Maximum Thermal Resistance, Junction-case	5	3	℃/W
Rthj-t	Maximum Thermal Resistance, Junction-top	15	9	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	70	60	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[4]	130	120	℃/W

CH-1 Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	-	-	V
V_{DSt}	Drain-Source Breakdown Voltage[7] (transient)	V_{GS}=0V, I_{AS}=60A, $t_{transient} \leq$ 50ns	36	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=14A	-	-	5.5	mΩ
		V_{GS}=4.5V, I_D=7A	-	-	8.8	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1.3	-	2.2	V
g_{fs}	Forward Transconductance	V_{DS}=5V, I_D=14A	-	52	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V, V_{GS}=0V	-	-	10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}= ±20V, V_{DS}=0V	-	-	±0.1	uA
$Q_{g(10V)}$	Total Gate Charge[5]	I_D=16A	-	19	30.4	nC
$Q_{g(4.5V)}$	Total Gate Charge[5]	V_{DS}=15V	-	9	14.4	nC
Q_{gs}	Gate-Source Charge[5]		-	4	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge[5]		-	3	-	nC
$t_{d(on)}$	Turn-on Delay Time[5]	V_{DS}=15V	-	8	-	ns
t_r	Rise Time[5]	I_D=16A	-	54	-	ns
$t_{d(off)}$	Turn-off Delay Time[5]	R_G=3Ω	-	18	-	ns
t_f	Fall Time[5]	V_{GS}=10V	-	3	-	ns
C_{iss}	Input Capacitance[5]	V_{GS}=0V	-	1070	1712	pF
C_{oss}	Output Capacitance[5]	V_{DS}=15V	-	550	-	pF
C_{rss}	Reverse Transfer Capacitance[5]	f=1.0MHz	-	30	-	pF
R_g	Gate Resistance	f=1.0MHz	-	2.2	4.4	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=16A, V_{GS}=0V	-	-	1.2	V
t_{rr}	Reverse Recovery Time[5]	I_S=16A, V_{GS}=0V	-	23	-	ns
Q_{rr}	Reverse Recovery Charge[5]	dI/dt=100A/μs	-	13	-	nC

CH-2 Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	-	-	V
V_{DSt}	Drain-Source Breakdown Voltage[7] (transient)	V_{GS}=0V, I_{AS}=80A, $t_{transient} \leq$ 50ns	36	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=20A	-	-	2.5	mΩ
		V_{GS}=4.5V, I_D=12A	-	-	3.9	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1.3	-	2.2	V
g_{fs}	Forward Transconductance	V_{DS}=5V, I_D=20A	-	92	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V, V_{GS}=0V	-	-	10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}= ±20V, V_{DS}=0V	-	-	±0.1	uA
$Q_{g(10V)}$	Total Gate Charge[5]	I_D=20A	-	40	64	nC
$Q_{g(4.5V)}$	Total Gate Charge[5]	V_{DS}=15V	-	19	30.4	nC
Q_{gs}	Gate-Source Charge[5]		-	9	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge[5]		-	5	-	nC
$t_{d(on)}$	Turn-on Delay Time[5]	V_{DS}=15V	-	10	-	ns
t_r	Rise Time[5]	I_D=20A	-	47	-	ns
$t_{d(off)}$	Turn-off Delay Time[5]	R_G=3Ω	-	28	-	ns
t_f	Fall Time[5]	V_{GS}=10V	-	6	-	ns
C_{iss}	Input Capacitance[5]	V_{GS}=0V	-	2450	3920	pF
C_{oss}	Output Capacitance[5]	V_{DS}=15V	-	1450	-	pF
C_{rss}	Reverse Transfer Capacitance[5]	f=1.0MHz	-	50	-	pF
R_g	Gate Resistance	f=1.0MHz	-	1.2	2.4	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=20A, V_{GS}=0V	-	-	1.2	V
t_{rr}	Reverse Recovery Time[5]	I_S=20A, V_{GS}=0V	-	40	-	ns
Q_{rr}	Reverse Recovery Charge[5]	dI/dt=100A/μs	-	38	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board, on steady-state

4.Surface mounted on Min. copper pad of FR4 board, on steady-state

5.Guaranteed by design.

6.Starting T_j=25°C , V_{DD}=30V , L=0.01mH , R_G=25Ω , V_{GS}=10V

7.T_j=25°C. Expected voltage stress during 100% EAS test. Production datalog is not available.

Channel-1

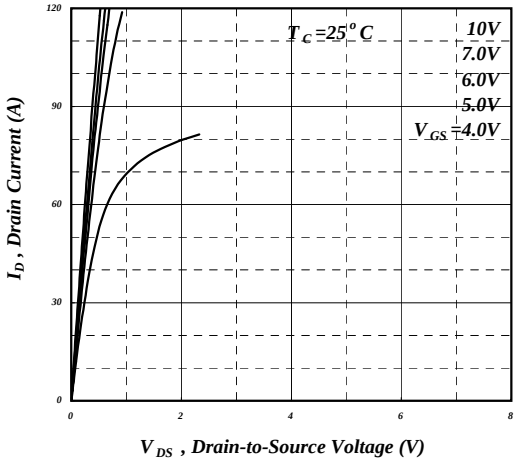


Fig 1. Typical Output Characteristics

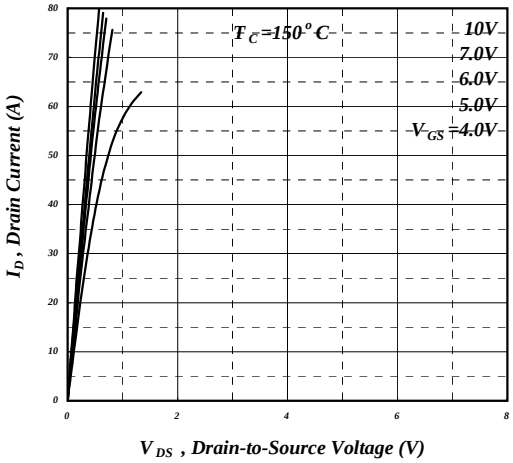


Fig 2. Typical Output Characteristics

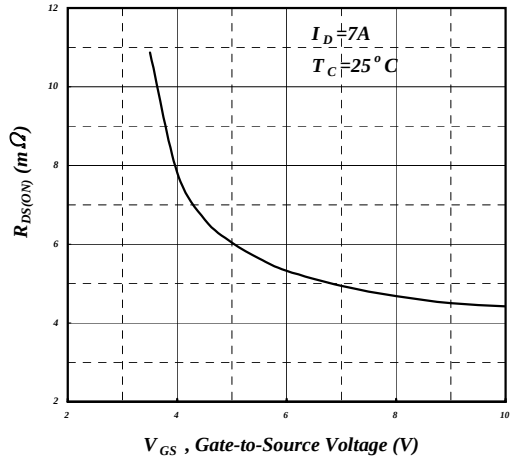


Fig 3. On-Resistance v.s. Gate Voltage

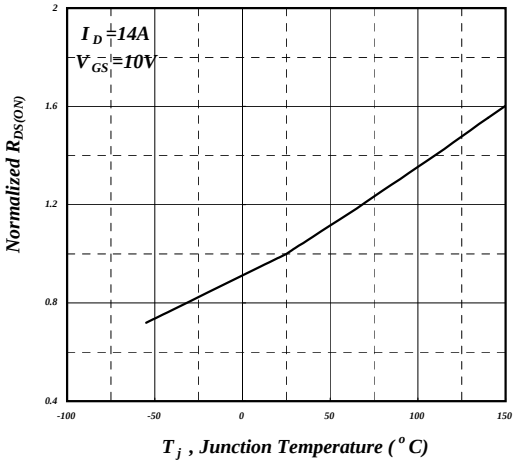


Fig 4. Normalized On-Resistance v.s. Junction Temperature

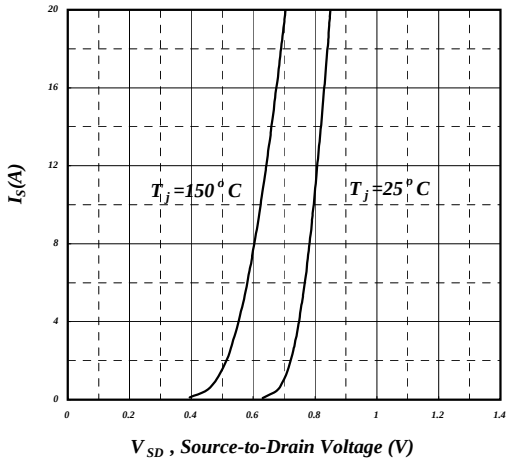


Fig 5. Forward Characteristic of Reverse Diode

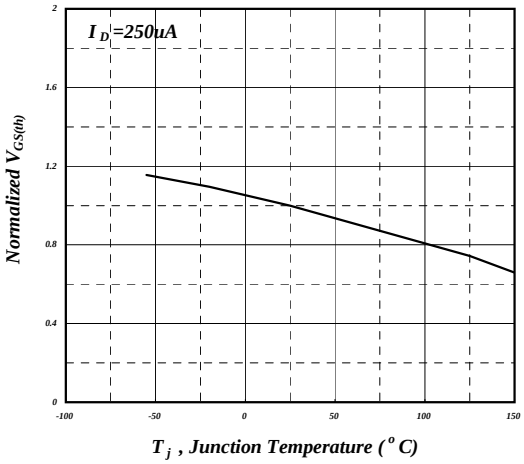


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

Channel-1

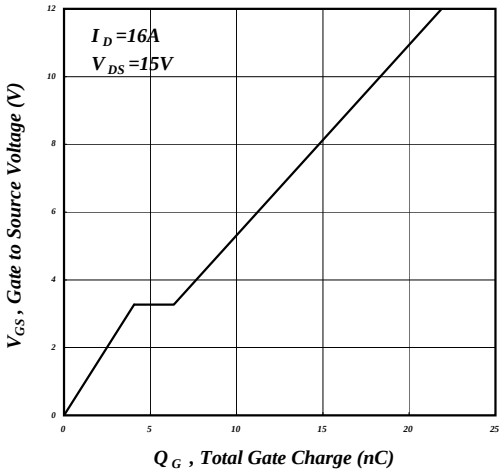


Fig 7. Gate Charge Characteristics

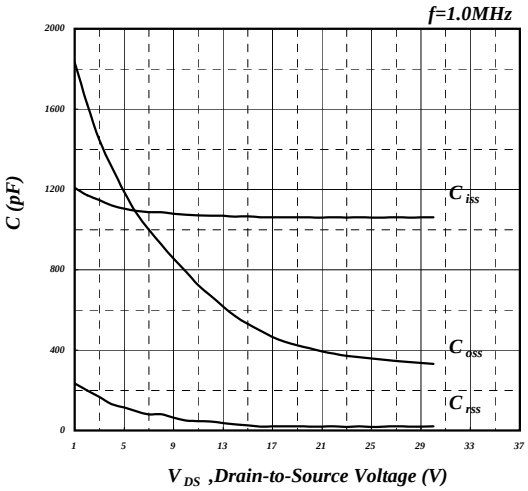


Fig 8. Typical Capacitance Characteristics

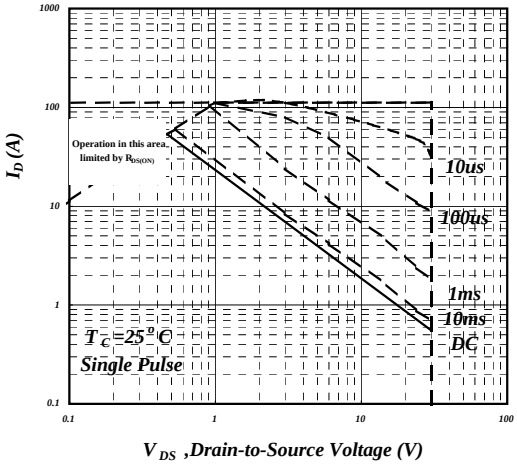


Fig 9. Maximum Safe Operating Area

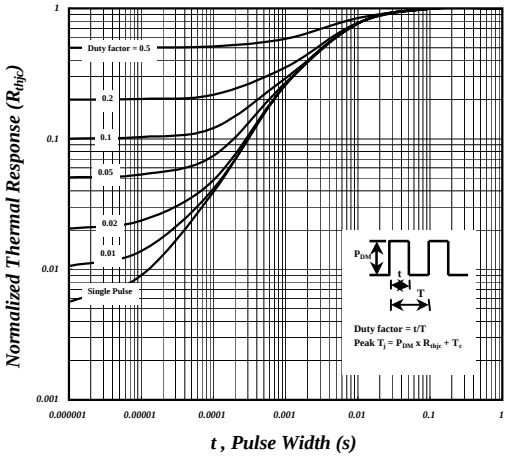


Fig 10. Effective Transient Thermal Impedance

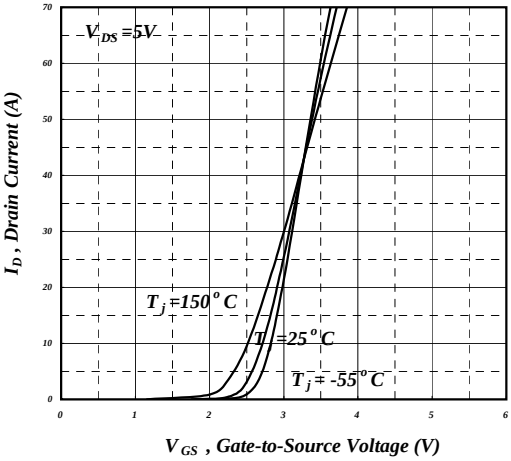


Fig 11. Transfer Characteristics

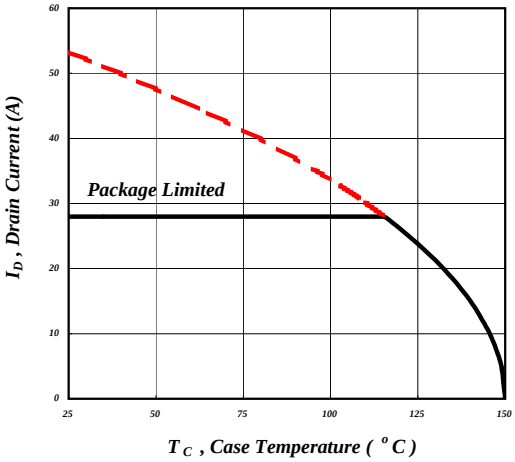


Fig 12. Drain Current v.s. Case Temperature

Channel-1

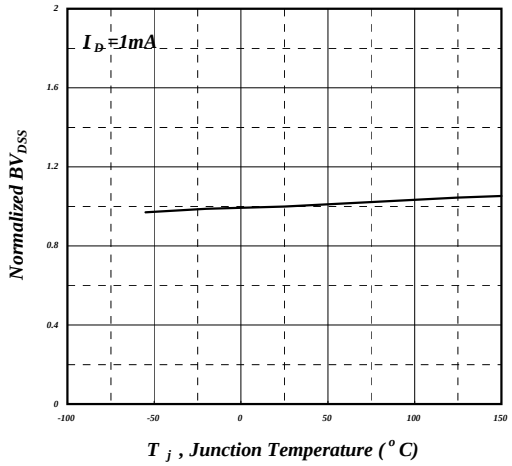


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

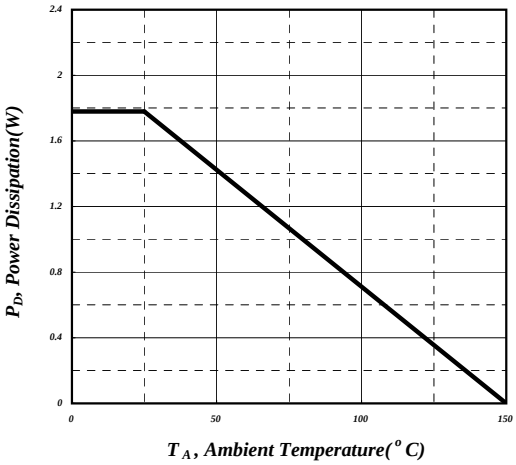


Fig 14. Total Power Dissipation

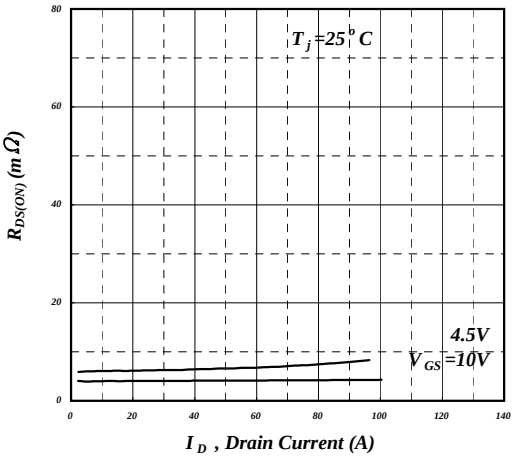


Fig 15. Typ. Drain-Source on State Resistance

Channel-2

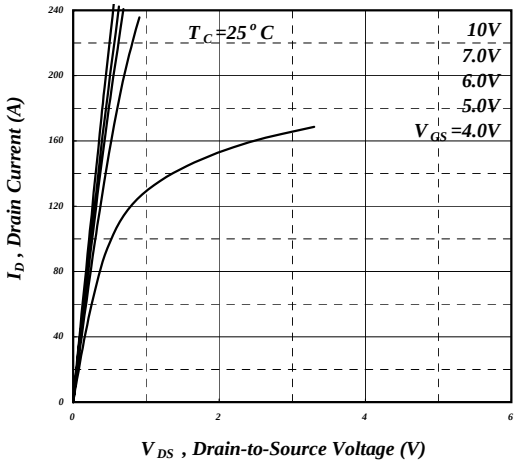


Fig 1. Typical Output Characteristics

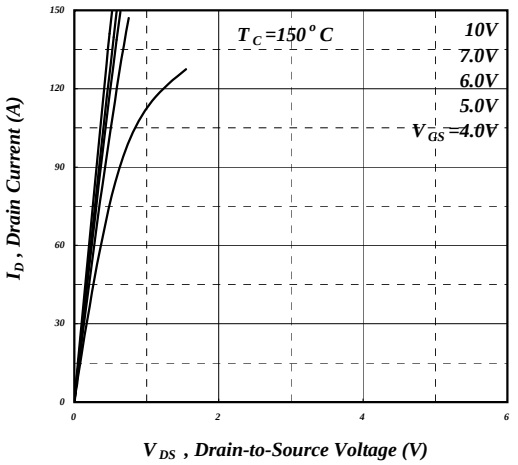


Fig 2. Typical Output Characteristics

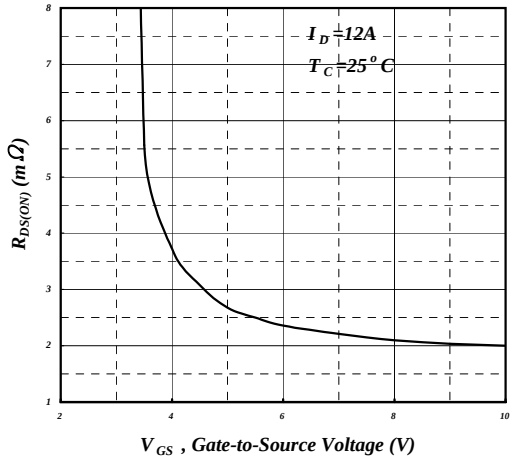


Fig 3. On-Resistance v.s. Gate Voltage

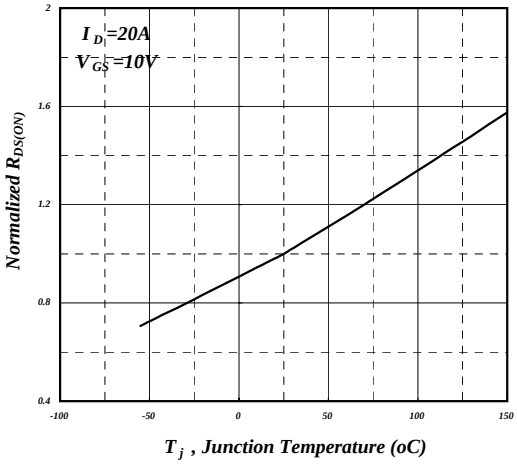


Fig 4. Normalized On-Resistance v.s. Junction Temperature

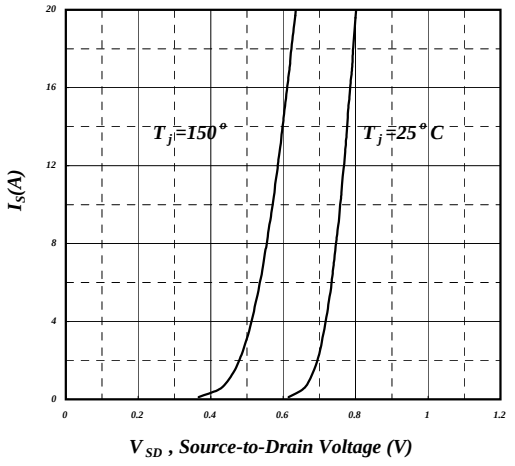


Fig 5. Forward Characteristic of Reverse Diode

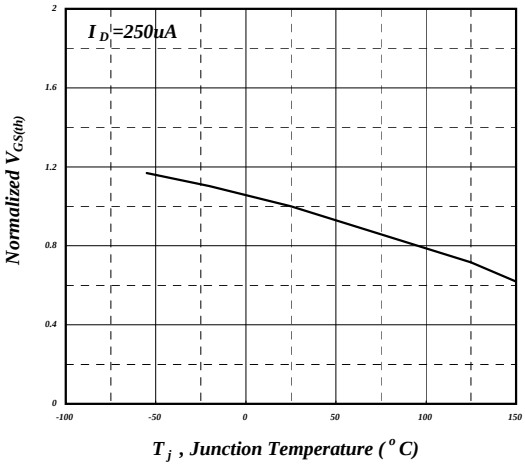


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

Channel-2

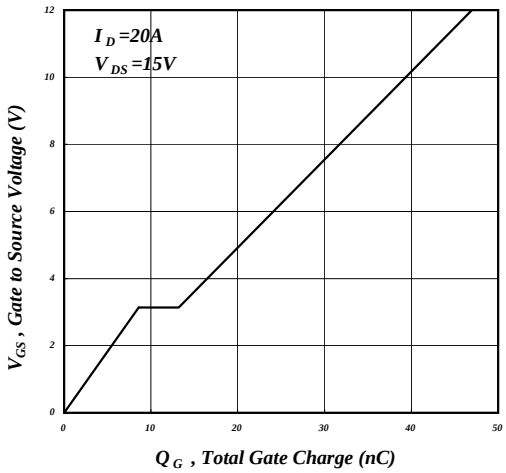


Fig 7. Gate Charge Characteristics

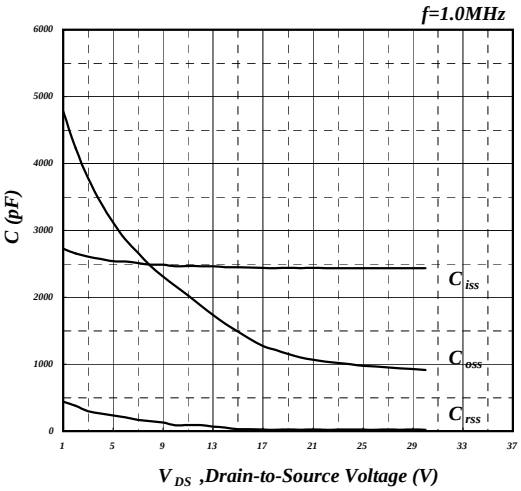


Fig 8. Typical Capacitance Characteristics

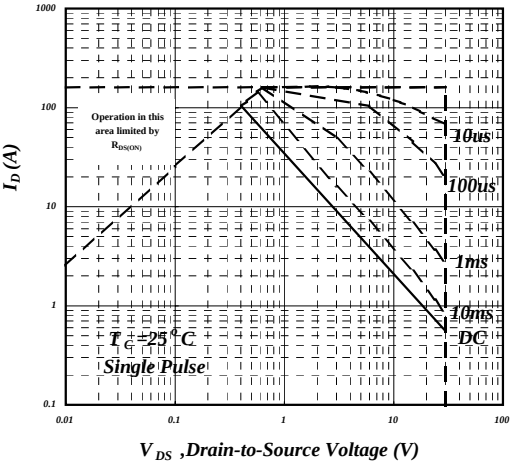


Fig 9. Maximum Safe Operating Area

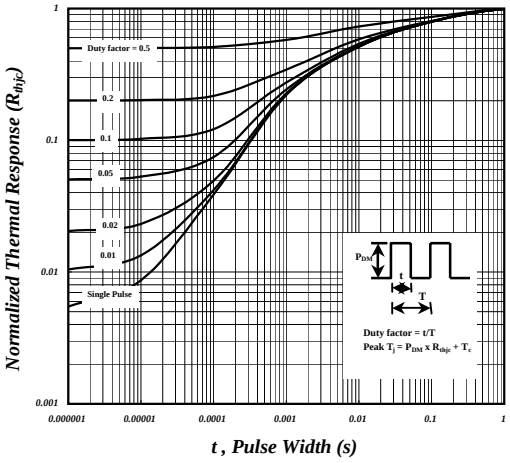


Fig 10. Effective Transient Thermal Impedance

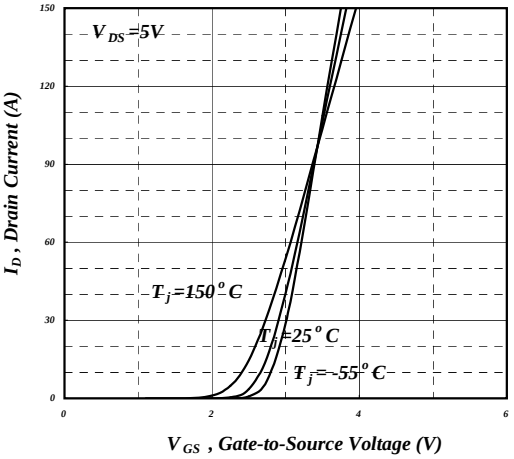


Fig 11. Transfer Characteristics

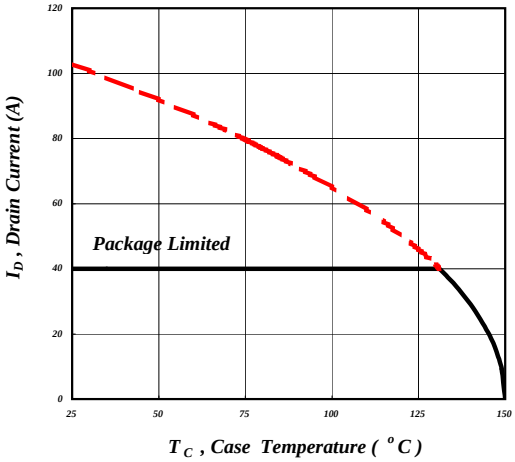


Fig 12. Drain Current v.s. Case Temperature

Channel-2

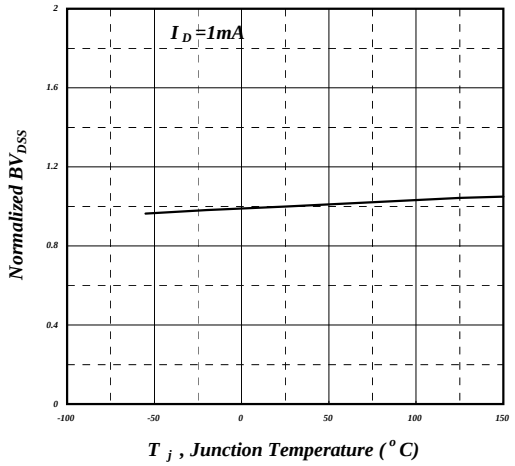


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

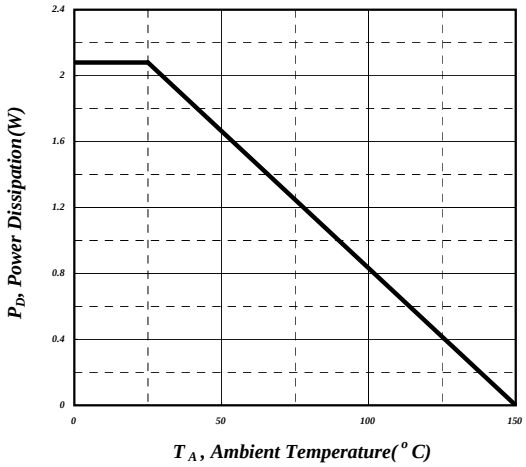


Fig 14. Total Power Dissipation

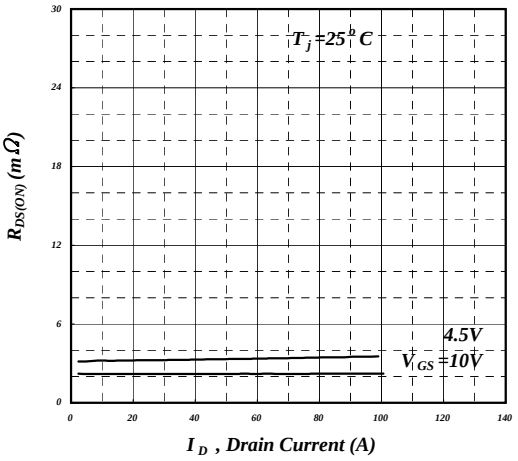
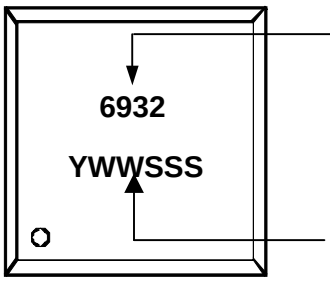


Fig 15. Typ. Drain-Source on State Resistance

MARKING INFORMATION



Part Number

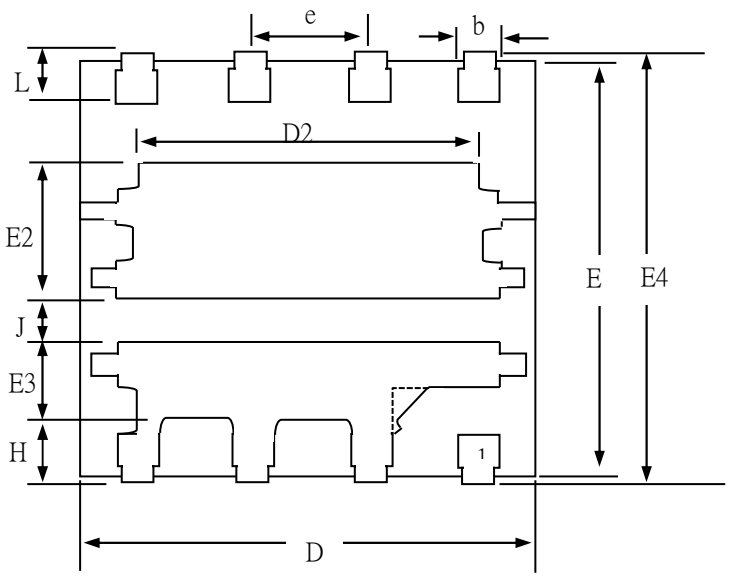
Date Code (YWWSSS)

Y：Last Digit Of The Year

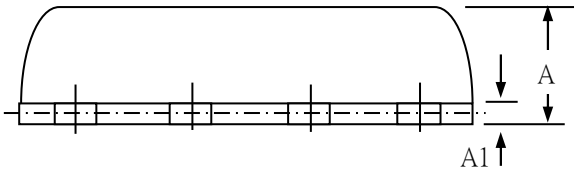
WW：Week

SSS：Sequence

Package Outline : PMPAK 5x6 (DUD)



BACKSIDE VIEW



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.42	0.51
A1	0.20	0.25	0.30
D	4.80	4.90	5.00
D2	3.61	3.79	3.96
E4	5.90	6.03	6.15
E	5.70	5.75	5.80
E2	2.02	2.22	2.42
E3	0.94	1.18	1.42
e	1.27BSC		
J	0.40	0.50	0.60
H	0.48	0.58	0.68
L	0.38	0.55	0.71

1.All dimension are in millimeters.

2.Dimension does not include burrs and mold flash/protrusions.

3.The outline schematic is not to scale and slightly different from the actual product appearance.

Draw No. M2-MT(DUD)-8-EI-G-v02

PMPAK 5x6 (DUD) FOOTPRINT：