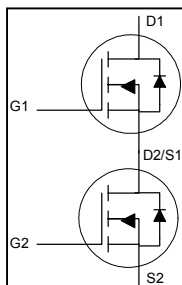


- ▼ Simple Drive Requirement
- ▼ Easy for Synchronous Buck Converter Application
- ▼ RoHS Compliant & Halogen-Free

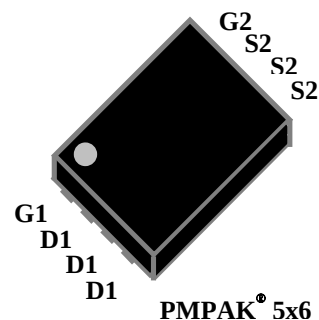
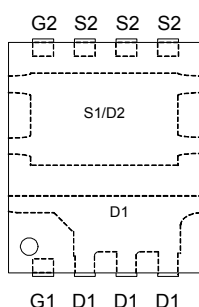
Description

XP6926 series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The control MOSFET (CH-1) and synchronous MOSFET (CH-2) co-package for synchronous buck converters.



CH-1	BV_{DSS}	40V
	$R_{DS(ON)}$	40m Ω
	I_D	15A
CH-2	BV_{DSS}	40V
	$R_{DS(ON)}$	20m Ω
	I_D	24A



Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating		Units
		CH-1	CH-2	
V_{DS}	Drain-Source Voltage	40	40	V
V_{GS}	Gate-Source Voltage	+20	+20	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current (Chip Limited)	15	24	A
$I_D@T_A=25^\circ\text{C}$	Continuous Drain Current ³	6.7	10.5	A
$I_D@T_A=70^\circ\text{C}$	Continuous Drain Current ³	5.4	8.4	A
I_{DM}	Pulsed Drain Current ¹	30	40	A
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation	3.13	3.9	W
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Rating		Units
		CH-1	CH-2	
Rthj-c	Maximum Thermal Resistance, Junction-case	8	6	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³	40	32	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient ⁴	70	60	$^\circ\text{C}/\text{W}$

CH-1 Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	40	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =6A	-	-	40	mΩ
		V _{GS} =4.5V, I _D =4A	-	-	60	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =6A	-	15	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =32V, V _{GS} =0V	-	-	10	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =4A	-	7.2	11.5	nC
Q _{gs}	Gate-Source Charge	V _{DS} =32V	-	1.6	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	3.7	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =20V	-	6	-	ns
t _r	Rise Time	I _D =6A	-	25	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω	-	16	-	ns
t _f	Fall Time	V _{GS} =10V	-	3	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	520	830	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	65	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	50	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1.8	3.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =6A, V _{GS} =0V	-	-	1.2	V
t _{rr}	Reverse Recovery Time	I _S =6A, V _{GS} =0V	-	23	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	3.3	-	nC

CH-2 Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	40	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =10A	-	-	20	mΩ
		V _{GS} =4.5V, I _D =6A	-	-	30	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =10A	-	34	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =32V, V _{GS} =0V	-	-	10	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =6A	-	15	24	nC
Q _{gs}	Gate-Source Charge	V _{DS} =32V	-	4	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	6	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =20V	-	10	-	ns
t _r	Rise Time	I _D =10A	-	35	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =1Ω	-	21	-	ns
t _f	Fall Time	V _{GS} =10V	-	4	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	1550	2480	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	130	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	100	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1.3	2.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =10A, V _{GS} =0V	-	-	1.2	V
t _{rr}	Reverse Recovery Time	I _S =10A, V _{GS} =0V,	-	13	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	3	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board, t ≤10sec.
- 4.Surface mounted on 1 in² copper pad of FR4 board, on steady-state

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

XSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

Channel-1

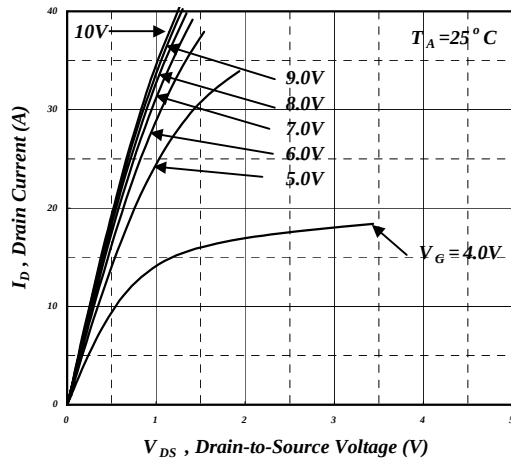


Fig 1. Typical Output Characteristics

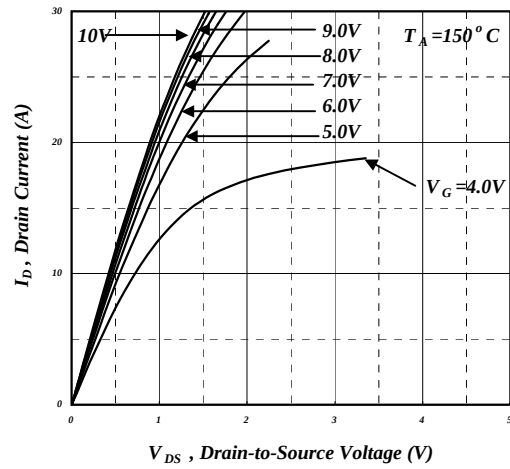


Fig 2. Typical Output Characteristics

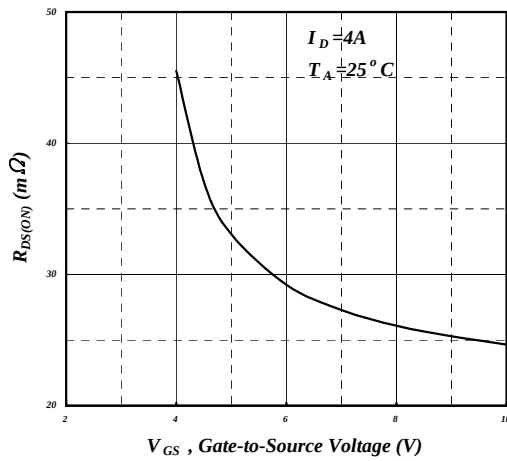
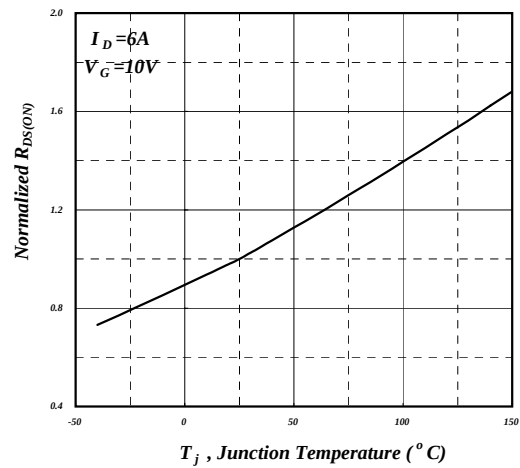
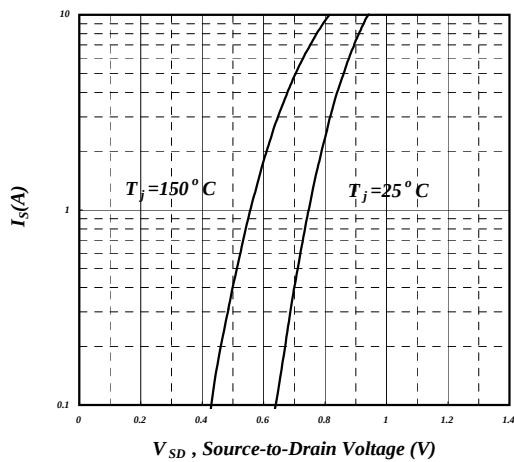


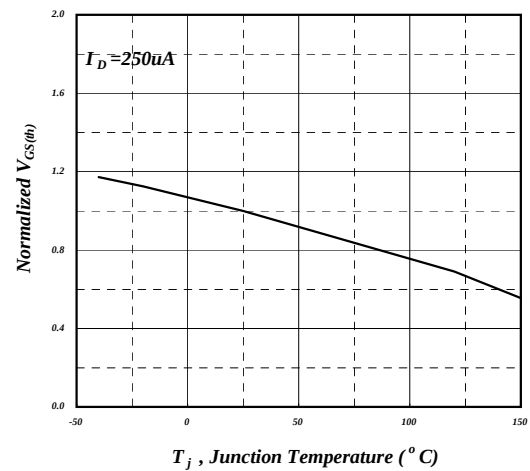
Fig 3. On-Resistance v.s. Gate Voltage



**Fig 4. Normalized On-Resistance
v.s. Junction Temperature**



**Fig 5. Forward Characteristic of
Reverse Diode**



**Fig 6. Gate Threshold Voltage v.s.
Junction Temperature**

Channel-1

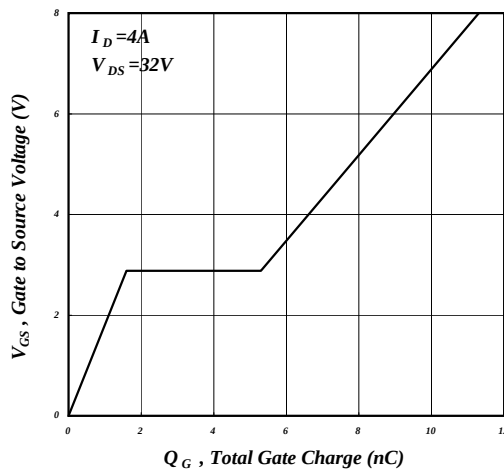


Fig 7. Gate Charge Characteristics

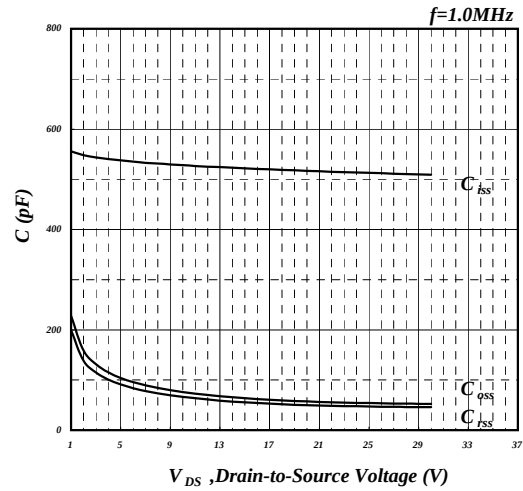


Fig 8. Typical Capacitance Characteristics

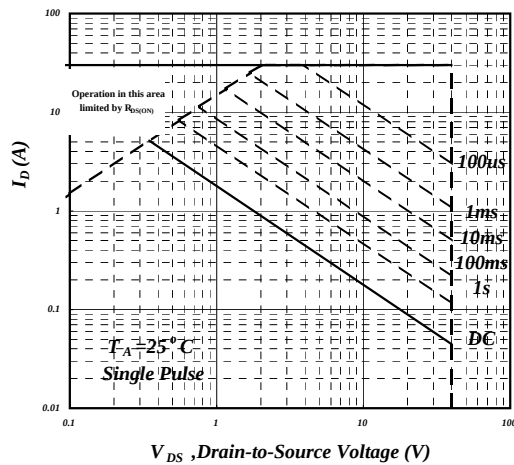


Fig 9. Maximum Safe Operating Area

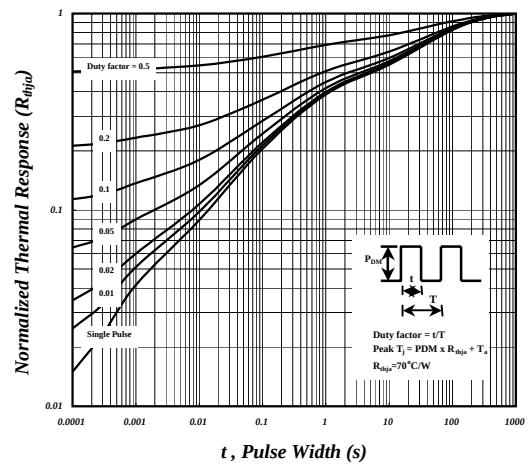


Fig 10. Effective Transient Thermal Impedance

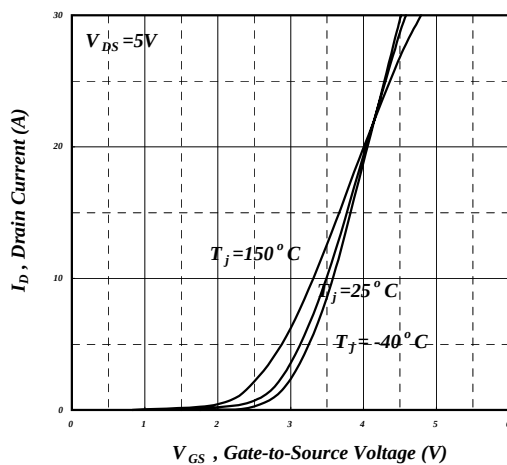


Fig 11. Transfer Characteristics

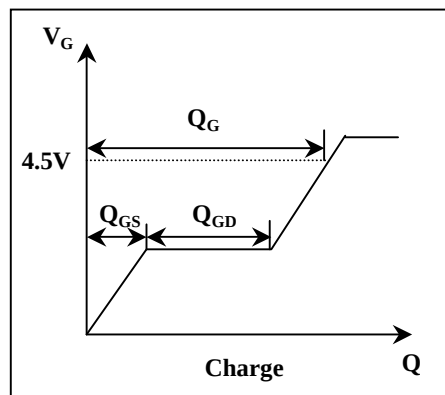


Fig 12. Gate Charge Waveform

Channel-2

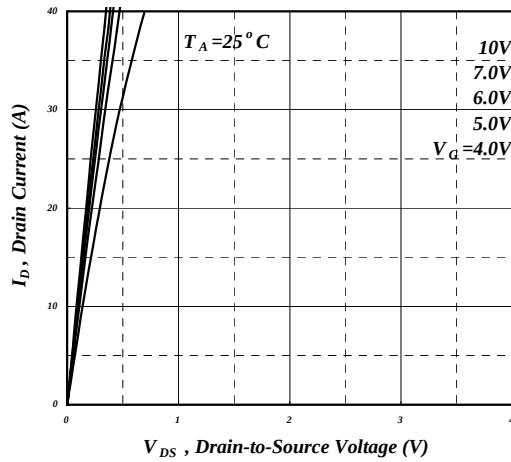


Fig 1. Typical Output Characteristics

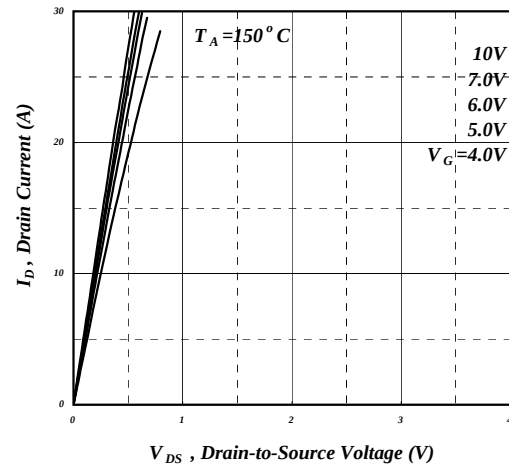


Fig 2. Typical Output Characteristics

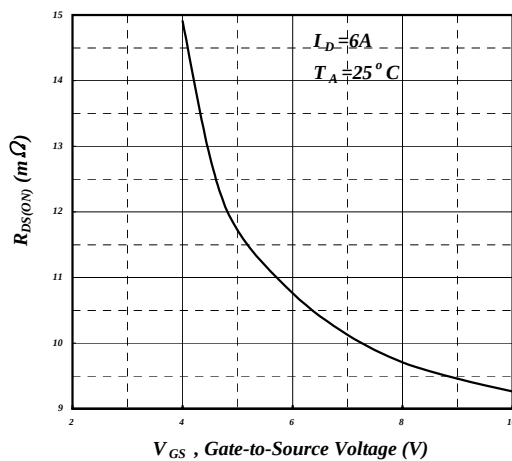
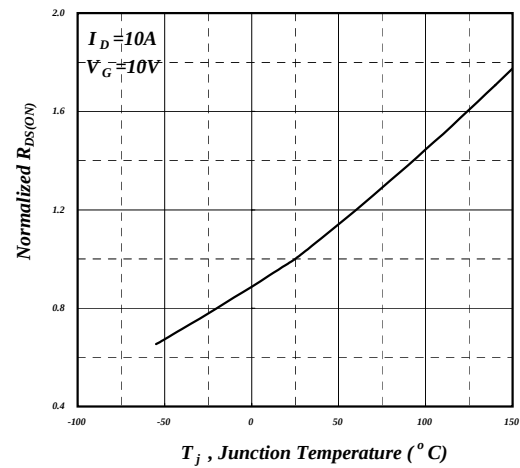
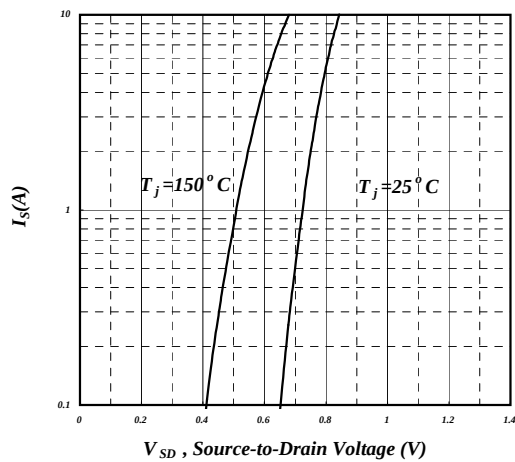


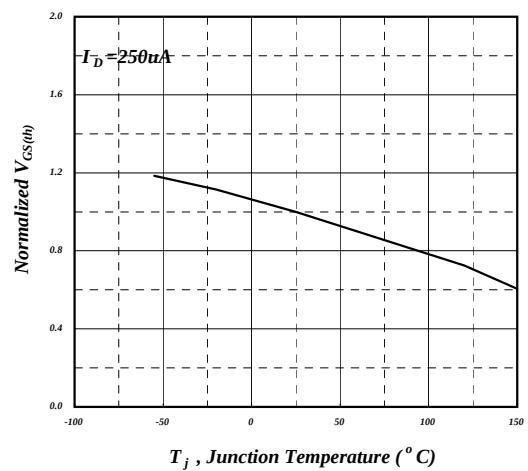
Fig 3. On-Resistance v.s. Gate Voltage



**Fig 4. Normalized On-Resistance
v.s. Junction Temperature**



**Fig 5. Forward Characteristic of
Reverse Diode**



**Fig 6. Gate Threshold Voltage v.s.
Junction Temperature**

Channel-2

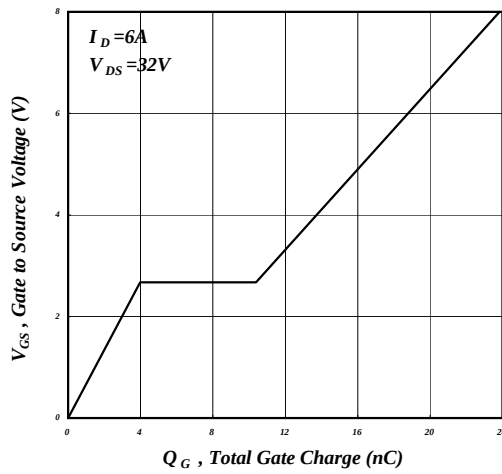


Fig 7. Gate Charge Characteristics

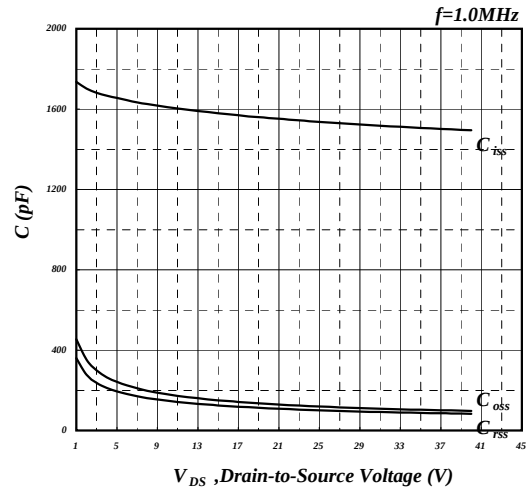


Fig 8. Typical Capacitance Characteristics

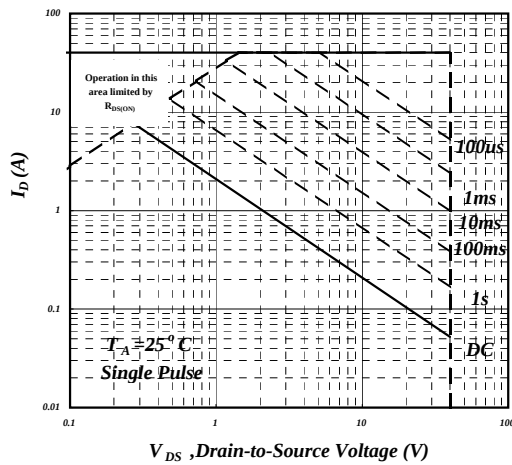


Fig 9. Maximum Safe Operating Area

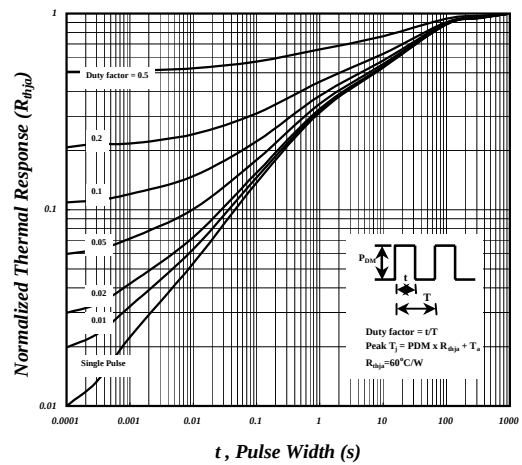


Fig 10. Effective Transient Thermal Impedance

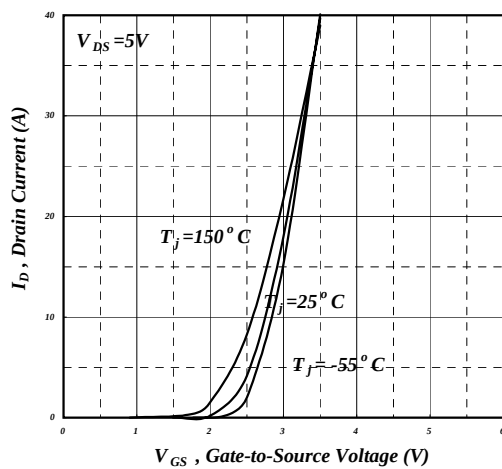


Fig 11. Transfer Characteristics

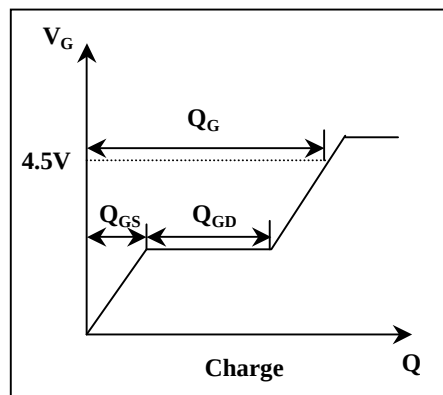
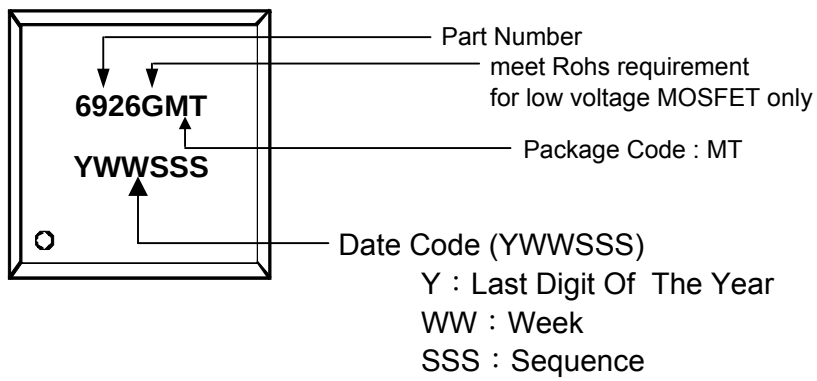
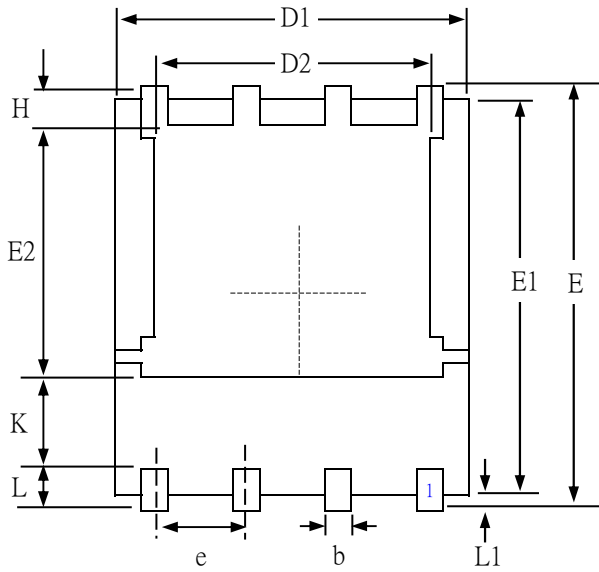


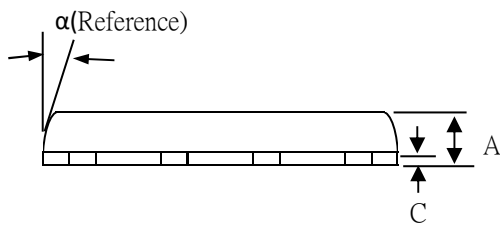
Fig 12. Gate Charge Waveform

MARKING INFORMATION

Package Outline : PMPAK 5x6



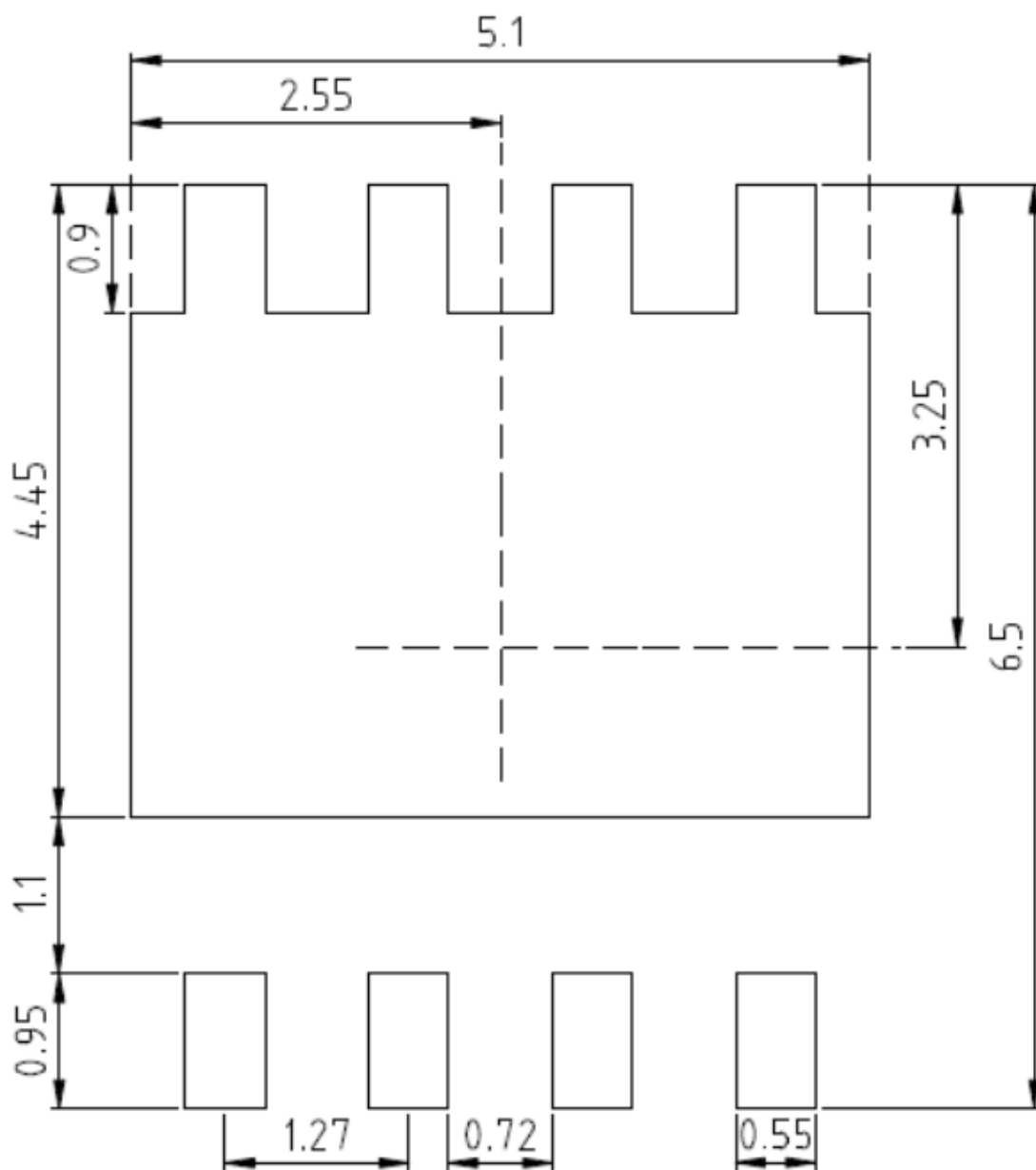
BACKSIDE VIEW



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.90	1.10	1.30
b	0.33	0.41	0.51
C	0.254(Ref.)		
D1	4.80	4.90	5.10
D2	3.61	4.00	4.40
E	5.80	6.03	6.25
E1 (Ref.)	5.60	5.75	5.90
E2 (Ref.)	3.30	3.55	3.80
e	1.27 BSC		
H	0.35	—	0.90
K (Ref.)	1.00	1.275	—
L	0.35	0.55	0.75
L1	0.06	0.13	0.20
$\alpha(\text{Ref.})$	0°	—	12°

- 1.All dimension are in millimeters.
- 2.Dimension does not include burrs and mold flash/protrusions.
- 3.The outline schematic is not to scale and slightly different from the actual product appearance.

PMPAK 5X6(E-TYPE) FOOTPRINT :



UNIT: mm