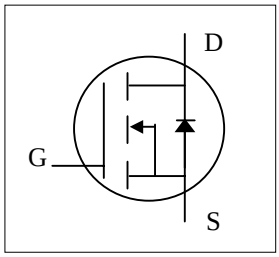
XP65SA430ADR

Halogen-Free Product

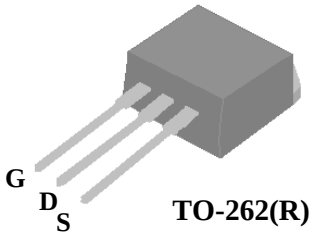
N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- **100% R_g & UIS Test**
- **Low t_{rr} / Q_{rr}**
- **Simple Drive Requirement**
- **RoHS Compliant & Halogen-Free**



BV_{DSS}	650V
$R_{DS(ON)}$	0.438Ω
I_D [3,4]	10A



TO-262(R)

Description

XP65SA430AD series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-262 package is widely preferred for commercial-industrial through-hole applications and suited for low voltage applications such as DC/DC converters.

Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	650	V
V_{GS}	Gate-Source Voltage	±20	V
V_{GS}	Gate-Source Voltage, AC (f > 1Hz)	±30	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V[3,4]	10	A
I_D@T_C=100℃	Drain Current, V_{GS} @ 10V[3,4]	6.5	A
I_{DM}	Pulsed Drain Current[1]	20	A
dv/dt	MOSFET dv/dt Ruggedness (V_{DS} = 0 …480V)	40	V/ns
P_D@T_C=25℃	Total Power Dissipation	78.1	W
P_D@T_A=25℃	Total Power Dissipation	2	W
E_{AS}	Single Pulse Avalanche Energy[5]	50	mJ
dv/dt	Peak Diode Recovery dv/dt[6]	50	V/ns
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	1.6	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient	62	℃/W

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	650	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=3.2A	-	-	0.438	Ω
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	3	-	5	V
g_{fs}	Forward Transconductance	V_{DS}=15V, I_D=5A	-	5.5	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=520V, V_{GS}=0V	-	-	100	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±1	uA
Q_g	Total Gate Charge[7]	I_D=3.2A	-	22	36	nC
Q_{gs}	Gate-Source Charge[7]	V_{DS}=520V	-	6	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge[7]	V_{GS}=10V	-	10.5	-	nC
$t_{d(on)}$	Turn-on Delay Time[7]	V_{DD}=325V	-	13	-	ns
t_r	Rise Time[7]	I_D=3.2A	-	10	-	ns
$t_{d(off)}$	Turn-off Delay Time[7]	R_G=3.3Ω	-	28	-	ns
t_f	Fall Time[7]	V_{GS}=10V	-	11	-	ns
C_{iss}	Input Capacitance[7]	V_{GS}=0V	-	790	1264	pF
C_{oss}	Output Capacitance[7]	V_{DS}=100V	-	34	-	pF
C_{rss}	Reverse Transfer Capacitance[7]	f=1.0MHz	-	10	-	pF
R_g	Gate Resistance	f=1.0MHz	-	3.3	6.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=3.2A, V_{GS}=0V	-	-	1.5	V
t_{rr}	Reverse Recovery Time[7]	I_S=3.2A, V_{GS}=0V	-	105	-	ns
Q_{rr}	Reverse Recovery Charge[7]	dI/dt=100A/μs	-	490	-	nC

Notes:

1.Pulse width limited by max. junction temperature.

2.Pulse test

3.Limited by max. junction temperature. Maximum duty cycle D=0.75

4.Ensure that the junction temperature does not exceed $T_{Jmax.}$.

5.Starting T_j=25°C , V_{DD}=90V , L=100mH , R_G=25Ω , V_{GS}=10V , I_{AS}=1A

6.$I_{SD} \leqq I_D$, $V_{DD} \leqq BV_{DSS}$, starting T_J = 25°C

7.Guaranteed by design.

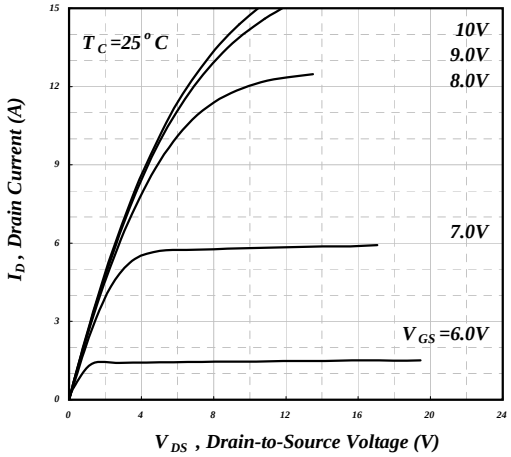


Fig 1. Typical Output Characteristics

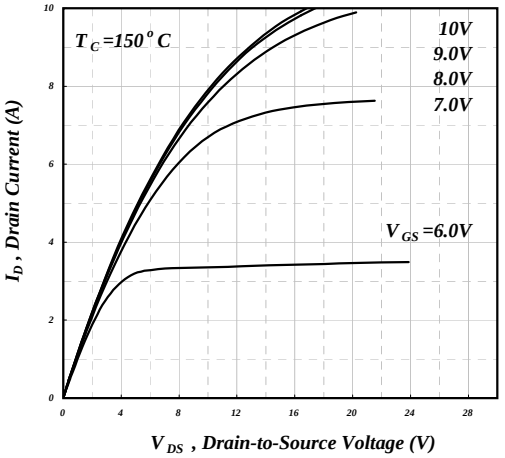


Fig 2. Typical Output Characteristics

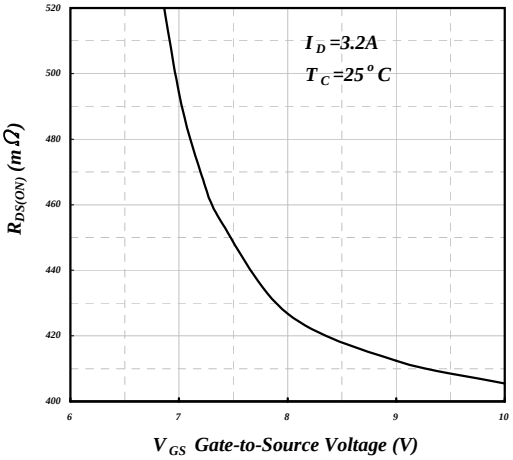


Fig 3. On-Resistance v.s. Gate Voltage

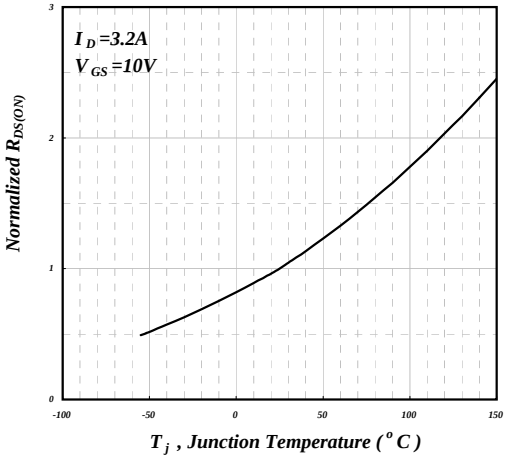


Fig 4. Normalized On-Resistance v.s. Junction Temperature

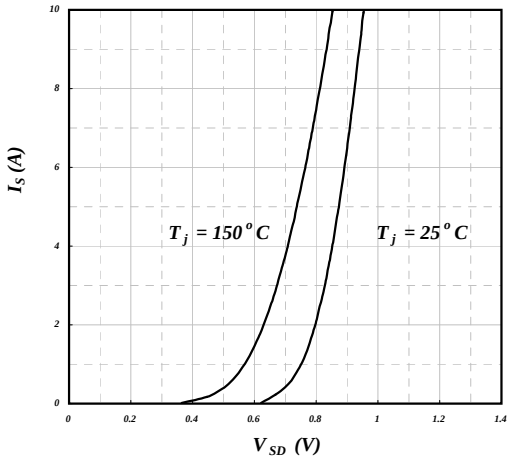


Fig 5. Forward Characteristic of Reverse Diode

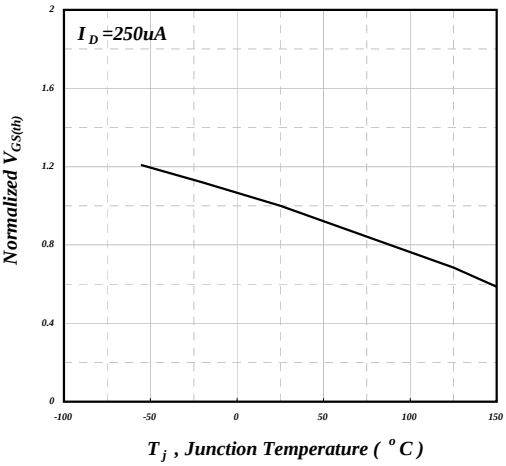


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

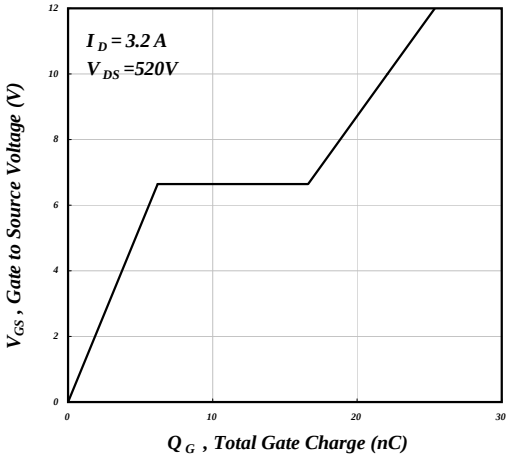


Fig 7. Gate Charge Characteristics

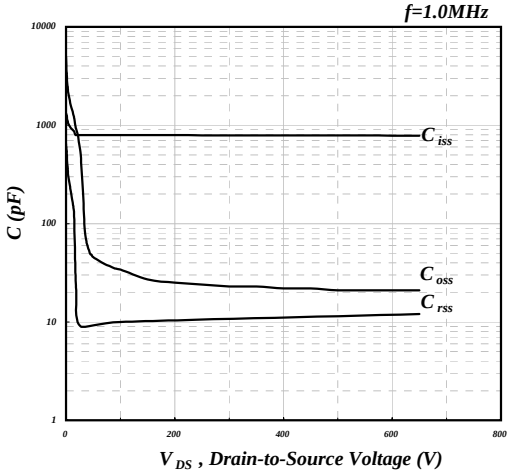


Fig 8. Typical Capacitance Characteristics

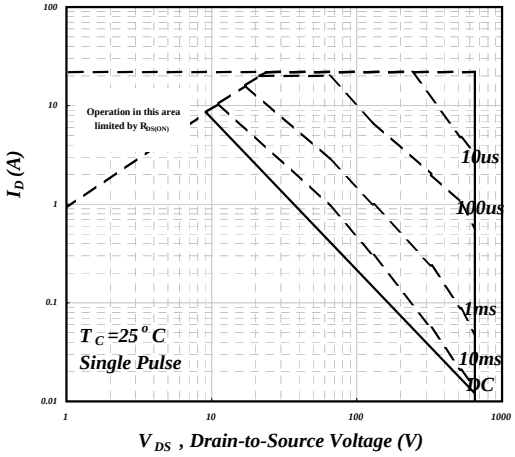


Fig 9. Maximum Safe Operating Area

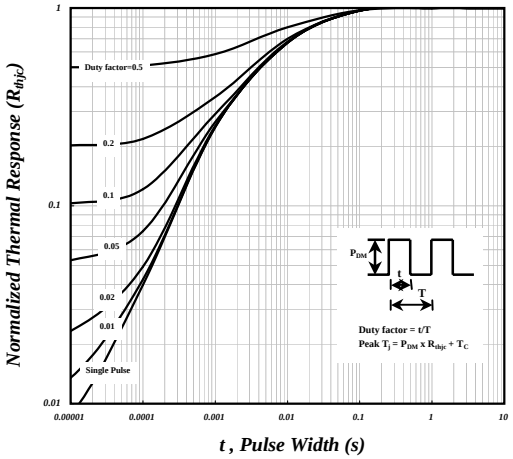


Fig10. Effective Transient Thermal Impedance

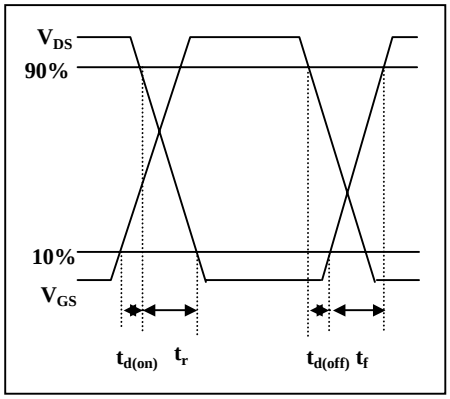


Fig 11. Switching Time Waveform

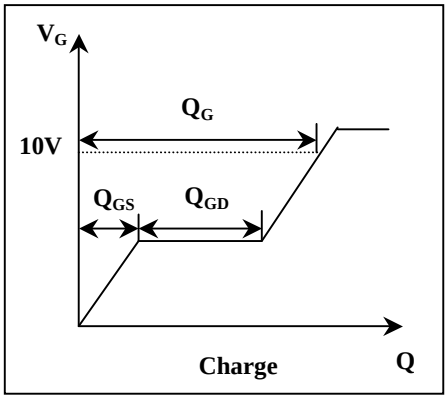


Fig 12. Gate Charge Waveform

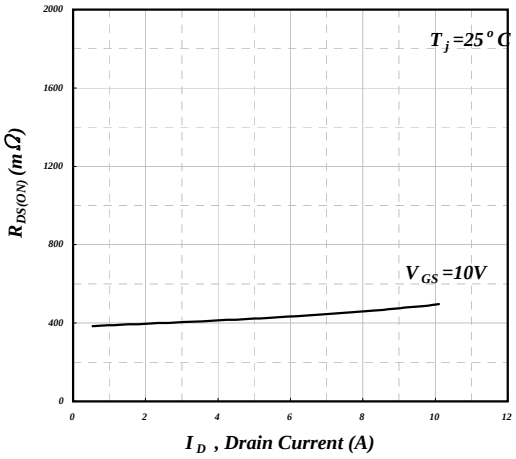


Fig 13. Typ. Drain-Source on State Resistance

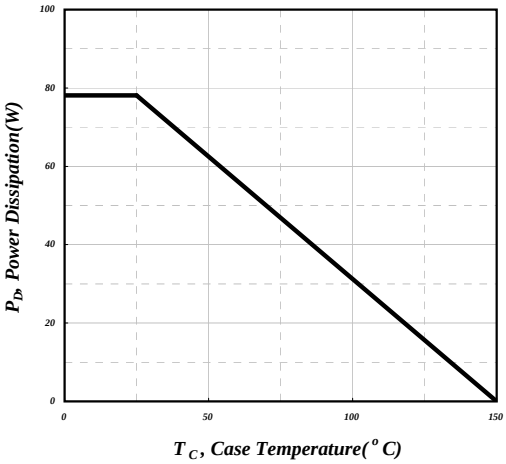


Fig 14. Total Power Dissipation

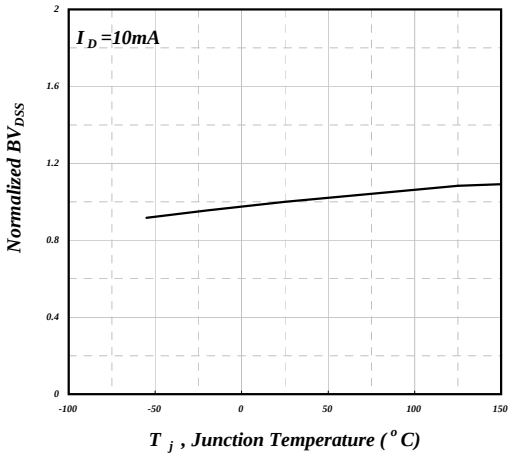
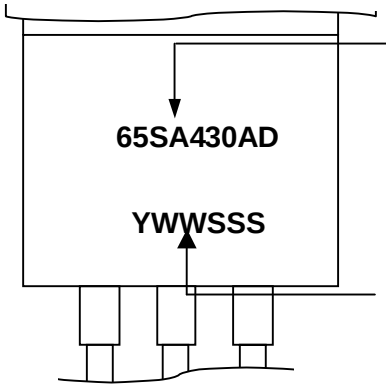
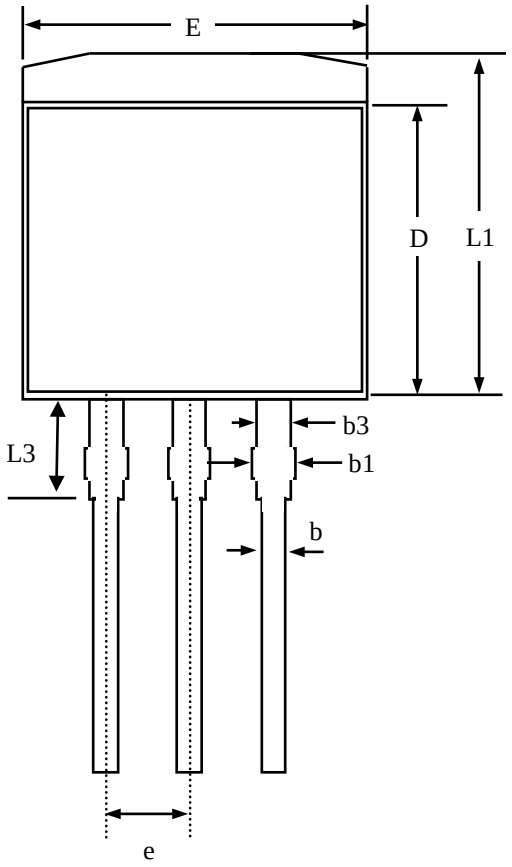


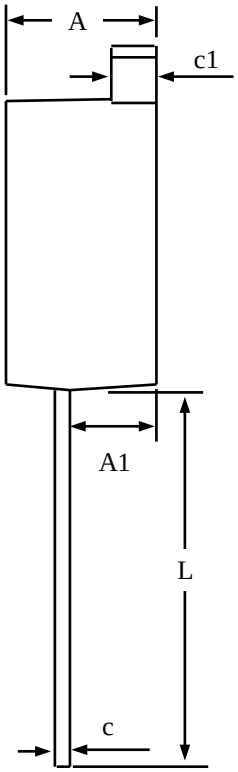
Fig 15. Normalized BV_{DSS} v.s. Junction Temperature

MARKING INFORMATION



Package Outline : TO-262





SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	4.24	4.54	4.84
A1	2.10	2.50	2.90
b	0.65	0.85	1.05
b1	0.75	1.25	1.75
b3	0.75	1.23	1.70
c	0.28	0.44	0.60
c1	1.15	1.3	1.45
D	8.30	8.9	9.50
E	9.50	10	10.50
e	2.04	2.54	3.04
L	10.50	12.5	14.50
L1	8.50	10	11.50
L3	1.3 ～ 4.8 (ref)		

1.All Dimensions Are in Millimeters.

2.Dimension Does Not Include Mold Protrusions.

Draw No. M1-R3-IFET-G-v07

TO-262 FOOTPRINT：