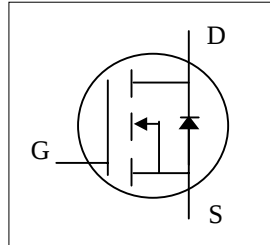


- ▼ 100% R_g & UIS Test
- ▼ Low t_{rr} / Q_{rr}
- ▼ Simple Drive Requirement
- ▼ RoHS Compliant & Halogen-Free

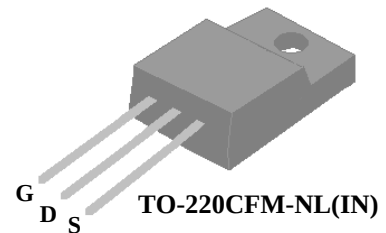


BV_{DSS}	600V
$R_{DS(ON)}$	$0.16\ \Omega$
$I_D^{3,4}$	20A

Description

XP60SL160D series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-220CFM package is widely preferred for all commercial-industrial through hole applications. The mold compound provides a high isolation voltage capability and low thermal resistance between the tab and the external heat-sink.



Absolute Maximum Ratings@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	600	V
V_{GS}	Gate-Source Voltage	± 20	V
V_{GS}	Gate-Source Voltage, AC ($f > 1\text{Hz}$)	± 30	V
$I_D@T_C=25^\circ\text{C}$	Drain Current, V_{GS} @ $10\text{V}^{3,4}$	20	A
$I_D@T_C=100^\circ\text{C}$	Drain Current, V_{GS} @ $10\text{V}^{3,4}$	12.3	A
I_{DM}	Pulsed Drain Current ¹	48	A
dv/dt	MOSFET dv/dt Ruggedness ($V_{DS} = 0 \dots 400\text{V}$)	20	V/ns
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation	34.7	W
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation	1.92	W
E_{AS}	Single Pulse Avalanche Energy ⁵	300	mJ
dv/dt	Peak Diode Recovery dv/dt ⁶	15	V/ns
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Units
R_{thj-c}	Maximum Thermal Resistance, Junction-case	3.6	$^\circ\text{C}/\text{W}$
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient	65	$^\circ\text{C}/\text{W}$

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	600	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =6.2A	-	-	0.16	Ω
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	2	-	5	V
g _{fs}	Forward Transconductance	V _{DS} =15V, I _D =6.2A	-	12	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =480V, V _{GS} =0V	-	-	100	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =6.2A	-	59	94.4	nC
Q _{gs}	Gate-Source Charge	V _{DS} =480V	-	12	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	27	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DD} =300V	-	16	-	ns
t _r	Rise Time	I _D =6.2A	-	15	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω	-	64	-	ns
t _f	Fall Time	V _{GS} =10V	-	12	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	2060	3296	pF
C _{oss}	Output Capacitance	V _{DS} =100V	-	66	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	5	-	pF
R _g	Gate Resistance	f=1.0MHz	-	4	8	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =6.2A, V _{GS} =0V	-	0.8	-	V
t _{rr}	Reverse Recovery Time	I _S =11A, V _{GS} =0V	-	150	-	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	-	1.17	-	uC

Notes:

- 1.Pulse width limited by max. junction temperature.
- 2.Pulse test
- 3.Limited by max. junction temperature. Maximum duty cycle D=0.75
- 4.Ensure that the junction temperature does not exceed T_{Jmax}.
- 5.Starting T_j=25°C , V_{DD}=90V , L=150mH , R_G=25Ω , V_{GS}=10V
- 6.I_{SD} ≤ I_D, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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XSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

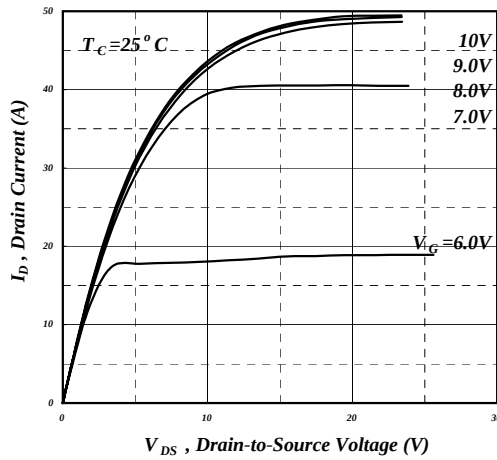


Fig 1. Typical Output Characteristics

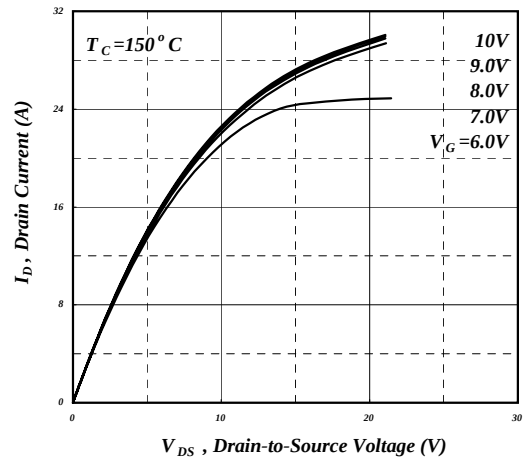


Fig 2. Typical Output Characteristics

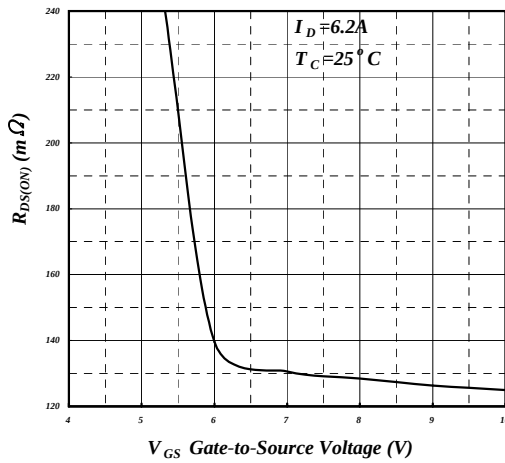
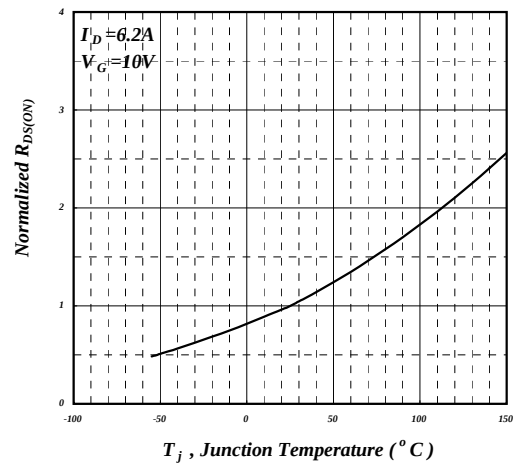
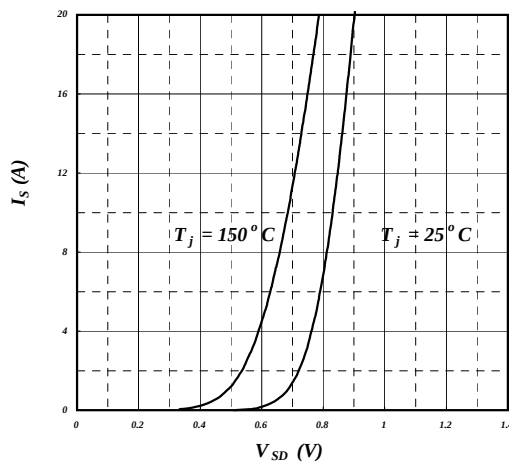


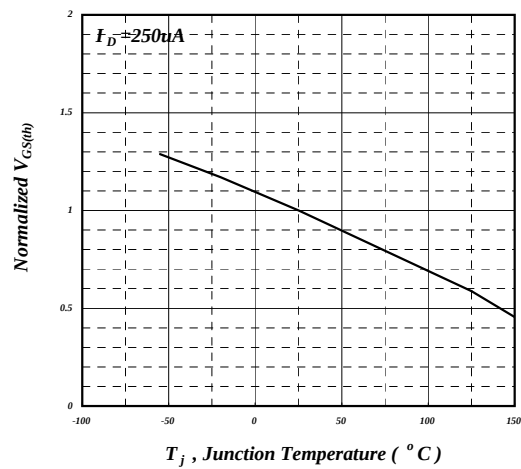
Fig 3. On-Resistance v.s. Gate Voltage



**Fig 4. Normalized On-Resistance
v.s. Junction Temperature**



**Fig 5. Forward Characteristic of
Reverse Diode**



**Fig 6. Gate Threshold Voltage v.s.
Junction Temperature**

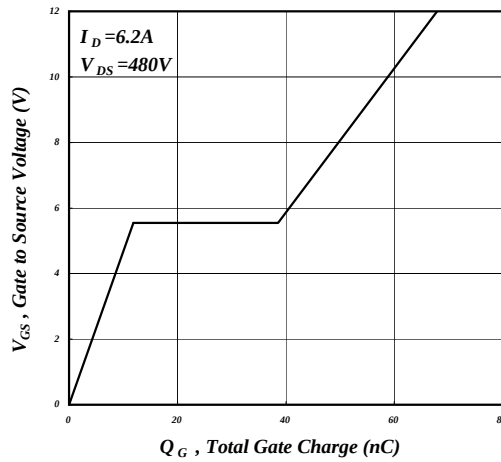


Fig 7. Gate Charge Characteristics

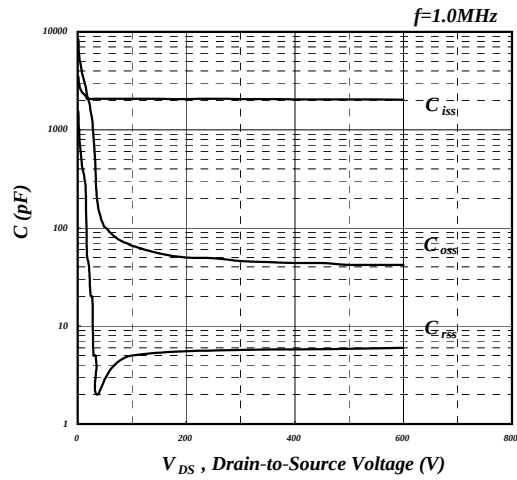


Fig 8. Typical Capacitance Characteristics

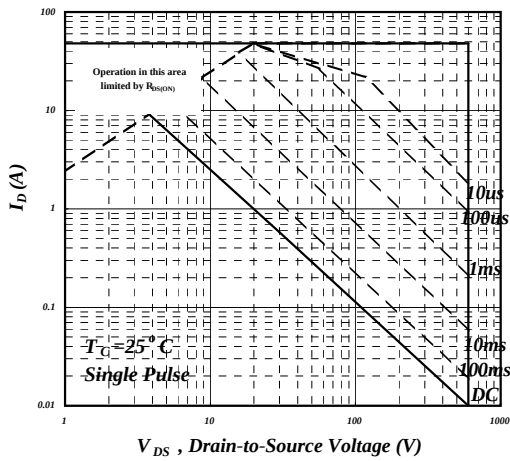


Fig 9. Maximum Safe Operating Area

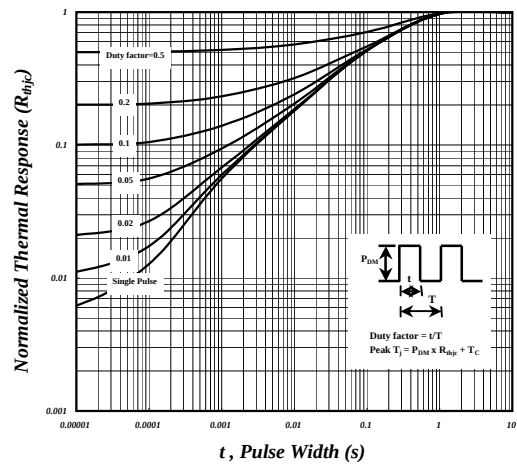


Fig10. Effective Transient Thermal Impedance

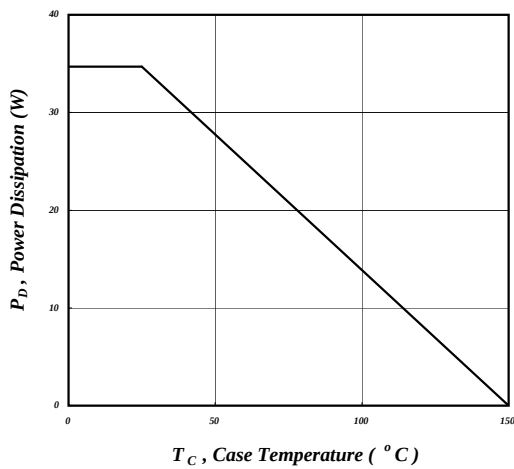


Fig 11. Total Power Dissipation

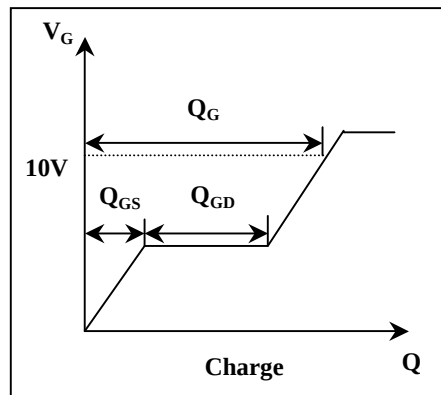
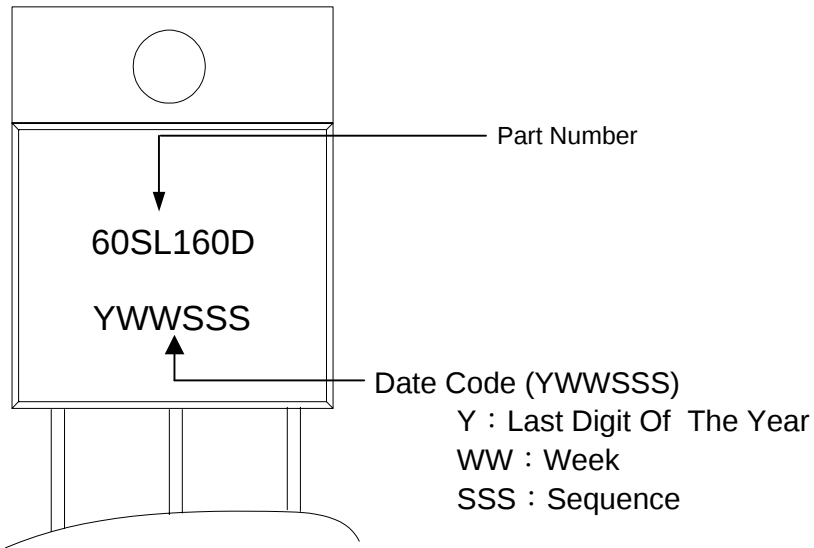


Fig 12. Gate Charge Waveform

MARKING INFORMATION

TO-220CFM-NL FOOTPRINT :

