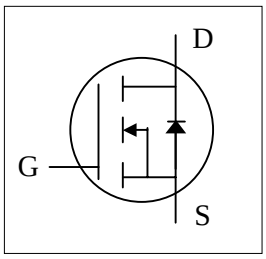
XP60SC060ADTL

Halogen-Free Product

N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- **100% R_g & UIS Test**
- **Low t_{rr} / Q_{rr}**
- **Simple Drive Requirement**
- **RoHS Compliant & Halogen-Free**

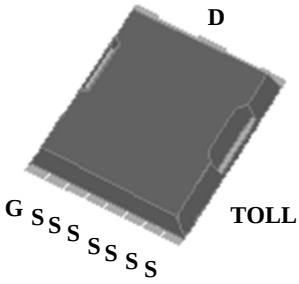


BV_{DSS}	600V
$R_{DS(ON)}$	60mΩ
I_D [3,4]	49A

Description

XP60SC060AD series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TOLL package is a perfect solution for high power density and high power efficiency application.



TOLL (TL)

Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	600	V
V_{GS}	Gate-Source Voltage	±20	V
V_{GS}	Gate-Source Voltage, AC (f > 1Hz)	±30	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V[3,4]	49	A
I_D@T_C=100℃	Drain Current, V_{GS} @ 10V[3,4]	31	A
I_{DM}	Pulsed Drain Current[1]	130	A
dv/dt	MOSFET dv/dt Ruggedness (V_{DS} = 0 …480V)	30	V/ns
P_D@T_C=25℃	Total Power Dissipation	277.7	W
P_D@T_A=25℃	Total Power Dissipation[7]	3.12	W
E_{AS}	Single Pulse Avalanche Energy[5]	450	mJ
dv/dt	Peak Diode Recovery dv/dt[6]	50	V/ns
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	0.45	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[7]	40	℃/W

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=1mA	600	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=18A	-	-	60	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	3	-	5	V
g_{fs}	Forward Transconductance	V_{DS}=10V, I_D=18A	-	31	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=480V, V_{GS}=0V	-	-	100	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±1	uA
Q_g	Total Gate Charge[8]	I_D=18A	-	93	149	nC
Q_{gs}	Gate-Source Charge[8]	V_{DS}=480V	-	26	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge[8]	V_{GS}=10V	-	42	-	nC
$t_{d(on)}$	Turn-on Delay Time[8]	V_{DD}=300V	-	83	-	ns
t_r	Rise Time[8]	I_D=18A	-	87	-	ns
$t_{d(off)}$	Turn-off Delay Time[8]	R_G=25Ω	-	230	-	ns
t_f	Fall Time[8]	V_{GS}=10V	-	60	-	ns
C_{iss}	Input Capacitance[8]	V_{GS}=0V	-	3650	5840	pF
C_{oss}	Output Capacitance[8]	V_{DS}=400V	-	85	-	pF
C_{rss}	Reverse Transfer Capacitance[8]	f=1.0MHz	-	10	-	pF
R_g	Gate Resistance	f=1.0MHz	-	1.3	2.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=18A, V_{GS}=0V	-	-	1.5	V
t_{rr}	Reverse Recovery Time[8]	I_S=18A, V_{GS}=0V	-	185	-	ns
Q_{rr}	Reverse Recovery Charge[8]	dI/dt=100A/μs	-	1.8	-	uC

Notes:

1.Pulse width limited by max. junction temperature.

2.Pulse test

3.Limited by max. junction temperature. Maximum duty cycle D=0.75

4.Ensure that the junction temperature does not exceed $T_{Jmax.}$.

5.Starting T_j=25°C , V_{DD}=90V , L=100mH , R_G=25Ω , V_{GS}=10V , I_{AS}=3A

6.I_{SD} ≦ I_D, V_{DD} ≦ BV_{DSS}, starting T_J = 25°C

7.Surface mounted on 1 in^2 copper pad of FR4 board

8.Guaranteed by design.

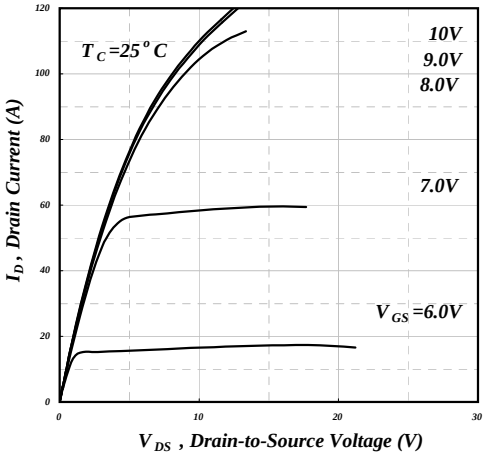


Fig 1. Typical Output Characteristics

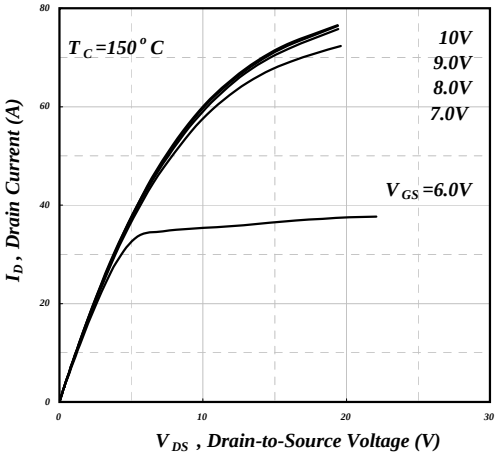


Fig 2. Typical Output Characteristics

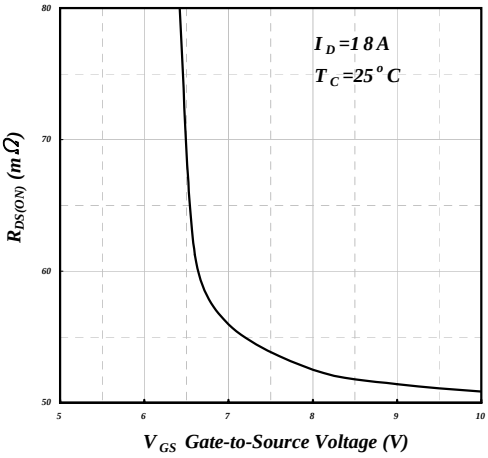


Fig 3. On-Resistance v.s. Gate Voltage

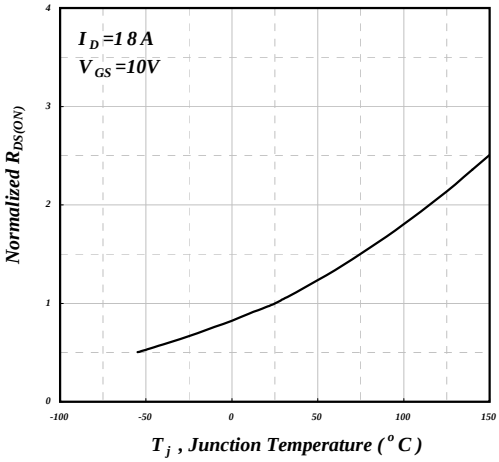


Fig 4. Normalized On-Resistance v.s. Junction Temperature

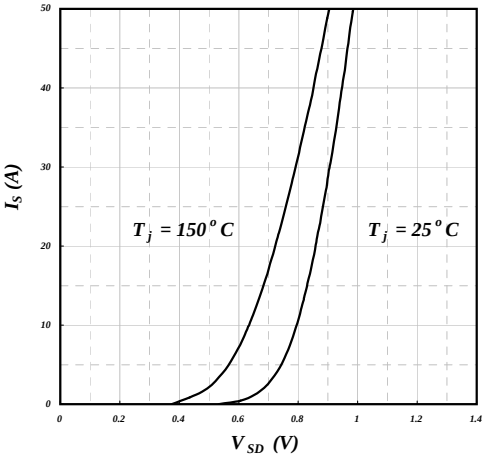


Fig 5. Forward Characteristic of Reverse Diode

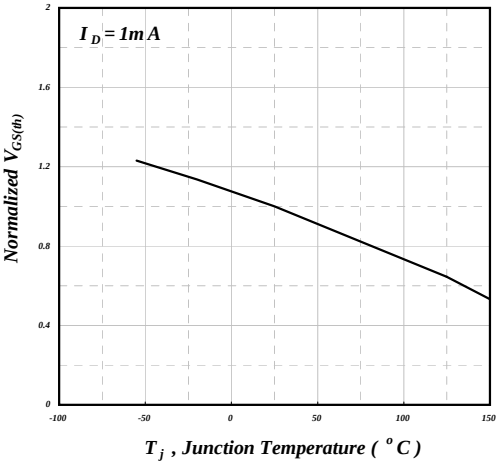


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

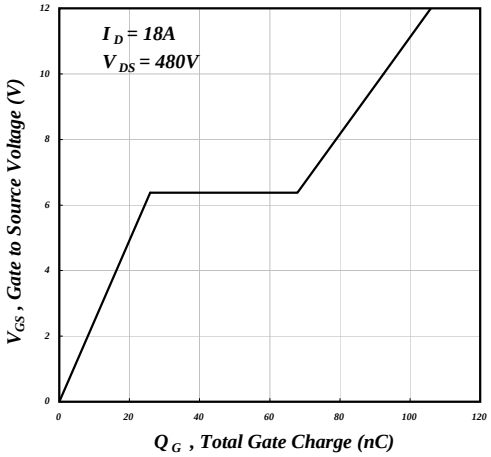


Fig 7. Gate Charge Characteristics

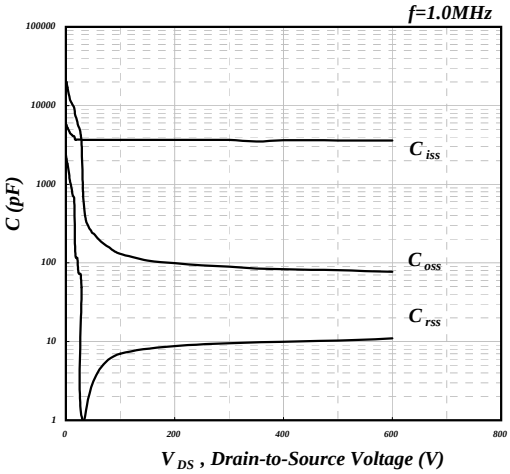


Fig 8. Typical Capacitance Characteristics

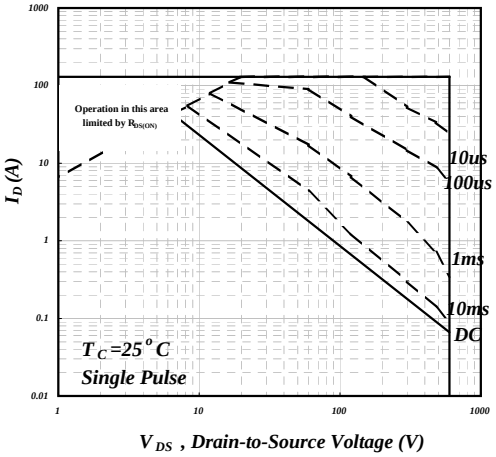


Fig 9. Maximum Safe Operating Area

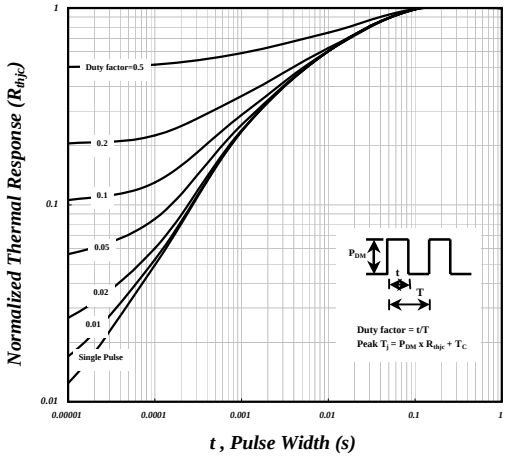


Fig10. Effective Transient Thermal Impedanc

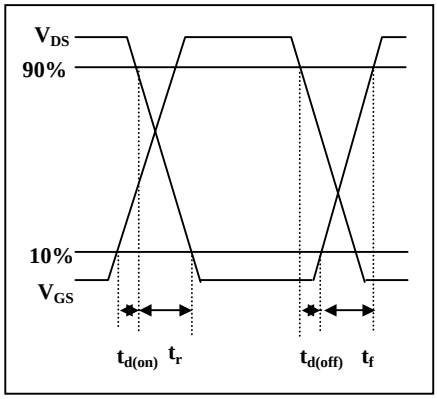


Fig 11. Switching Time Waveform

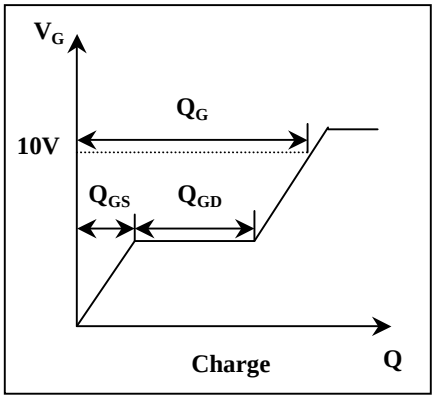


Fig 12. Gate Charge Waveform

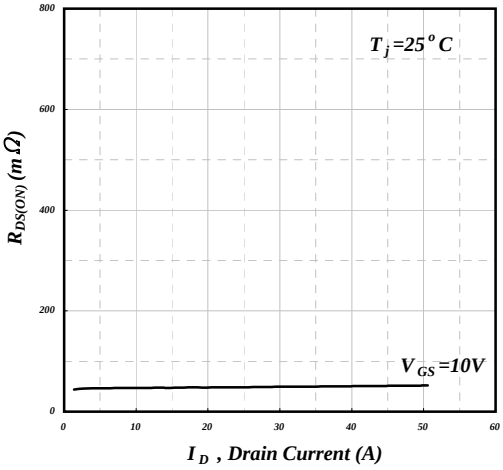


Fig 13. Typ. Drain-Source on State Resistance

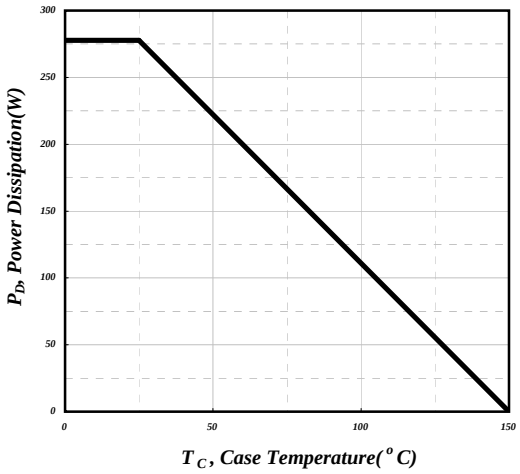
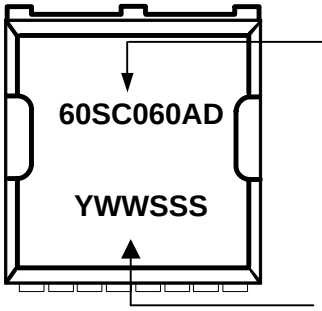


Fig 14. Total Power Dissipation

MARKING INFORMATION



Part Number

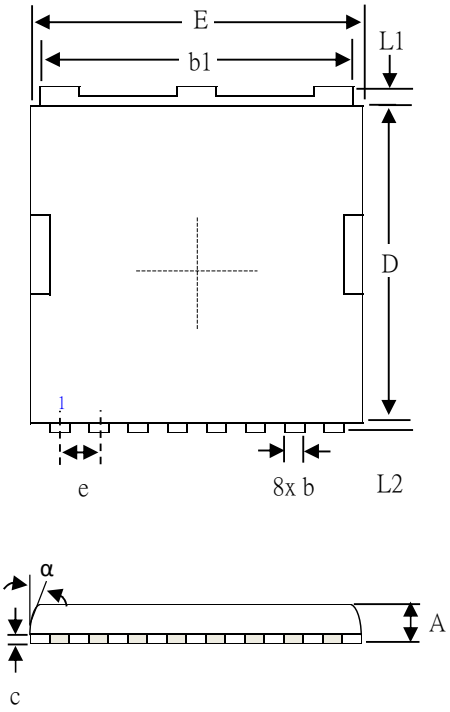
Date Code (YWWSSS)

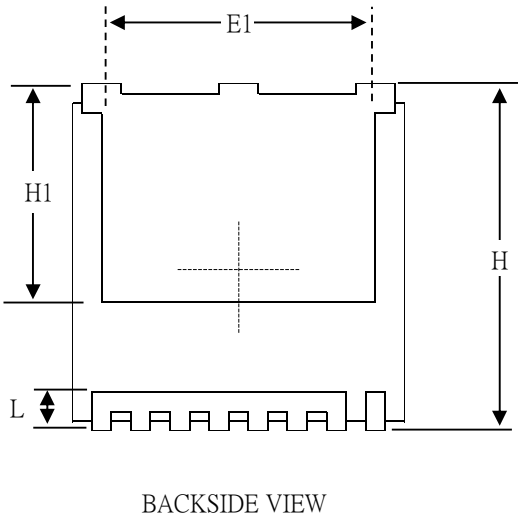
Y：Last Digit Of The Year

WW：Week

SSS：Sequence

Package Outline : TOLL





BACKSIDE VIEW

SYMBOLS	MIN	NOM	MAX
A	2.20	2.30	2.40
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
c	0.40	0.50	0.60
D	10.28	10.38	10.58
E	9.70	9.90	10.10
E1	7.90	8.70	9.50
e	1.20BCS		
H	11.48	11.68	11.88
H1	6.75	-	7.43
L	1.40	1.90	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
α	10° REF.		

1.All dimension are in millimeters.

2.Dimension does not include burrs and mold flash/protrusions.

3.The outline schematic is not to scale and slightly different from the actual product appearance.

Draw No. M1-TL-8-EFIM-G-V04

TOLL FOOTPRINT：