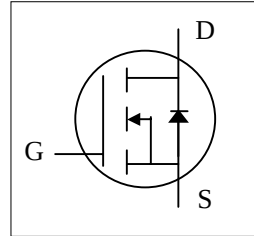
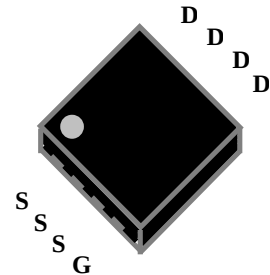


- ▼ Simple Drive Requirement
- ▼ Small Size & Ultra_Low $R_{DS(ON)}$
- ▼ RoHS Compliant & Halogen-Free



BV_{DSS}	30V
$R_{DS(ON)}$	4.2m Ω



PMPAK® 3 x 3

Description

XP3NA4R2A series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK® 3 x 3 package is special for voltage conversion application using standard infrared reflow technique with the backside heat sink to achieve the good thermal performance.

Absolute Maximum Ratings@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^4$ (Silicon Limited)	66	A
$I_D@T_C=25^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^4$ (Package Limited)	40	A
$I_D@T_C=100^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^4$ (Package Limited)	40	A
$I_D@T_A=25^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^3$	20.9	A
$I_D@T_A=70^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^3$	16.7	A
I_{DM}	Pulsed Drain Current ¹	160	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation	31.2	W
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation	3.12	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_j	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
R_{thj-c}	Maximum Thermal Resistance, Junction-case	4	$^\circ\text{C/W}$
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	40	$^\circ\text{C/W}$

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =19A	-	-	4.2	mΩ
		V _{GS} =4.5V, I _D =12A	-	-	7.8	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1.3	-	2.3	V
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =19A	-	65	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V	-	-	10	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±0.1	uA
Q _g	Total Gate Charge ⁵	I _D =19A	-	38	60.8	nC
Q _{gs}	Gate-Source Charge ⁵	V _{DS} =15V	-	6	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge ⁵	V _{GS} =10V	-	10	-	nC
t _{d(on)}	Turn-on Delay Time ⁵	V _{DS} =15V	-	9.5	-	ns
t _r	Rise Time ⁵	I _D =19A	-	57	-	ns
t _{d(off)}	Turn-off Delay Time ⁵	R _G =6Ω	-	39	-	ns
t _f	Fall Time ⁵	V _{GS} =10V	-	82	-	ns
C _{iss}	Input Capacitance ⁵	V _{GS} =0V	-	1610	2576	pF
C _{oss}	Output Capacitance ⁵	V _{DS} =25V	-	245	-	pF
C _{rss}	Reverse Transfer Capacitance ⁵	f=1.0MHz	-	200	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1.8	3.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =19A, V _{GS} =0V	-	-	1.2	V
t _{rr}	Reverse Recovery Time ⁵	I _S =19A, V _{GS} =0V,	-	12	-	ns
Q _{rr}	Reverse Recovery Charge ⁵	dI/dt=100A/μs	-	4	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² 2oz copper pad of FR4 board, t ≤10sec; 135°C/W when mounted on min. copper pad.
- 4.Package limitation current is 40A .
- 5.Guaranteed by design.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT, AUTOMOTIVE OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

XSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

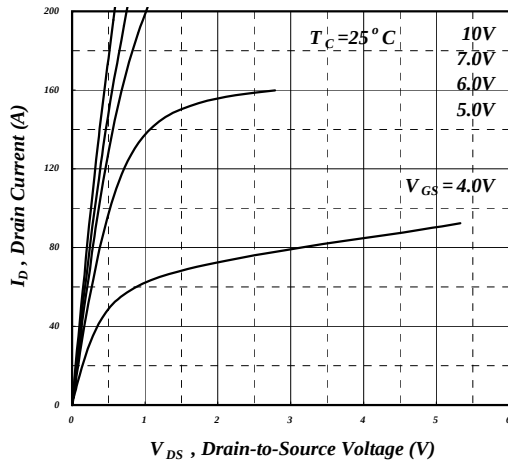


Fig 1. Typical Output Characteristics

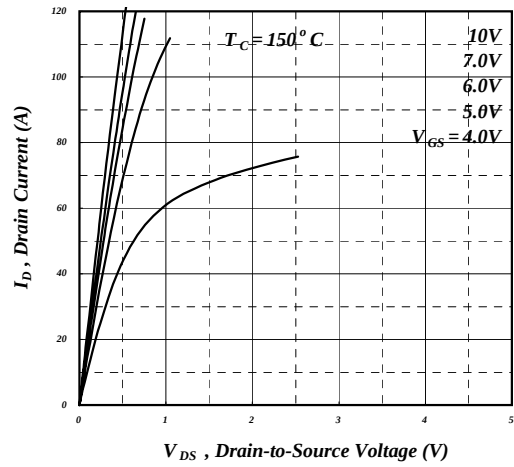


Fig 2. Typical Output Characteristics

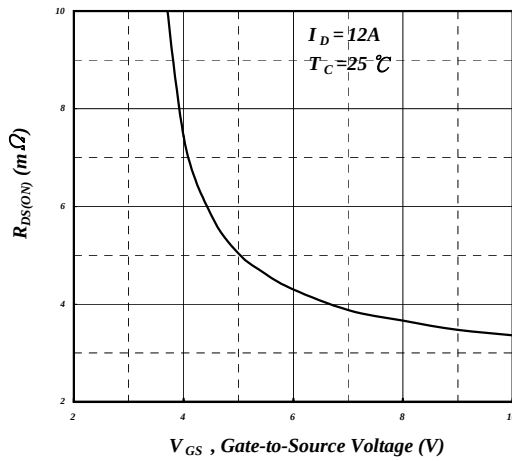
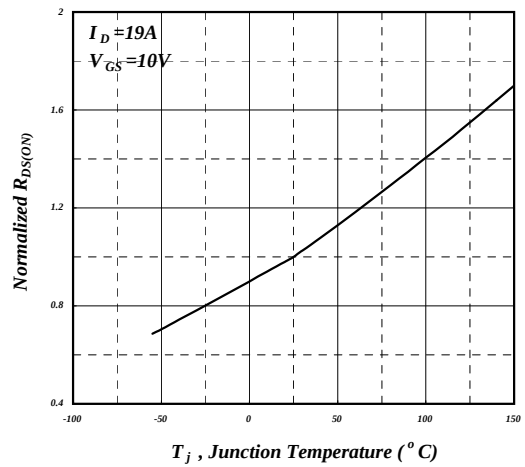
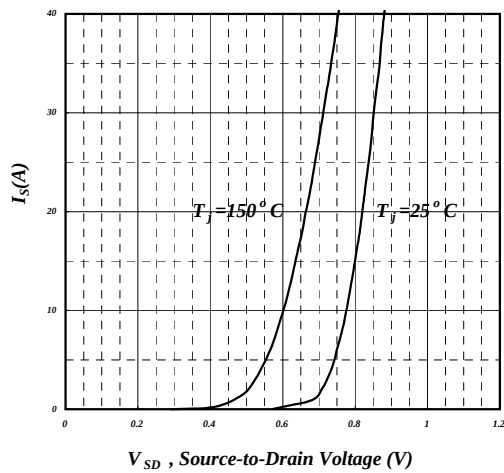


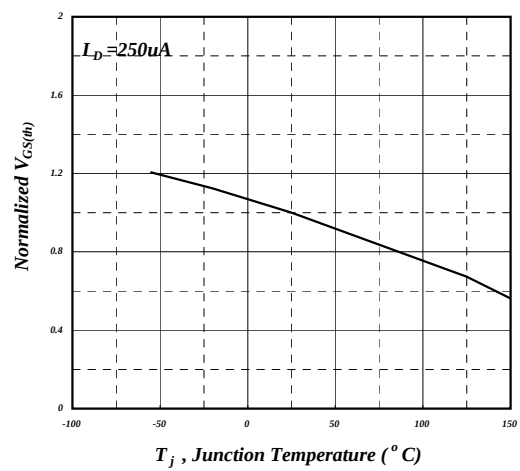
Fig 3. On-Resistance v.s. Gate Voltage



**Fig 4. Normalized On-Resistance
v.s. Junction Temperature**



**Fig 5. Forward Characteristic of
Reverse Diode**



**Fig 6. Gate Threshold Voltage v.s.
Junction Temperature**

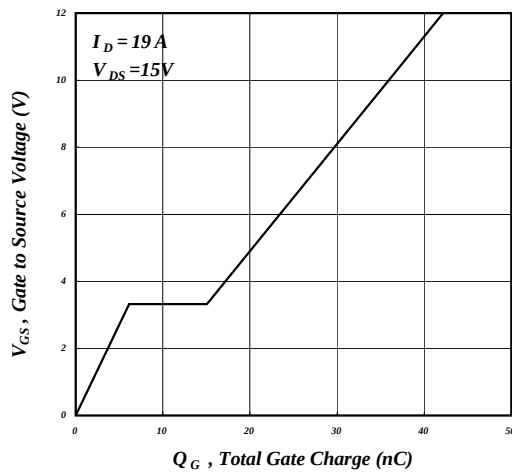


Fig 7. Gate Charge Characteristics

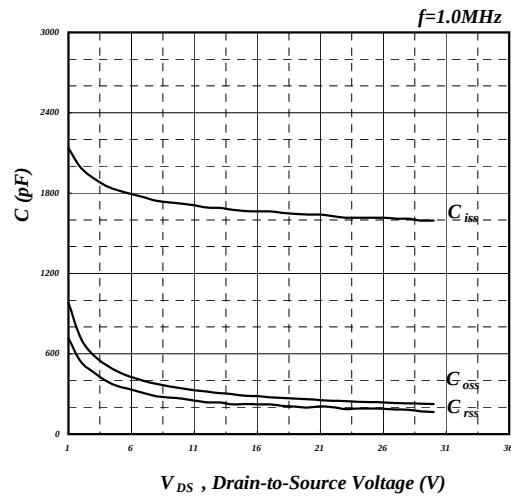


Fig 8. Typical Capacitance Characteristics

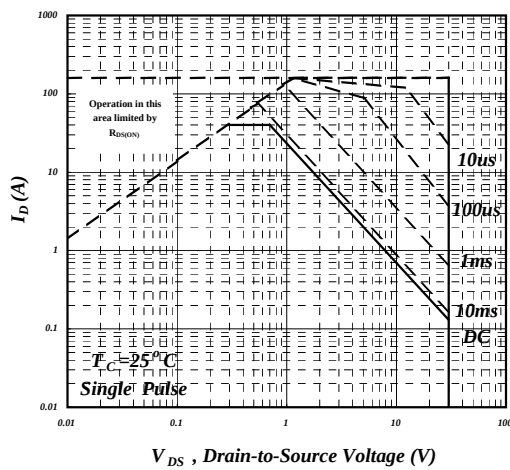


Fig 9. Maximum Safe Operating Area

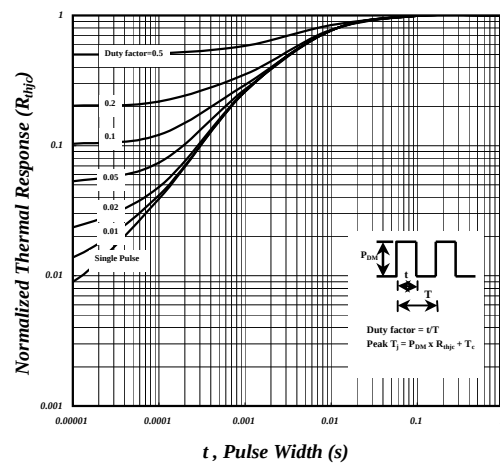


Fig 10. Effective Transient Thermal Impedance

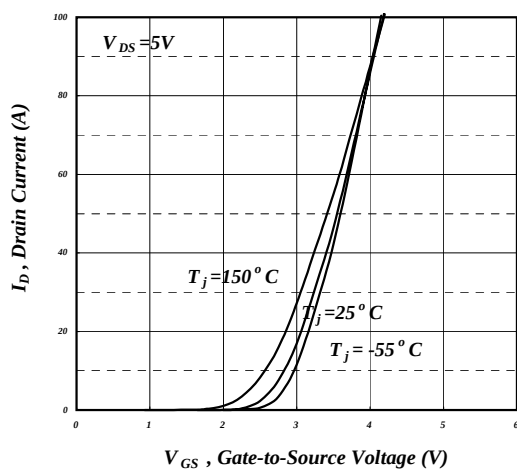


Fig 11. Transfer Characteristics

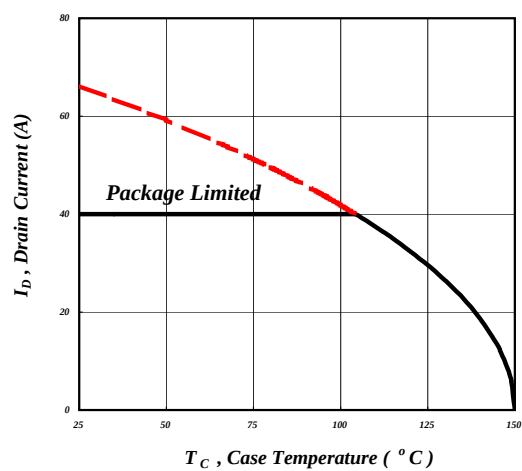


Fig 12. Drain Current v.s. Case Temperature

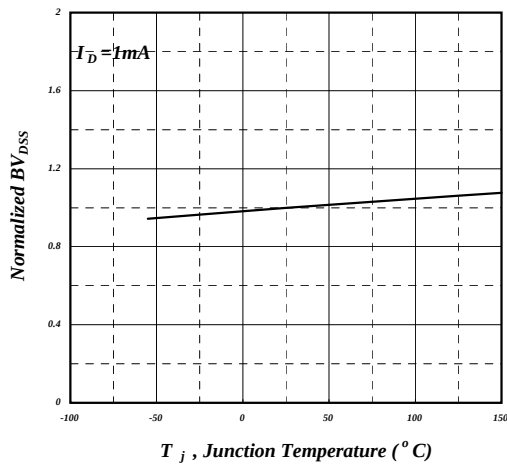


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

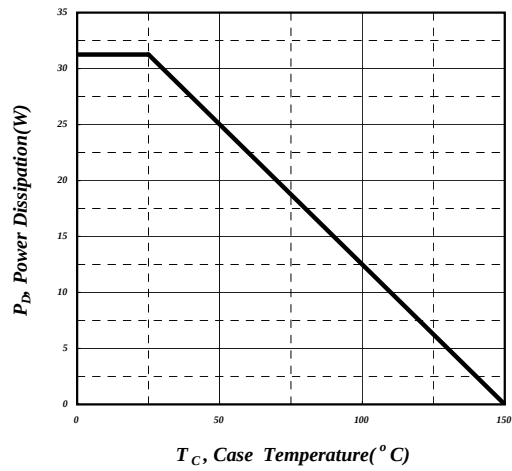


Fig 14. Total Power Dissipation

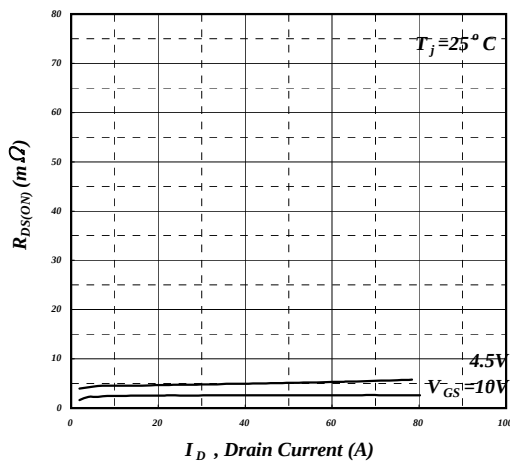


Fig 15. Typ. Drain-Source on State Resistance

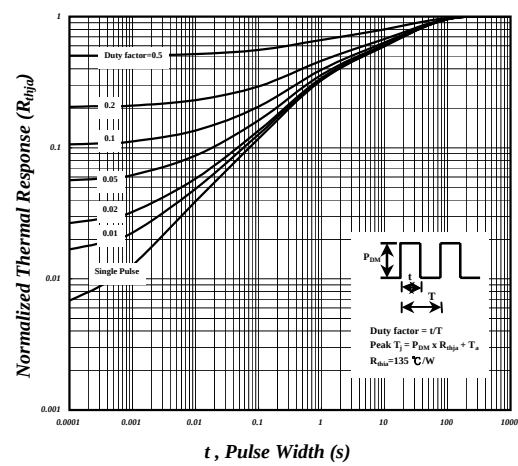
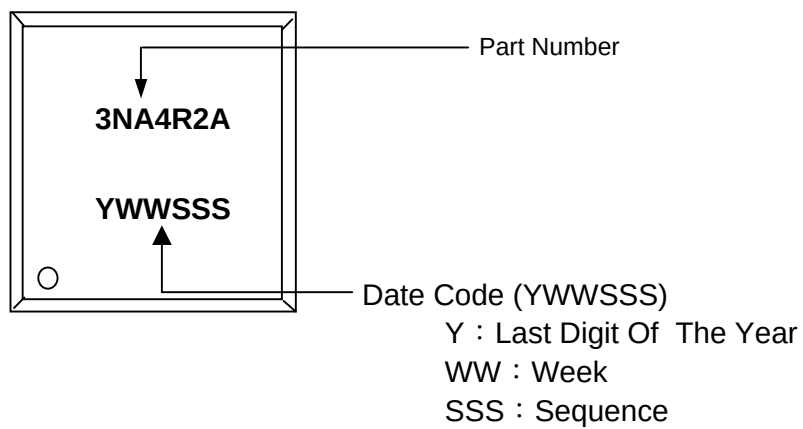
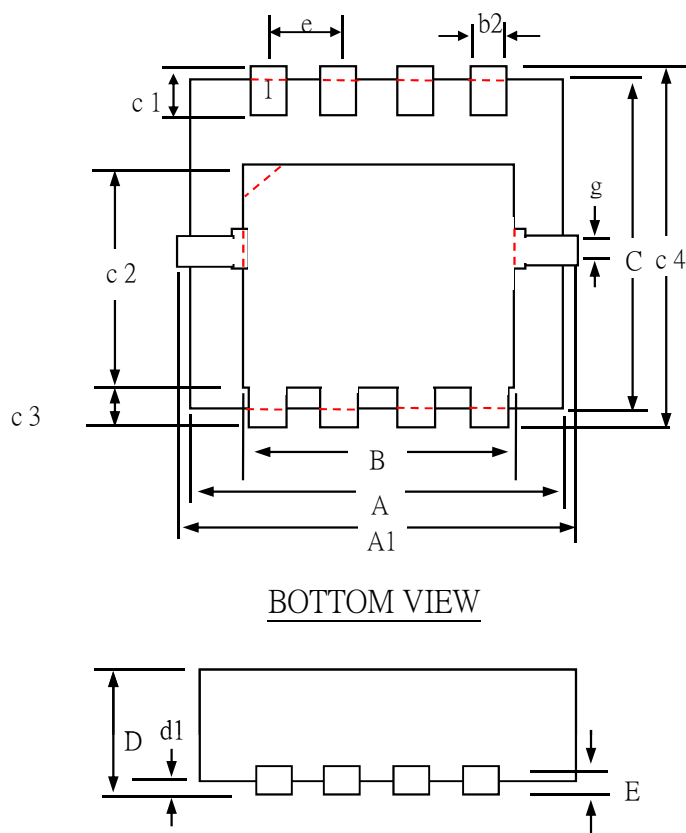


Fig 16. Effective Transient Thermal Impedance

MARKING INFORMATION

Package Outline : PMPAK 3x3



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	2.90	3.10	3.40
B	2.20	2.45	2.80
e	0.60	0.65	0.70
b2	0.20	0.30	0.40
C	2.90	3.10	3.40
c1	0.10	0.30	0.50
c2	1.20	1.70	2.20
c3	0.10	0.38	0.65
D	0.65	0.80	1.05
d1	0.00	0.10	0.20
E	0.10	0.18	0.25
A1	2.900	3.30	3.600
c4	2.900	3.30	3.600
g	0.20 (ref)		

- 1.All Dimension Are In Millimeters.
- 2.Dimension Does Not Include Mold Protrusions.
3. Thermal PAD and Pin contour is for reference, it may has little difference by option.

PMPAK3X3 FOOTPRINT :

