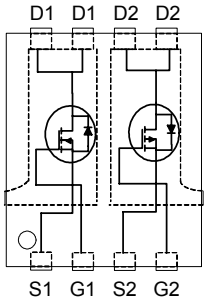
XP3CA010MT

Halogen-Free Product

N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

- **Simple Drive Requirement**
- **Low Gate Charge**
- **Fast Switching Performance**
- **RoHS Compliant & Halogen-Free**

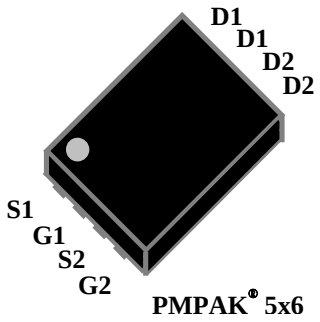


N-CH	BV_{DSS}	30V
	$R_{DS(ON)}$	9.6mΩ
	I_D[3]	15A
P-CH	BV_{DSS}	-30V
	$R_{DS(ON)}$	19mΩ
	I_D[3]	-11A

Description

XP3CA010 series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK® 5x6 package is special for voltage conversion application using standard infrared reflow technique with the backside heat sink to achieve the good thermal performance.



PMPAK® 5x6

Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D@T_A=25℃	Drain Current, V_{GS} @ 10V[3]	15	-11	A
I_D@T_A=70℃	Drain Current, V_{GS} @ 10V[3]	12	-9	A
I_{DM}	Pulsed Drain Current[1]	40	-30	A
P_D@T_A=25℃	Total Power Dissipation	3.57		W
T_{STG}	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃

Thermal Data

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
Rthj-c	Maximum Thermal Resistance, Junction-case	5	5	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	35	35	℃/W

N-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=9A	-	-	9.6	mΩ
		V_{GS}=4.5V, I_D=5A	-	-	14.5	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1.3	-	2.3	V
g_{fs}	Forward Transconductance	V_{DS}=5V, I_D=9A	-	35	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V, V_{GS}=0V	-	-	10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±0.1	uA
Q_g	Total Gate Charge	I_D=9A	-	20	32	nC
Q_{gs}	Gate-Source Charge	V_{DS}=15V	-	4	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=10V	-	4	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=15V	-	9	-	ns
t_r	Rise Time	I_D=1A	-	8	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω	-	23	-	ns
t_f	Fall Time	V_{GS}=10V	-	6	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	1000	1600	pF
C_{oss}	Output Capacitance	V_{DS}=25V	-	120	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	100	-	pF
R_g	Gate Resistance	f=1.0MHz	-	1.8	3.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=2.9A, V_{GS}=0V	-	-	1.2	V
t_{rr}	Reverse Recovery Time	I_S=9A, V_{GS}=0V	-	10	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	3.5	-	nC

P-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V, I_D=-7A	-	-	19	mΩ
		V_{GS}=-4.5V, I_D=-4A	-	-	32	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1.3	-	-2.3	V
g_{fs}	Forward Transconductance	V_{DS}=-5V, I_D=-7A	-	18	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-24V, V_{GS}=0V	-	-	-10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±0.1	uA
Q_g	Total Gate Charge	I_D=-7A	-	30	48	nC
Q_{gs}	Gate-Source Charge	V_{DS}=-15V	-	6	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=-10V	-	5	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=-15V	-	12	-	ns
t_r	Rise Time	I_D=-1A	-	10	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω	-	65	-	ns
t_f	Fall Time	V_{GS}=-10V	-	33	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	1680	2688	pF
C_{oss}	Output Capacitance	V_{DS}=-25V	-	210	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	160	-	pF
R_g	Gate Resistance	f=1.0MHz	-	11	22	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=-2.9A, V_{GS}=0V	-	-	-1.2	V
t_{rr}	Reverse Recovery Time	I_S=-7A, V_{GS}=0V	-	14	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=-100A/μs	-	6	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board, t ≤10sec ; 85°C/W at steady state.

N-Channel

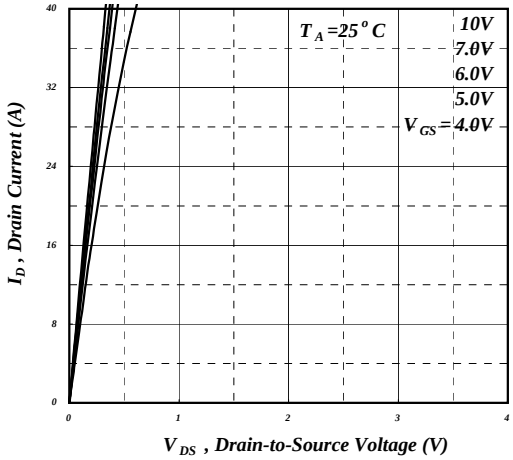


Fig 1. Typical Output Characteristics

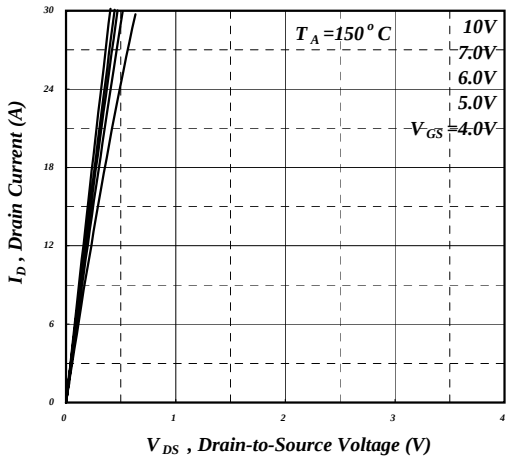


Fig 2. Typical Output Characteristics

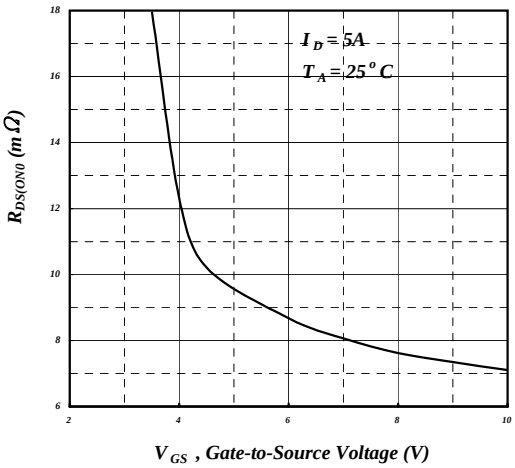


Fig 3. On-Resistance v.s. Gate Voltage

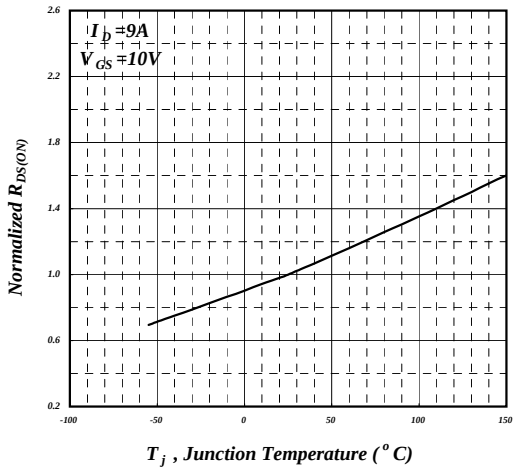


Fig 4. Normalized On-Resistance v.s. Junction Temperature

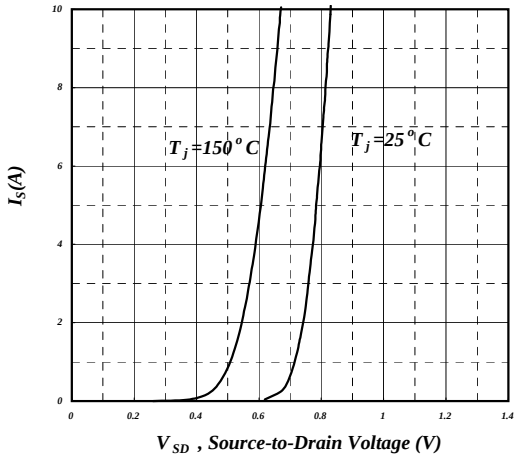


Fig 5. Forward Characteristic of Reverse Diode

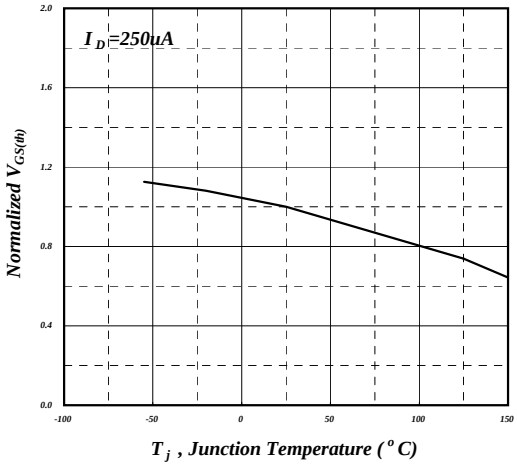


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

N-Channel

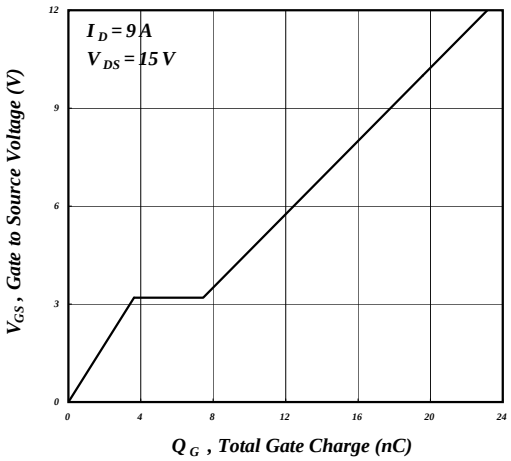


Fig 7. Gate Charge Characteristics

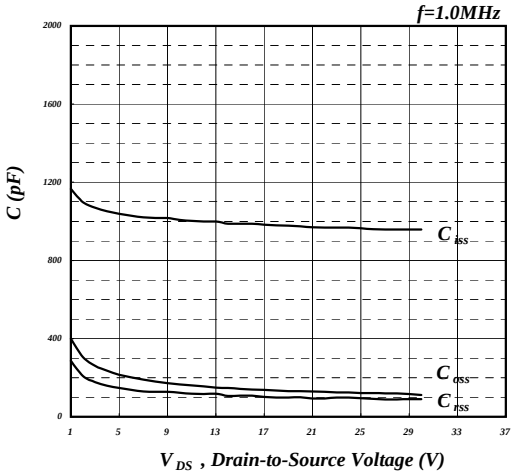


Fig 8. Typical Capacitance Characteristics

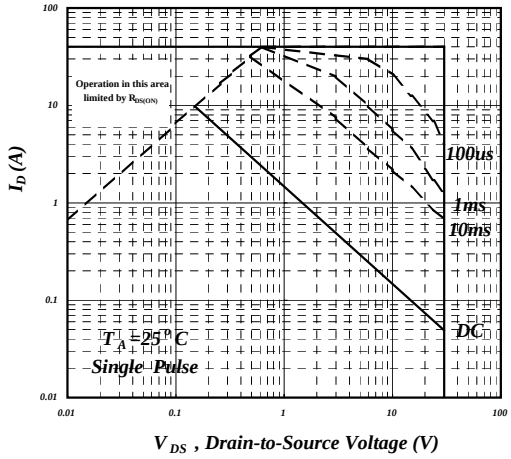


Fig 9. Maximum Safe Operating Area

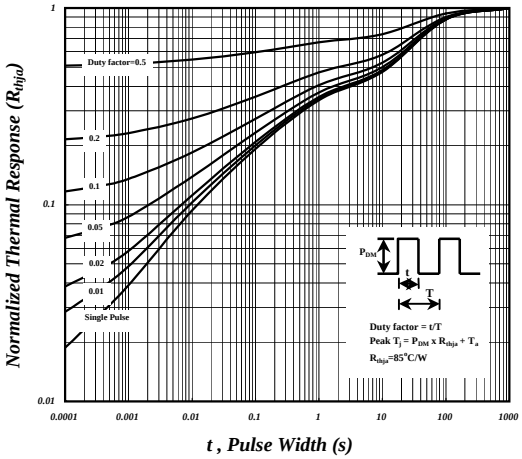


Fig 10. Effective Transient Thermal Impedance

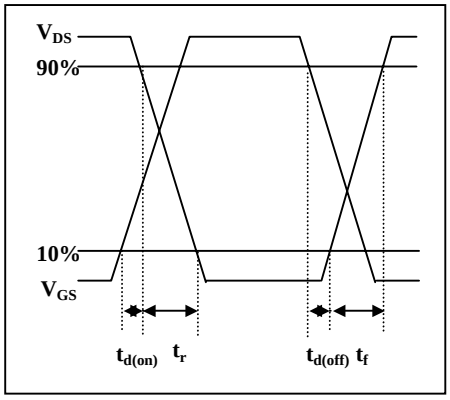


Fig 11. Switching Time Waveform

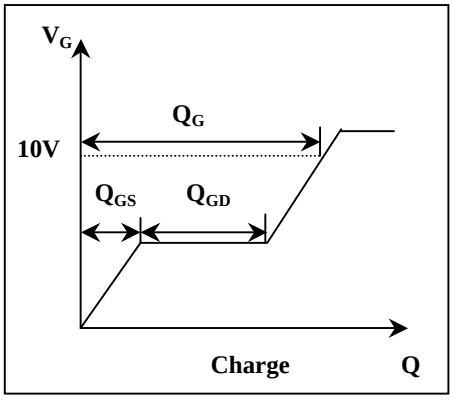


Fig 12. Gate Charge Waveform

N-Channel

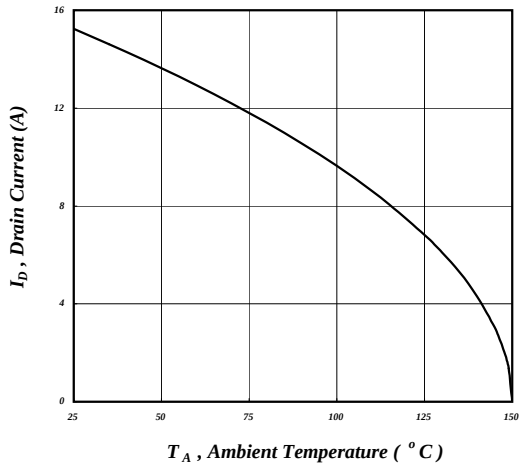


Fig 13. Drain Current v.s. Ambient Temperature

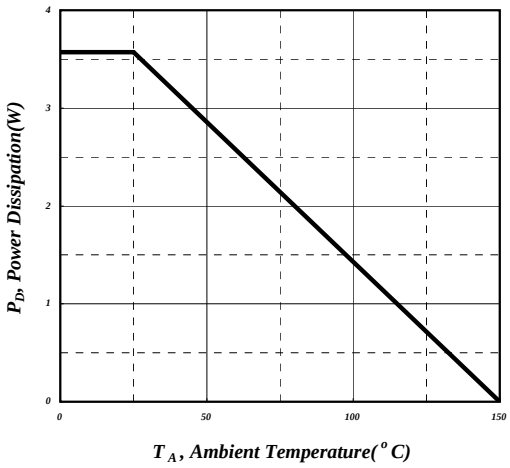


Fig 14. Total Power Dissipation

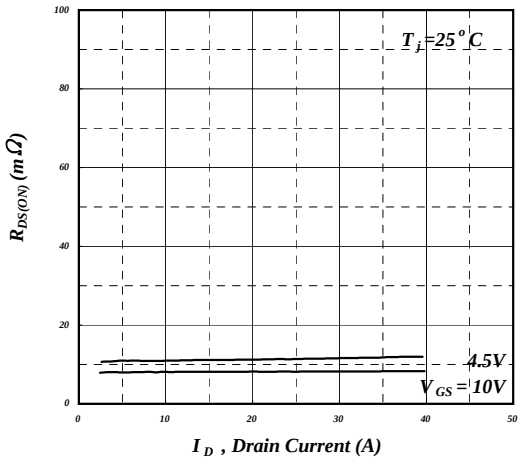


Fig 15. Typ. Drain-Source on State Resistance

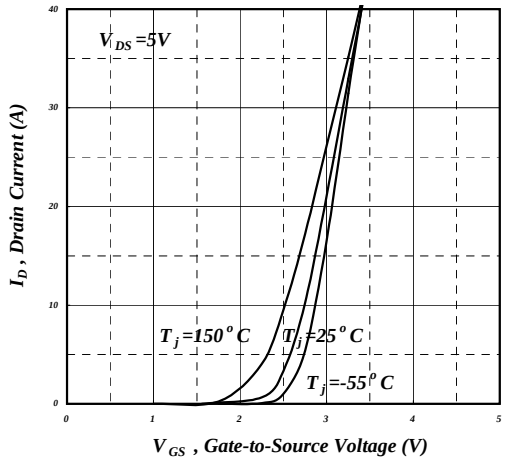


Fig 16. Transfer Characteristics

P-Channel

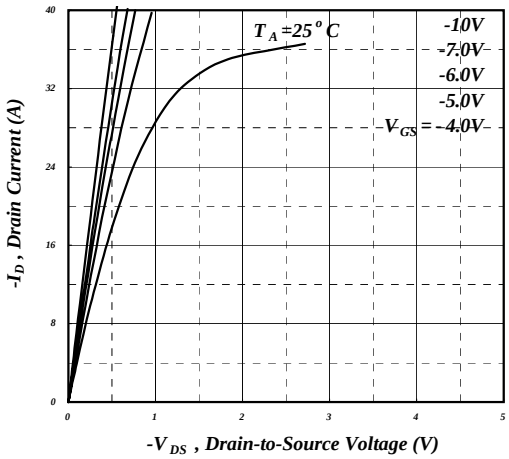


Fig 1. Typical Output Characteristics

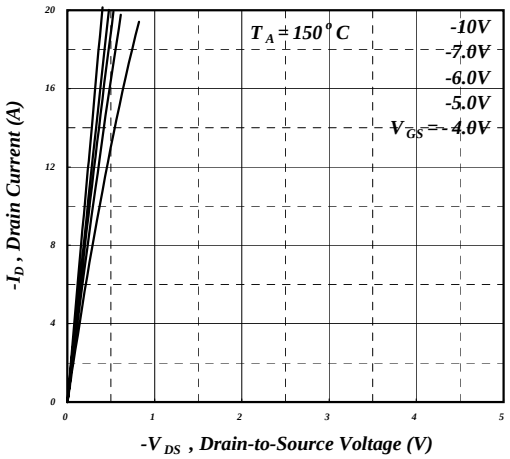


Fig 2. Typical Output Characteristics

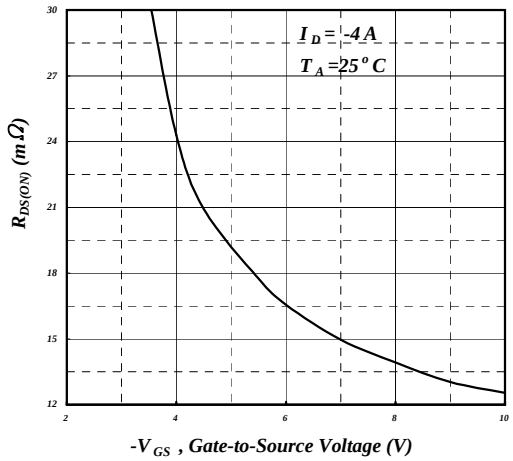


Fig 3. On-Resistance v.s. Gate Voltage

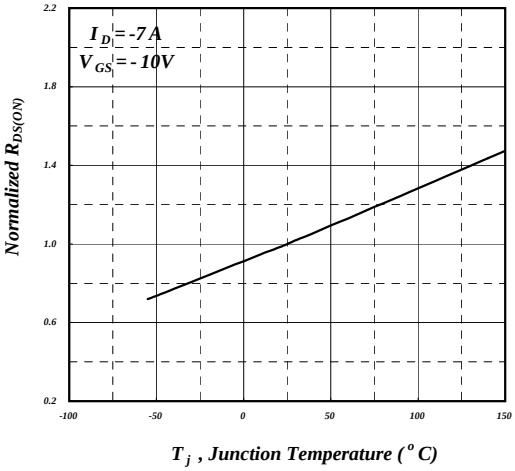


Fig 4. Normalized On-Resistance v.s. Junction Temperature

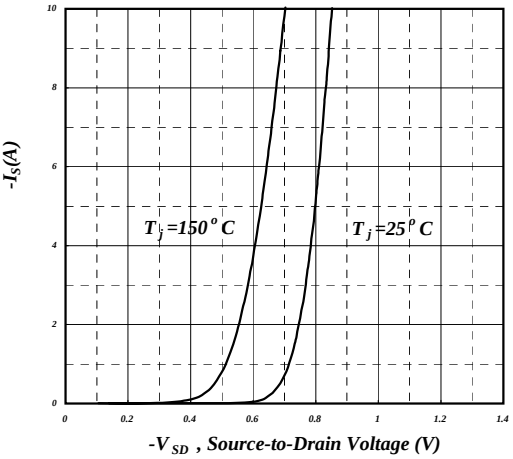


Fig 5. Forward Characteristic of Reverse Diode

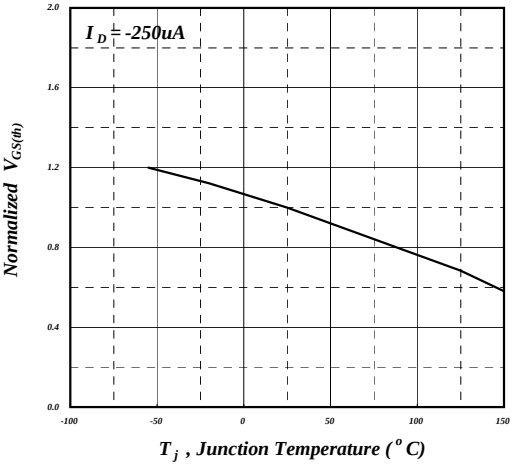


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

P-Channel

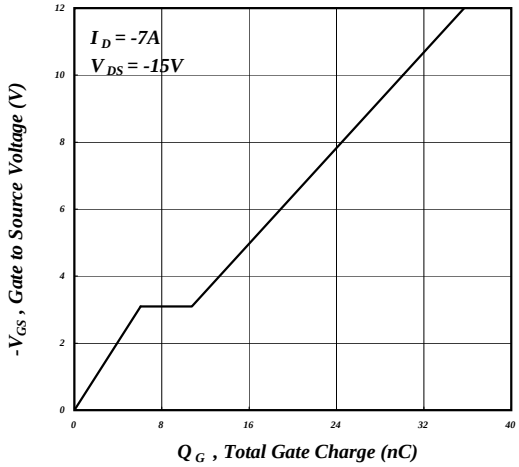


Fig 7. Gate Charge Characteristics

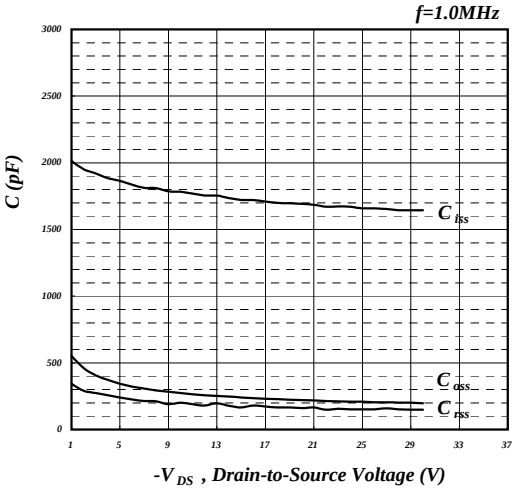


Fig 8. Typical Capacitance Characteristics

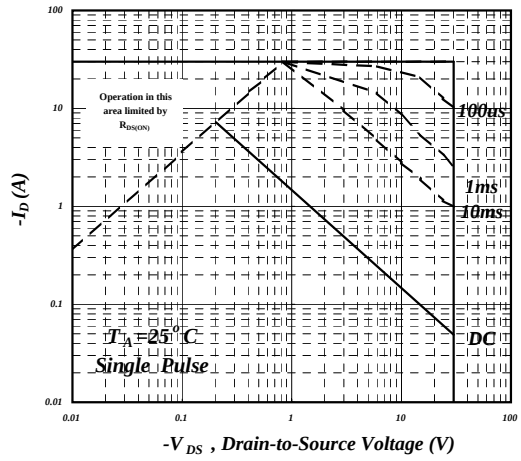


Fig 9. Maximum Safe Operating Area

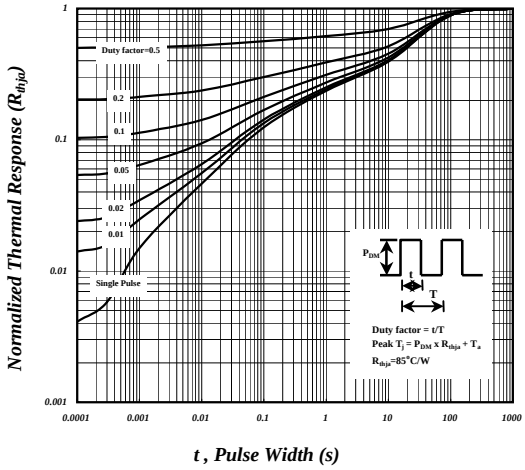


Fig 10. Effective Transient Thermal Impedance

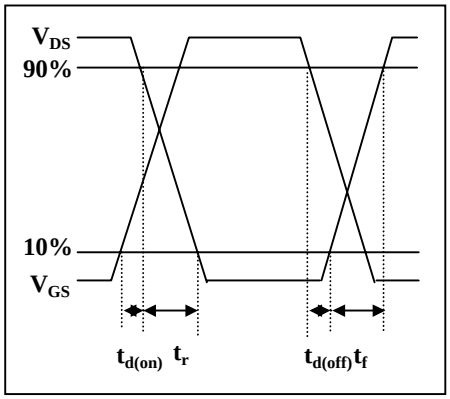


Fig 11. Switching Time Waveform

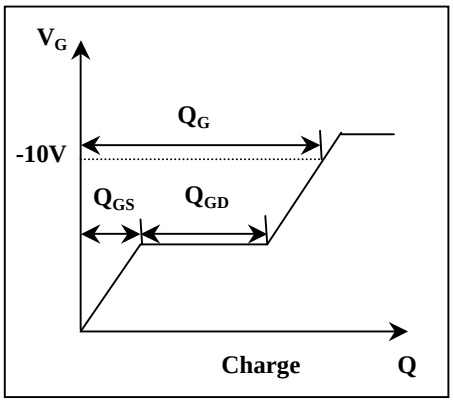


Fig 12. Gate Charge Waveform

P-Channel

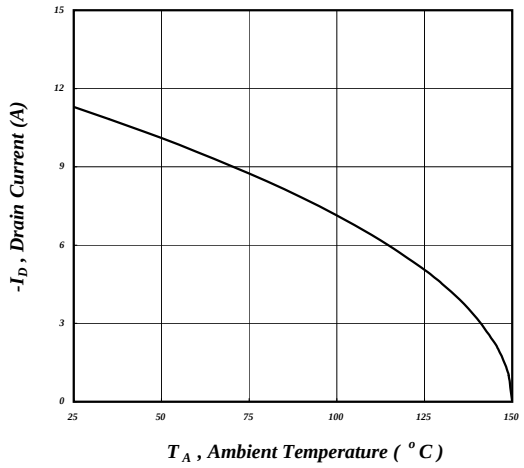


Fig 13. Drain Current v.s. Ambient Temperature

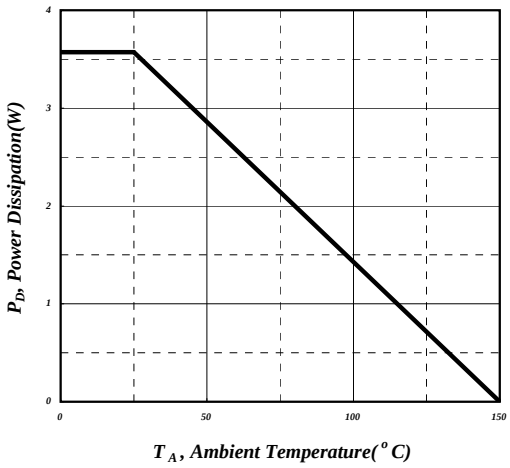


Fig 14. Total Power Dissipation

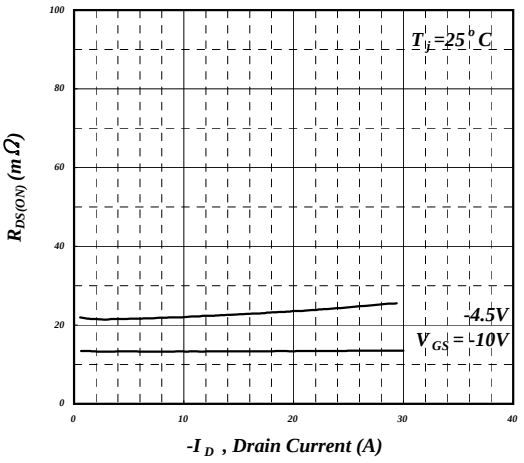


Fig 15. Typ. Drain-Source on State Resistance

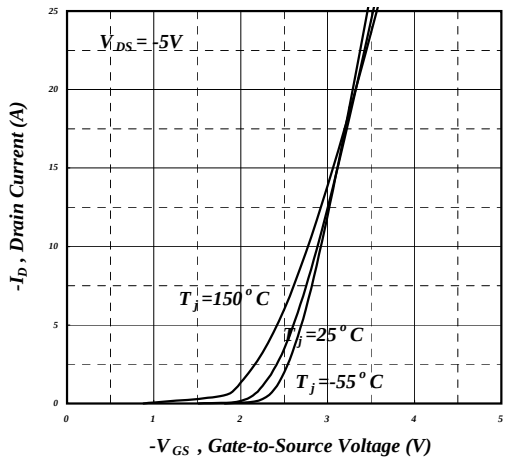
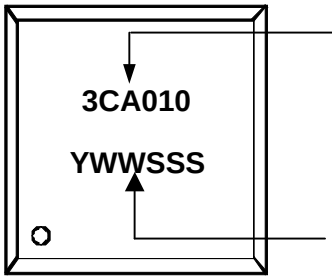


Fig 16. Transfer Characteristics

MARKING INFORMATION



Part Number

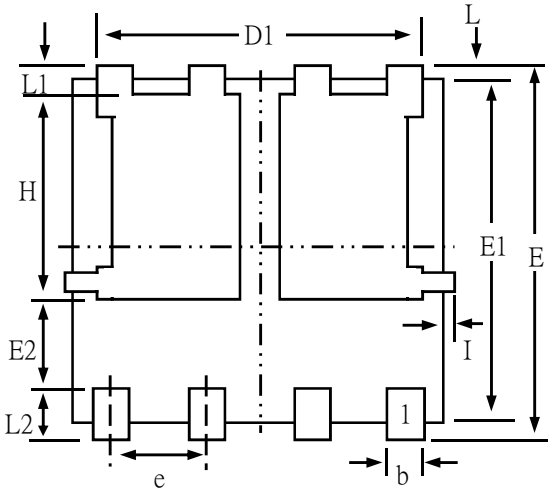
Date Code (YWWSSS)

Y：Last Digit Of The Year

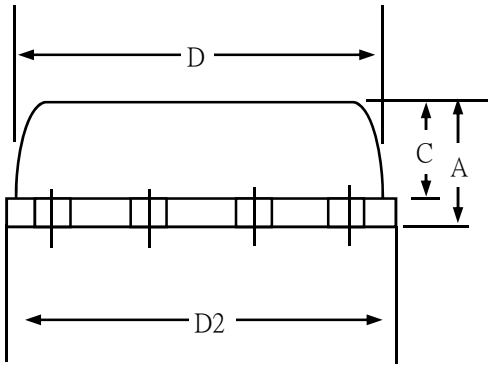
WW：Week

SSS：Sequence

Package Outline : PMPAK 5x6 (Dual Pad)



BACKSIDE VIEW



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.80	1.00	1.20
b	0.34	0.42	0.50
C	0.54	0.76	0.97
D	4.80	4.95	5.10
D1	4.11	4.21	4.31
E	5.90	6.05	6.20
E1	5.60	5.75	5.90
E2	1.60 (ref.)		
e	1.27 (ref.)		
L	0.05	0.15	0.25
L1	0.60 (ref.)		
L2	0.60 (ref.)		
H	3.60 (ref.)		
I	0.15 (ref.)		
D2	4.80	5.15	5.50

1.All Dimension Are In Millimeters.

2.Dimension Does Not Include Mold Protrusions.

Draw No. M2-1MT8-G-v02

PMPAK5X6(Dual Pad,左右) FOOTPRINT：