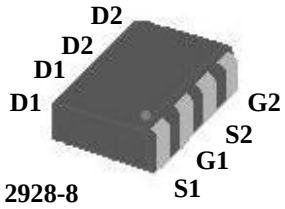
XP3C017AY

Halogen-Free Product

N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

- **Simple Drive Requirement**
- **Low Gate Charge**
- **Fast Switching Performance**
- **RoHS Compliant & Halogen-Free**

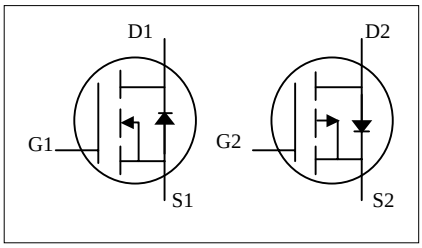


N-CH	BV_{DSS}	30V
	$R_{DS(ON)}$	17.8mΩ
	I_D	7A
P-CH	BV_{DSS}	-30V
	$R_{DS(ON)}$	30mΩ
	I_D	-5.5A

Description

XP3C017A series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The 2928-8 J-lead package provides good on-resistance performance and space saving like TSOP-6.



Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D@T_A=25℃	Drain Current, V_{GS} @ 10V[3]	7	-5.5	A
I_D@T_A=70℃	Drain Current, V_{GS} @ 10V[3]	5.5	-4.5	A
I_{DM}	Pulsed Drain Current[1]	20	-20	A
P_D@T_A=25℃	Total Power Dissipation	1.38		W
T_{STG}	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	90	℃/W

N-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=7A	-	-	17.8	mΩ
		V_{GS}=4.5V, I_D=4A	-	-	27	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1.4	-	2.5	V
g_{fs}	Forward Transconductance	V_{DS}=5V, I_D=7A	-	20	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V, V_{GS}=0V	-	-	10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge	I_D=4A	-	10	16	nC
Q_{gs}	Gate-Source Charge	V_{DS}=15V	-	4	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=4.5V	-	3	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=15V	-	9	-	ns
t_r	Rise Time	I_D=1A	-	7	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω	-	22	-	ns
t_f	Fall Time	V_{GS}=10V	-	5	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	1200	1920	pF
C_{oss}	Output Capacitance	V_{DS}=15V	-	120	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	100	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=1.2A, V_{GS}=0V	-	-	1.2	V
t_{rr}	Reverse Recovery Time	I_S=7A, V_{GS}=0V	-	11	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	4	-	nC

P-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V, I_D=-5A	-	-	30	mΩ
		V_{GS}=-4.5V, I_D=-3A	-	-	57	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1.4	-	-2.5	V
g_{fs}	Forward Transconductance	V_{DS}=-5V, I_D=-5A	-	12	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-24V, V_{GS}=0V	-	-	-10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge	I_D=-3A	-	9	14.4	nC
Q_{gs}	Gate-Source Charge	V_{DS}=-15V	-	4	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=-4.5V	-	3	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=-15V	-	11	-	ns
t_r	Rise Time	I_D=-1A	-	6	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω	-	30	-	ns
t_f	Fall Time	V_{GS}=-10V	-	8	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	1000	1600	pF
C_{oss}	Output Capacitance	V_{DS}=-15V	-	140	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	100	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=-1.2A, V_{GS}=0V	-	-	-1.2	V
t_{rr}	Reverse Recovery Time	I_S=-5A, V_{GS}=0V,	-	11	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	4	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board, t ≤10sec ; 210 °C/W when mounted on Min. copper pad.

N-Channel

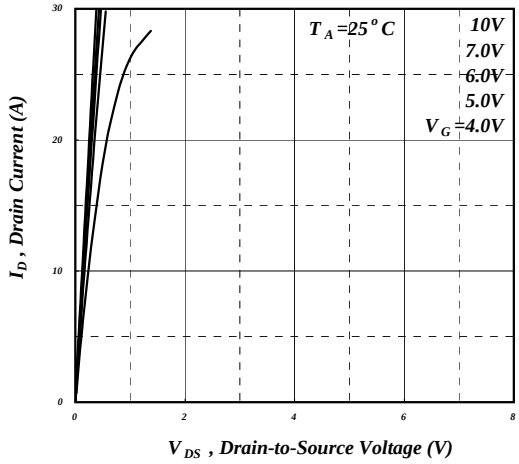


Fig 1. Typical Output Characteristics

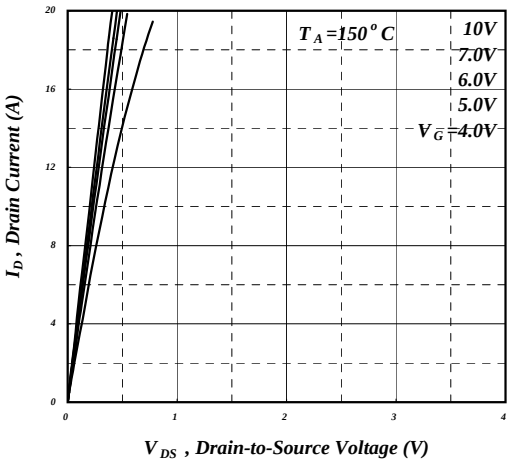


Fig 2. Typical Output Characteristics

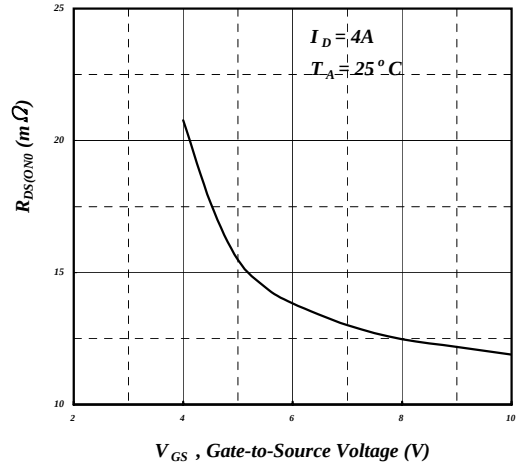


Fig 3. On-Resistance v.s. Gate Voltage

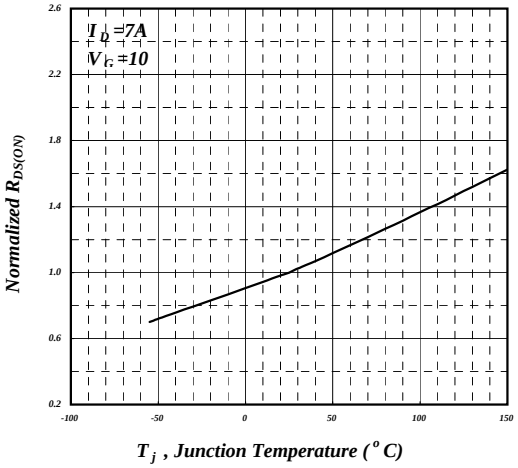


Fig 4. Normalized On-Resistance v.s. Junction Temperature

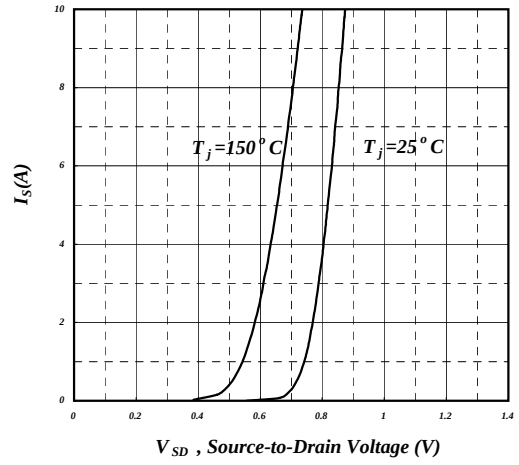


Fig 5. Forward Characteristic of Reverse Diode

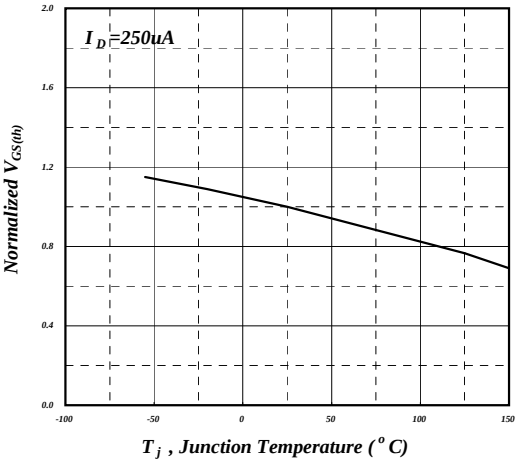


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

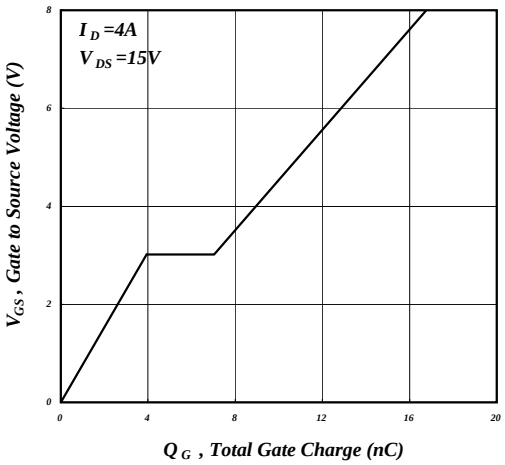


Fig 7. Gate Charge Characteristics

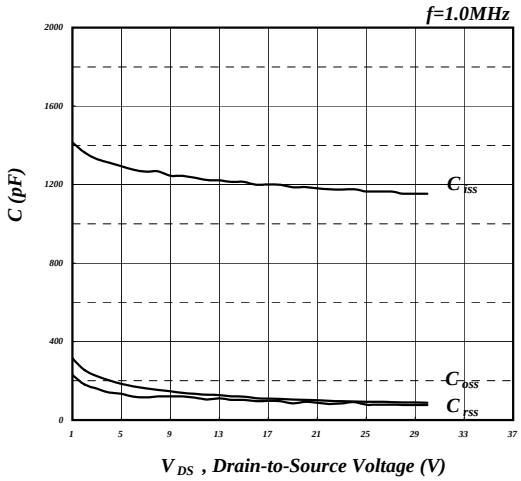


Fig 8. Typical Capacitance Characteristics

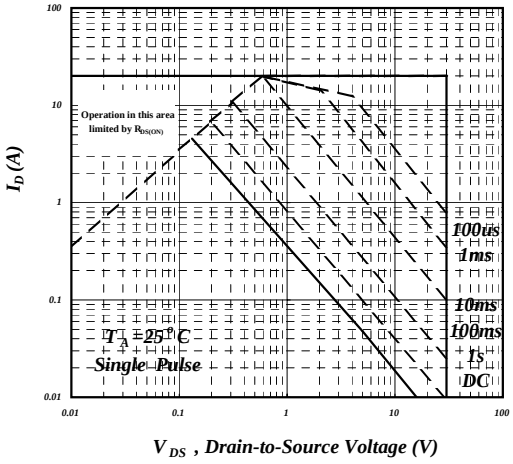


Fig 9. Maximum Safe Operating Area

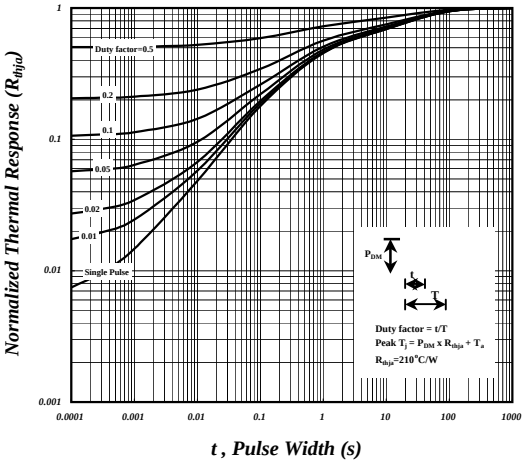


Fig 10. Effective Transient Thermal Impedance

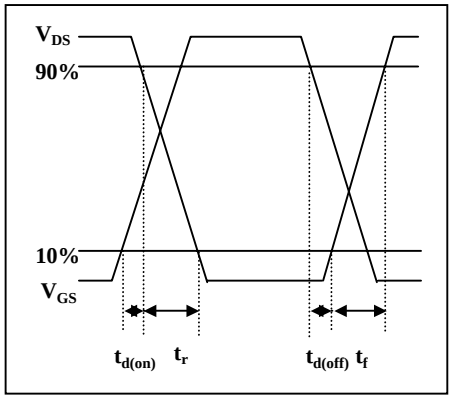


Fig 11. Switching Time Waveform

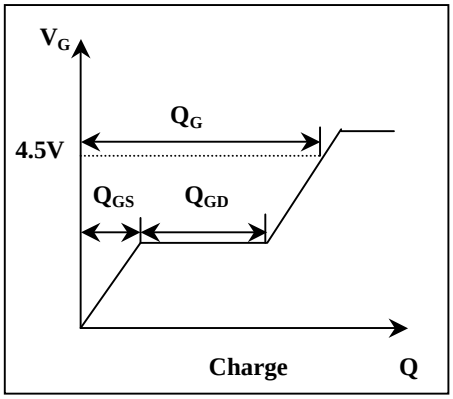


Fig 12. Gate Charge Waveform

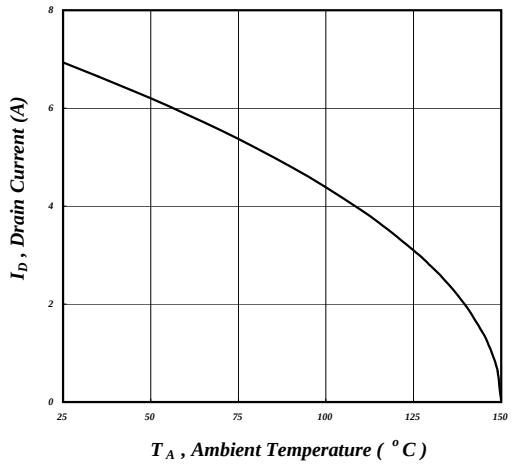


Fig 13. Drain Current v.s. Ambient Temperature

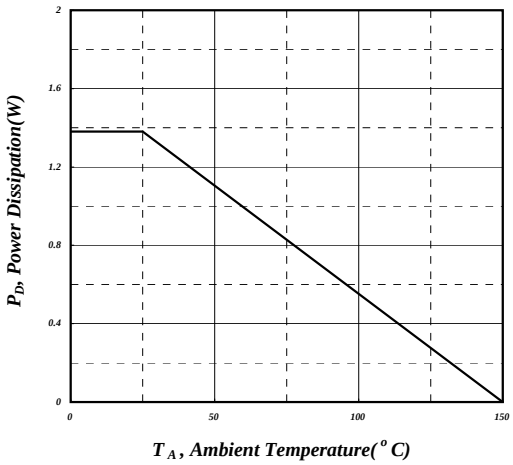


Fig 14. Total Power Dissipation

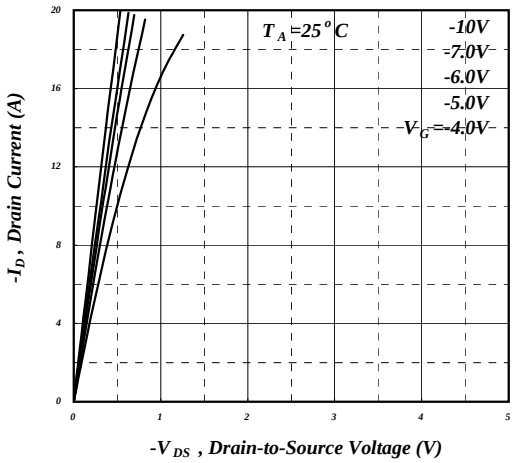


Fig 1. Typical Output Characteristics

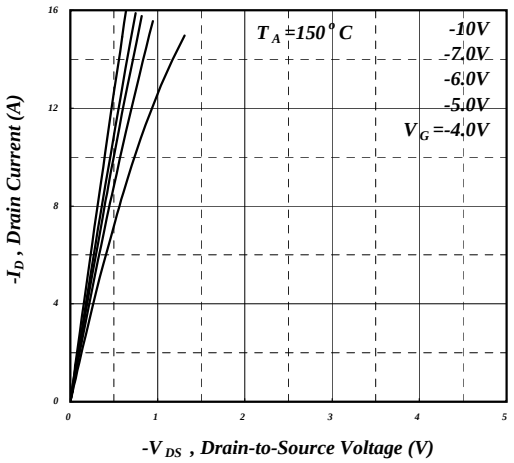


Fig 2. Typical Output Characteristics

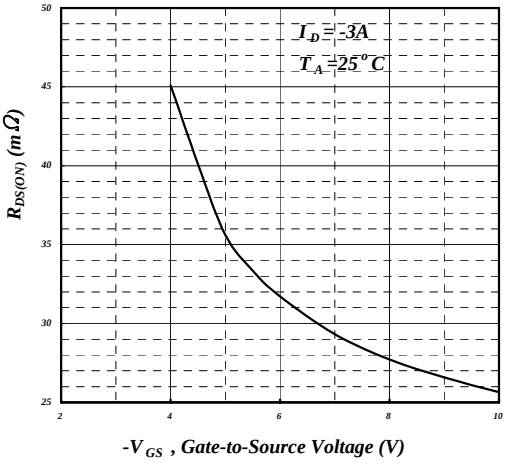


Fig 3. On-Resistance v.s. Gate Voltage

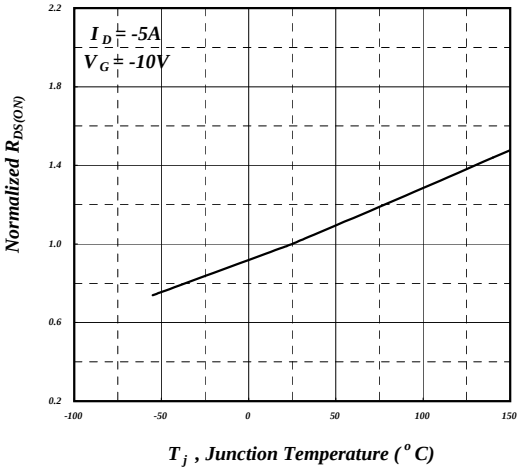


Fig 4. Normalized On-Resistance v.s. Junction Temperature

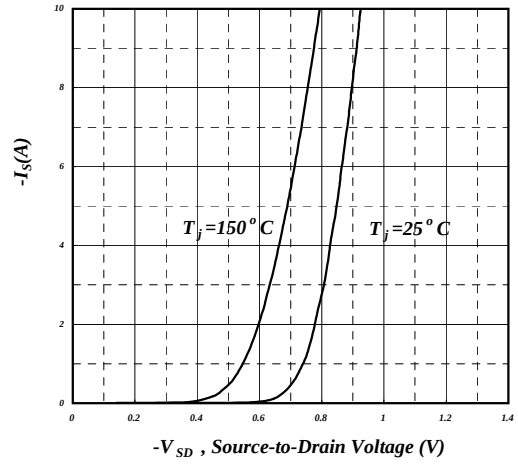


Fig 5. Forward Characteristic of Reverse Diode

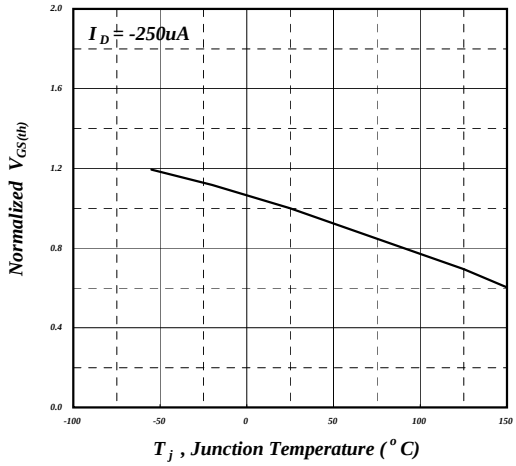


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

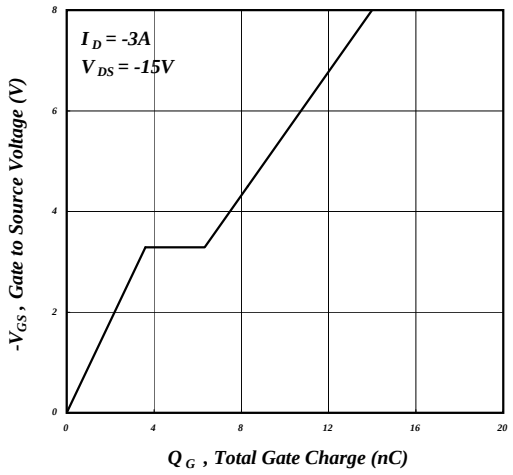


Fig 7. Gate Charge Characteristics

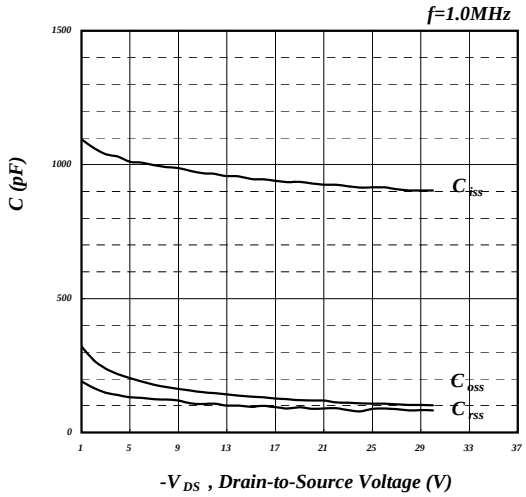


Fig 8. Typical Capacitance Characteristics

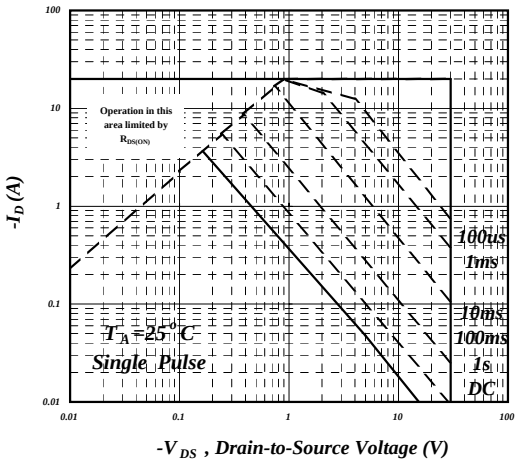


Fig 9. Maximum Safe Operating Area

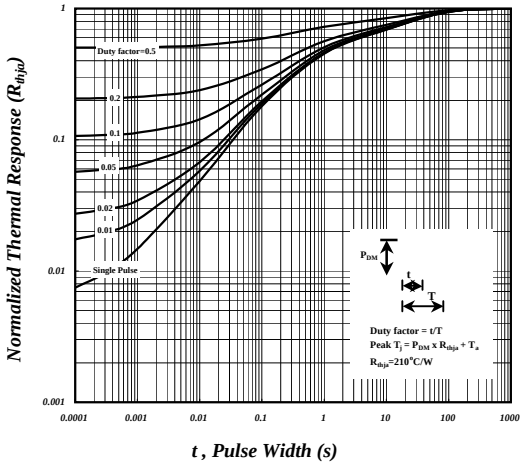


Fig 10. Effective Transient Thermal Impedance

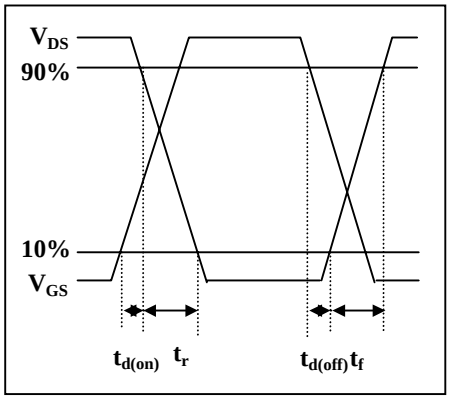


Fig 11. Switching Time Waveform

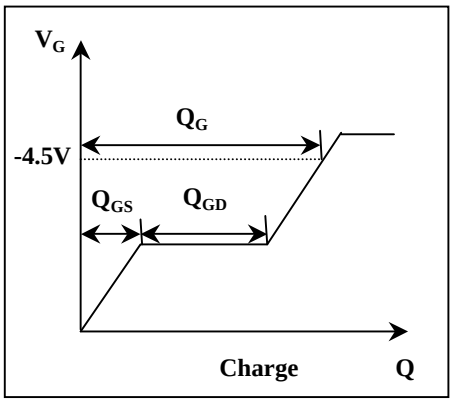


Fig 12. Gate Charge Waveform

P-Channel

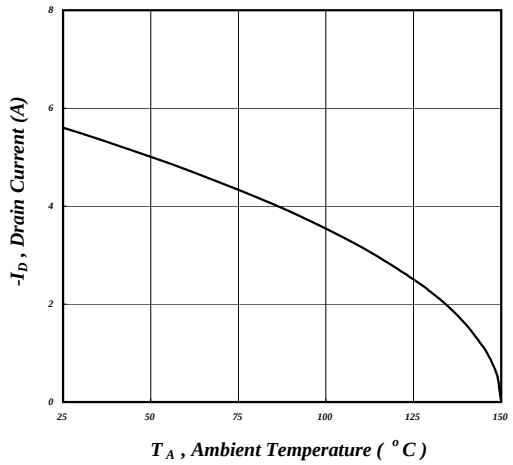


Fig 13. Drain Current v.s. Ambient Temperature

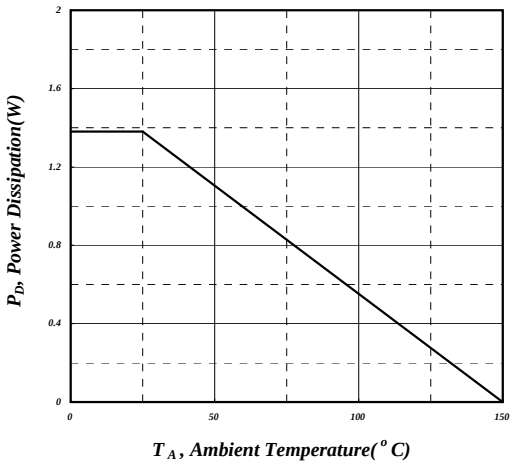
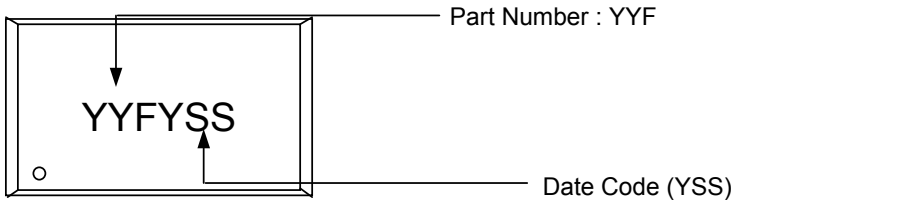
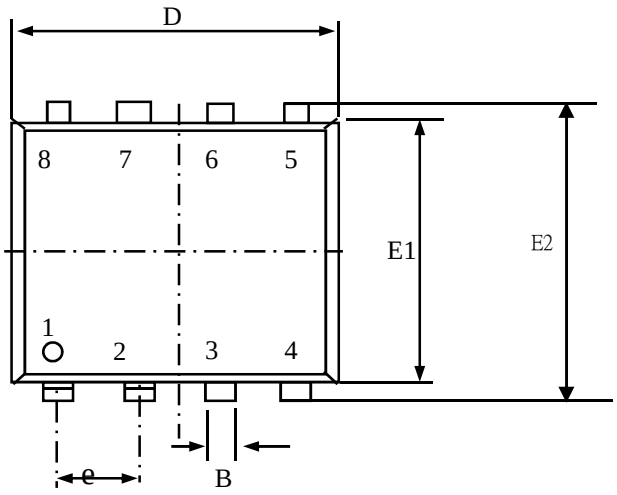


Fig 14. Total Power Dissipation

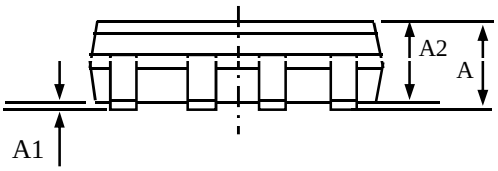
MARKING INFORMATION

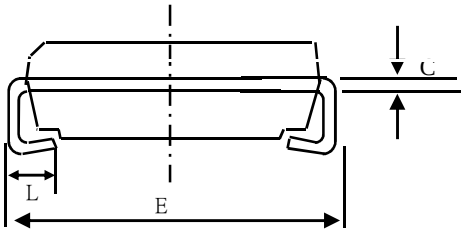


Package Outline : 2928-8



SYMBOLS	Millimeters		
	MIN	NOM	MAX
E	2.50	----	3.00
E1	2.30	2.40	2.50
E2	2.65	2.85	3.05
L	0.30	0.45	0.60
A	0.93	---	1.10
A1	0.01	---	0.10
A2	0.92	---	1.00
D	2.95	3.05	3.10
B	0.25	0.32	0.40
C	0.10	0.15	0.20
e	0.65BSC		





Note: 1.All Dimensions Are in Millimeters.

2.Package Body Sizes Exclude Mold Flash, Protrusion or Gate Burrs.
Mold Flash, Protrusion or Gate Burrs Shall Not Exceed 0.10mm Per Side.

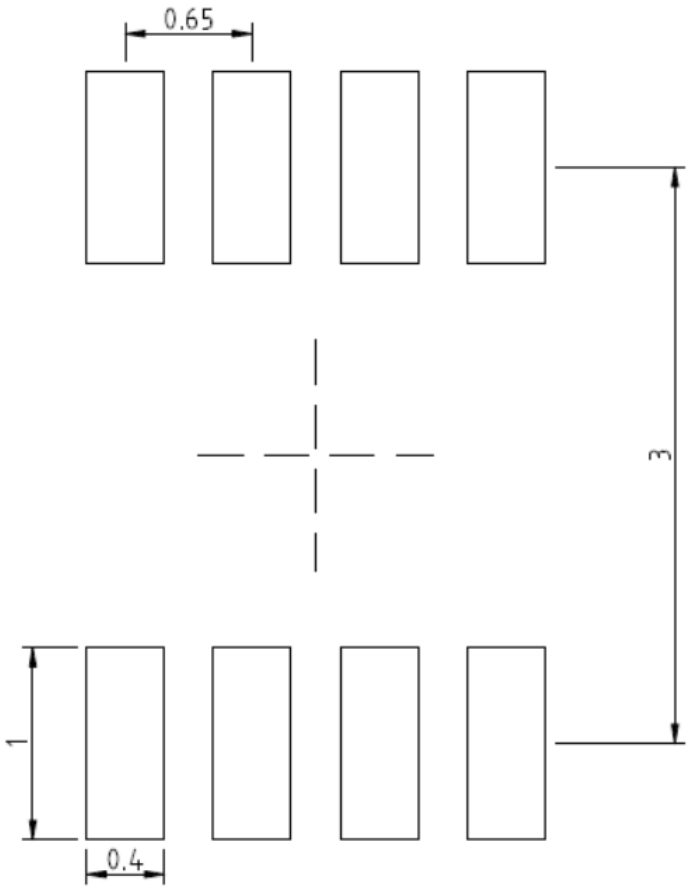
3.Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.

4.The Package Top May Be Smaller Than The Package Bottom.

5. Dimension"b" Does Not Include Dambar Protrusion. Allowable Damber Protrusion Shall Be 0.08mm Total In Excess Of "b" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.

Draw No. M1-Y8-G-v02

2928-8 FOOTPRINT：



UNIT: mm