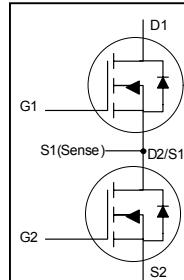


- ▼ Simple Drive Requirement
- ▼ Buck-boost in Computing
- ▼ RoHS Compliant & Halogen-Free

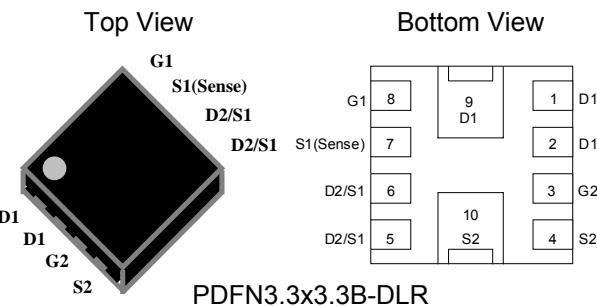


CH-1	BV_{DSS}	30V
	$R_{DS(ON)}$	3.7mΩ
CH-2	BV_{DSS}	30V
	$R_{DS(ON)}$	4.7mΩ

Description

XP3840 series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PDFN3.3x3.3B-DLR package is special for buck-boost converters in computing application using bottom source technique with the backside heat sink to achieve the good thermal performance.



Absolute Maximum Ratings@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating		Units
		CH-1	CH-2	
V_{DS}	Drain-Source Voltage	30	30	V
V_{GS}	Gate-Source Voltage	± 12	± 12	V
$I_D @ T_C = 25^\circ\text{C}$	Drain Current (Package Limited)	50	50	A
$I_D @ T_C = 100^\circ\text{C}$	Drain Current	48.6	40.4	A
$I_D @ T_A = 25^\circ\text{C}$	Drain Current, $V_{GS} @ 10\text{V}^3$	25	20.7	A
$I_D @ T_A = 70^\circ\text{C}$	Drain Current, $V_{GS} @ 10\text{V}^3$	20	16.6	A
I_{DM}	Pulsed Drain Current ¹	110	88	A
$P_D @ T_C = 25^\circ\text{C}$	Total Power Dissipation	32.8	29.7	W
$P_D @ T_A = 25^\circ\text{C}$	Total Power Dissipation ³	3.47	3.12	W
E_{AS}	Single Pulse Avalanche Energy ⁶	12.5	8	mJ
I_{AS}	Avalanche Current	50	40	A
T_{STG}	Storage Temperature Range	-55 to 150		°C
T_J	Operating Junction Temperature Range	-55 to 150		°C

Thermal Data

Symbol	Parameter	Rating		Units
		CH-1	CH-2	
R_{thj-c}	Maximum Thermal Resistance, Junction-case	3.8	4.2	°C/W
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	36	40	°C/W
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient ⁴	70	75	°C/W

CH-1 Electrical Characteristics@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	30	-	-	V
$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=20\text{A}$	-	-	3.7	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=20\text{A}$	-	-	4.7	$\text{m}\Omega$
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1.1	-	1.9	V
g_{fs}	Forward Transconductance	$V_{\text{DS}}=5\text{V}, I_{\text{D}}=20\text{A}$	-	105	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=24\text{V}, V_{\text{GS}}=0\text{V}$	-	-	10	uA
I_{GSS}	Gate-Source Leakage	$V_{\text{GS}}=\pm 12\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 0.1	uA
$Q_g @ V_{\text{GS}}=10\text{V}$	Total Gate Charge ⁵	$I_{\text{D}}=20\text{A}$ $V_{\text{DS}}=15\text{V}$	-	38	49.4	nC
$Q_g @ V_{\text{GS}}=4.5\text{V}$	Total Gate Charge ⁵		-	18	23.4	nC
Q_{gs}	Gate-Source Charge ⁵		-	5.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge ⁵		-	6	-	nC
$t_{\text{d}(\text{on})}$	Turn-on Delay Time ⁵	$V_{\text{DS}}=15\text{V}$ $I_{\text{D}}=20\text{A}$ $R_{\text{G}}=3\Omega$ $V_{\text{GS}}=10\text{V}$	-	8	-	ns
t_r	Rise Time ⁵		-	47	-	ns
$t_{\text{d}(\text{off})}$	Turn-off Delay Time ⁵		-	28	-	ns
t_f	Fall Time ⁵		-	4	-	ns
C_{iss}	Input Capacitance ⁵	$V_{\text{GS}}=0\text{V}$ $V_{\text{DS}}=25\text{V}$	-	1800	2340	pF
C_{oss}	Output Capacitance ⁵		-	355	-	pF
C_{rss}	Reverse Transfer Capacitance ⁵		-	40	-	pF
R_g	Gate Resistance	f=1.0MHz	-	1	2	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_{\text{S}}=20\text{A}, V_{\text{GS}}=0\text{V}$	-	-	1.2	V
t_{rr}	Reverse Recovery Time ⁵	$I_{\text{S}}=20\text{A}, V_{\text{GS}}=0\text{V},$ $dI/dt=100\text{A}/\mu\text{s}$	-	23	-	ns
Q_{rr}	Reverse Recovery Charge ⁵		-	13	-	nC

CH-2 Electrical Characteristics@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_{\text{D}}=250\mu\text{A}$	30	-	-	V
$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=10\text{V}$, $I_{\text{D}}=20\text{A}$	-	-	4.7	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}$, $I_{\text{D}}=20\text{A}$	-	-	5.9	$\text{m}\Omega$
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}$, $I_{\text{D}}=250\mu\text{A}$	1.1	-	1.9	V
g_{fs}	Forward Transconductance	$V_{\text{DS}}=5\text{V}$, $I_{\text{D}}=20\text{A}$	-	100	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=24\text{V}$, $V_{\text{GS}}=0\text{V}$	-	-	10	μA
I_{GSS}	Gate-Source Leakage	$V_{\text{GS}}=\pm 12\text{V}$, $V_{\text{DS}}=0\text{V}$	-	-	± 0.1	μA
$Q_g @ V_{\text{GS}}=10\text{V}$	Total Gate Charge ⁵	$I_{\text{D}}=20\text{A}$	-	34	44.2	nC
$Q_g @ V_{\text{GS}}=4.5\text{V}$	Total Gate Charge ⁵	$V_{\text{DS}}=15\text{V}$	-	16	20.8	nC
Q_{gs}	Gate-Source Charge ⁵		-	5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge ⁵		-	5	-	nC
$t_{\text{d}(\text{on})}$	Turn-on Delay Time ⁵	$V_{\text{DS}}=15\text{V}$	-	8	-	ns
t_r	Rise Time ⁵		-	51	-	ns
$t_{\text{d}(\text{off})}$	Turn-off Delay Time ⁵	$R_{\text{G}}=3\Omega$	-	28	-	ns
t_f	Fall Time ⁵		-	5	-	ns
C_{iss}	Input Capacitance ⁵	$V_{\text{GS}}=0\text{V}$	-	1600	2080	pF
C_{oss}	Output Capacitance ⁵		-	275	-	pF
C_{rss}	Reverse Transfer Capacitance ⁵	$f=1.0\text{MHz}$	-	30	-	pF
R_g	Gate Resistance		-	1.8	3.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_{\text{S}}=20\text{A}$, $V_{\text{GS}}=0\text{V}$	-	-	1.2	V
t_{rr}	Reverse Recovery Time ⁵	$I_{\text{S}}=20\text{A}$, $V_{\text{GS}}=0\text{V}$,	-	21	-	ns
Q_{rr}	Reverse Recovery Charge ⁵	$dI/dt=100\text{A}/\mu\text{s}$	-	9	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board, t \leq 10sec.
- 4.Surface mounted on min. copper pad of FR4 board, on steady-state
- 5.Guaranteed by design.
- 6.Starting $T_j=25^\circ\text{C}$, $V_{\text{DD}}=30\text{V}$, $L=0.01\text{mH}$, $R_{\text{G}}=25\Omega$, $V_{\text{GS}}=10\text{V}$
- 7.These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{\text{J}(\text{MAX})}=150^\circ\text{C}$.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT, AUTOMOTIVE OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

XSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

Channel-1

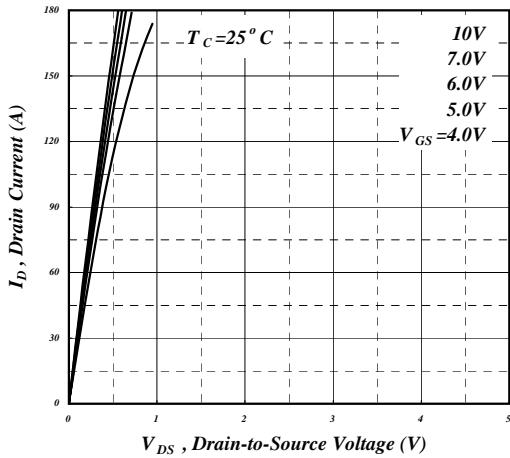


Fig 1. Typical Output Characteristics

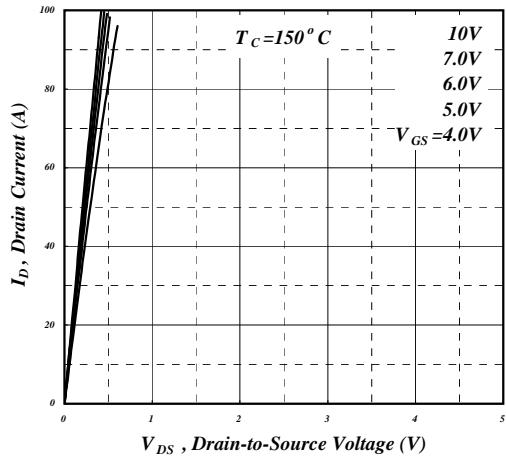


Fig 2. Typical Output Characteristics

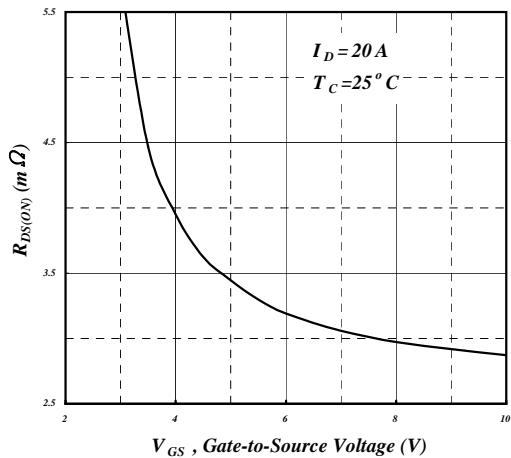


Fig 3. On-Resistance v.s. Gate Voltage

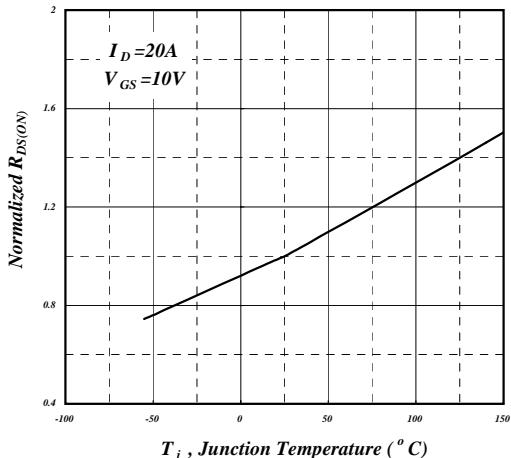


Fig 4. Normalized On-Resistance v.s. Junction Temperature

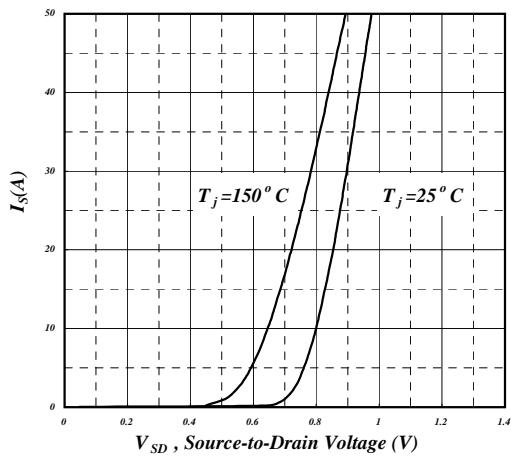


Fig 5. Forward Characteristic of Reverse Diode

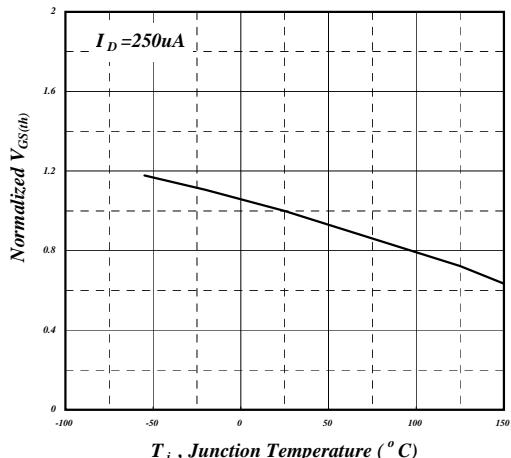


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

Channel-1

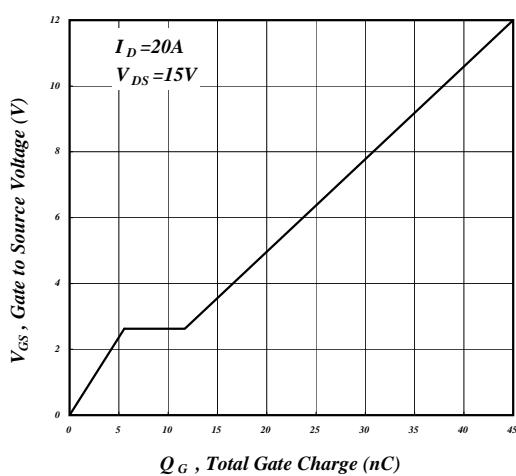


Fig 7. Gate Charge Characteristics

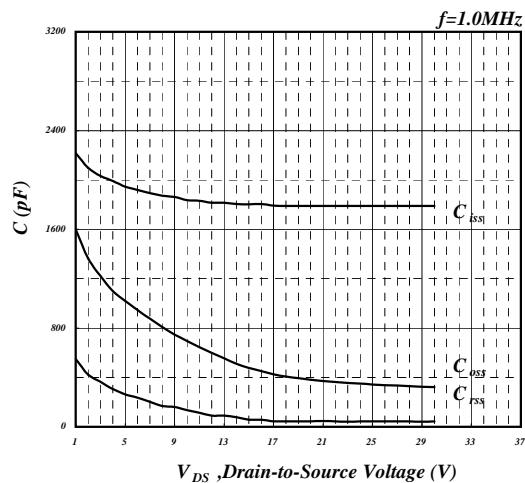


Fig 8. Typical Capacitance Characteristics

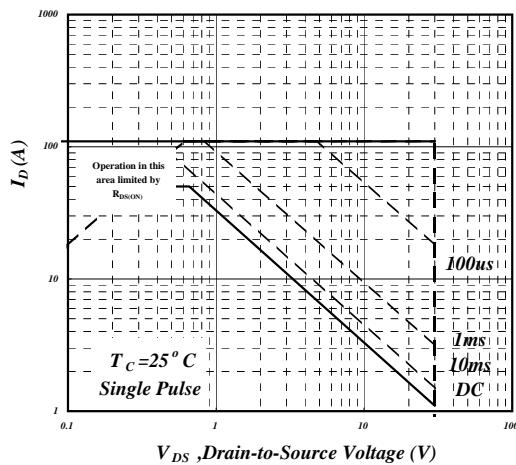


Fig 9. Maximum Safe Operating Area⁷

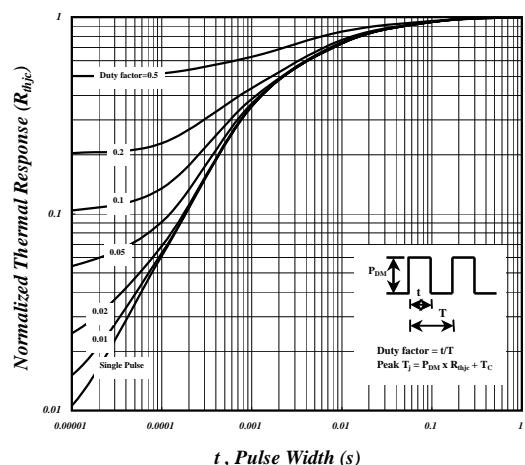


Fig 10. Effective Transient Thermal Impedance

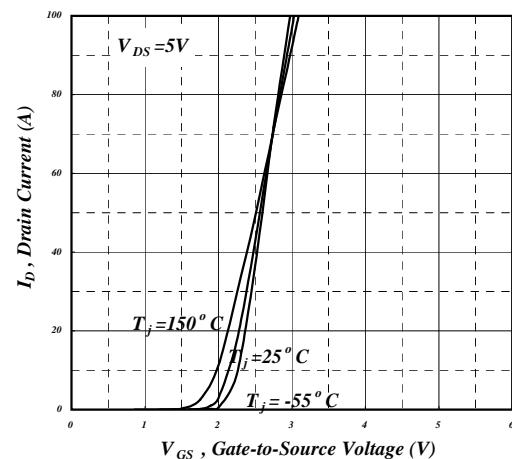


Fig 11. Transfer Characteristics

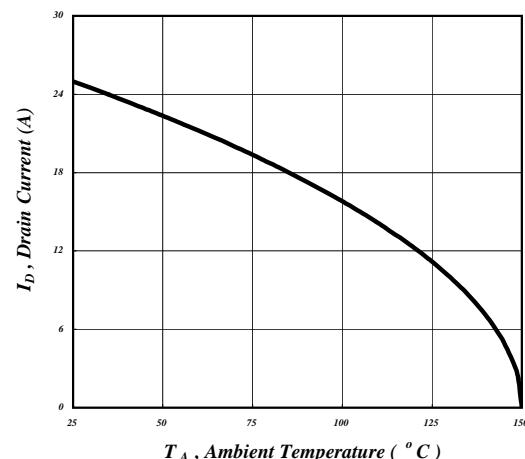


Fig 12. Drain Current v.s. Ambient Temperature

Channel-1

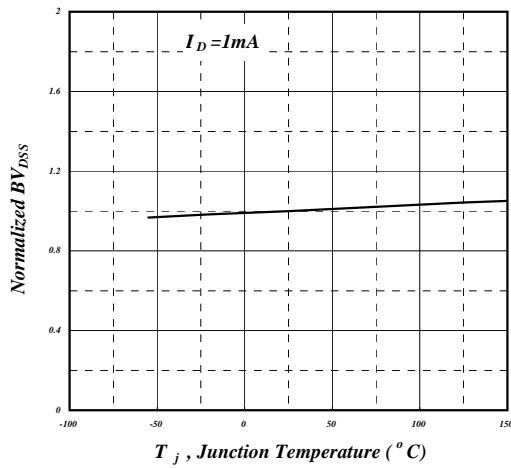


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

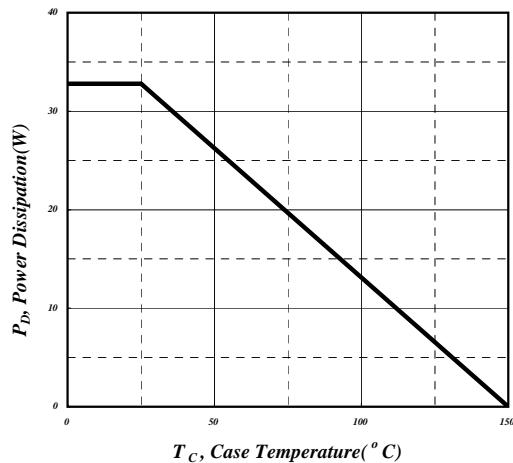


Fig 14. Total Power Dissipation

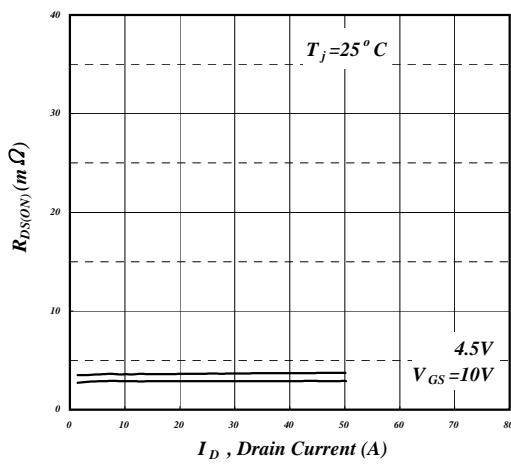


Fig 15. Typ. Drain-Source on State Resistance

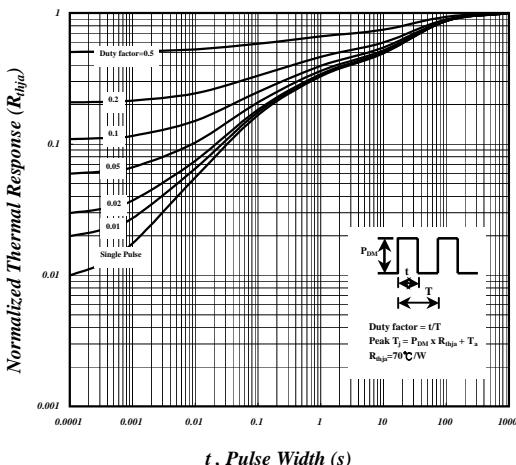


Fig 16. Effective Transient Thermal Impedance

Channel-2

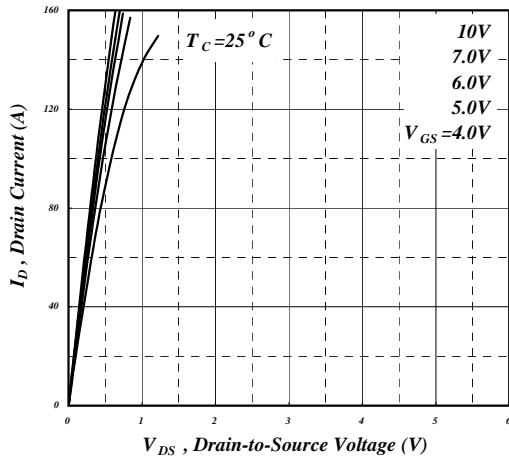


Fig 1. Typical Output Characteristics

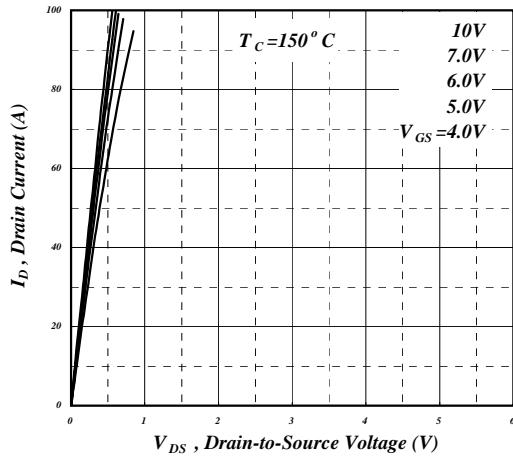


Fig 2. Typical Output Characteristics

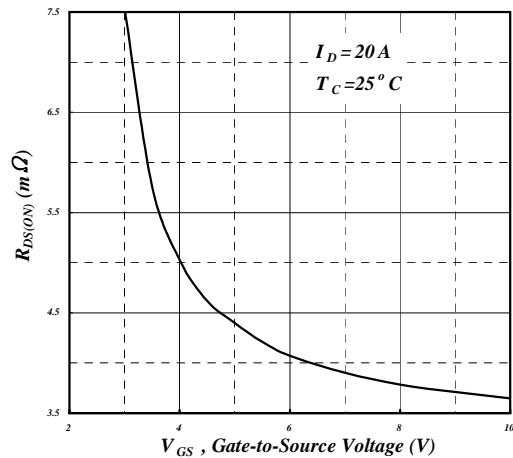


Fig 3. On-Resistance v.s. Gate Voltage

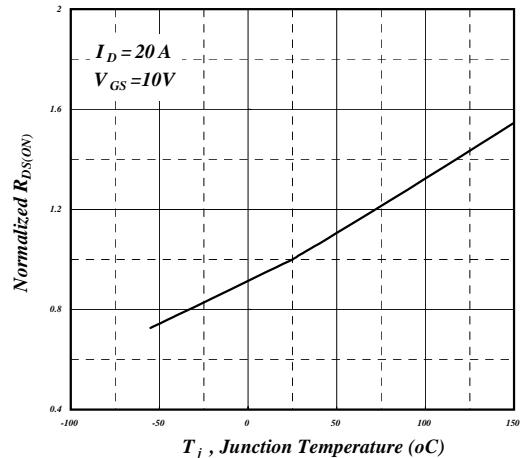


Fig 4. Normalized On-Resistance v.s. Junction Temperature

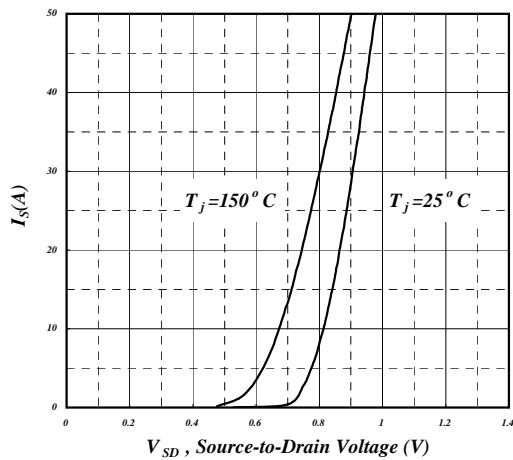


Fig 5. Forward Characteristic of Reverse Diode

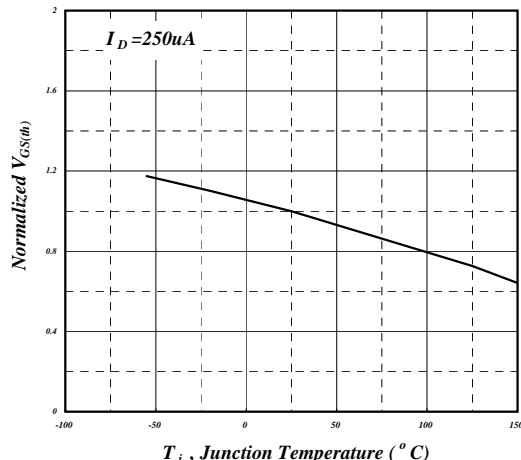


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

Channel-2

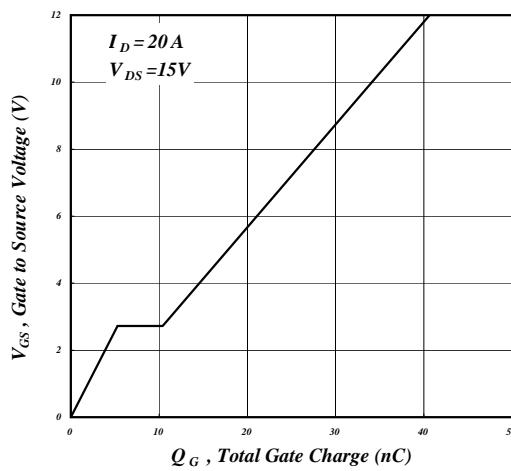


Fig 7. Gate Charge Characteristics

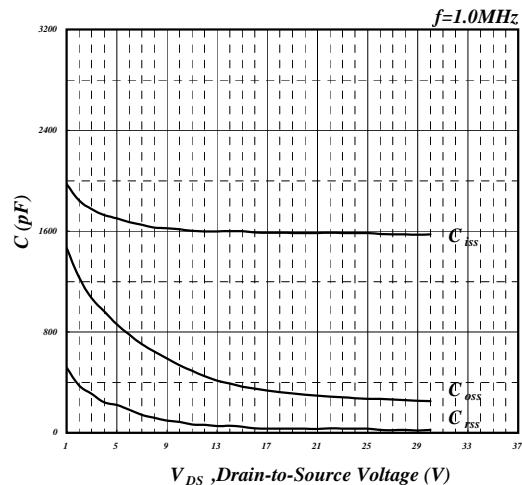


Fig 8. Typical Capacitance Characteristics

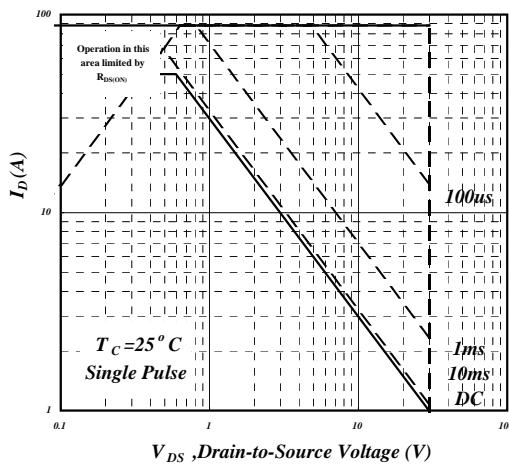


Fig 9. Maximum Safe Operating Area⁷

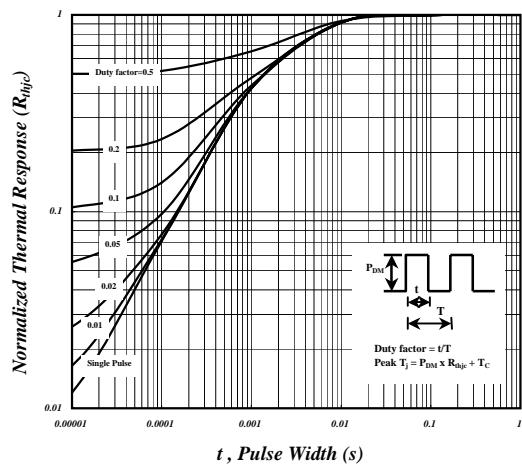


Fig 10. Effective Transient Thermal Impedance

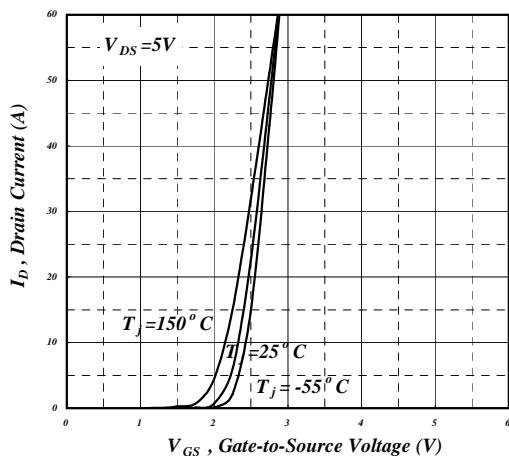


Fig 11. Transfer Characteristics

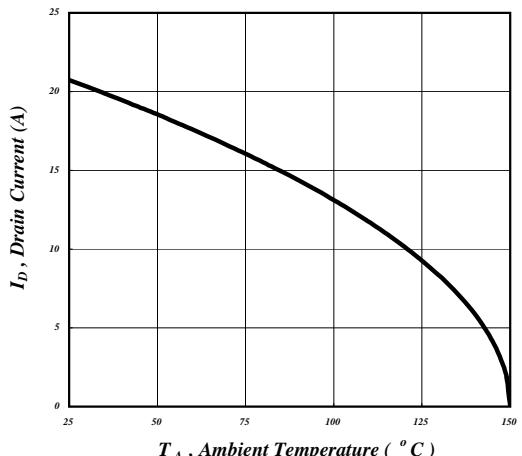


Fig 12. Drain Current v.s. Ambient Temperature

Channel-2

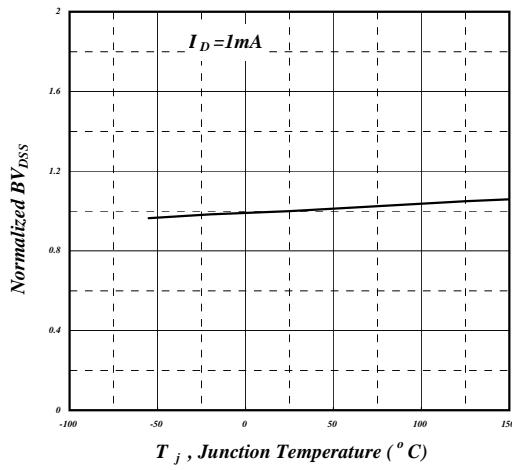


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

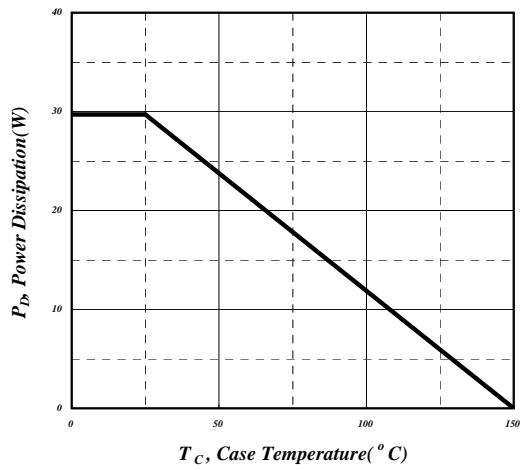


Fig 14. Total Power Dissipation

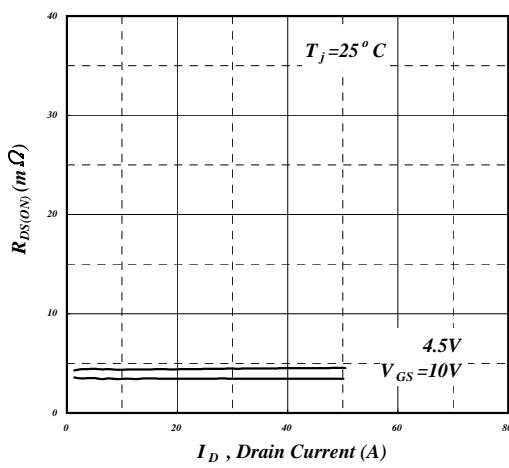


Fig 15. Typ. Drain-Source on State Resistance

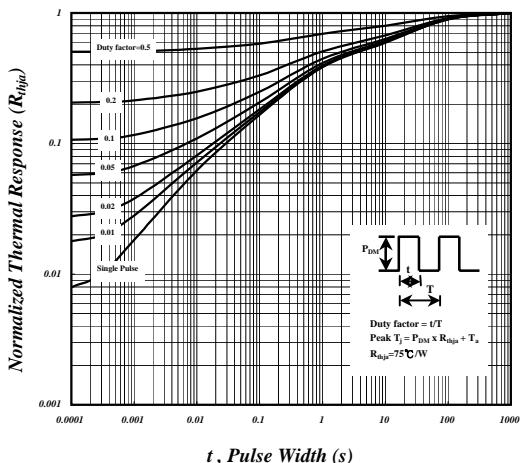
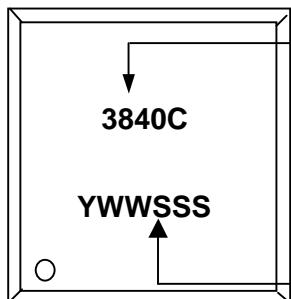


Fig 16. Effective Transient Thermal Impedance

MARKING INFORMATION

Part Number

Date Code (YWWSSS)

Y : Last Digit Of The Year

WW : Week

SSS : Sequence

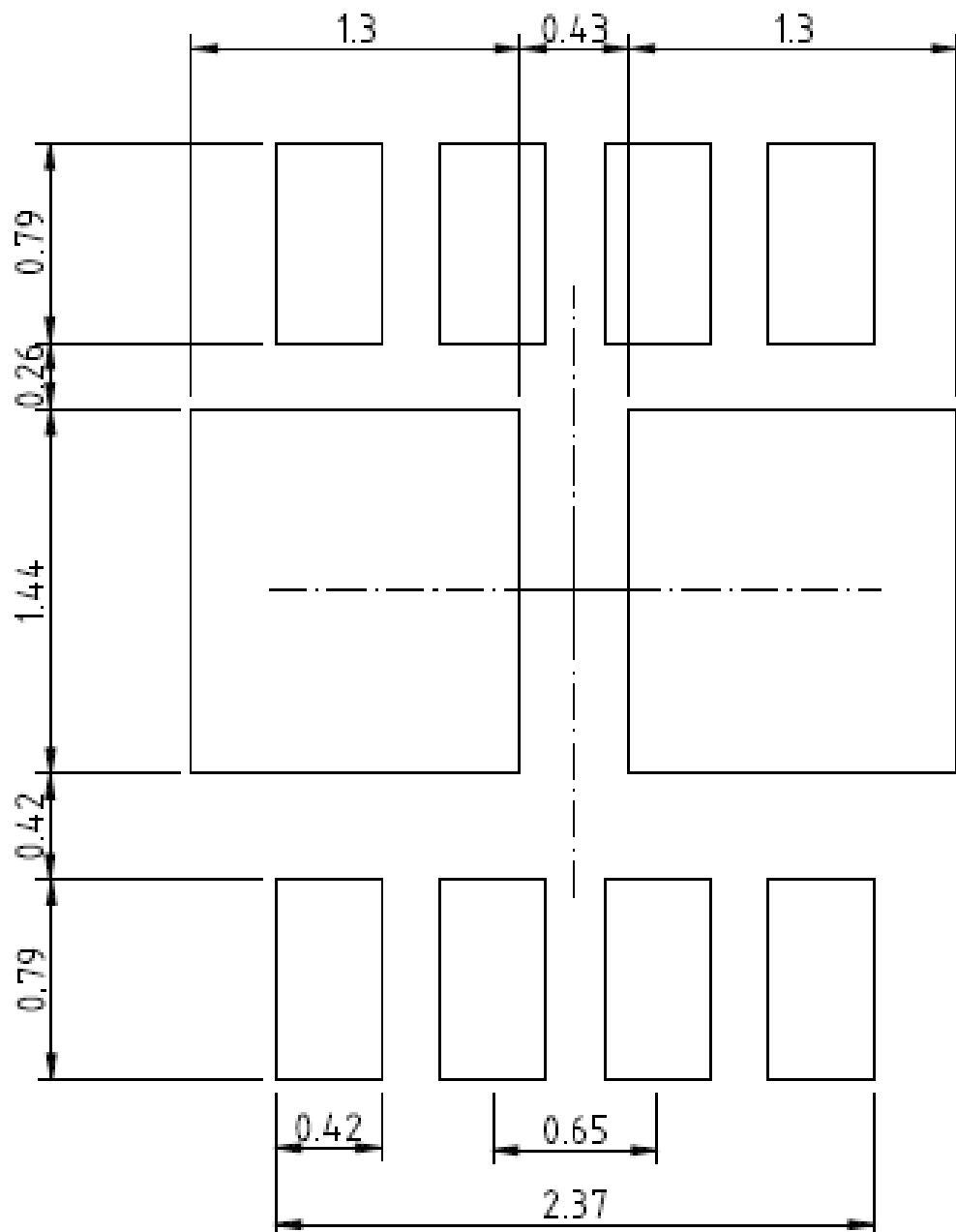
Package Outline : PDFN 3.3x3.3B-DLR

SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.65	0.75	0.85
A1	0.00	0.02	0.05
b	0.27	0.32	0.37
b1	0.15	0.20	0.25
c	0.203 BSC		
D	3.20	3.30	3.40
D1	2.80	2.90	3.00
D2	1.09	1.19	1.29
D3	1.09	1.19	1.29
E	3.20	3.30	3.40
E1	1.24	1.34	1.44
e	0.65 BSC		
L	0.44	0.54	0.64
K1	0.42	0.52	0.62
K2	0.26	0.36	0.46
K3	0.43	0.53	0.63

BOTTOM VIEW

1. All dimension are in millimeters.
 2. Dimension does not include burrs and mold flash/protrusions.
 3. The outline schematic is not to scale and slightly different from the actual product appearance.

Draw No. M2-DT33(B-DLR)-8-E-G-v01

PDFN 3.3 x 3.3B-DLR FOOTPRINT :

UNIT: mm