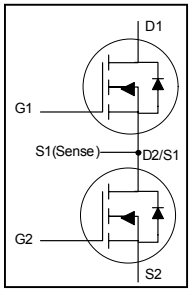
XP3838CDT33

Halogen-Free Product

DUAL N-CHANNEL ENHANCEMENT MODE POWER MOSFET

- **Simple Drive Requirement**
- **Buck-boost in Computing**
- **RoHS Compliant & Halogen-Free**



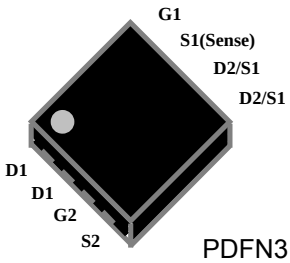
CH-1	BV_{DSS}	30V
	$R_{DS(ON)}$	4.2mΩ
CH-2	BV_{DSS}	30V
	$R_{DS(ON)}$	5.2mΩ

Description

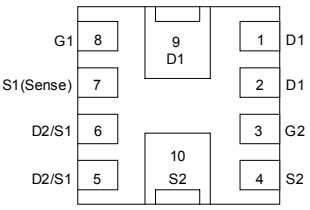
XP3838 series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PDFN3.3x3.3B-DLR package is special for buck-boost conveters in computing application using bottom source technique with the backside heat sink to achieve the good thermal performance.

Top View



Bottom View



PDFN3.3x3.3B-DLR

Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating		Units
		CH-1	CH-2	
V_{DS}	Drain-Source Voltage	30	30	V
V_{GS}	Gate-Source Voltage	±12	±12	V
I_D@T_C=25℃	Drain Current (Package Limited)	50	50	A
I_D@T_C=100℃	Drain Current	45	39	A
I_D@T_A=25℃	Drain Current, V_{GS} @ 10V[3]	23.5	19.5	A
I_D@T_A=70℃	Drain Current, V_{GS} @ 10V[3]	18.8	15.6	A
I_{DM}	Pulsed Drain Current[1]	110	88	A
P_D@T_C=25℃	Total Power Dissipation	32.8	29.7	W
P_D@T_A=25℃	Total Power Dissipation[3]	3.47	3.12	W
E_{AS}	Single Pulse Avalanche Energy[6]	18	12.5	mJ
I_{AS}	Avalanche Current	60	50	A
T_{STG}	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃

Thermal Data

Symbol	Parameter	Rating		Units
		CH-1	CH-2	
Rthj-c	Maximum Thermal Resistance, Junction-case	3.8	4.2	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	36	40	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[4]	70	75	℃/W

CH-1 Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=20A	-	-	4.2	mΩ
		V_{GS}=4.5V, I_D=12A	-	-	5.9	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1.1	-	1.9	V
g_{fs}	Forward Transconductance	V_{DS}=5V, I_D=20A	-	65	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V, V_{GS}=0V	-	-	10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±12V, V_{DS}=0V	-	-	±0.1	uA
Q_g@V_{GS}=10V	Total Gate Charge[5]	I_D=20A	-	25	32.5	nC
Q_g@V_{GS}=4.5V	Total Gate Charge[5]	V_{DS}=15V	-	12	15.6	nC
Q_{gs}	Gate-Source Charge[5]		-	4	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge[5]		-	5.5	-	nC
$t_{d(on)}$	Turn-on Delay Time[5]	V_{DS}=15V	-	7	-	ns
t_r	Rise Time[5]	I_D=20A	-	55	-	ns
$t_{d(off)}$	Turn-off Delay Time[5]	R_G=3Ω	-	21	-	ns
t_f	Fall Time[5]	V_{GS}=10V	-	4	-	ns
C_{iss}	Input Capacitance[5]	V_{GS}=0V	-	1150	1500	pF
C_{oss}	Output Capacitance[5]	V_{DS}=25V	-	320	-	pF
C_{rss}	Reverse Transfer Capacitance[5]	f=1.0MHz	-	40	-	pF
R_g	Gate Resistance	f=1.0MHz	-	1	2	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=20A, V_{GS}=0V	-	-	1.2	V
t_{rr}	Reverse Recovery Time[5]	I_S=20A, V_{GS}=0V,	-	23	-	ns
Q_{rr}	Reverse Recovery Charge[5]	dI/dt=100A/μs	-	13	-	nC

CH-2 Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=18A	-	-	5.2	mΩ
		V_{GS}=4.5V, I_D=12A	-	-	7.2	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1.1	-	1.9	V
g_{fs}	Forward Transconductance	V_{DS}=5V, I_D=18A	-	60	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V, V_{GS}=0V	-	-	10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±12V, V_{DS}=0V	-	-	±0.1	uA
Q_g@V_{GS}=10V	Total Gate Charge[5]	I_D=18A	-	22	28.6	nC
Q_g@V_{GS}=4.5V	Total Gate Charge[5]	V_{DS}=15V	-	11	14.3	nC
Q_{gs}	Gate-Source Charge[5]		-	3.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge[5]		-	5	-	nC
$t_{d(on)}$	Turn-on Delay Time[5]	V_{DS}=15V	-	7	-	ns
t_r	Rise Time[5]	I_D=18A	-	46	-	ns
$t_{d(off)}$	Turn-off Delay Time[5]	R_G=3Ω	-	21	-	ns
t_f	Fall Time[5]	V_{GS}=10V	-	5	-	ns
C_{iss}	Input Capacitance[5]	V_{GS}=0V	-	1000	1300	pF
C_{oss}	Output Capacitance[5]	V_{DS}=25V	-	285	-	pF
C_{rss}	Reverse Transfer Capacitance[5]	f=1.0MHz	-	25	-	pF
R_g	Gate Resistance	f=1.0MHz	-	1.8	3.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=18A, V_{GS}=0V	-	-	1.2	V
t_{rr}	Reverse Recovery Time[5]	I_S=18A, V_{GS}=0V,	-	21	-	ns
Q_{rr}	Reverse Recovery Charge[5]	dI/dt=100A/μs	-	9	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board, t ≤10sec.

4.Surface mounted on min. copper pad of FR4 board, on steady-state

5.Guaranteed by design.

6.Starting T_j=25°C , V_{DD}=30V , L=0.01mH , R_G=25Ω , V_{GS}=10V

7.These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C.

Channel-1

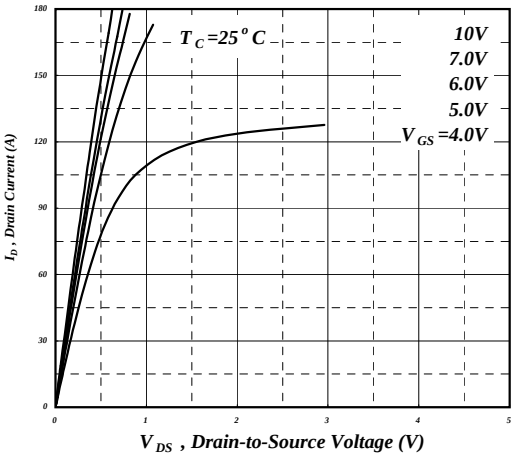


Fig 1. Typical Output Characteristics

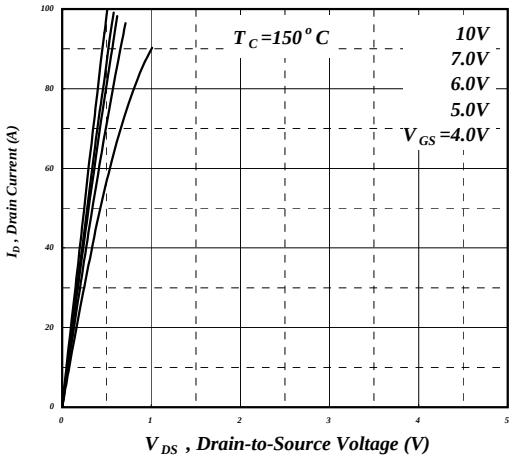


Fig 2. Typical Output Characteristics

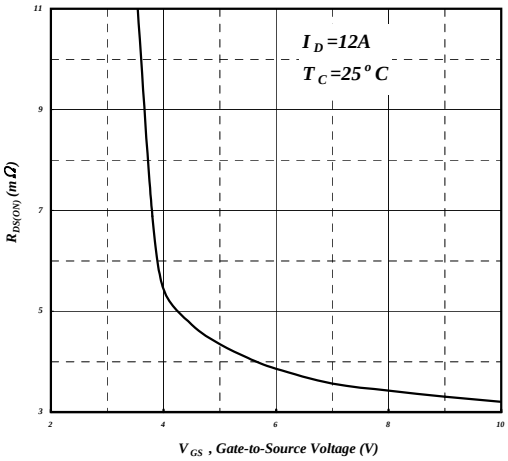


Fig 3. On-Resistance v.s. Gate Voltage

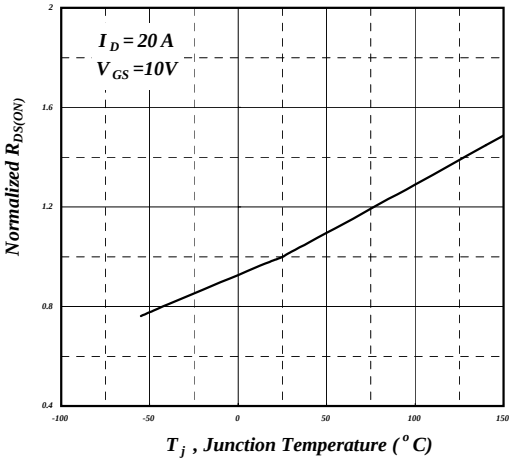


Fig 4. Normalized On-Resistance v.s. Junction Temperature

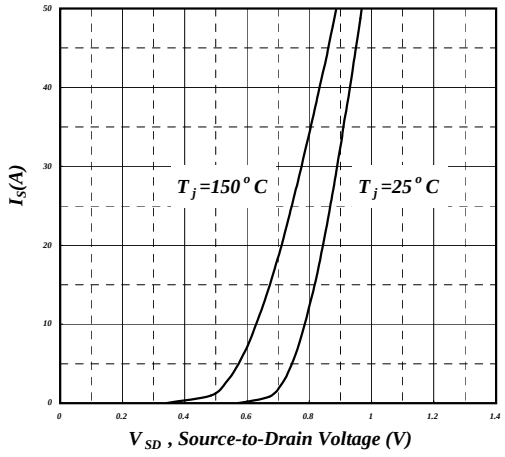


Fig 5. Forward Characteristic of Reverse Diode

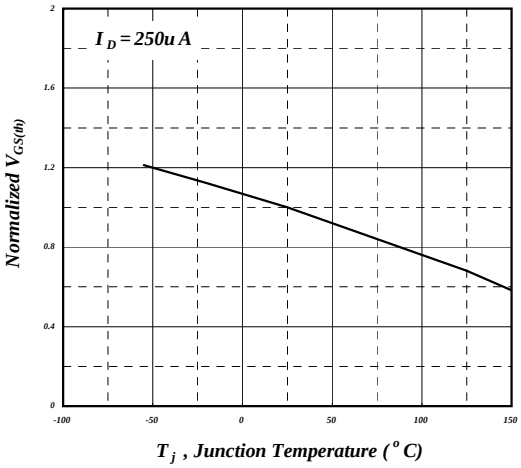


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

Channel-1

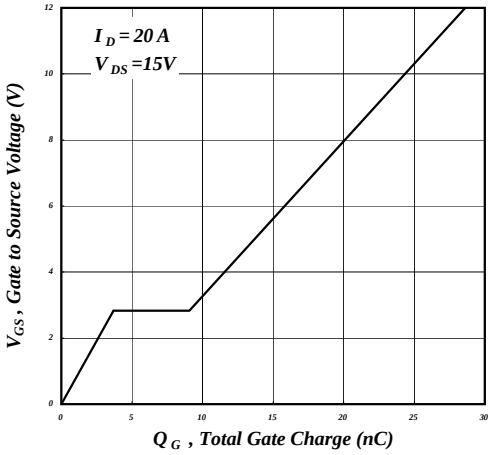


Fig 7. Gate Charge Characteristics

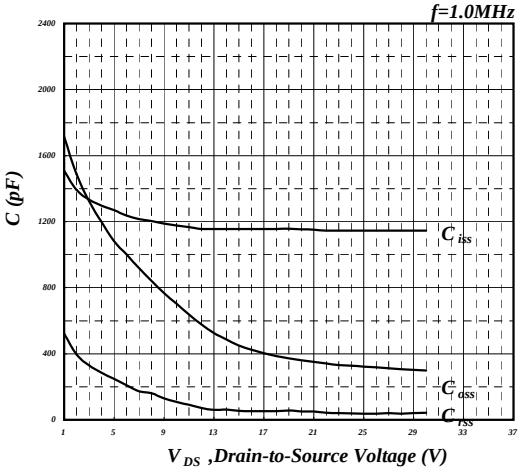


Fig 8. Typical Capacitance Characteristics

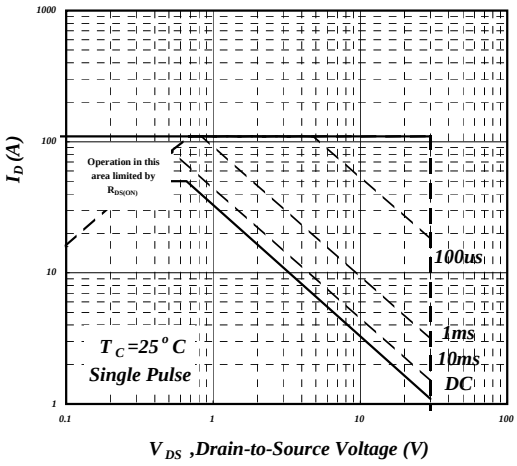


Fig 9. Maximum Safe Operating Area[7]

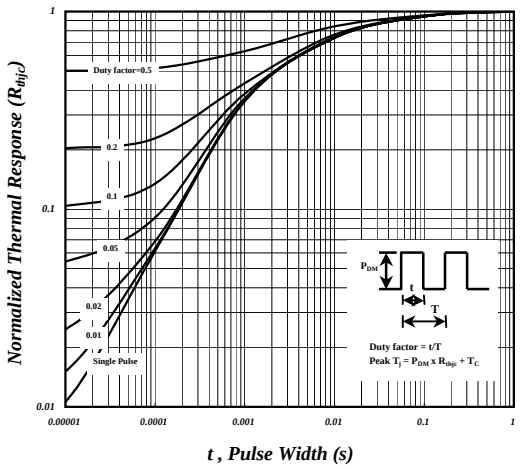


Fig 10. Effective Transient Thermal Impedance

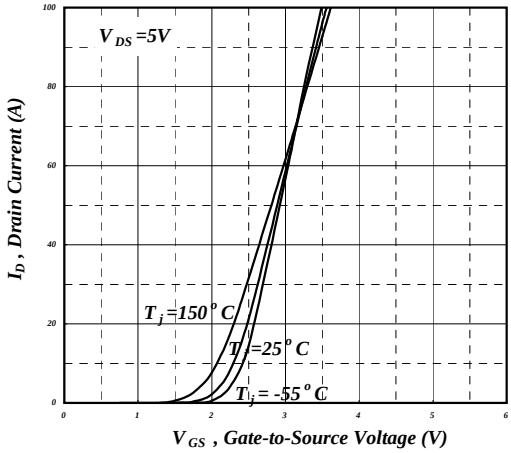


Fig 11. Transfer Characteristics

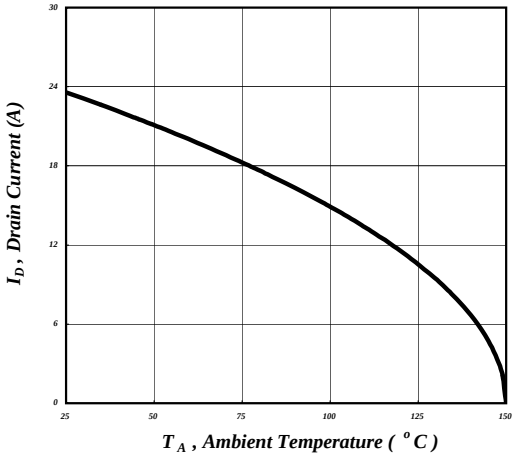


Fig 12. Drain Current v.s. Ambient Temperature

Channel-1

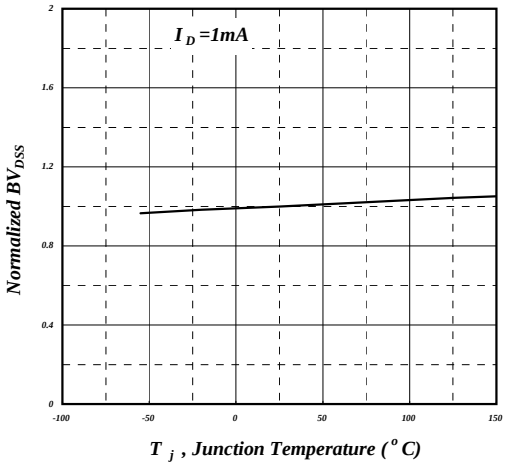


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

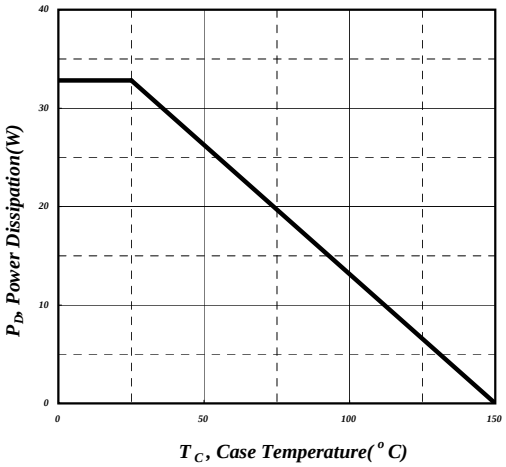


Fig 14. Total Power Dissipation

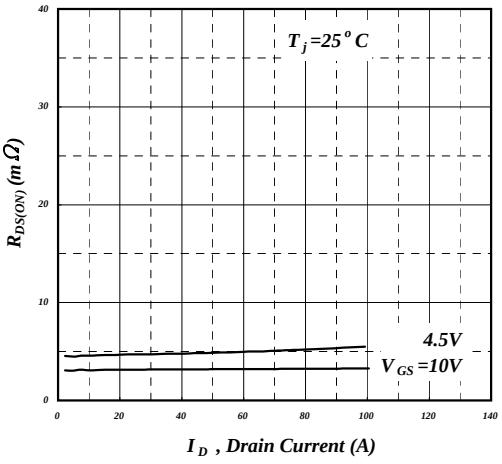


Fig 15. Typ. Drain-Source on State Resistance

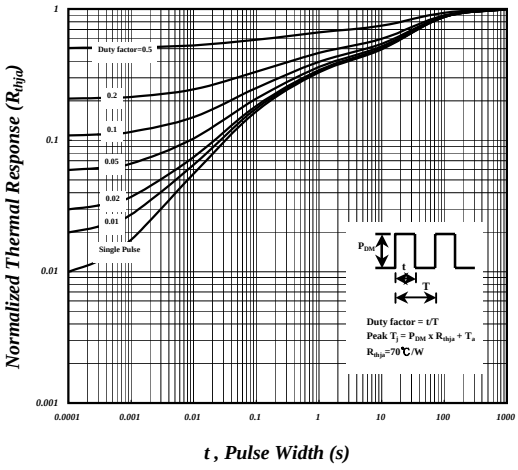


Fig 16. Effective Transient Thermal Impedance

Channel-2

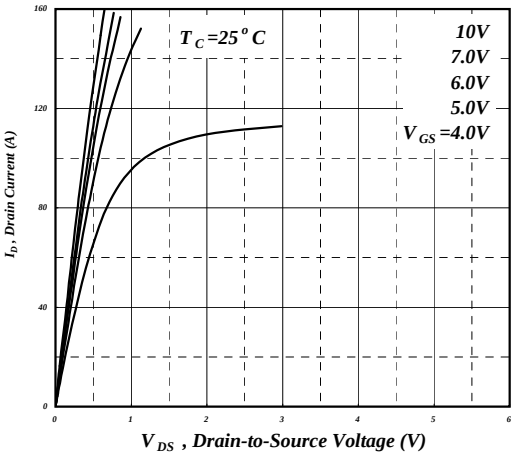


Fig 1. Typical Output Characteristics

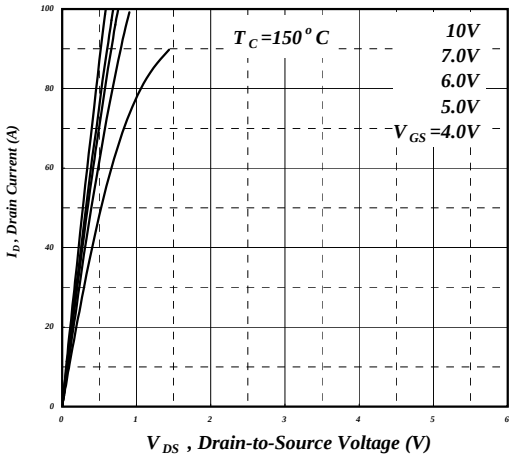


Fig 2. Typical Output Characteristics

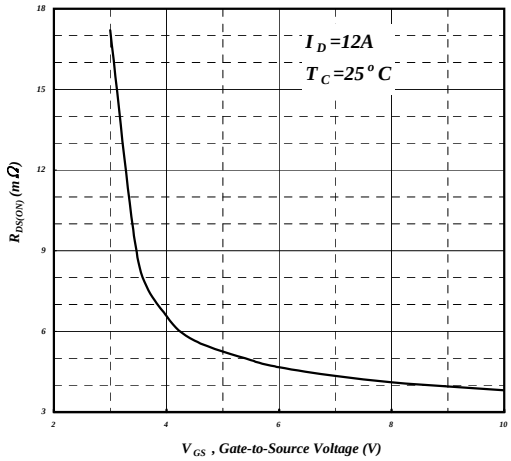


Fig 3. On-Resistance v.s. Gate Voltage

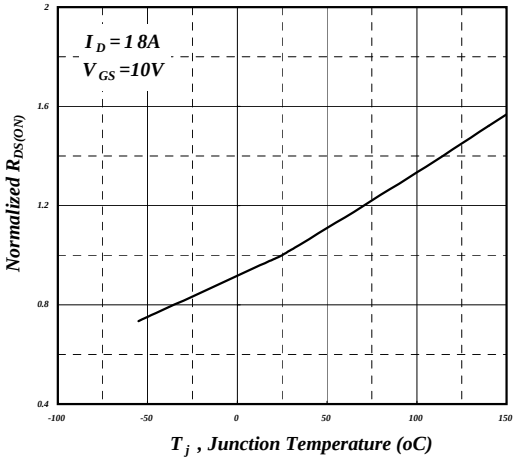


Fig 4. Normalized On-Resistance v.s. Junction Temperature

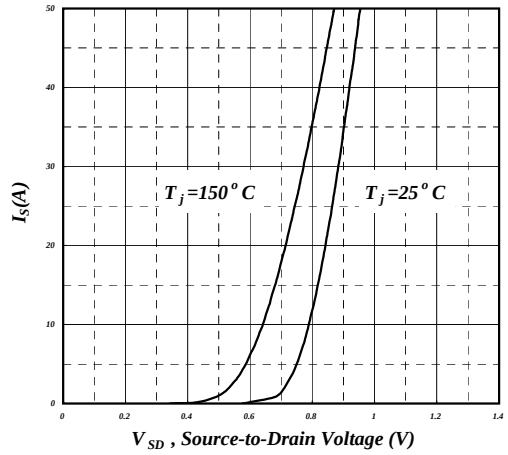


Fig 5. Forward Characteristic of Reverse Diode

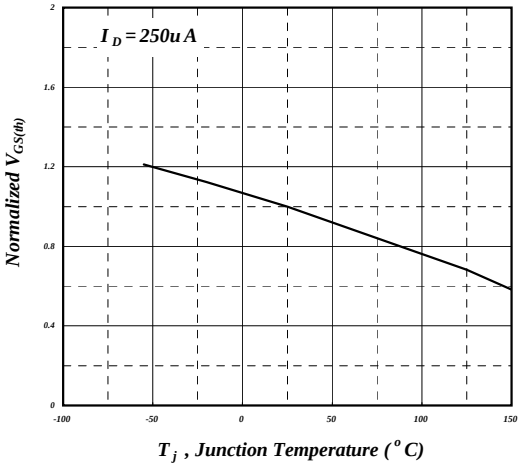


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

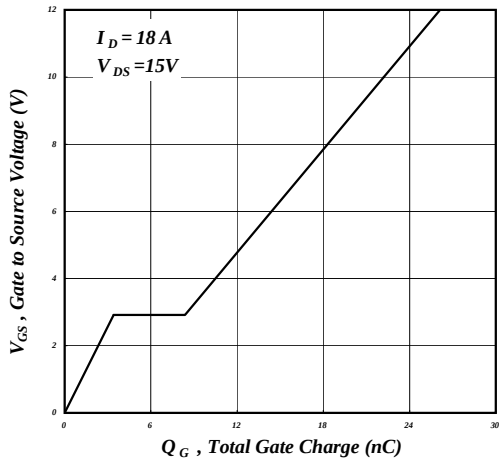


Fig 7. Gate Charge Characteristics

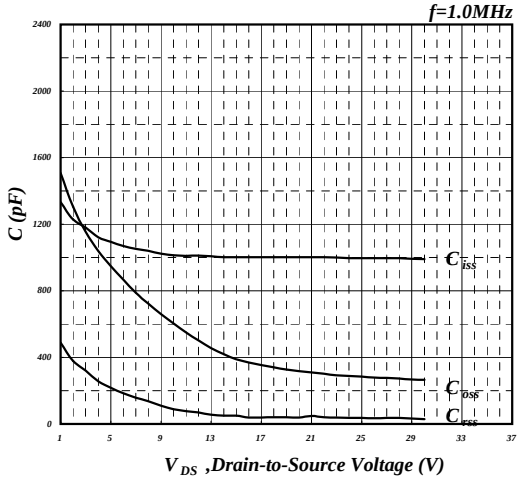


Fig 8. Typical Capacitance Characteristics

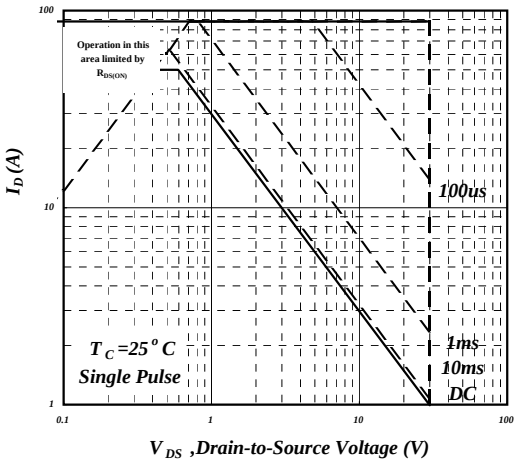


Fig 9. Maximum Safe Operating Area[7]

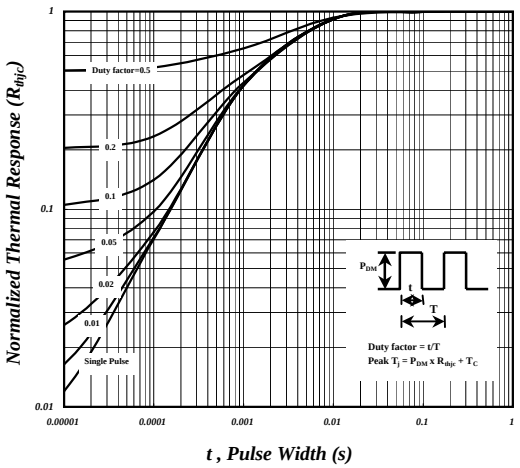


Fig 10. Effective Transient Thermal Impedance

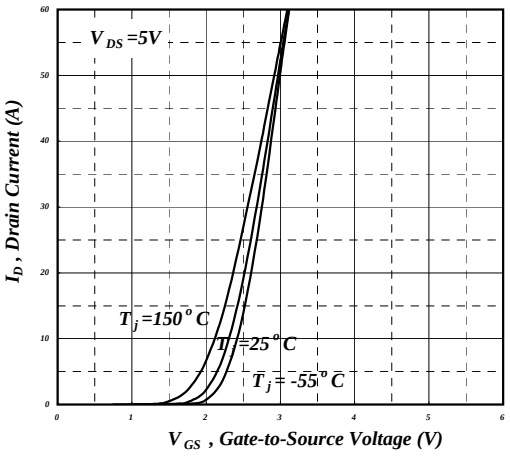


Fig 11. Transfer Characteristics

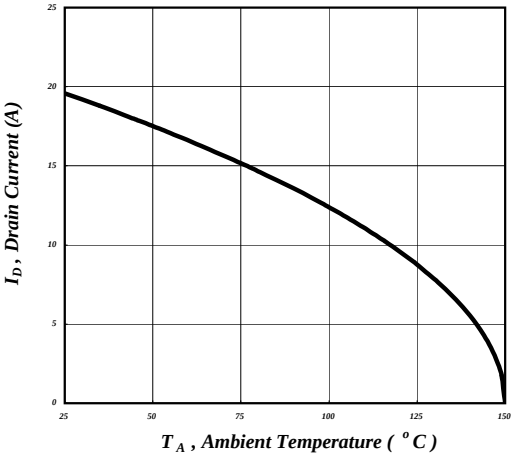


Fig 12. Drain Current v.s. Ambient Temperature

Channel-2

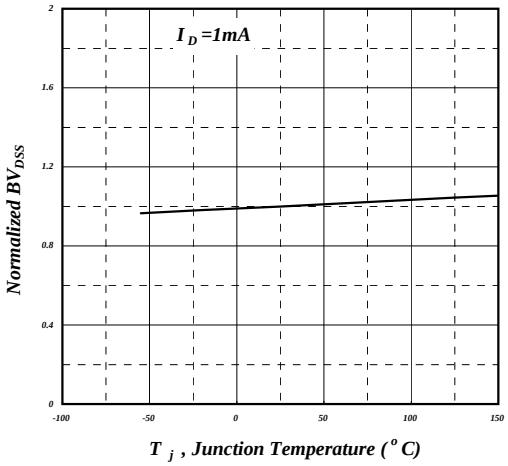


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

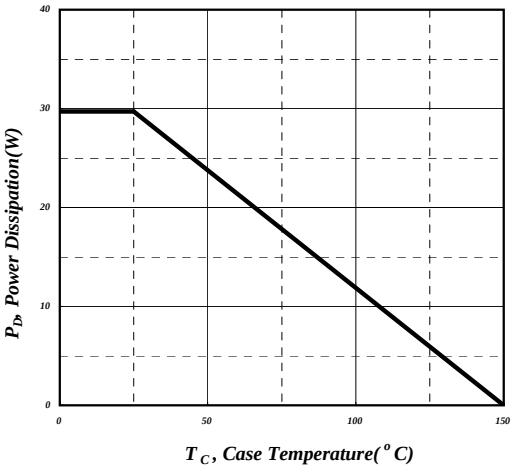


Fig 14. Total Power Dissipation

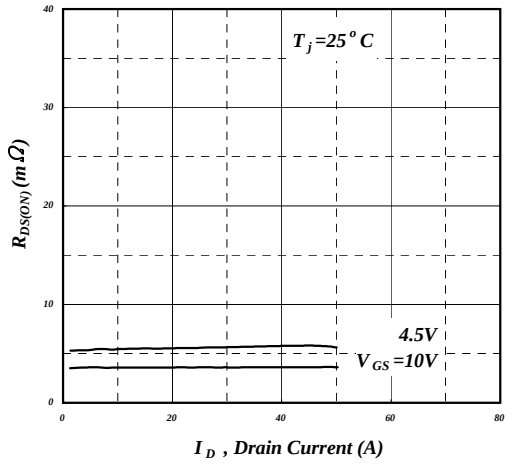


Fig 15. Typ. Drain-Source on State Resistance

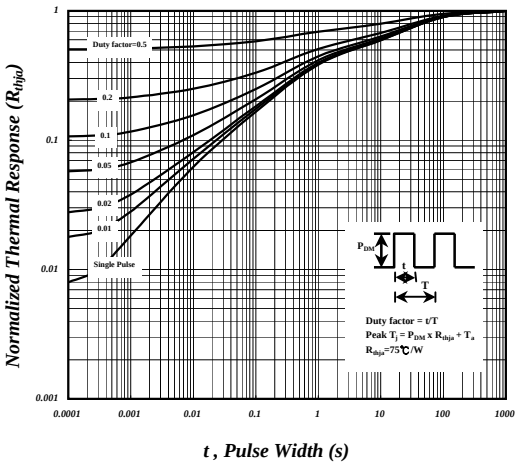
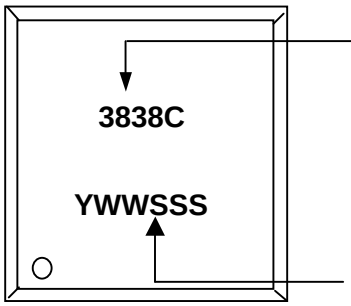
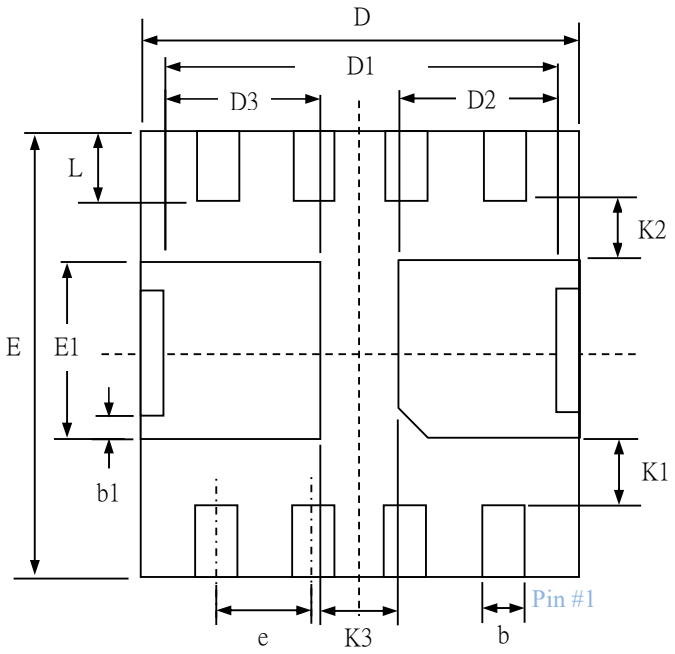


Fig 16. Effective Transient Thermal Impedance

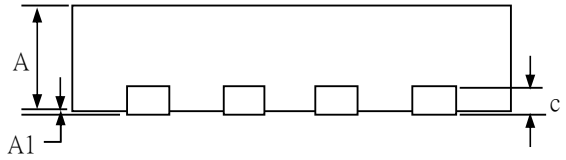
MARKING INFORMATION



Package Outline : PDFN 3.3x3.3B-DLR



BOTTOM VIEW



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.65	0.75	0.85
A1	0.00	0.02	0.05
b	0.27	0.32	0.37
b1	0.15	0.20	0.25
c	0.203 BSC		
D	3.20	3.30	3.40
D1	2.80	2.90	3.00
D2	1.09	1.19	1.29
D3	1.09	1.19	1.29
E	3.20	3.30	3.40
E1	1.24	1.34	1.44
e	0.65 BSC		
L	0.44	0.54	0.64
K1	0.42	0.52	0.62
K2	0.26	0.36	0.46
K3	0.43	0.53	0.63

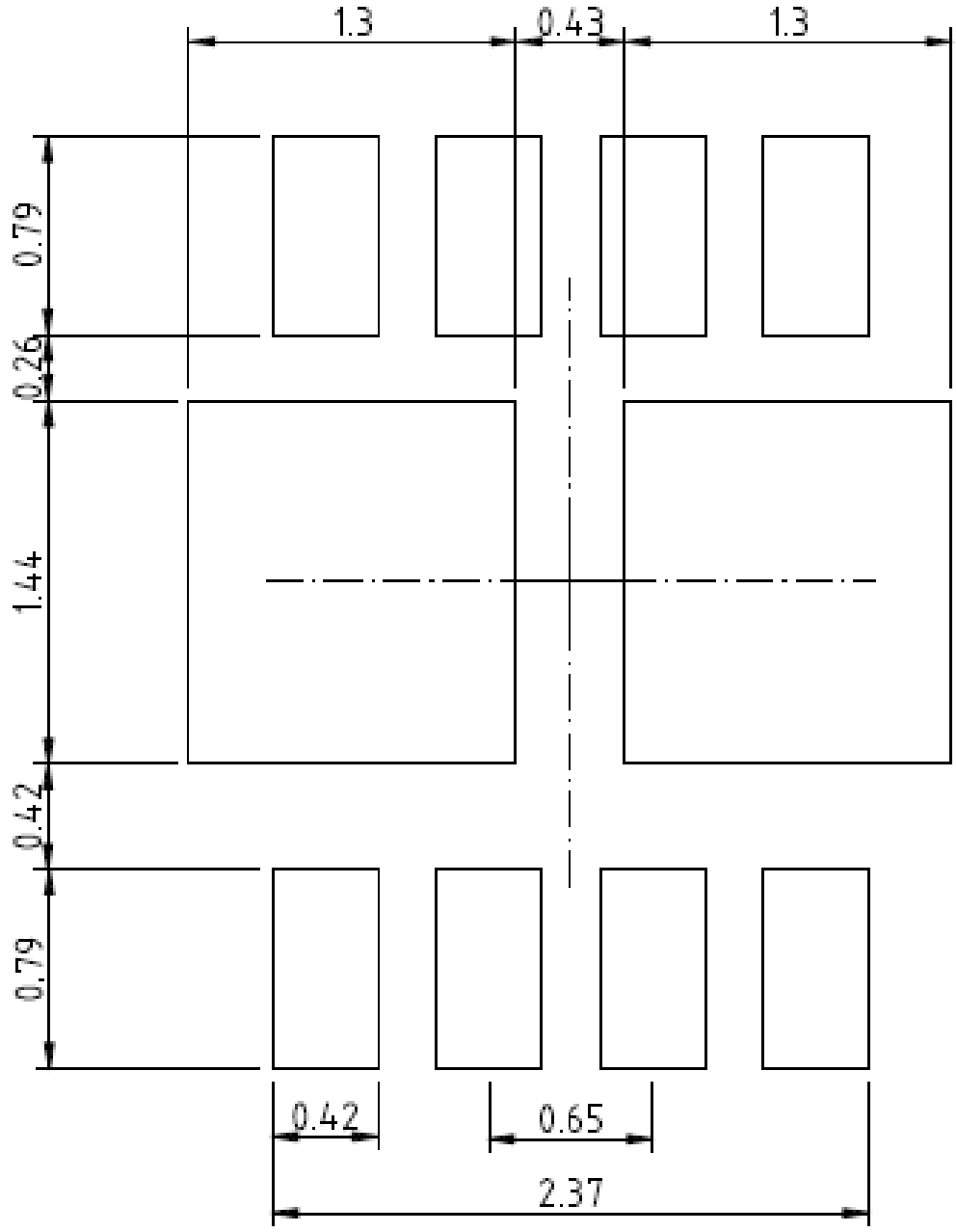
1.All dimension are in millimeters.

2.Dimension does not include burrs and mold flash/protrusions.

3.The outline schematic is not to scale and slightly different from the actual product appearance.

Draw No. M2-DT33(B-DLR)-8-E-G-v01

PDFN 3.3 x 3.3B-DLR FOOTPRINT：



UNIT: mm